AMD-640™

Chipset BIOS Design

Application Note

AMD

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This document highlights the BIOS modifications required to fully support the AMD-640™ Chipset, which includes the AMD-640™ System Controller and the AMD-645™ Peripheral Bus Controller. This document is a supplement to the *AMD-640™ System Controller Data Sheet,* order# 21090, and the *AMD-645™ Peripheral Bus Controller Data Sheet*, order# 21095.

There can be more than one way to implement the functionality detailed in this document. The information provided is for demonstration purposes.

Audience

It is assumed that the reader possesses the proper knowledge of the AMD-640 Chipset, the x86 architecture, and programming requirements to understand the information presented in this document.

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PCI Configuration Mechanism

The AMD-640 Chipset uses PCI configuration mechanism #1 to convey and receive configuration data to and from the host processor. This mechanism, described in PCI Local Bus Specification Revision 2.1, employs I/O locations 0CF8h–0CFBh to specify the target address, and locations 0CFCh–0CFFh for data to or from the target address. The target address includes the PCI bus, device, function, and register numbers of the PCI device. Figure 1 shows a layout of the target address numbers within I/O addresses 0CFBh–0CF8h.

31	bit 30 – bit 24	bit 23 – bit 16	bit 15 – bit 11	10 – 8	bit 7 – bit 2	1	0
En	Reserved	Bus Number	Device Number	Function #	Register Number	0	0

Figure 1. PCI Mechanism #1 Target Address Layout (I/O Address 0CFBh–0CF8h)

To specify the PCI configuration space, set bit 31 (the enable bit) to 1. If bit 31 is cleared, the AMD-640 System Controller passes the data through as an I/O transaction. The bus number, device number, and function number of the AMD-640 System Controller are all 0000h. The bus number, device number, and function number of the AMD-645 Peripheral Bus Controller are all 00000000_00001_XXXb.

The register number addresses a 32-bit word which, in conjunction with the PCI byte enable lines C/$\overline{BE3}$–C/$\overline{BE0}$, specifies the configuration register offset number. Table 1 shows the registers from a logical/functional standpoint by describing them as distinct 8-bit or 16-bit entities. Offsets 0, 1, 2, and 3 are addressed in the same 32-bit physical register. For example, the Non-Cacheable Control register is described as residing at offset 52h. To access this register, write bits 7–2 of 52h (010100b) to the register number (bits 7–2 of I/O address 0CF8h), and assert byte enable 2 (clear C/$\overline{BE2}$).

Table 1 shows the ports used to access the AMD-640 System Controller and AMD-645 Peripheral Bus Controller.

Table 1. Configuration Port Register Summary

Register Name	I/O Address	Type	Default Value	Size
IO_CNTRL	0CF8h	RW	0000_0000h	32
IO_DATA32	0CFCh	RW	0000_0000h	32
IO_EVEN_DATA16	0CFCh	RW	0000h	16
IO_ODD_DATA16	0CFEh	RW	0000h	16
IO_0_DATA8	0CFCh	RW	00h	8
IO_1_DATA8	0CFDh	RW	00h	8
IO_2_DATA8	0CFEh	RW	00h	8
IO_3_DATA8	0CFFh	RW	00h	8

AMD-640™ System Controller

Initialization

All programmable features in the AMD-640 System Controller are controlled by the PCI configuration registers, which are normally written to only during system initialization. This section summarizes the register functions, default values, access types, and addresses (offset numbers). For more detailed descriptions of the configuration registers, see the *AMD-640™ System Controller Data Sheet*, order# 21090.

Access types are indicated as follows:

- RW—Read/Write
- RO—Read Only
- RWC—Read: write 1's to clear individual bits

Table 2 shows the PCI defined registers read by the BIOS during system initialization.

Table 2. Configuration Space Header Registers

Offset	PCI Header	Default	Access
01–00h	Vendor ID	1106h	RO
03-02h	Device ID	0595h	RO
05-04h	Command	0017h	RW
07-06h	Status	02A0h	RWC
08h	Revision ID	nn*	RO
09h	Program Interface	00h	RO
0Ah	Bus Class Code	00h	RO
0Bh	Base Class Code	06h	RO
0Ch	Cache Line Size	00h	RO
0Dh	Latency Timer	00h	RW
0Eh	Header Type	00h	RO
0Fh	Built-In Self Test (BIST)	00h	RO
10h–3Fh	Reserved	00h	–

Note:

* *nn changes for each device revision. Rev D = 02 is the current revision as of publication of this document. Rev E = 03 and Rev F = 04.*

Table 3 shows device-specific cache control registers and recommended values.

Table 3. Configuration Space Cache Control Registers

Offset	Cache Control	Default	Recommended		Access
			Setting	Result	
50h	Cache Control 1	00h	83h	Normal operation, PBSRAM	RW
51h	Cache Control 2	00h	01h	1 bank; 512k bytes	RW
52h	Non-Cacheable Control	02h	96h	L1=L2=WB	RW
53h	System Performance Control	00h	78h	PCI concurrency	RW
55h–54h	Non-Cacheable Region #1	0000h	–	Disabled	RW
57h-56h	Non-Cacheable Region #2	0000h	–	Disabled	RW

Table 4 shows the recommended values for Fast Page mode, EDO, and SDRAM. These values, which are programmed during initialization, ensure acceptable performance but may not be optimal for a particular system.

Table 4. Configuration Space DRAM Control Registers

Offset	Cache Control	Default	Recommended		Access
			Setting	Result	
58h	DRAM Configuration Register #1	40h	44h	10 bit Col	RW
59h	DRAM Configuration Register #2	05h	03h	banks 0-3 populated	RW
5Ah	DRAM Bank 0 Ending [HA29-22]	01h	10h	64M—02 for 8 Meg	RW
5Bh	DRAM Bank 1 Ending [HA29-22]	01h	20h	64M—04 for 8 Meg	RW
5Ch	DRAM Bank 2 Ending [HA29-22]	01h	30h	64M—06 for 8 Meg	RW
5Dh	DRAM Bank 3 Ending [HA29-22]	01h	40h	64M—08 for 8 Meg	RW
5Eh	DRAM Bank 4 Ending [HA29-22]	01h	50h	64M—08 for no RAM	RW
5Fh	DRAM Bank 5 Ending [HA29-22]	01h	60h	64M—08 for no RAM	RW
60h	DRAM Type	00h	00h 05h	Fast Page Mode banks 0–3 EDO mode	RW
61h	Shadow RAM Control Register #1	00h	CAh	Video BIOS	RW
62h	Shadow RAM Control Register #2	00h	00h	disable	RW
63h	Shadow RAM Control Register #3	00h	22h	main BIOS	RW
64h	DRAM Timing	ABh	FFh 4h 57h	slowest initially 60 nsec EDO 60 nsec FP	RW
65h	DRAM Control Register #1	00h	A4h	Page open Fast decode Latch delay	RW
66h	DRAM Control Register #2	00h	00h		RW
67h	32-Bit DRAM Width Control Register	00h	00h	64 bit DRAM	RW
69h–68h	Reserved	–	–	–	–
6Ah	DRAM Refresh Counter	00h	43h	15 μsec	RW
6Bh	DRAM Refresh Control Register	00h	80h	CBR	RW
6Ch	SDRAM Control Register	00h	00h	–	RW
6Dh	DRAM Drive Strength Control Register	00h	4Fh	24 ma drive	RW
6Eh	ECC Control Register	00h	00h	–	RW
6Fh	ECC Status Register	00h	00h	–	RO

Table 5 shows the PCI control registers. These registers, which are programmed during initialization, control the processor bus to PCI bus.

Table 5. Configuration Space PCI Control Registers

Offset	Cache Control	Default	Recommended		Access
			Setting	Result	
70h	PCI Buffer Control 1	00h	E0h	Enable Write Buffers and prefetch	RW
71h	Processor to PCI Flow Control #1	00h	DEh	Post writes to DRAM and Merge	RW
72h	Processor to PCI Flow Control #2	02h	ECh	Reduce FRAME	RW
73h	PCI Target Control	00h	8Dh	STOP control	RW
74h	PCI Initiator Control	00h	C0h	Enhance Commands	RW
75h	PCI Arbitration Control #1	00h	00h	PCI has priority, REQ based	RW
76h	PCI Arbitration Control #2	00h	80h	CPU has priority, Override 75	RW

AMD-645™ Peripheral Bus Controller

Initialization

All programmable features in the AMD-645 Peripheral Bus Controller are controlled by the PCI configuration registers, which are normally written to during system initialization. This section summarizes the register functions, default values, access types, and addresses. For more detailed descriptions of the configuration registers, see the *AMD-645™ Peripheral Bus Controller Data Sheet*, order# 21095.

Access types are indicated as follows:

- RW—Read/Write
- RO—Read Only
- WO—Write Only
- RWC—Read; write 1's to clear individual bits

Legacy I/O Registers

Table 6 contains registers that control Master DMA channels 0–3. There are 16 Master DMA control registers, which are provided for backwards compatibility.

Table 6. Master DMA Controller Registers

Port	Register Name	Default	Recommended		Access
			Setting	Result	
00h	Ch 0 Base/Current Address	n/a	n/a		RW
01h	Ch 0 Base/Current Count	n/a	n/a		RW
02h	Ch 1 Base/Current Address	n/a	n/a		RW
03h	Ch 1 Base/Current Count	n/a	n/a		RW
04h	Ch 2 Base/Current Address	n/a	n/a		RW
05h	Ch 2 Base/Current Count	n/a	n/a		RW
06h	Ch 3 Base/Current Address	n/a	n/a		RW
07h	Ch 3 Base/Current Count	n/a	n/a		RW
08h	Status/Command	n/a	n/a		RW
09h	Write Request	n/a	n/a		WO
0Ah	Write Single Mask	n/a	n/a		WO
0Bh	Write Mode	n/a	n/a		WO
0Ch	Clear Byte Pointer F/F	n/a	n/a		WO
0Dh	Master Clear	n/a	n/a		WO
0Eh	Clear Mask	n/a	n/a		WO
0Fh	RW All Mask Bits	n/a	n/a		RW

Table 7 shows the registers for the master hardware interrupt controller channels 0–7.

Table 7. Master Interrupt Controller Registers

Port	Register Name	Default	Recommended		Access
			Setting	Result	
20h	Master Interrupt Control	n/a	n/a		*
21h	Master Interrupt Mask	n/a	n/a		*
20h	Master Interrupt Control Shadow	n/a	n/a		RW
21h	Master Interrupt Mask Shadow	n/a	n/a		RW

Note:
* *RW, if shadow registers are disabled.*

Table 8 shows the timer/counter registers. These registers are used for ISA REFRESH and speaker sounds.

Table 8. Timer/Counter Registers

Port	Register Name	Default	Recommended		Access
			Setting	Result	
40h	Timer/Counter 0	n/a	n/a		RW
41h	Timer/Counter 1	n/a	n/a		RW
42h	Timer/Counter 2	n/a	n/a		RW
43h	Timer/Counter Control	n/a	n/a		WO

Table 9 shows the registers used for controlling the commands and status of the keyboard and mouse interfaces.

Table 9. Keyboard Controller Registers

Port	Register Name	Default	Recommended		Access
			Setting	Result	
60h	Keyboard Controller Data	n/a	n/a		RW
61h	Miscellaneous Functions and Speaker Control	n/a	n/a		RW
64h	Keyboard Controller Command/Status	n/a	n/a		RW

Table 10 shows the registers used for controlling the storing of system configurations saved in CMOS.

Table 10. CMOS/RTC/NMI Registers

Port	Register Name	Default	Recommended		Access
			Setting	Result	
70h	CMOS Memory Address & NMI Disable	n/a	n/a		WO
71h	CMOS Memory Data (128 bytes)	n/a	n/a		RW
72h	CMOS Memory Address	n/a	n/a		RW
73h	CMOS Memory Data (256 bytes)	n/a	n/a		RW
74h	CMOS Memory Address	n/a	n/a		RW
75h	CMOS Memory Data (256 bytes)	n/a	n/a		RW

Table 11 shows the registers used to access the upper 8 bits of the DMA address space (A16–A23). The bits for A0–A15 are shown in Table 6 on page 7 and in Table 14 on page 10.

Table 11. DMA Page Registers

Port	Register Name	Default	Recommended		Access
			Setting	Result	
87h	DMA Page—DMA Channel 0	n/a	n/a		RW
83h	DMA Page—DMA Channel 1	n/a	n/a		RW
81h	DMA Page—DMA Channel 2	n/a	n/a		RW
82h	DMA Page—DMA Channel 3	n/a	n/a		RW
8Fh	DMA Page—DMA Channel 4	n/a	n/a		RW
8Bh	DMA Page—DMA Channel 5	n/a	n/a		RW
89h	DMA Page—DMA Channel 6	n/a	n/a		RW
8Ah	DMA Page—DMA Channel 7	n/a	n/a		RW

Table 12 shows a system control register that is used for fast A20 switching, hard disk activity LED, and high-speed resets.

Table 12. System Control Registers

Port	Register Name	Default	Recommended		Access
			Setting	Result	
92h	System Control	n/a	n/a		RW

Table 13 shows the registers used to control the slave interrupt controller. These registers are use to control the hardware interrupts 8–15.

Table 13. Slave Interrupt Controller Registers

Port	Register Name	Default	Recommended		Access
			Setting	Result	
A0h	Slave Interrupt Control	n/a	n/a		*
A1h	Slave Interrupt Mask	n/a	n/a		*
A0h	Slave Interrupt Control Shadow	n/a	n/a		RW
A1h	Slave Interrupt Mask Shadow	n/a	n/a		RW

Note:
* *RW, if shadow registers are disabled.*

Table 14 shows channels 0–3 of the slave DMA controller. These channels are used to control the system DMA channels 4–7.

Table 14. Slave DMA Controller Registers

Port	Register Name	Default	Recommended		Access
			Setting	Result	
C0h	Ch 0 Base/Current Address	n/a	n/a		RW
C2h	Ch 0 Base/Current Count	n/a	n/a		RW
C4h	Ch 1 Base/Current Address	n/a	n/a		RW
C6h	Ch 1 Base/Current Count	n/a	n/a		RW
C8h	Ch 2 Base/Current Address	n/a	n/a		RW
CAh	Ch 2 Base/Current Count	n/a	n/a		RW
CCh	Ch 3 Base/Current Address	n/a	n/a		RW
CEh	Ch 3 Base/Current Count	n/a	n/a		RW
D0h	Status/Command	n/a	n/a		RW
D2h	Write Request	n/a	n/a		WO
D4h	Write Single Mask	n/a	n/a		WO
D6h	Write Mode	n/a	n/a		WO
D8h	Clear Byte Pointer F/F	n/a	n/a		WO
DAh	Master Clear	n/a	n/a		WO
DCh	Clear Mask	n/a	n/a		WO
DEh	RW All Mask Bits	n/a	n/a		RW

PCI Function 0 Registers—PCI-to-ISA Bridge

Table 15 shows configuration registers of the PCI-to-ISA bridge.

Table 15. Configuration Space PCI-to-ISA Header Registers

Offset	PCI Header	Default	Recommended		Access
			Setting	Result	
01h–00h	Vendor ID	1106h	n/a		RO
03h–02h	Device ID	0586h	n/a		RO
05h–04h	Command	000Fh	n/a		RW
07h–06h	Status	0200h	n/a		RWC
08h	Revision ID (00h = first silicon)	–	n/a		RO
09h	Program Interface	00h	n/a		RO
0Ah	Sub Class Code	01h	n/a		RO
0Bh	Base Class Code	06h	n/a		RO
0Ch	Reserved (Cache Line Size)	00h	n/a		–
0Dh	Reserved (Latency Timer)	00h	n/a		–
0Eh	Header Type	80h	n/a		RO
0Fh	Built-In Self Test (BIST)	00h	n/a		RO
3Fh–10h	Reserved	00h	n/a		–

Table 16 shows the registers used to control the ISA bus.

Table 16. ISA Bus Control Registers

Offset	Register	Default	Recommended		Access
			Setting	Result	
40h	ISA Bus Control	00h	00h	Normal ISA Timing	RW
41H	ISA Test Mode	00h	01h	Refresh test mode	RW
42h	ISA Clock Control	00h	00h	ISA clock=PCICLK/4	RW
43h	ROM Decode Control	00h	00h	$\overline{\text{ROMCS}}$ F0000h-FFFFFh	RW
44h	Keyboard Controller Control	00h	01h	Disable mouse lock	RW
45h	Type F DMA Control	00h	00h	Set DMA type F if needed	RW
46h	Miscellaneous Control 1	00h	10h	Disable Post Memory Write	RW
47h	Miscellaneous Control 2	00h	C0h	INIT as CPU reset Enable PCI delay transaction	RW
48h	Miscellaneous Control 3	01h	01h	Enable USB, IDE	RW
49h	Reserved	00h	00h	—	—
4Ah	IDE Interrupt Routing	04h	C4h	Wait for PGNT before Grant to ISA Master/DMA Access ports 00-FFh via SD IDE Primary Channel IRQ14 Secondary Ch IRQ 15	RW
4Bh	Reserved	00h	00h	—	—
4Ch	DMA/Master Mem Access Ctrl 1	00h	00h	PCI memory hole bottom address HA[23–16]=0	RW
4Dh	DMA/Master Mem Access Ctrl 2	00h	00h	PCI Memory hole top address HA[23–16]=0	RW
4Fh–4Eh	DMA/Master Mem Access Ctrl 3	0300h	F300h	Top of PCI memory for ISA=16Mbytes Forward 00000h-9FFFFh access to PCI	RW

Table 17 shows the registers used to control plug and play routing to ISA IRQs.

Table 17. Plug and Play Control Registers

Offset	Register	Default	Recommended		Access
			Setting	Result	
50h	Reserved (do not program)	24h	24h	–	RW
53h–51h	Reserved	00h	00h	–	–
54h	PCI IRQ Edge/Level Selection	00h	00h	PIRQs inverted edge trigger/ Non-inverted level trigger	RW
55h	PnP Routing for External MIRQ0–1	00h	00h	MIRQs disabled	RW
56h	PnP Routing for PCI INTB–A	00h	B0h	INTB routes to IRQ11 INTA disabled	RW
57h	PnP Routing for PIC INTD–C	00h	57h	INTD routes to IRQ5 INTC routes to IRQ7	RW
58h	PnP Routing for External MIRQ2	00h	00h	MIRQ2 disabled	RW
59h	MIRQ Pin Configuration	04h	04h	Configure as $\overline{\text{MASTER}}$	RW
5Ah	XD Power-On Strap Options	*	F7h	Enable Int RTc, PS2 mouse, Int KBC	RW
5Bh	Internal RTC Test Mode	00h	00h	RTC reset enable, SRAM access enable, Test enable	RW
5Fh–5Ch	Reserved	00h	00h	–	–

Note:
* *Power-up default value depends on external strapping.*

Table 18 shows the registers used to control Distributed DMA.

Table 18. Distributed DMA

Offset	Register	Default	Recommended		Access
			Setting	Result	
61h–60h	Channel 0 Base Address/ Enable	0000h	0000h	Disabled	RW
63h–62h	Channel 1Base Address/ Enable	0000h	0000h	Disabled	RW
65h–64h	Channel 2 Base Address/ Enable	0000h	0000h	Disabled	RW
67h–66h	Channel 3 Base Address/ Enable	0000h	0000h	Disabled	RW
69h–68h	Reserved	0000h	0000h	Disabled	–
6Bh–6Ah	Channel 5 Base Address/ Enable	0000h	0000h	Disabled	RW
6Dh–6Ch	Channel 6 Base Address/ Enable	0000h	0000h	Disabled	RW
6Fh–6Eh	Channel 7 Base Address/ Enable	0000h	0000h	Disabled	RW
FFh–70h	Reserved	00h	00h	–	–

PCI Function 1 Registers—IDE Control

Table 19 shows configuration registers used for enhanced IDE and PCI.

Table 19. Configuration Space IDE Header Registers

Offset	PCI Header	Default	Recommended		Access
			Setting	Result	
01h–00h	Vendor ID	1106h	n/a		RO
03h–02h	Device ID	0571h	n/a		RO
05h–04h	Command	0080h	n/a		RW
07h–06h	Status	0280h	n/a		RW
08h	Revision ID (00h = first silicon)	—	n/a		RO
09h	Program Interface	8Ah	n/a		RW
0Ah	Sub Class Code	01h	n/a		RO
0Bh	Base Class Code	01h	n/a		RO
0Ch	Reserved (Cache Line Size)	00h	n/a		—
0Dh	Latency Timer	20h	n/a		RW
0Eh	Header Type	00h	n/a		RO
0Fh	Built-In Self Test (BIST)	00h	n/a		RO
13h–10h	Base Address—Primary Data/Command	000001F0h	n/a		RW
17h–14h	Base Address—Primary Control/Status	000003F4h	n/a		RW
1Bh–18h	Base Address—Secondary Data/Command	00000170h	n/a		RW
1Fh–1Ch	Base Address—Secondary Control/Status	00000374h	n/a		RW
23h–20h	Base Address—Bus Master Control	0000CC01h	n/a		RW
2Fh–24h	Reserved (unassigned)	00h	n/a		—
33h–30h	Reserved (expansion ROM base address)	00h	n/a		—
3Bh–33h	Reserved (unassigned)	00h	n/a		—
3Ch	Interrupt Line	0Eh	n/a		RW
3Dh	Interrupt Pin	00h	n/a		RO
3Eh	Minimum Grant	00h	n/a		RO
3Fh	Maximum Latency	00h	n/a		RO

Table 20 shows registers used to control IDE control parameters.

Table 20. Configuration Space IDE Registers

Offset	Register	Default	Recommended		Access
			Setting	Result	
40h	Chip Enable	04h	0Bh	Enable Pri and Sec Channel	RW
41h	IDE Configuration	02h	E2h	Enable Pri and Sec read prefetch buffer Enable Pri Post Write Buffer	RW
42h	Reserved (do not program)	09h	09h	–	RW
43h	FIFO Configuration	3Ah	3Ah	Allocate 8 word buffers in both Pri and Sec Channel Set threshold to 1/2	RW
44h	Miscellaneous Control 1	68h	68h	Master Read/Write Cycle $\overline{\text{IRDY}}$ 1 wait state FIFO output Data 12 clock advance	RW
45h	Miscellaneous Control 2	00h	00h	No channel interrupts swap	RW
46h	Miscellaneous Control 3	C0h	C0h	Pri and Sec Ch Read DMA FIFO flush enabled No limit in DRDY pulse width	RW
4Bh–48h	Drive Timing Control	A8A8A8 A8h	A8A8A8 A8h	$\overline{\text{DIOR}}$ and $\overline{\text{DIOW}}$ pulse width set to 11 PCI clocks Recovery time set to 9 clocks	RW
4Ch	Address Setup Time	FFh	FFh	Address setup time 4T	RW
4Dh	Reserved (do not program)	00h	00h	–	RW
4Eh	Sec Non-1F0h Port Access Timing	FFh	FFh	Sec non-1F0 Port Access, $\overline{\text{DIOR}}$ and $\overline{\text{DIOW}}$ pulse width set to 17 PCI clocks	RW
4Fh	Pri Non-1F0h Port Access Timing	FFh	FFh	Pri non-1F0 Port Access, $\overline{\text{DIOR}}$ and $\overline{\text{DIOW}}$ pulse width set to 17 PCI clocks	RW
53h–50h	UltraDMA33 Exit Timing Control	03030303h	030303 03h	Pri and Sec Drive 0 and 1 Mode enabled by Set Feature command Disabled UltraDMA33-Mode	RW
57h-54h	Reserved	00h	00h	–	–

Table 20. Configuration Space IDE Registers (continued)

Offset	Register	Default	Recommended		Access
			Setting	Result	
5Fh–58h	Reserved	A8A8A8 A8h	A8A8A8 A8h	–	–
61h–60h	Primary Sector Size	0200h	0200h	200h bytes per sector	RW
67h–62h	Reserved	00h	00h	–	–
69h–68h	Secondary Sector Size	0200h	0200	200h bytes per sector	RW
FFh–6Ah	Reserved	00h	00	–	–

Table 21 shows the registers used for controlling IDE. These registers are provided for backwards compatibility.

Table 21. IDE Controller I/O Registers

Offset	Register Name	Default	Recommended		Access
			Setting	Result	
00h	Primary Channel Command	00h	n/a		RW
01h	Reserved	00h	n/a		–
02h	Primary Channel Status	00h	n/a		RWC
03h	Reserved	00h	n/a		–
07h–04h	Primary Channel PRD Table Address	00h	n/a		RW
08h	Secondary Channel Command	00h	n/a		RW
09h	Reserved	00h	n/a		–
0Ah	Secondary Channel Status	00h	n/a		RWC
0Bh	Reserved	00h	n/a		–
0Fh–0Ch	Secondary Channel PRD Table Address	00h	n/a		RW

PCI Function 2 Registers—USB Controller

Table 22 shows configuration registers used for the universal serial bus (USB). This implementation of USB is compatible with UHCI v1.1.

Table 22. Configuration Space USB Header Registers

Offset	PCI Header	Default	Recommended		Access
			Setting	Result	
01h–00h	Vendor ID	1106h	n/a		RO
03h–02h	Device ID	3038h	n/a		RO
05h–04h	Command	0000h	n/a		RW
07h–06h	Status	0200h	n/a		RWC
08h	Revision ID (00h = first silicon)	—	n/a		RO
09h	Program Interface	00h	n/a		RO
0Ah	Sub Class Code	03h	n/a		RO
0Bh	Base Class Code	0Ch	n/a		RO
0Ch	Reserved (Cache Line Size)	00h	n/a		RO
0Dh	Latency Timer	16h	n/a		RW
0Eh	Header Type	00h	n/a		RO
0Fh	Built-In Self Test (BIST)	00h	n/a		RO
10h–1Fh	Reserved	00h	n/a		—
23h–20h	Base Address	0000301h	n/a		RW
3Bh–24h	Reserved	00h	n/a		—
3Ch	Interrupt Line	00h	n/a		RW
3Dh	Interrupt Pin	04h	n/a		RW
3Fh–3Eh	Reserved	00h	n/a		—

Table 23 shows registers used to control the USB.

Table 23. Configuration Space USB Registers

Offset	Register	Default	Recommended		Access
			Setting	Result	
40h	Miscellaneous Control 1	00h	00h	Support MRL, MRM, MWI ISB Data Length 1280 Disable USB Power Management DMA 16 DW burst access PCI zero wait state	RW
41h	Miscellaneous Control 1	00h	00h	Always set trap 60/64 status bit A20 gate pass through	RW
43h–42h	Reserved	00h	00h	–	RO
45h–44h	Reserved (do not program)	00C2h	00C2h	–	RW
47h	Reserved	0Ch	0Ch	–	–
5Fh–48h	Reserved	00h	00h	–	–
60h	Serial Bus Release Number	10h	10h	Always read 10h	RO
BFh–61h	Reserved	00h	00h	–	–
C1h–C0h	Legacy Support	2000h	2000h	Always read 2000h	RO
FFh–C2h	Reserved	00h	00h	–	–

Table 24 shows registers used to access the USB through I/O.

Table 24. USB Controller I/O Registers

Offset	Register Name	Default	Recommended		Access
			Setting	Result	
1h–0h	USB Command	0000h	n/a		RW
3h–2h	USB Status	0000h	n/a		RWC
5h–4h	USB Interrupt Enable	0000h	n/a		RW
7h–6h	Frame Number	0000h	n/a		RW
Bh–8h	Frame List Base Address	00000000h	n/a		RW
Ch	Start of Frame Modify	40h	n/a		RW
11h–10h	Port 1 Status/Control	0080h	n/a		RWC
13h–12h	Port 2 Status/control	0080h	n/a		RWC

PCI Function 3 Registers—Power Management

Power Management Configuration Space Registers

Table 25 shows configuration registers used for the Advanced Configuration Power Interface (ACPI) and legacy power management.

Table 25. Configuration Space Power Management Header Registers

Offset	PCI Header	Default	Recommended		Access
			Setting	Result	
01h–00h	Vendor ID	1106h	n/a		RO
03h–02h	Device ID	3040h	n/a		RO
05h–04h	Command	0000h	n/a		RW
07h–06h	Status	0280h	n/a		RWC
08h	Revision ID (00h = first silicon)	–	n/a		RO
09h	Program Interface	00h	n/a		RO
0Ah	Sub Class Code	00h	n/a		RO
0Bh	Base Class Code	00h	n/a		RO
0Ch	Reserved	00h	n/a		RO
0Dh	Latency Timer	16h	n/a		RW
0Eh	Header Type	00h	n/a		RO
0Fh	Built-In Self Test (BIST)	00h	n/a		RO
10h–1Fh	Reserved	00h	n/a		–
23h–20h	I/O Register Base Address	00000001h	n/a		RW
3Fh–24h	Reserved	00h	n/a		–

Table 26 shows registers used to control ACPI through the PCI bus.

Table 26. Configuration Space Power Management Registers

Offset	Register	Default	Recommended		Access
			Setting	Result	
40h	Pin Configuration	C0h	C0h	Define pin 136 as GPIO4 Define pin 92 as GPIO4	RW
41h	General Configuration	00h	00h	Disable $\overline{\text{PWRBTN}}$ debounce Disable ACPI Timer Reset ACPI 24-bit timer count 32us Clock Throttling	RW
42h	SCI Interrupt Configuration	00h	00h	Disable SCI interrupt	RW
43h	Reserved	00h	00h		RW
45h–44h	Primary Interrupt Channel	0000h	0000h	Disable Pri interrupt Channel	RW
47h–46h	Secondary Interrupt Channel	0000h	0000h	Disable Sec interrupt Channel	RW
53h–50h	GP Timer Control	00000000h	00000000h	Disable Conserve Mode Disable Sec Event Time Disable GP1 Timer Disable GP0 Timer	RW
54h–60h	Reserved	00h	00h	–	–
61h	Programming Interface Read Value	00h	00h	Value to be returned by register at offset 09h	WO
62h	Sub Class Read Value	00h	00h	Value to be returned by register at offset 0Ah	WO
63h	Base Class Read Value	00h	00h	Value to be returned by register at offset 0Bh	WO
64h–FFh	Reserved	00h	00h	–	–

Power Management I/O Space Registers

Table 27 shows registers used to control legacy power management features through I/O.

Table 27. Basic Power Management Control/Status Registers

Offset	Register Name	Default	Recommended		Access
			Setting	Result	
01h–00h	Power Management Status	00h	n/a		RWC
03h–02h	Power Management Enable	00h	n/a		RW
05h–04h	Power Management Control	00h	n/a		RW
0Bh–08h	Power Management Timer	00h	n/a		RW

Table 28 shows power management registers used to control $\overline{\text{SPTCLK}}$.

Table 28. Processor Power Management Registers

Offset	Register Name	Default	Recommended		Access
			Setting	Result	
13h–10h	Processor Control	0000h	n/a		RW
14h	Processor Level 2	00h	n/a		RO
15h	Processor Level 3	00h	n/a		RO

Table 29 shows registers used to control SCI and SMI features.

Table 29. General Purpose Power Management Registers

Offset	Register Name	Default	Recommended		Access
			Setting	Result	
21h–20h	General Purpose Status	00h	n/a		RWC
23h–22h	General Purpose SCI Enable	00h	n/a		RW
25h–24h	General Purpose SMI Enable	00h	n/a		RW
27h–26h	Power Supply Control	00h	n/a		RW

Table 30 shows registers used to control generic global power management registers.

Table 30. Generic Power Management Registers

Offset	Register Name	Default	Recommended		Access
			Setting	Result	
29h–28h	Global Status	00h	n/a		RWC
2Bh–2Ah	Global Enable	00h	n/a		RW
2Dh–2Ch	Global Control	00h	n/a		RW
2Fh	SMI Command	00h	n/a		RW
33h–30h	Primary Activity Detect Status	00h	n/a		RWC
37h–34h	Primary Activity Detect Enable	00h	n/a		RW
3Bh–38h	GP Timer Reload Enable	00h	n/a		RW

Table 31 shows registers used to control I/O features of SCI and SMI.

Table 31. General Purpose I/O

Offset	Register Name	Default	Recommended		Access
			Setting	Result	
40h	GPIO Direction Control	00h	n/a		RW
42h	GPIO Port Output Value	00	n/a		RW
44h	GPIO Port Input Value	input	n/a		RO
47h–46h	GPO Port Output Value	0000	n/a		RW
49h–48h	GPI Port Input Value	input	n/a		RO

Additional Considerations

Software Timing Dependencies Relative to Memory Controller Setup

The AMD-K6 MMX processor differs from other processors with regards to instruction latencies and the order or priority of processor bus cycles. Timing dependent software that relies on the specific latencies of other processors should be retested for proper operation with the AMD-K6 processor. In addition, retesting should be performed on components with variable timing (i.e., memory modules, oscillators, and timers).

Particular attention should be paid to memory-setup subroutines that determine the type of DRAM in the system. Some chipsets may not tolerate a DRAM mode change (i.e, EDO to SDRAM) on the same clock as a DRAM refresh cycle. For example, the Intel 84437VX chipset does not tolerate having its memory refresh enabled prior to changing memory mode types. Refresh should only be enabled after the memory type has been determined.

Note: *As a general rule, the AMD-K6 processor write allocate feature should not be enabled during memory sizing and typing algorithms.*