



# RAGE™6

## Register Reference Guide

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### Technical Reference Manual

P/N: RRG-215R6-00-01 OEM

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## Record of Revisions

Release	Date
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## Related Manuals

### ***RAGE 6 Series***

- RAGE™ 6 Register Reference Guide (RRG-G05000)
- RAGE™ 6 Graphics Controller Specifications (GCS-C05000)

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## 1.1 About this Manual

This manual serves as a register reference guide to the RAGE 6 graphics controller.

- Chapter 1 outlines the notations and conventions used throughout this manual.
- Chapter 2 provides a detailed description of the registers.
- Appendix A provides several cross-referenced lists (sorted by Register Name and Address).

## 1.2 Nomenclature and Conventions

### 1.2.1 Numeric Representations

- Hexadecimal numbers are appended with “h” whenever there is a risk of ambiguity. Other numbers are assumed to be in decimal.
- Registers (or fields) of identical function are sometimes indicated by a single expression in which the part of the signal name that differs is enclosed in [ ] brackets. For example, the eight Host Data registers — HOST\_DATA0 through to HOST\_DATA7 — are represented by the single expression HOST\_DATA[7:0].

### 1.2.2 Register Description

All registers in this document are described with the format of the sample table below. All offsets are in hexadecimal notation, while programmed bits are in either binomial or hexadecimal notation.

<b>DST_HEIGHT_WIDTH_8 - W - 32 bits - [MMReg:0x158C]</b>			
Field Name	Bits	Default	Description
DST_WIDTH <i>(mirror bits 0:7 of DST_WIDTH:DST_WIDTH)</i>	23:16	0x0	Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete
DST_HEIGHT <i>(mirror bits 0:7 of DST_HEIGHT:DST_HEIGHT)</i>	31:24	0x0	Destination Height Write 15: 0 to E2_DST_Y, Write 31: 16 to E2_DST_HEIGHT

[ W ] (Reserved) 15: 0 DST\_WIDTH 23: 16 Destination width: range 0 to 256 (ZERO extent)

**Table 1-1 Register description table notation**

Register Information	Example
Register name	DST_HEIGHT_WIDTH_8
Read / Write capability R = Readable W = Writable RW = Readable and Writable	W
Register size	32 bits
Register address(es)*	MMReg:0x158C
Field name	DST_WIDTH
Field position/size	23:16
Field default value	0x0
Field description	Destination....complete
Field mirror information	<i>(mirror bits 0:7 of DST_WIDTH:DST_WIDTH)</i>
Brief register description	[ W] (Reserved) 15: 0 DST_WIDTH 23: 16 Destination width: range 0 to 256 (ZERO extent)
<p><b>* Note:</b>                      There maybe more than one address; the convention used is as follows:  <b>[aperName:offset]</b> - single mapping, to one aperture/decode and one offset  <b>[aperName1, aperName2, ..., aperNameN:offset]</b> - multiple mappings to different apertures/decodes but same offset  <b>[aperName:startOffset-endOffset]</b> - mapped to an offset range in the same aperture/decode</p>	

### 2.1 HostInterface Registers

Host Interface Registers

## 2.2 RegisterBackboneManager Registers

### Register Backbone Manager(RBBM)Control Registers.

GEN_INT_CNTL - RW - 32 bits - [IOReg,MMReg:0x40]			
Field Name	Bits	Default	Description
CRTC_VBLANK_MASK (DISPLAY)	0	0x0	Vertical blank interrupt mask. 0=Disable 1=Enable
CRTC_VLINE_MASK (DISPLAY)	1	0x0	Vertical line interrupt mask. 0=Disable 1=Enable
CRTC_VSYNC_MASK (DISPLAY)	2	0x0	Vertical sync interrupt mask. 0=Disable 1=Enable
SNAPSHOT_MASK (DISPLAY)	3	0x0	Snapshot interrupt mask. 0=Disable 1=Enable
FP_DETECT_MASK (DISPLAY)	4	0x0	Hot plug detect (HPD) interrupt mask. 0=Disable 1=Enable
DMA_VIPH0_INT_EN (VIP)	12	0x0	VIP host port channel 0 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH1_INT_EN (VIP)	13	0x0	VIP host port channel 1 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH2_INT_EN (VIP)	14	0x0	VIP host port channel 2 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH3_INT_EN (VIP)	15	0x0	VIP host port channel 3 DMA interrupt mask. 0=Disable 1=Enable
I2C_INT_EN (VIP)	17	0x0	I2C interrupt mask. 0=Disable 1=Enable
GUI_IDLE_MASK (RBBM)	19	0x0	GUI idle interrupt mask. 0=Disable 1=Enable
VIPH_INT_EN (VIP)	24	0x0	VIP host port interrupt mask. 0=Disable 1=Enable

SW_INT_EN (HDP)	25	0x0	Software interrupt mask. 0=Disable 1=Enable
GUIDMA_MASK (CP)	30	0x0	GUI DMA channel interrupt mask. 0=Disable 1=Enable
VIDDMA_MASK (CP)	31	0x0	Video capture DMA channel interrupt mask. 0=Disable 1=Enable

General Interrupt Control register.

The MASK/EN fields control whether the respective status bits are enabled to drive the system interrupt pin. Even if enabled here, the interrupt line is not driven unless enabled in the PCI configuration space.

<b>GEN_INT_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CRTC_VBLANK_STAT (R) (DISPLAY)	0	0x0	Vertical blank interrupt. Set when display in vertical retrace. 0=No event 1=Event has occurred, interrupting if enabled
CRTC_VBLANK_STAT_AK (W) (DISPLAY)	0	0x0	Vertical blank interrupt acknowledge. 0=No effect 1=Clear status
CRTC_VLINE_STAT (R) (DISPLAY)	1	0x0	Vertical line interrupt. Set on display line on programmed by the CRTC_VLINE_CRNT_VLINE.CRTC_VLINE register. 0=No event 1=Event has occurred, interrupting if enabled
CRTC_VLINE_STAT_AK (W) (DISPLAY)	1	0x0	Vertical line interrupt acknowledge. 0=No effect 1=Clear status
CRTC_VSYNC_STAT (R) (DISPLAY)	2	0x0	Vertical sync interrupt. Set on start of VSYNC at the DAC. 0=No event 1=Event has occurred, interrupting if enabled
CRTC_VSYNC_STAT_AK (W) (DISPLAY)	2	0x0	Vertical sync interrupt acknowledge. 0=No effect 1=Clear status
SNAPSHOT_STAT (R) (DISPLAY)	3	0x0	Snapshot interrupt. Set as controlled by SNAPSHOT_VIF_COUNT register. 0=No event 1=Event has occurred, interrupting if enabled
SNAPSHOT_STAT_AK (W) (DISPLAY)	3	0x0	Snapshot interrupt acknowledge. 0=No effect 1=Clear status

FP_DETECT_STAT (R) (DISPLAY)	4	0x0	Hot plug detect (HPD) interrupt. Set on HPD connect or disconnect as controlled by FP_GEN_CNTL.FP_DETECT_INT_POL. 0=No event 1=Event has occurred, interrupting if enabled
FP_DETECT_STAT_AK (W) (DISPLAY)	4	0x0	Hot plug detect (HPD) interrupt acknowledge. 0=No effect 1=Clear status
CAPO_INT_ACTIVE (R) (VIP)	8	0x0	Capture port 0 has active interrupt(s). 0=Capture port 0 not source of any active interrupt 1=Capture port 0 has active interrupt(s)
DMA_VIPH0_INT (R) (VIP)	12	0x0	VIP host port channel 0 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH0_INT_AK (W) (VIP)	12	0x0	VIP host port channel 0 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH1_INT (R) (VIP)	13	0x0	VIP host host channel 1 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH1_INT_AK (W) (VIP)	13	0x0	VIP host port channel 1 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH2_INT (R) (VIP)	14	0x0	VIP host port channel 2 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH2_INT_AK (W) (VIP)	14	0x0	VIP host port channel 2 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH3_INT (R) (VIP)	15	0x0	VIP host port channel 3 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH3_INT_AK (W) (VIP)	15	0x0	VIP host port channel 3 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
I2C_INT (R) (VIP)	17	0x0	I2C interrupt. 0=No event 1=Event has occurred, interrupting if enabled
I2C_INT_AK (W) (VIP)	17	0x0	I2C interrupt acknowledge/reset. 0=No effect 1=Clear status
GUI_IDLE_STAT (R) (RBBM)	19	0x1	GUI idle interrupt. 0=No event 1=Event has occurred, interrupting if enabled

GUI_IDLE_STAT_AK (W) (RBBM)	19	0x0	GUI idle interrupt acknowledge. 0=No effect 1=Clear status
VIPH_INT (R) (VIP)	24	0x0	VIP host port interrupt. 0=No event 1=Event has occurred, interrupting if enabled
SW_INT (R) (HDP)	25	0x0	Software interrupt. General purpose interrupt that can only be set by software event by writing to SW_INT_SET. 0=No event 1=Event has occurred, interrupting if enabled
SW_INT_AK (W) (HDP)	25	0x0	Software interrupt acknowledge. 0=No effect 1=Clear SW_INT (set low)
SW_INT_SET (W) (HDP)	26	0x0	Software interrupt trigger. 0=No effect 1=Set SW_INT active (high)
GUIDMA_STAT (R) (CP)	30	0x0	GUI DMA channel interrupt. 0=No event 1=Event has occurred, interrupting if enabled
GUIDMA_AK (W) (CP)	30	0x0	GUI DMA channel interrupt acknowledge. 0=No effect 1=Clear status
VIDDMA_STAT (R) (CP)	31	0x0	Video capture DMA channel interrupt. 0=No event 1=Event has occurred, interrupting if enabled
VIDDMA_AK (W) (CP)	31	0x0	Video capture DMA channel interrupt acknowledge. 0=No effect 1=Clear status

General Interrupt Status register.

These fields can be polled and acknowledged even if interrupts are disabled, or the respective fields are masked in the GEN\_INT\_CNTL register.

<b>RBBM_CNTL - RW - 32 bits - [IOReg,MMReg:0xEC] [MMReg:0xE44]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
RB_SETTLE	3:0	0xf	Read Daisy Chain Bus Settling Time. (in clocks + 2; minimum time is 2 clocks) Default = 15
ABORTCLKS_HI	6:4	0x0	The number of clocks that we will allow a non-queued write from the Host Interface to stall before it is aborted. A value of 0 means never abort. Default = 0.

ABORTCLKS_CP	10:8	0x0	The number of clocks that we will allow a non-queued write from the Command Processor to stall before it is aborted. A value of 0 means never abort. Default = 0.
ABORTCLKS_CFIFO	14:12	0x0	The number of clocks that we will allow a write from the Command FIFO to stall before it is aborted. A value of 0 means never abort. Default = 0.
CPQ_DATA_SWAP	17	0x0	Endian Swap Control for writes to the Command Stream Queue. 0 = No swap 1 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA Default = 0
NO_ABORT_IDCT	21	0x0	Any write transaction to the IDCT block cannot be aborted. Default = 0.
NO_ABORT_BIOS	22	0x0	Any write transaction to the BIOS block cannot be aborted. Default = 0.
NO_ABORT_FB	23	0x0	Any write transaction to the Feature Block cannot be aborted. Default = 0.
NO_ABORT_CP	24	0x0	Any write transaction to the Command Processor block cannot be aborted. Default = 0.
NO_ABORT_HI	25	0x0	Any write transaction to the Host Interface block cannot be aborted. Default = 0.
NO_ABORT_HDP	26	0x0	Any write transaction to the Host Data Processor block cannot be aborted. Default = 0.
NO_ABORT_MC	27	0x0	Any write transaction to the Memory Controller block cannot be aborted. Default = 0.
NO_ABORT_AIC	28	0x0	Any write transaction to the AGP Interface block cannot be aborted. Default = 0.
NO_ABORT_VIP	29	0x0	Any write transaction to the VIP block cannot be aborted. Default = 0.
NO_ABORT_DISP	30	0x0	Any write transaction to the Display block cannot be aborted. Default = 0.
NO_ABORT_CG	31	0x0	Any write transaction to the CG or CGM blocks cannot be aborted. Default = 0.

Control Register

<b>RBBM_SOFT_RESET - RW - 32 bits - [IOReg,MMReg:0xF0] [MMReg:0xE48]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SOFT_RESET_CP	0	0x0	Soft Reset to the Command Processor block. Default = 0
SOFT_RESET_HI	1	0x0	Soft Reset to the Host Interface block. Default = 0
SOFT_RESET_SE	2	0x0	Soft Reset to the 3D Setup Engine block. Default = 0
SOFT_RESET_RE	3	0x0	Soft Reset to the 3D Raster Engine block. Default = 0
SOFT_RESET_PP	4	0x0	Soft Reset to the 3D Pixel Pipe block. Default = 0
SOFT_RESET_E2	5	0x0	Soft Reset to the 2D Engine block. Default = 0
SOFT_RESET_RB	6	0x0	Soft Reset to the 2D/3D Render Backend block. Default = 0
SOFT_RESET_HDP	7	0x0	Soft Reset to the Host Data Processor block. Default = 0
SOFT_RESET_MC	8	0x0	Soft Reset to the Memory Controller block. Default = 0
SOFT_RESET_AIC	9	0x0	Soft Reset to the AGP Interface block. Default = 0
SOFT_RESET_VIP	10	0x0	Soft Reset to the VIP block. Default = 0
SOFT_RESET_DISP	11	0x0	Soft Reset to the Display block. Default = 0
SOFT_RESET_CG	12	0x0	Soft Reset to Clock Generator blocks. Default = 0

Soft Reset Generation

<b>RBBM_STATUS - R - 32 bits - [MMReg:0xE40] [MMReg:0x1740]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CMDFIFO_AVAIL	6:0	0x40	Number of available entries (doublewords) in the Command FIFO. Default = 64
HIRQ_ON_RBB	8	0x0	There is a request from the Host Interface on the backbone.

CPRQ_ON_RBB	9	0x0	There is a request from the Command Processor on the backbone.
CFRQ_ON_RBB	10	0x0	There is a request from the Command FIFO on the backbone.
HIRQ_IN_RTBUF	11	0x0	There is a request from the Host Interface present in the Retry Buffer.
CPRQ_IN_RTBUF	12	0x0	There is a request from the Command Processor present in the Retry Buffer.
CFRQ_IN_RTBUF	13	0x0	There is a request from the Command FIFO present in the Retry Buffer.
CF_PIPE_BUSY	14	0x0	The Command FIFO pipeline is busy. This indicates that there is something in the command FIFO, or a command fifo request is present further down in the RBBM pipe, eg, on the backbone.
ENG_EV_BUSY	15	0x0	The RBBM's Event Engine is Busy. That is, we are waiting for a WAIT_UNTIL synchronization event.
CP_CMDSTRM_BUSY	16	0x0	The Command Processor's Command Stream is Busy. This covers from the Ring Buffer (in memory) through the CP's internal processing pipeline.
E2_BUSY	17	0x0	2D Engine is Busy
RB2D_BUSY	18	0x0	2D portion of Render Backend is Busy
RB3D_BUSY	19	0x0	3D portion of Render Backend is Busy
SE_BUSY	20	0x0	3D Setup Engine is Busy
RE_BUSY	21	0x0	3D Raster Engine is Busy
TAM_BUSY	22	0x0	3D Texture Address Module (sub-block of Pixel Pipe) is Busy
TDM_BUSY	23	0x0	3D Texture Data Module (sub-block of Pixel Pipe) is Busy
PB_BUSY	24	0x0	3D Pixel Blender (sub-block of Pixel Pipe) is Busy
GUI_ACTIVE	31	0x0	2D engine busy OR 3D engine busy OR Command FIFO not empty OR CP Microengine busy OR Command Stream Queue not empty OR Ring Buffer not empty

Status Register

WAIT_UNTIL - RW - 32 bits - [MMReg:0x1720]			
Field Name	Bits	Default	Description
WAIT_CRTC_PFLIP	0	0x0	Wait for the 'Pending Flip' signal to be OFF
WAIT_RE_CRTC_VLINE	1	0x0	Wait for Rising Edge of CRTC_VLINE signal
WAIT_FE_CRTC_VLINE	2	0x0	Wait for Falling Edge of CRTC_VLINE signal
WAIT_CRTC_VLINE	3	0x0	Wait for CRTC_VLINE signal to be ON
WAIT_DMA_VIPH0_IDLE	4	0x0	Wait for VIP Host DMA Channel 0 to be idle
WAIT_DMA_VIPH1_IDLE	5	0x0	Wait for VIP Host DMA Channel 1 to be idle
WAIT_DMA_VIPH2_IDLE	6	0x0	Wait for VIP Host DMA Channel 2 to be idle
WAIT_DMA_VIPH3_IDLE	7	0x0	Wait for VIP Host DMA Channel 3 to be idle
WAIT_DMA_VID_IDLE	8	0x0	Wait for VID DMA Channel to be idle
WAIT_DMA_GUI_IDLE	9	0x0	Wait for GUI DMA Channel to be idle
WAIT_CMDFIFO	10	0x0	Wait until there are at least CMDFIFO_ENTRIES number of occupied entries in the Command FIFO. Used to 'batch-up' a group of writes, to ensure they get written within a short time period of each other.
WAIT_OV0_FLIP	11	0x0	Wait for Overlay Flip signal to be ON
WAIT_OV0_SLICEDONE	12	0x0	Wait for Overlay Slice Done signal to be ON
WAIT_2D_IDLE	14	0x0	Wait for 2D engine (including 2D render backend) to be idle
WAIT_3D_IDLE	15	0x0	Wait for 3D engine (including 3D render backend) to be idle
WAIT_2D_IDLECLEAN	16	0x0	Wait for 2D engine to be idle and 2D render backend to be clean and Memory Controller to be clean of 2D destination data
WAIT_3D_IDLECLEAN	17	0x0	Wait for 3D engine to be idle and 3D render backend to be clean and Memory Controller to be clean of 3D destination data
WAIT_HOST_IDLECLEAN	18	0x0	Wait for Host Interface/Host Data Path to be idle and clean
WAIT_EXTERN_SIG	19	0x0	Wait for External Signal (from VIP block) to be ON
CMDFIFO_ENTRIES	26:20	0x0	Number of entries to wait for if the WAIT_CMDFIFO bit is ON

This register is for Explicit Synchronization.

A write to this register will travel through the Command FIFO, and when it gets to the bottom of the FIFO, the write will stall until its condition(s) is/are met. If multiple conditions are being tested, they \*all\* must be true in order to un-stall the write. While it is stalled, other writes can continue to fill-up the Command FIFO behind it.

NQWAIT_UNTIL - W - 32 bits - [MMReg:0xE50]			
Field Name	Bits	Default	Description
WAIT_GUI_IDLE	0	0x0	Wait for 2D and 3D engines to be idle, and for Command FIFO to be empty.

This register is for Explicit Synchronization.

A write to this register will stall \*at the top of the Command FIFO\*, so that the entire FIFO has to flush before this write can become un-stalled. This technique helps you control ordering of a write to a non-queued register (particularly, the IDCT registers, which are the only non-queued registers in the Command Processor's address-space), to make sure it happens after a certain group of writes to the queued registers.

\*\*This register is not implemented in the host's address space; only the CP's\*\*

ISYNC_CNTL - RW - 32 bits - [MMReg:0x1724]			
Field Name	Bits	Default	Description
ISYNC_ANY2D_IDLE3D	0	0x0	A write to any 2D Engine register stalls if the 3D Engine is busy OR the Render Backend is not clean of 3D destination data OR the Memory Controller is not clean of 3D destination data. Default = 0.
ISYNC_ANY3D_IDLE2D	1	0x0	A write to any 3D Engine register stalls if the 2D Engine is busy OR the Render Backend is not clean of 3D destination data OR the Memory Controller is not clean of 3D destination data. Default = 0.
ISYNC_TRIG2D_IDLE3D	2	0x0	A write to any 2D trigger register stalls if the 3D Engine is busy OR the Render Backend is not clean of 3D destination data OR the Memory Controller is not clean of 3D destination data. The 2D trigger registers are: DST_WIDTH_HEIGHT DST_HEIGHT_WIDTH DST_HEIGHT_WIDTH_8 DST_WIDTH_X DST_WIDTH_X_INCY DP_GUI_MASTER_CNTL DP_DATATYPE DP_WRITE_MSK DP_MIX CLR_CMP_CNTL RB2D_WRITEBACK_DATA_LO RB2D_WRITEBACK_DATA_HI RB2D_WRITEBACK_ADDR RB2D_DSTCACHE_CTLSTAT Default = 0.

ISYNC_TRIG3D_IDLE2D	3	0x0	A write to any 3D trigger register stalls if the 2D Engine is busy OR the Render Backend is not clean of 2D destination data OR the Memory Controller is not clean of 2D destination data. The 3D trigger registers are: SE_VF_CNTL RE_E2_3 PP_CNTL PP_MC_CONTEXT RB3D_WRITEBACK_DATA_LO RB3D_WRITEBACK_DATA_HI RB3D_WRITEBACK_ADDR RB3D_CNTL RB3D_PLANEMASK RB3D_BLEND_CNTL RB3D_ROPCNTL RB3D_DSTCACHE_CTLSTAT Default = 0.
ISYNC_WAIT_IDLEGUI	4	0x0	A write to the WAIT_UNTIL register stalls if the 2D or 3D Engine is busy. Default = 0.
ISYNC_CPSCRATCH_IDLEGUI	5	0x0	A write to any of the CP's GUI ScratchPad Registers stalls if the 2D or 3D Engine is busy. (For Rage128 compatibility) Default = 0.

Implicit Synchronization Control

RBBM_GUICNTL - RW - 32 bits - [MMReg:0x172C]			
Field Name	Bits	Default	Description
HOST_DATA_SWAP	1:0	0x0	Endian Swap Control for 'Host Data' writes to 2D engine. 0 = No swap 1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC 2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA 3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB Default = 0

GUI Control

RBBM_CMDFIFO_ADDR - W - 32 bits - [MMReg:0xE70]			
Field Name	Bits	Default	Description
CMDFIFO_ADDR	5:0	0x0	Address into the Command FIFO which is to be read from. Used for debug, to read the contents of the Command FIFO.

Command FIFO Address

<b>RBBM_CMDFIFO_DATA_L - R - 32 bits - [MMReg:0xE74]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CMDFIFO_DATA_L	31:0	0x0	Data from the Command FIFO, from location pointed to by the RBBM_CMDFIFO_ADDR register. Used for debug, to read the contents of the Command FIFO.

Command FIFO Data Low

<b>RBBM_CMDFIFO_DATA_H - R - 32 bits - [MMReg:0xE78]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CMDFIFO_DATA_H	11:0	0x0	Upper Data from the Command FIFO, from location pointed to by the RBBM_CMDFIFO_ADDR register. Used for debug, to read the contents of the Command FIFO. These bits contain the register-space Address and the Byte Enables.

Command FIFO Data High

<b>RBBM_CMDFIFO_STAT - R - 32 bits - [MMReg:0xE7C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CMDFIFO_RPTR	5:0	0x0	Current Read Pointer into the Command FIFO. Default = 0.
CMDFIFO_WPTR	13:8	0x0	Current Write Pointer into the Command FIFO. Default = 0.

Command FIFO Status

## 2.3 CG Registers

General description of the clock generator block.

### Clock Generator Control Registers

CLK_PWRMGT_CNTL - RW - 32 bits - CLKIND:0x14			
Field Name	Bits	Default	Description
MPLL_PWRMGT_OFF (CGM)	0	0x0	M domain clock power management off
SPLL_PWRMGT_OFF (CG)	1	0x0	S domain clock power management off
PPLL_PWRMGT_OFF (CG)	2	0x0	Pixel clock power management off
MCLK_TURNOFF (CGM)	4	0x0	Turn off M domain clocks
SCLK_TURNOFF (CG)	5	0x0	Turn off S domain clocks
PCLK_TURNOFF (CG)	6	0x0	Turn off pixel clocks
MC_CH_MODE (CGM)	8	0x1	Single/Dual channel mode control for memory controller 0=single channel 1=dual channel
TEST_MODE (CG) (CGM)	9	0x0	Disable long internal timing to speed up regression tests
GLOBAL_PMAN_EN (CG)	10	0x0	0=Power management off 1=Power management on
ENGINE_DYNCLK_MODE (CG)	12	0x1	0=Provide Clock for each Eng block separately 1=Treat Engine as one single block
MC_BUSY (R) (CGM)	16	0x0	0=MC is idle 1=MC is busy

MC_INT_CNTL (CGM)	17	0x0	0=HW control 1=SW over-ride
MC_SWITCH (CGM)	18	0x0	0=source of memory clock is not changed 1=source of memory clock is changed
DLL_READY (CGM)	19	0x0	0=DLL is not ready 1=DLL is ready
CG_NO1_DEBUG (CG) (CGM)	31:24	0x0	1st 16-bit hardware debug register

Clock power management control

<b>PLL_PWRMGT_CNTL - RW - 32 bits - CLKIND:0x15</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
MPLL_TURNOFF (CGM)	0	0x0	Enable M domain PLL to be turned off at power state D3
SPLL_TURNOFF (CG)	1	0x0	Enable S domain PLL to be turned off at power state D3
PPLL_TURNOFF (CG)	2	0x0	Enable pixel clock PLL to be turned off at power state D3
CG_NO2_DEBUG (CG) (CGM)	31:24	0x0	2nd 16-bit hardware debug register

PLL power management control

## 2.4 MemoryController Registers

### Memory Controller Registers

MEM_CNTL - RW - 32 bits - [MMReg:0x140]			
Field Name	Bits	Default	Description
MEM_NUM_CHANNELS	0	0x0	Defines whether 1 or 2 memory channels are to be used. 0=One channel 1=Two channels
MC_USE_B_CH_ONLY	1	0x0	In a 1-channel system, defines whether to use the A or B channel. NOTE: B-channel only not supported for Rage 6A 0=Use A channel in 1 channel system 1=Use B channel in 1 channel system
DISABLE_AP	2	0x0	When set, instructs MC to disable precharging of banks. Useful only for HW debug or auto-detection of memory configuration. NOTE: Not supported for Rage 6A. 0=Auto-Precharge Enabled 1=Auto-Precharge Disabled
MEM_BANK_MAPPING_A	7:4	0x0	Reserved for future use. 0=Reserved

MEM_ADDR_MAPPING_A	15:8	0x0	<p>Defines the memory configuration in the A channel. (Bit definitions relative to 8-bit field)</p> <p>(7) : Ranks - Groups of devices sharing common CS 0 = 1 rank 1 = 2 ranks</p> <p>(6:5) : Banks per device 0 = 2 banks 1 = 4 banks 2 = 8 banks (not supported for Rage 6A) 3 = not supported</p> <p>(4:2) : Rows per bank 0 = 2**9 rows 1 = 2**10 rows 2 = 2**11 rows 3 = 2**12 rows 4 = 2**13 rows 5-7 = not supported</p> <p>(1:0) : Columns per page 0 = 128 columns (not supported for Rage 6A) 1 = 256 columns 2 = 512 columns 3 = not supported</p>
MEM_BANK_MAPPING_B	23:20	0x0	Reserved for future use. 0=Reserved
MEM_ADDR_MAPPING_B	31:24	0x0	Defines the memory configuration in the B channel. See MEM_ADDR_MAPPING_A for field details.

This register defines the physical configuration of frame buffer memory and how it is mapped to the chip internal address space.

MC_FB_LOCATION - RW - 32 bits - [MMReg:0x148]			
Field Name	Bits	Default	Description
MC_FB_START (MC) (HDP)	15:0	0x0	<p>Start of local frame buffer section of 32 bit internal address space. Recommend setting this register to same as CONFIG_APER_0_BASE.APER_0_BASE shr 16.</p> <p>NOTE: Bits 0:5 of this field are hardwired to ZERO.</p>
MC_FB_TOP (MC)	31:16	0x3f	<p>End of local frame buffer section of 32 bit internal address space. Recommend setting this register to (CONFIG_APER_0_BASE.APER_0_BASE + CONFIG_APER_SIZE.APER_SIZE - 1) shr 16.</p> <p>NOTE: Bits 0:5 of this field are hardwired to ONE.</p>

This register defines the location of the frame buffer in the internal address space. The internal address space has 32 address bits. Minimum Frame buffer size for Rage 5 is 2 MB, and the start location is required to be on a 4 MB boundary. Therefore START(21:0) must be 0x000000 and TOP(21:0) must be 0x3FFFFFF. Only the 16 MSBs of each are loaded in the register.

<b>MC_AGP_LOCATION - RW - 32 bits - [MMReg:0x14C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
MC_AGP_START	15:0	0x0	Start location of AGP aperture. Load 16 MSBs only. LSBs assumed to be 0x0.  NOTE: Bits 0:5 of this field are hardwired to ZERO.
MC_AGP_TOP	31:16	0x3f	Top location within AGP aperture. Load 16 MSBs only. LSBs assumed to be 0xFFFF.  NOTE: Bits 0:5 of this field are hardwired to ONE.

Defines the location of AGP in the chip internal address space.  
Aperture must be aligned to a 4 MB boundary.

<b>MEM_INIT_LATENCY_TIMER - RW - 32 bits - [MMReg:0x154]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
MEM_RB0R_INIT_LAT	3:0	0x0	The arbiter will increase the priority of a request (ignoring efficiency) if a request is not selected within (INIT_LAT*16) MCLKs. Timer is started when request reaches the arbiter, not when request is received by MC.  Timeout setting for RB0 read requests
MEM_RB1R_INIT_LAT	7:4	0x0	Timeout setting for RB1 read requests
MEM_PPR_INIT_LAT	11:8	0x0	Timeout setting for Pixel Pipe read requests
MEM_DISPR_INIT_LAT	15:12	0x0	Timeout setting for Display read requests
MEM_RB0W_INIT_LAT	19:16	0x0	Timeout setting for RB0 write requests
MEM_RB1W_INIT_LAT	23:20	0x0	Timeout setting for RB1 write requests
MEM_FIXED_INIT_LAT	27:24	0x0	Timeout setting for fixed priority client arbitration winner. Timer is started when request wins fixed priority arbitration.
SAME_PAGE_PRIO	30:28	0x0	Indicates that (VALUE+1) consecutive page hits are needed before the arbiter may switch to another bank in the same device with no timing penalty.

This register provides controls used to trade off memory efficiency and request latency.

MEM_SDRAM_MODE_REG - RW - 32 bits - [MMReg:0x158]			
Field Name	Bits	Default	Description
MEM_MODE_REG	14:0	0x0	Value to be loaded in SDRAM mode or extended mode register
MEM_RBS_POSITION_A	17:16	0x0	Used to advance or delay capture of read data coming from A channel IO pads 0=Nominal 1=Advance 1 clock 2=Delay 1 clock 3=Not Used
MEM_RBS_POSITION_B	19:18	0x0	Used to advance or delay capture of read data coming from B channel IO pads 0=Nominal 1=Advance 1 clock 2=Delay 1 clock 3=Not Used
MEM_CAS_LATENCY	22:20	0x0	Must match CAS latency programmed into MEM_MODE_REG 1=1 clock 2=2 clocks 3=3 clocks 5=1.5 clocks 6=2.5 clocks
WR_LAT_EQ_CAS_LAT	23	0x0	Reserved. Must be programmed to '0' 0=Default WR Latency 1=Use CAS Latency for WR Latency
MEM_ERST_POSITION_A	25:24	0x0	Used to advance or delay the A channel ERST signal, which indicates to the IO pads when to begin capturing a burst of read data. 0=Nominal 1=Advance 1 clock 2=Delay 1 clock 3=Not Used
MEM_ERST_POSITION_B	27:26	0x0	Used to advance or delay the B channel ERST signal, which indicates to the IO pads when to begin capturing a burst of read data. 0=Nominal 1=Advance 1 clock 2=Delay 1 clock 3=Not Used
MC_INIT_COMPLETE	28	0x0	As long as this bit is '0', the MC will not accept requests from the clients. Used primarily to block requests when the MC might mishandle them, such as when the FB or AGP apertures are undefined or unstable. 0=Register Initialization Not Complete 1=Register Initialization Complete

MEM_NON_JEDEC	29	0x0	This bit should be set when using a DDR memory which has no internal delay-locked loop (DLL). Ignored for SDR memory. 0=JEDEC 1=1 Non-JEDEC
MEM_CFG_TYPE	30	0x0	0=SDR 1=DDR
MEM_SDRAM_RESET	31	0x0	The MC will program the SDRAM mode register on a transition from 0 to 1 0=Normal 1=Reset

Register used to control the programming of the SDRAM mode register.

Also contains controls used to compensate for different CAS latency settings, SDR/DDR differences, and variations in board-level timing.

EXT_MEM_CNTL - RW - 32 bits - [MMReg:0x144]			
Field Name	Bits	Default	Description
MEM_TRP	1:0	0x0	Min time from Precharge to RAS in same bank 0=1 clock 1=2 clocks 2=3 clocks 3=4 clocks
MEM_TRCD	3:2	0x0	Min RAS to CAS delay in same bank 0=1 clock 1=2 clocks 2=3 clocks 3=4 clocks
MEM_TRAS	6:4	0x0	Min time between RAS operations in same bank 0=1 clock 1=2 clocks 2=3 clocks 3=4 clocks 4=5 clocks 5=6 clocks 6=7 clocks 7=8 clocks
MEM_TRRD	9:8	0x0	Min time between RAS operations in different banks of same device 0=1 clock 1=2 clocks 2=3 clocks 3=4 clocks

MEM_TR2W	11:10	0x0	Min Read to Write turnaround time 0=0 clock 1=1 clocks 2=2 clocks 3=3 clocks
MEM_TWR	13:12	0x0	Write Recovery time 0=1 clock 1=2 clocks 2=3 clocks 3=4 clocks
MEM_TW2R	15:14	0x0	Write to Read turnaround time Not implemented in Rage 6A - see MEM_TWR_MODE 0=0 clock 1=1 clocks 2=2 clocks 3=3 clocks
MEM_TR2R	17:16	0x0	Read to Read (rank switch) time 0=0 clock 1=1 clocks 2=2 clocks 3=3 clocks
MEM_TWR_MODE	18	0x0	When set, use TWR timer for TW2R. Otherwise, use 0 clocks. 0=Ignore TWR Rule 1=Use TWR Rule
MEM_REFRESH_DIS	20	0x0	Disables all refreshing when set 0=Not Disabled 1=Disabled
MEM_REFRESH_RATE	31:24	0x0	One memory refresh is performed every ( MEM_REFRESH_RATE+1 ) * 64 MCLK cycles.

Defines the SDRAM timing parameters and refresh rate.

## 2.5 HostDatapath Registers

### Host Datapath Control Registers

HOST_PATH_CNTL - RW - 32 bits - [MMReg:0x130]			
Field Name	Bits	Default	Description
HDP_APER_CNTL	23	0x0	Selects how the two PCI linear memory apertures map into the internal 32bit address space of the graphics controller. 0=Both host apertures map to same area in MC address space (starting at MC_FB_START). Surface ranges are limited to the size of CONFIG_APER_SIZE. 1=Two host apertures are mapped one above the other in MC address space starting at MC_FP_START. i.e. they become one big aperture. Surface ranges can cover the double size of CONFIG_APER_SIZE.
HP_LIN_RD_CACHE_DIS	24	0x0	Selects whether to disable HDP prefetching. 0=HDP prefetching enabled. 1=HDP prefetching disabled.
HP_RBBM_LOCK_DIS	25	0x0	Controls coherency between linear aperture cycles and register cycles that affect linear aperture operation (e.g. changing SURFACE registers or VGA write/read mode). This field should normally be 0 to ensure proper coherency, and should be changed only if needed to avoid deadlock problems. 0=The RBBM write requests will be held until the data pipe is idle. 1=The RBBM write requests will not be held.
HDP_SOFT_RESET	26	0x0	Software reset for HDP. 0=HDP running in normal operating mode 1=Soft Reset to HDP
HDP_WRITE_COMBINER_TIMEOUT	30:28	0x0	Controls internal timeout for write combining optimization. This allows separate dword writes to be combined into octawords before sending to the internal memory controller. This reduces bandwidth cost of slave writes and increases performance. It is recommended this register be set to 0x7 (28 BCLKs) unless otherwise noted. 0=0 BCLK 1=4 BCLK 2=8 BCLK 3=12 BCLK 4=16 BCLK 5=20 BCLK 6=24 BCLK 7=28 BCLK
HP_TEST_RST_CNTL	31	0x0	For HW test and debugging only. No use to software.

Controls for the Merged Register Bus internal to the controller for non-FIFOed register writes, and all register reads

<b>SW_SEMAPHORE - RW - 32 bits - [MMReg:0x13C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SW_SEMAPHORE	15:0	0x0	Scratch register for use by software to implement status flags and semaphores. No affect on the hardware.

Scratch register

<b>SURFACE_CNTL - RW - 32 bits - [MMReg:0xB00]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SURF_TRANSLATION_DIS	8	0x1	Disable register for Tiling address translation. 0=Enable tiling translation based on SURFACE registers. 1=Disable tiling based on SURFACE registers. Swapping still based on SURFACE comparisons and settings.
NONSURF_AP0_SWP	21:20	0x0	Endian Swap control for Aperture 0 accesses not in a surface. Always used when SURF_TRANSLATION_DIS is set to 1. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
NONSURF_AP1_SWP	23:22	0x0	Endian Swap control for Aperture 1 accesses not in a surface. Always used when SURF_TRANSLATION_DIS is set to 1. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.

General Tiling Control Registers

<b>SURFACE0_INFO - RW - 32 bits - [MMReg:0xB0C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SURF0_PITCHSEL	9:0	0x0	Pitch in octawords (16 bytes) of Surface 0. A value of 0 disables tiling in Surface 0. For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512. For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514. For 16-bit Z tiling the pitch may be in 1 octoword increments from 1 to 257. Pitch bits less than min increment are ignored.

SURF0_TILE_MODE	17:16	0x0	Mode of tiling for Surface 0. Set SURF0_PITCHSEL to 0 to disable tiling surface 0. 0=Color macro tiling (no micro tiling). 1=Color macro&micro tiling. 2=32 bit Z tiling. 3=16 bit Z tiling.
SURF0_AP0_SWP	21:20	0x0	Endian swap control for Aperture 0 accesses in Surface 0. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
SURF0_AP1_SWP	23:22	0x0	Endian swap control for Aperture 1 accesses in Surface 0. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
SURF0_WRITE_FLAG <i>(mirror of SURFACE_ACCESS_FLAGS:SURF0_WRITE_FLAG) (R)</i>	24	0x0	Indicates if write to surface 0 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF0_READ_FLAG <i>(mirror of SURFACE_ACCESS_FLAGS:SURF0_READ_FLAG) (R)</i>	25	0x0	Indicates if read to surface 0 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.

Control register for Surface 0

SURFACE0_LOWER_BOUND - RW - 32 bits - [MMReg:0xB04]			
Field Name	Bits	Default	Description
SURF_LOWER	27:0	0x0	Starting address of lowest tile in Surface 0.  NOTE: Bits 0:10 of this field are hardwired to ZERO.

Surface 0 Lower Bound Register

SURFACE0_UPPER_BOUND - RW - 32 bits - [MMReg:0xB08]			
Field Name	Bits	Default	Description
SURF_UPPER	27:0	0x7ff	Starting address of highest tile in Surface 0.  NOTE: Bits 0:10 of this field are hardwired to ONE.

Surface 0 Upper Bound Register

SURFACE1_INFO - RW - 32 bits - [MMReg:0xB1C]			
Field Name	Bits	Default	Description
SURF1_PITCHSEL	9:0	0x0	Pitch in octawords (16 bytes) of Surface 1. A value of 0 disables tiling in Surface 0. For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512. For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514. For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257. Pitch bits less than min increment are ignored.
SURF1_TILE_MODE	17:16	0x0	Mode of tiling for Surface 1. Set SURF1_PITCHSEL to 0 to disable tiling surface 1. 0=Color macro tiling (no micro tiling). 1=Color macro&micro tiling. 2=32 bit Z tiling. 3=16 bit Z tiling.
SURF1_AP0_SWP	21:20	0x0	Endian swap control for Aperture 0 accesses in Surface 1. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
SURF1_AP1_SWP	23:22	0x0	Endian swap control for Aperture 1 accesses in Surface 1. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
SURF1_WRITE_FLAG <i>(mirror of SURFACE_ACCESS_FLAGS:SURF1_WRITE_FLAG) (R)</i>	24	0x0	Indicates if write to surface 1 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF1_READ_FLAG <i>(mirror of SURFACE_ACCESS_FLAGS:SURF1_READ_FLAG) (R)</i>	25	0x0	Indicates if read to surface 1 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.

Control register for Surface 1

SURFACE1_LOWER_BOUND - RW - 32 bits - [MMReg:0xB14]			
Field Name	Bits	Default	Description
SURF_LOWER	27:0	0x0	Starting address of lowest tile in Surface 1.  NOTE: Bits 0:10 of this field are hardwired to ZERO.

Surface 1 Lower Bound Register

SURFACE1_UPPER_BOUND - RW - 32 bits - [MMReg:0xB18]			
Field Name	Bits	Default	Description
SURF_UPPER	27:0	0x7ff	Starting address of highest tile in Surface 1.  NOTE: Bits 0:10 of this field are hardwired to ONE.

Surface 1 Upper Bound Register

SURFACE2_INFO - RW - 32 bits - [MMReg:0xB2C]			
Field Name	Bits	Default	Description
SURF2_PITCHSEL	9:0	0x0	Pitch in octawords (16 bytes) of Surface 2. A value of 0 disables tiling in Surface 0. For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512. For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514. For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257. Pitch bits less than min increment are ignored.
SURF2_TILE_MODE	17:16	0x0	Mode of tiling for Surface 2. Set SURF2_PITCHSEL to 0 to disable tiling surface 2. 0=Color macro tiling (no micro tiling). 1=Color macro&micro tiling. 2=32 bit Z tiling. 3=16 bit Z tiling.
SURF2_AP0_SWP	21:20	0x0	Endian swap control for Aperture 0 accesses in Surface 2. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
SURF2_AP1_SWP	23:22	0x0	Endian swap control for Aperture 1 accesses in Surface 2. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
SURF2_WRITE_FLAG  <i>(mirror of SURFACE_ACCESS_FLAGS:SURF2_WRITE_FLAG) (R)</i>	24	0x0	Indicates if write to surface 2 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF2_READ_FLAG  <i>(mirror of SURFACE_ACCESS_FLAGS:SURF2_READ_FLAG) (R)</i>	25	0x0	Indicates if read to surface 2 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.

Control register for Surface 2

<b>SURFACE2_LOWER_BOUND - RW - 32 bits - [MMReg:0xB24]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SURF_LOWER	27:0	0x0	Starting address of lowest tile in Surface 2.  NOTE: Bits 0:10 of this field are hardwired to ZERO.

Surface 2 Lower Bound Register

<b>SURFACE2_UPPER_BOUND - RW - 32 bits - [MMReg:0xB28]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SURF_UPPER	27:0	0x7ff	Starting address of highest tile in Surface 2.  NOTE: Bits 0:10 of this field are hardwired to ONE.

Surface 2 Upper Bound Register

<b>SURFACE3_INFO - RW - 32 bits - [MMReg:0xB3C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SURF3_PITCHSEL	9:0	0x0	Pitch in octawords (16 bytes) of Surface 3. A value of 0 disables tiling in Surface 0. For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512. For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514. For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257. Pitch bits less than min increment are ignored.
SURF3_TILE_MODE	17:16	0x0	Mode of tiling for Surface 3. Set SURF3_PITCHSEL to 0 to disable tiling surface 3. 0=Color macro tiling (no micro tiling). 1=Color macro&micro tiling. 2=32 bit Z tiling. 3=16 bit Z tiling.
SURF3_AP0_SWP	21:20	0x0	Endian swap control for Aperture 0 accesses in Surface 3. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
SURF3_AP1_SWP	23:22	0x0	Endian swap control for Aperture 1 accesses in Surface 3. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.

SURF3_WRITE_FLAG <i>(mirror of SURFACE_ACCESS_FLAGS:SURF3_WRITE_FLAG) (R)</i>	24	0x0	Indicates if write to surface 3 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF3_READ_FLAG <i>(mirror of SURFACE_ACCESS_FLAGS:SURF3_READ_FLAG) (R)</i>	25	0x0	Indicates if read to surface 3 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.

Control register for Surface 3

SURFACE3_LOWER_BOUND - RW - 32 bits - [MMReg:0xB34]			
Field Name	Bits	Default	Description
SURF_LOWER	27:0	0x0	Starting address of lowest tile in Surface 3.  NOTE: Bits 0:10 of this field are hardwired to ZERO.

Surface 3 Lower Bound Register

SURFACE3_UPPER_BOUND - RW - 32 bits - [MMReg:0xB38]			
Field Name	Bits	Default	Description
SURF_UPPER	27:0	0x7ff	Starting address of highest tile in Surface 3.  NOTE: Bits 0:10 of this field are hardwired to ONE.

Surface 3 Upper Bound Register

SURFACE4_INFO - RW - 32 bits - [MMReg:0xB4C]			
Field Name	Bits	Default	Description
SURF4_PITCHSEL	9:0	0x0	Pitch in octawords (16 bytes) of Surface 4. A value of 0 disables tiling in Surface 0. For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512. For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514. For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257. Pitch bits less than min increment are ignored.

SURF4_TILE_MODE	17:16	0x0	Mode of tiling for Surface 4. Set SURF4_PITCHSEL to 0 to disable tiling surface 4. 0=Color macro tiling (no micro tiling). 1=Color macro&micro tiling. 2=32 bit Z tiling. 3=16 bit Z tiling.
SURF4_AP0_SWP	21:20	0x0	Endian swap control for Aperture 0 accesses in Surface 4. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
SURF4_AP1_SWP	23:22	0x0	Endian swap control for Aperture 1 accesses in Surface 4. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
SURF4_WRITE_FLAG <i>(mirror of SURFACE_ACCESS_FLAGS: SURF4_WRITE_FLAG) (R)</i>	24	0x0	Indicates if write to surface 4 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF4_READ_FLAG <i>(mirror of SURFACE_ACCESS_FLAGS: SURF4_READ_FLAG) (R)</i>	25	0x0	Indicates if read to surface 4 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.

Control register for Surface 4

SURFACE4_LOWER_BOUND - RW - 32 bits - [MMReg:0xB44]			
Field Name	Bits	Default	Description
SURF_LOWER	27:0	0x0	Starting address of lowest tile in Surface 4.  NOTE: Bits 0:10 of this field are hardwired to ZERO.

Surface 4 Lower Bound Register

SURFACE4_UPPER_BOUND - RW - 32 bits - [MMReg:0xB48]			
Field Name	Bits	Default	Description
SURF_UPPER	27:0	0x7ff	Starting address of highest tile in Surface 4.  NOTE: Bits 0:10 of this field are hardwired to ONE.

Surface 4 Upper Bound Register

SURFACE5_INFO - RW - 32 bits - [MMReg:0xB5C]			
Field Name	Bits	Default	Description
SURF5_PITCHSEL	9:0	0x0	Pitch in octawords (16 bytes) of Surface 5. A value of 0 disables tiling in Surface 0. For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512. For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514. For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257. Pitch bits less than min increment are ignored.
SURF5_TILE_MODE	17:16	0x0	Mode of tiling for Surface 5. Set SURF5_PITCHSEL to 0 to disable tiling surface 5. 0=Color macro tiling (no micro tiling). 1=Color macro&micro tiling. 2=32 bit Z tiling. 3=16 bit Z tiling.
SURF5_AP0_SWP	21:20	0x0	Endian swap control for Aperture 0 accesses in Surface 5. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
SURF5_AP1_SWP	23:22	0x0	Endian swap control for Aperture 1 accesses in Surface 5. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
SURF5_WRITE_FLAG <i>(mirror of SURFACE_ACCESS_FLAGS:SURF5_WRITE_FLAG) (R)</i>	24	0x0	Indicates if write to surface 5 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF5_READ_FLAG <i>(mirror of SURFACE_ACCESS_FLAGS:SURF5_READ_FLAG) (R)</i>	25	0x0	Indicates if read to surface 5 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.

Control register for Surface 5

SURFACE5_LOWER_BOUND - RW - 32 bits - [MMReg:0xB54]			
Field Name	Bits	Default	Description
SURF_LOWER	27:0	0x0	Starting address of lowest tile in Surface 5.  NOTE: Bits 0:10 of this field are hardwired to ZERO.

Surface 5 Lower Bound Register

SURFACE5_UPPER_BOUND - RW - 32 bits - [MMReg:0xB58]			
Field Name	Bits	Default	Description
SURF_UPPER	27:0	0x7ff	Starting address of highest tile in Surface 5.  NOTE: Bits 0:10 of this field are hardwired to ONE.

Surface 5 Upper Bound Register

SURFACE6_INFO - RW - 32 bits - [MMReg:0xB6C]			
Field Name	Bits	Default	Description
SURF6_PITCHSEL	9:0	0x0	Pitch in octawords (16 bytes) of Surface 6. A value of 0 disables tiling in Surface 0. For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512. For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514. For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257. Pitch bits less than min increment are ignored.
SURF6_TILE_MODE	17:16	0x0	Mode of tiling for Surface 6. Set SURF6_PITCHSEL to 0 to disable tiling surface 6. 0=Color macro tiling (no micro tiling). 1=Color macro&micro tiling. 2=32 bit Z tiling. 3=16 bit Z tiling.
SURF6_AP0_SWP	21:20	0x0	Endian swap control for Aperture 0 accesses in Surface 6. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
SURF6_AP1_SWP	23:22	0x0	Endian swap control for Aperture 1 accesses in Surface 6. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
SURF6_WRITE_FLAG <i>(mirror of SURFACE_ACCESS_FLAGS:SURF6_WRITE_FLAG) (R)</i>	24	0x0	Indicates if write to surface 6 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF6_READ_FLAG <i>(mirror of SURFACE_ACCESS_FLAGS:SURF6_READ_FLAG) (R)</i>	25	0x0	Indicates if read to surface 6 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.

Control register for Surface 6

<b>SURFACE6_LOWER_BOUND - RW - 32 bits - [MMReg:0xB64]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SURF_LOWER	27:0	0x0	Starting address of lowest tile in Surface 6.  NOTE: Bits 0:10 of this field are hardwired to ZERO.

Surface 6 Lower Bound Register

<b>SURFACE6_UPPER_BOUND - RW - 32 bits - [MMReg:0xB68]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SURF_UPPER	27:0	0x7ff	Starting address of highest tile in Surface 6.  NOTE: Bits 0:10 of this field are hardwired to ONE.

Surface 6 Upper Bound Register

<b>SURFACE7_INFO - RW - 32 bits - [MMReg:0xB7C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SURF7_PITCHSEL	9:0	0x0	Pitch in octawords (16 bytes) of Surface 7. A value of 0 disables tiling in Surface 0. For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512. For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514. For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257. Pitch bits less than min increment are ignored.
SURF7_TILE_MODE	17:16	0x0	Mode of tiling for Surface 7. Set SURF7_PITCHSEL to 0 to disable tiling surface 7. 0=Color macro tiling (no micro tiling). 1=Color macro&micro tiling. 2=32 bit Z tiling. 3=16 bit Z tiling.
SURF7_AP0_SWP	21:20	0x0	Endian swap control for Aperture 0 accesses in Surface 7. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.
SURF7_AP1_SWP	23:22	0x0	Endian swap control for Aperture 1 accesses in Surface 7. 0=Little endian: no swapping. 1=Big endian: 16-bit swapping. 2=Big endian: 32-bit swapping.

SURF7_WRITE_FLAG  <i>(mirror of SURFACE_ACCESS_FLAGS:SURF7_WRITE_FLAG) (R)</i>	24	0x0	Indicates if write to surface 7 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF7_READ_FLAG  <i>(mirror of SURFACE_ACCESS_FLAGS:SURF7_READ_FLAG) (R)</i>	25	0x0	Indicates if read to surface 7 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.

Control register for Surface 7

<b>SURFACE7_LOWER_BOUND - RW - 32 bits - [MMReg:0xB74]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SURF_LOWER	27:0	0x0	Starting address of lowest tile in Surface 7.  NOTE: Bits 0:10 of this field are hardwired to ZERO.

Surface 7 Lower Bound Register

<b>SURFACE7_UPPER_BOUND - RW - 32 bits - [MMReg:0xB78]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SURF_UPPER	27:0	0x7ff	Starting address of highest tile in Surface 7.  NOTE: Bits 0:10 of this field are hardwired to ONE.

Surface 7 Upper Bound Register

## 2.6 Display Registers

### Display Control Registers

## 2.7 BaseDisplay Registers

### Base Display Control Registers

GENFC_RD - R - 8 bits - VGA_IO:0x3CA			
Field Name	Bits	Default	Description
VSYNC_SEL_R <i>(mirror of GENFC_WT:VSYNC_SEL_W)</i>	3	0x0	Vertical sync select (read). 0=Normal vertical sync 1=Sync is 'vertical sync' ORed with 'vertical display enable'

Feature Control Register (Read)

GENFC_WT - W - 8 bits - [VGA_IO:0x3BA] [VGA_IO:0x3DA]			
Field Name	Bits	Default	Description
VSYNC_SEL_W	3	0x0	Vertical sync select (write). 0=Normal vertical sync 1=Sync is 'vertical sync' ORed with 'vertical display enable'

Feature Control Register (Read)

GENS0 - R - 8 bits - VGA_IO:0x3C2			
Field Name	Bits	Default	Description
SENSE_SWITCH	4	0x0	DAC comparator read back. Used for monitor detection. Mirror of DAC_CMP_OUTPUT@DAC_CNTL. See description there.
CRT_INTR	7	0x0	CRT Interrupt: 0=Vertical retrace interrupt is cleared 1=Vertical retrace interrupt is pending

Input Status 0 Register

GENS1 - R - 8 bits - [VGA_IO:0x3BA] [VGA_IO:0x3DA]			
Field Name	Bits	Default	Description
NO_DIPLAY	0	0x0	Display enable. 0=Enable 1=Disable

VGA_VSTATUS	3	0x0	Vertical Retrace Status. 0=Vertical retrace not active 1=Vertical retrace active
PIXEL_READ_BACK	5:4	0x0	Diagnostic bits 0, 1 respectively. These two bits are connected to two of the eight colour outputs (P7:P0) of the attribute controller. Connections are controlled by ATTR12(5,4) as follows: 0=P2,P0 1=P5,P4 2=P3,P1 3=P7,P6

Input Status 1 Register

DAC_CNTL - RW - 32 bits - [IOReg,MMReg:0x58]			
Field Name	Bits	Default	Description
DAC_RANGE_CNTL (DISPLAY)	1:0	0x2	DAC control bits. Default = 2. 0=YPr output level 1=Reserved 2=PS2 Output Level
DAC_BLANKING (DISPLAY)	2	0x0	Controls use of DAC blanking pedestal during horizontal and vertical blanks. VGA PS2 compatible monitors expect a 0 IRE blanking pedestal. 0=0 IRE blanking pedestal 1=7.5 IRE blanking pedestal

DAC_CMP_EN (DISPLAY)	3	0x1	<p>Control DAC comparators for analog termination checking. When enabled, the results of the three comparators are read back in the DAC_CMP_OUT_R/G/B fields. Use for the DAC_FORCE fields of DAC_EXT_CNTL is recommended for testing analog monitor connection. DAC_FORCE allows the correct 10 bit data values to be forced on the DAC channels without corrupting the TMDS or TV out images.</p> <p>When using the DAC comparators, be sure the comparator settling times are met by waiting at least 1us between changing the DAC_FORCE parameters and reading the comparator status bits.</p> <p>The comparator reference voltage is 0.440V. The recommended 10 bit DAC value for testing 75 or 37.5 ohm termination for PS2 current levels is 0x1AC.</p> <p>For each channel, if the comparator output is 0, it indicates the termination is 75 ohms, and therefore no monitor is attached. When the comparator output is 1, the termination is 37.5 ohms and a monitor is attached.</p> <p>0=Disable DAC comparators. Best for power and noise coupling. 1=Enable DAC comparators. Used only for analog monitor detection.</p>
DAC_CMP_OUT_R (R) (DISPLAY)	4	0x0	<p>Red channel comparator output.</p> <p>0=Red output voltage above reference level, or comparators disabled 1=Red output voltage below reference level(connected)</p>
DAC_CMP_OUT_G (R) (DISPLAY)	5	0x0	<p>Green channel comparator output.</p> <p>0=Green output voltage above reference level, or comparators disabled 1=Green output voltage below reference level(connected)</p>
DAC_CMP_OUT_B (R) (DISPLAY)	6	0x0	<p>Blue channel comparator output.</p> <p>0=Blue output voltage above reference level, or comparators disabled 1=Blue output voltage below reference level(connected)</p>
DAC_CMP_OUTPUT (R) (DISPLAY)	7	0x0	<p>Logical AND of R, G &amp; B comparator outputs.</p> <p>0=Comparators are off, or at least one of R, G &amp; B above reference level 1=R, G &amp; B comparators all below reference level(connected)</p>
DAC_8BIT_EN (DISPLAY)	8	0x0	<p>Enables 8 bit DAC operation. 8 bit is normal, 6 bit used for VGA emulation.</p> <p>When in 6 bit writes and reads to DAC_DATA and PALETTE_DATA are affected. Writes shift 6 bits left by 2 to make 8 bits in the palette memory. Reads shift 8 bit palette data right by 2 to give 6 MSBs to the host.</p> <p>0=DAC_DATA and PALETTE_DATA read/writes emulate 6 bit palette 1=DAC_DATA and PALETTE_DATA read/writes emulate 8 bit palette</p>

DAC_4BPP_PIX_ORDER (DISPLAY)	9	0x0	Selects the order of pixel nibbles within bytes for 4 bpp extended (non-VGA) display modes. 0=Most significant nibble is left pixel 1=Least significant nibble is left pixel
DAC_TVO_EN (DISPLAY)	10	0x0	Enables generation of TV output byte stream for use by ImpactTV/Ripper encoder. Use the MPP_TB_TVO_EN or MPP_GP_TVO_EN bits to control which MPP port drives out the display data. This depends on the board design. The display clock generation must also be programmed for TV out to get an image on the TV. 0=Disable 1=Enable
DAC_VGA_ADR_EN (BIF)	13	0x0	Enables access of the palette (DAC) at the VGA I/O DAC addresses when in extended display modes (non-VGA, or CRTC_EXT_DISP_EN=1).
DAC_EXPAND_MODE (DISPLAY)	14	0x0	Method to expand 4,5 or 6 bit Red/Green/Blue color codes to 8 bit addresses. 0 = Zero Extension 1 = Dynamic Expansion 0=Convert 4, 5 & 6 bit colors to 8 bits by zero extension 1=Convert 4, 5 & 6 bit colors to 8 bits by dynamic expansion
DAC_PDWN (DISPLAY)	15	0x0	Power down internal DAC macro bandgap unit. Should also set the R, G & B powerdowns in the DAC_MACRO_CNTL register at the same time. Powering down the DAC does not affect the digital outputs (TV or flat panel). The DAC is automatically powered down when the PMI_POWER_STATE register is not in the D0 state. Setting all DAC_PDWN fields should save about 56 mA when PS2 output levels.
DAC_CRC_CONT_EN (DISPLAY)	18	0x0	When CRC is in one shot mode, one-and-only-one frame or field is CRCed after DAC_CRC_EN is set high. In continuous mode every frame/field is CRCed and the results are valid for one field/frame until the next set of results are ready. If a field/frames results are not read within one frame in continuous mode they are over written. In one-shot mode the results remain and can be read until DAC_CRC_EN is cleared. 0=DAC CRC runs in one shot mode. 1=DAC CRC runs in continuous mode.

DAC_CRC_EN (DISPLAY)	19	0x0	Enables the CRC signature check on the data going to the DAC macro. This is what appears on the screen, and includes graphics, HW cursor, video overlay, sub-picture, and overscan. CRC will start in next vertical blank on the first pixel of the line where VSYNC goes active, and run for one field/frame. For interlaced modes the CRC block will not start working until the beginning of a field with odd/even polarity matching the DAC_CRC_FIELD setting. 0=Reset DAC CRC. 1=Enable DAC CRC for next frame/field in one shot, or all frames/fields in continuous mode.
DAC_CRC_FIELD (DISPLAY)	20	0x0	Used only for interlaced mode CRCs. Controls which field polarity starts the CRC block after DAC_CRC_EN is set high. 0=If interlace display, then start CRC on even field 1=If interlace display, then start CRC on odd field
DAC_LUT_COUNTER_LIMIT (DISPLAY)	22:21	0x0	Anti-sparkle timeout. The palette circuit will search for a place in the display image to hide palette reads or writes. If no hiding location is found within this many pixels, a dot-stretch is forced to hide the cycle as best as possible. Setting this register too high in low resolution modes may cause long delays on the PCI/AGP bus. The recommended settings are best. 0=Not recommended. Use a higher setting unless real problems. Anti-sparkle timeout 3 clocks on the palette. 1=This setting will give even better palette read/write speed than '10' or '11', but does it need to be this good? Might be useful in very low res modes. Anti-sparkle timeout 7 clocks on the palette. 2=This setting should be used only if '11' setting creates palette write/read speed issue. Anti-sparkle timeout 15 clocks on the palette. 3=This setting is recommended as the default. Anti-sparkle timeout 31 clocks on the palette.
DAC_LUT_READ_SEL (DISPLAY)	23	0x0	Used for diagnostics only. Selects palette for HOST reads. 0=Palette reads come from main palette 1=Palette reads come from secondary palette
DAC_MASK (DISPLAY)	31:24	0xff	Mirror VGA DAC_MASK. No affect in non-VGA modes. Masks off usage of individual palette index bits before pixel index is looked-up in the palette. 0 = do not use this bit of the index 1 = use this bit of the index This is a mirror of the VGA DAC_MASK register. It only has an effect in VGA emulation modes (CRTX_EXT_DISP_EN=0), not for VESA modes or extended display modes.

General control for the RGB DAC and palette.

DAC_DATA - RW - 8 bits - VGA_IO:0x3C9			
Field Name	Bits	Default	Description
DAC_DATA	7:0	0x0	VGA Palette (DAC) Data. Use DAC_R_INDEX and DAC_W_INDEX to set read or write mode, and entry to access. Access order is Red, Green, Blue, and then auto-increment occurs to next entry. DAC_8BIT_EN controls whether 6 or 8 bit access.

VGA Palette (DAC) Data

DAC_MASK - RW - 8 bits - VGA_IO:0x3C6			
Field Name	Bits	Default	Description
DAC_MASK <i>(mirror of DAC_CNTL:DAC_MASK)</i>	7:0	0x0	Masks off usage of individual palette index bits before pixel index is looked-up in the palette. 0 = do not use this bit of the index 1 = use this bit of the index Only has an effect in VGA emulation modes (CRTC_EXT_DISP_EN=0), not for VESA modes or extended display modes.

Palette index mask for VGA emulation modes.

DAC_R_INDEX - RW - 8 bits - VGA_IO:0x3C7			
Field Name	Bits	Default	Description
DAC_R_INDEX	7:0	0x0	Write: Sets the index for a palette (DAC) read operation. Index auto-increments after every third read of DAC_DATA. Read: Indicates if palette in read or write mode. 0 = Palette in write mode (DAC_W_INDEX last written). 3 = Palette in read mode (DAC_R_INDEX last written). Also see DAC_W_INDEX.

Palette (DAC) Read Index

DAC_W_INDEX - RW - 8 bits - VGA_IO:0x3C8			
Field Name	Bits	Default	Description
DAC_W_INDEX	7:0	0x0	Sets the index for a palette (DAC) write operation. Index auto-increments after every third write of DAC_DATA. Also see DAC_R_INDEX.

Palette (DAC) Write Index

ATTRX - RW - 8 bits - VGA_IO:0x3C0			
Field Name	Bits	Default	Description
ATTR_IDX	4:0	0x0	ATTR Index. This index points to one of the internal registers of the attribute controller (ATTR) at addresses 0x3C1/0x3C0, for the next ATTR read/write operation. Since both the index and data registers are at the same I/O, a pointer to the registers is necessary. This pointer can be initialized to point to the index register by a read of GENS1.
ATTR_PAL_RW_ENB	5	0x0	Palette Address Source. After loading the colour palette, this bit should be set to logical 1. 0=Processor to load 1=Memory data to access

Attribute Index Register

ATTRDW - W - 8 bits - VGA_IO:0x3C0			
Field Name	Bits	Default	Description
ATTR_DATA	7:0	0x0	Attribute Data Write

Attribute Data Write Register

ATTRDR - R - 8 bits - VGA_IO:0x3C1			
Field Name	Bits	Default	Description
ATTR_DATA <i>(mirror of ATTRDW:ATTR_DATA)</i>	7:0	0x0	Attribute Data Read

Attribute Data Read Register

CRTC_GEN_CNTL - RW - 32 bits - [IOReg,MMReg:0x50]			
Field Name	Bits	Default	Description
CRTC_DBL_SCAN_EN (DISPLAY)	0	0x0	Double scan enable. Double scan only affects the calculation of display addresses by adding the CRTC_PITCH every second line (also applies to the hardware cursor pitch). Enabling double scan does not change the CRTC vertical programming or VSYNC timing. The overscan top & bottom are not affected and remain the number of lines programmed (i.e. not double). The hardware cursor programming remains in terms of physical lines (not logical lines). The cursor vertical position must begin on an even line number when in double scan. The cursor itself is limited to 64 physical lines in height, which means only 32 logical lines. This is because the cursor pitch is only added at the end of odd scan lines, but the CRTC vertical logic stops the cursor after 64 physical lines. 0=Disable 1=Enable
CRTC_INTERLACE_EN (DISPLAY)	1	0x0	Interlace display mode enable. 0=Non-Interlace 1=Interlace
CRTC_C_SYNC_EN (DISPLAY)	4	0x0	Enables composite sync on horizontal sync output. When this is set, the VSYNC pin should be disabled by setting CRTC_EXT_CNTL.CRTC_VSYNC_TRISTATE=1. 0=Disable 1=Enable
CRTC_PIX_WIDTH (DISPLAY)	11:8	0x0	Display pixel width (actually depth). For 4bpp mode DAC_CNTL.DAC_4BPP_PIX_ORDER selects the order of nibbles within bytes. When R, G, or B components are only 4, 5 or 6 bits, DAC_CNTL.DAC_EXPAND_MODE selects how these components are expanded to 8 bits each for keying and palette lookup. When alpha values are 1 or 4 bits, they are expanded to 8 bits by dynamic expansion of the high order bits to the missing lower order bits. 1=4bpp Indexed 2=8bpp Indexed 3=15bpp aRGB 1555 4=16bpp RGB 565 5=24bpp RGB 888 6=32bpp aRGB 8888 7=16bpp aRGB 4444 8=16bpp aIndex 88
CRTC_CUR_EN (DISPLAY)	16	0x0	Hardware cursor enable. This field is double buffered and locked with the CUR_LOCK register field. 0=Disable 1=Enable

<p>CRTC_VSTAT_MODE</p> <p>(DISPLAY)</p>	18:17	0x0	<p>Selects the location of the display updating of CRTC_OFFSET and CUR_OFFSET and related fields during the vertical retrace. Also determines where the VGA_VSTATUS update will occur within the vertical retrace for VGA modes.</p> <p>For non-VGA modes only the upper bit of this field is used. When 00 or 01 in non-VGA the updating of the CRTC_OFFSET and the CUR_OFFSET is delayed as long as possible within the vertical retrace until the start of the last line of the retrace. When 10 or 11 in non-VGA the CRTC_OFFSET and CUR_OFFSET are updated at the leading edge of VSYNC, which is normally relatively early in the vertical retrace. No matter how this is set, the update of status bits like WAIT_UNTIL_PFLIP will reflect the actual location of the update. Any writes to CRTC_OFFSET or CUR_OFFSET after the selected point has passed in the vertical retrace will have no affect until the display frame after the next vertical retrace.</p> <p>For VGA modes this field affects the behaviour of page flipping in some applications/games that poll the VGA_VSTATUS flag. This field should be tuned by the BIOS for compatibility with the most games.</p> <p>0=VGA_VSTATUS until vcount= vtotal, DISP_ADDR loads when vcount=vtotal  1=VGA_VSTATUS until vblank end, DISP_ADDR loads when vcount=vtotal  2=VGA_VSTATUS until vcount= vtotal,DISP_ADDR loads in vsync start  3=VGA_VSTATUS until vblank end,DISP_ADDR loads in vsync start</p>
<p>CRTC_CUR_MODE</p> <p>(DISPLAY)</p>	22:20	0x0	<p>Hardware cursor mode.</p> <p>For 2bpp mode, each line of cursor data is stored in memory as 64 bits of AND data followed by 64 bits of XOR data. For color AND/XOR mode, each pixel is stored sequentially in memory as 32bits each in aRGB8888 format with bit 31 of each DWord being the AND bit.</p> <p>For the color alpha modes the format is also 32bpp aRGB8888 with all 8 bits of the alpha being used.</p> <p>All HW cursor lines must be 64 pixels wide and all lines must be stored sequentially in memory.</p> <p>0=Mono + 1 bit AND (2bpp)  1=Color 24bpp + 1 bit AND  2=Color 24bpp + 8 bit premultiplied alpha  3=Color 24bpp + 8 bit unmultiplied alpha</p>
<p>CRTC_EXT_DISP_EN</p> <p>(BIF) (DISPLAY)</p>	24	0x0	<p>Extended display mode enable. No affect if strapped VGA_DISABLE=1.</p> <p>0=VGA  1=Extended</p>

CRTC_EN (DISPLAY)	25	0x0	Enables CRT controller. When reset, the CRTC horizontal counter is set to zero, and the vertical counter is set to the current value of CRTC_V_TOTAL_DISP.CRTC_V_DISP. 0=Reset 1=Enable
CRTC_DISP_REQ_EN_B (DISPLAY)	26	0x1	Enables display graphics requests to the memory controller. Affects only graphics and VGA text requests. Does not affect HW cursor, overlay or subpic. When setting this bit, CRTC_EXT_CNTL.CRTC_DISPLAY_DIS is also normally set to blank the screen. Active low. 0=Enable 1=Disable

CRTC general controls

CRTC_EXT_CNTL - RW - 32 bits - [IOReg,MMReg:0x54]			
Field Name	Bits	Default	Description
CRTC_VGA_XOVERSCAN (DISPLAY)	0	0x0	Set low for VGA compatible borders. When set high extended overscan registers control border in VGA modes. See also auto-centering in CRTC_MORE_CNTL and FP_GEN_CNTL.CRTC_VGA_XOVERSCAN_COLOR. 0=Disable extended overscan in VGA 1=Enable extended overscan in VGA
VGA_BLINK_RATE (DISPLAY)	2:1	0x0	Controls number of frames per blink for VGA modes. 0=Default VGA blink rate (16 frames) 1=1/2 default VGA blink rate (32 frames) 2=1/3 default VGA blink rate (48 frames) 3=1/4 default VGA blink rate (64 frames)
VGA_ATI_LINEAR (HDP) (DISPLAY)	3	0x0	Enable linear addressing through VGA memory aperture. 0=Disable 1=Enable
VGA_128KAP_PAGING (HDP) (DISPLAY)	4	0x0	Enable extended aperture paging in 128K VGA aperture mode. 0=Normal 1=Enable
VGA_TEXT_132 (HDP) (DISPLAY)	5	0x0	Extended text mode select (linear address 132 column text mode). Set low for VGA compatible 40 or 80 column text modes. 0=inActive 1=Active

VGA_XCRT_CNT_EN (DISPLAY)	6	0x0	Extended CRTC display address counter enable. Active High 0=Disable 1=Enable Ext CRTC Counter
CRTC_HSYNC_DIS (DISPLAY)	8	0x0	Disables horizontal sync output. Could be used for DPMS signaling, but DISP_PWR_MAN.DISP_PWR_MAN_DPMS is recommended instead. 0=Enable 1=Disable
CRTC_VSYNC_DIS (DISPLAY)	9	0x0	Disables vertical sync output. Could be used for DPMS signaling, but DISP_PWR_MAN.DISP_PWR_MAN_DPMS is recommended instead. Note this must remain enabled while using composite SYNC on HSYNC (CRTC_C_SYNC_EN=1). 0=Enable 1=Disable
CRTC_DISPLAY_DIS (DISPLAY)	10	0x0	Disables the display, forcing the blanking signal to be active. When blanking the screen with this bit, the overlay, sub-picture, graphics and cursor should also be disabled to save power. See CRTC_DISP_REQ_EN_B, CRTC_CUR_EN, OV0_OVERLAY_EN and SUBPIC_ON. 0=Enable 1=Blanked
CRTC_SYNC_TRISTATE (DISPLAY)	11	0x0	Tristates HSYNC and VSYNC outputs. For individual tristate control, see the next two fields. 0=Normal 1=Tristate HSYNC and VSYNC outputs
CRTC_HSYNC_TRISTATE (DISPLAY)	12	0x0	Tristates HSYNC output. 0=Normal HSYNC 1=Tristate HSYNC output
CRTC_VSYNC_TRISTATE (DISPLAY)	13	0x0	Tristates VSYNC output. This is recommended for use with composite sync mode when only the HSYNC output pin should be enabled. 0=Normal VSYNC 1=Tristate VSYNC output
VGA_CUR_B_TEST (DISPLAY)	17	0x0	Test cursor blinking. Only used for diagnostic testing. 0=Disable VGA cursor test 1=Test VGA cursor blinking
VGA_PACK_DIS (HDP)	18	0x0	Controls host write pipe for packed VGA modes (e.g. mode 13). Should only be set high if HW problem with fast writes. 0=Fast VGA write in packed modes 1=Normal VGA write in packed modes
VGA_MEM_PS_EN (HDP)	19	0x0	VGA page select enable: 0=Don't use MEM_VGA_WP_SEL and MEM_VGA_RP_SEL registers 1=Use MEM_VGA_WP_SEL and MEM_VGA_RP_SEL registers

VCRTC_IDX_MASTER (HDP) (DISPLAY)	30:24	0x0	VGA CRTC master index. Only bits 5:0 of the VGA CRTC index can be written (or read) in VGA I/O space at 0x3B4 or 0x3D4. Bit 6 controls whether the master or shadow set of VGA CRTC registers is seen in VGA I/O space. The shadow set is for use when supporting panel operation in VGA modes. The BIOS will leave either the master or shadow set active as needed after a mode switch call.
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More CRTC general controls

<b>CRTC_STATUS - RW - 32 bits - [IOReg,MMReg:0x5C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CRTC_VBLANK_CUR (R)	0	0x0	Indicates if raster currently in vertical blank. 0=Not in vertical blank 1=In vertical blank
CRTC_VBLANK_SAVE (R)	1	0x0	Clearable vertical blank indicator. Used by software to determine if still the same vertical blank as the last time polling (or interrupt) occurred. 0=No vertical blank since last clear 1=Vertical Blank since last cleared
CRTC_VBLANK_SAVE_CLEAR (W)	1	0x0	Used to clear CRTC_VBLANK_SAVE. 0=No effect 1=Clear CRTC_VBLANK_SAVE
CRTC_VLINE_SYNC (R)	2	0x0	Indicates if the scan line is even or odd. 0=Even scan line 1=Odd scan line
CRTC_FRAME (R)	3	0x0	Indicates if even or odd frame currently displayed. 0=Even frame 1=Odd frame

Status bits to determine current state of the display.

<b>GPIO_MONID - RW - 32 bits - [IOReg,MMReg:0x68]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
GPIO_MONID_0_OUTPUT	0	0x0	Output data for MONID(0) pin. 0=Drive MONID(0) low, if enabled. 1=Drive MONID(0) high, if enabled.
GPIO_MONID_1_OUTPUT	1	0x0	Output data for MONID(1) pin. 0=Drive MONID(0) low, if enabled. 1=Drive MONID(1) high, if enabled.

GPIO_MONID_0_INPUT (R)	8	0x0	Input data from MONID(0) pin. 0=MONID(0) pin input is low. 1=MONID(0) pin input is high.
GPIO_MONID_1_INPUT (R)	9	0x0	Input data from MONID(1) pin. 0=MONID(1) pin input is low. 1=MONID(1) pin input is high.
GPIO_MONID_0_OUT_EN	16	0x0	Output enable for MONID(0) pin. 0=MONID(0) output disabled. 1=MONID(0) output enabled.
GPIO_MONID_1_OUT_EN	17	0x0	Output enable for MONID(1) pin. 0=MONID(0) output disabled. 1=MONID(1) output enabled.

Control and read of MONID general purpose IO pins.

<b>PALETTE_INDEX - RW - 32 bits - [IOReg,MMReg:0xB0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
PALETTE_W_INDEX	7:0	0x0	Write: Sets starting index for palette writes. Auto-increments on each write to PALETTE_DATA. Read: Indicates index where next write to PALETTE_DATA will be written.
PALETTE_R_INDEX	23:16	0x0	Write: Sets starting index for palette reads. Auto-increments on each read from PALETTE_DATA. Read: Indicates index where next read from PALETTE_DATA will be read.

Display palette read and write index setting.

Recommend using byte writes to set either read mode or write mode for the palette. If both bytes are written at once, the write index will win and read index will be ignored. Note there is only one internal index register, so writing to one of them changes the read for both.

<b>PALETTE_30_DATA - RW - 32 bits - [IOReg,MMReg:0xB8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
PALETTE_DATA_B	9:0	0x0	Blue palette data.
PALETTE_DATA_G	19:10	0x0	Green palette data.
PALETTE_DATA_R	29:20	0x0	Red palette data.

Display palette 30 bit data read/write. Use register instead of PALETTE\_DATA to take advantage of the 30 bit DACs and improved gamma correction.

<b>CRTC_H_TOTAL_DISP - RW - 32 bits - [MMReg:0x200]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CRTC_H_TOTAL	9:0	0x0	Horizontal total (pixels * 8). Sum of display width, overscan right, front porch, sync width, back porch and overscan left.
CRTC_H_DISP	24:16	0x0	Horizontal display end (pixels * 8). Determines number of visible pixels, not including overscan.

Horizontal Total and Displayed Control

<b>CRTC_H_SYNC_STRT_WID - RW - 32 bits - [MMReg:0x204]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CRTC_H_SYNC_STRT_PIX	2:0	0x0	CRT Horizontal sync start delay in pixels. Allows pixel accurate horizontal positioning by delaying sync position within character position set below.
CRTC_H_SYNC_STRT_CHAR	12:3	0x0	Horizontal sync start (pixels * 8). Sum of display width, overscan right and front porch.
CRTC_H_SYNC_WID	21:16	0x0	Horizontal sync width (pixels * 8)
CRTC_H_SYNC_POL	23	0x0	CRT Horizontal sync polarity 0 = Active high 1 = Active Low 0=Active high 1=Active low
CRTC_H_SYNC_SKEW_TUNE	26:24	0x0	Per pixel HSYNC skew tuning value used when manual tuning selected. Value is per display pixel. For VGA display adjustment range varies with VGA mode. For extended display the range is -1 (0x0) to +6 (0x7) pixels.
CRTC_H_SYNC_SKEW_TUNE_MODE	28	0x0	Used mostly in VGA mode to have HW automatically adjust HSYNC position pixel accurately based on current VGA mode. 0=Auto tune the DAC HSYNC pixel skew. 1=Manually tune the DAC HSYNC pixel skew using CRTC_H_SYNC_SKEW_TUNE.

Horizontal Sync Control.

The CRTC\_H\_SYNC\_STRT\_PIX and CRTC\_H\_SYNC\_POL always apply to the CRT Horizontal Sync regardless of other control bits.(DFP\_SYNC\_SEL/CRT\_SYNC\_SEL/CRT\_SYNC\_ALT\_SEL/horz. blanking mode/horz. autocentering)

<b>CRTC_V_TOTAL_DISP - RW - 32 bits - [MMReg:0x208]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CRTC_V_TOTAL	11:0	0x0	Vertical total. Sum of display height, overscan bottom, front porch, sync width, back porch and overscan top.

CRTC_V_DISP	27:16	0x0	Vertical display end. Determines number of visible lines, not including overscan.
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Vertical Total Control

CRTC_V_SYNC_STRT_WID - RW - 32 bits - [MMReg:0x20C]			
Field Name	Bits	Default	Description
CRTC_V_SYNC_STRT	11:0	0x0	Vertical sync start. Sum of display height, overscan bottom and front porch.
CRTC_V_SYNC_WID	20:16	0x0	Vertical sync width
CRTC_V_SYNC_POL	23	0x0	Vertical sync polarity 0 = Active high 1 = Active low 0=Active high 1=Active low

Vertical Sync Control

CRTC_VLINE_CRNT_VLINE - RW - 32 bits - [MMReg:0x210]			
Field Name	Bits	Default	Description
CRTC_VLINE	11:0	0x0	Vertical line at which vertical line interrupt is triggered.
CRTC_CRNT_VLINE (R)	27:16	0x0	Current vertical line.

Display Current Vertical Line

CRTC_CRNT_FRAME - R - 32 bits - [MMReg:0x214]			
Field Name	Bits	Default	Description
CRTC_CRNT_FRAME	20:0	0x0	Readback of current value of display frame counter. Used by display time sensitive applications such as video playback.

Current Frame

CRTC_GUI_TRIG_VLINE - RW - 32 bits - [MMReg:0x218]			
Field Name	Bits	Default	Description
CRTC_GUI_TRIG_VLINE_START	11:0	0x0	The START (upper in display, lower in memory) for the GUI_TRIG_VLINE compare. First line of display is line 0.

CRTC_GUI_TRIG_VLINE_INV	15	0x0	Controls whether VLINE region signal is active high or active low. Can be used to stall command stream parser until inside region, or not inside region. 0=Active when raster between START and END. 1=Active when raster outside START and END.
CRTC_GUI_TRIG_VLINE_END	27:16	0x0	The END (lower in display, higher in memory) for the GUI_TRIG_VLINE compare. First line of display is line 0.
CRTC_GUI_TRIG_VLINE_STALL	30	0x0	If waiting on rising or falling edge of VLINE using WAIT_UNTIL register, then always set the stall to 0. If using WAIT_UNTIL VLINE=1, then always set this stall bit to 1. This bit controls the timing of the signal from the display to the command stream parser during writes to this register. 0=Normal operation. 1=Force low during write of this register.
CRTC_GUI_TRIG_VLINE (R)	31	0x0	This signal is active active when the raster is between the START and END. $START \leq \text{raster} \leq \text{END}$ . The polarity is controlled as above. This signal goes to the command stream parser as a condition in the WAIT_UNTIL register. 0=Current line not between VLINE start and end. 1=Current line is between VLINE start and end, inclusive.

Trigger to GUI engine activated in certain vertical region of the display, when the raster is between START and END. Normally used to delay rendering operations until the raster has passed a specific point.

<b>CRTC_DEBUG - RW - 32 bits - [MMReg:0x21C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CRTC_GUI_TRIG_BYPASS_EN	0	0x0	Enables manual testing of display GUI trigger signals to the WAIT_UNTIL register and the render backend. 0=Don't bypass gui triggers generated by dispeng. 1=Bypass gui triggers generated by dispeng.
GUI_TRIG_VLINE_BYPASS	1	0x0	When GUI triggers are bypassed, this sets the value of the VLINE status signal to the WAIT_UNTIL register.
GUI_TRIG_OFFSET_BYPASS	2	0x0	When GUI triggers are bypassed, this sets the value of the CRTC_OFFSET status signal to the WAIT_UNTIL register.
GUI_TRIG_PITCH_ADD_BYPASS	3	0x0	When GUI triggers are bypassed, this sets the value of the CRTC_PITCH_ADD status signal to the render backend (this is for rendering stall behind the raster, which Rage 6 render backend may not support).

Controls for HW testing and debug of display systems. Should not be needed by software.

CRTC_OFFSET_RIGHT - RW - 32 bits - [MMReg:0x220]			
Field Name	Bits	Default	Description
CRTC_OFFSET_RIGHT	26:0	0x0	Graphics surface origin offset in memory for right eye. Alignment must be as for CRTC_OFFSET. Used only when CRTC_STEREO_OFFSET_EN = 1. This is added to DISP_BASE_ADDR to get the full 32 bit address of the graphics surface.  NOTE: Bits 0:2 of this field are hardwired to ZERO.
CRTC_GUI_TRIG_OFFSET <i>(mirror of CRTC_OFFSET:CRTC_GUI_TRIG_OFFSET)</i> (R)	30	0x0	Indicates if visible buffer is last written, or still the previous one. See CRTC_OFFSET register. 0=Last CRTC_OFFSET or CRTC_OFFSET_RIGHT written is being displayed 1=Last CRTC_OFFSET or CRTC_OFFSET_RIGHT written not yet displayed
CRTC_OFFSET_LOCK <i>(mirror of CRTC_OFFSET:CRTC_OFFSET_LOCK)</i>	31	0x0	Prevents hardware from internally updating certain fields until cleared. See CRTC_OFFSET register. 0=Unlock these regs 1=Lock'em

Right eye visible surface origin. Only used in stereo

CRTC_OFFSET - RW - 32 bits - [MMReg:0x224]			
Field Name	Bits	Default	Description
CRTC_OFFSET	26:0	0x0	Graphics surface origin offset in memory. Must be 8 byte aligned for 4bpp, 8bpp and 24bpp modes. Must be 16 byte aligned for all 16bpp modes. Must be 32 byte aligned for 32bpp mode. When CRTC_STEREO_OFFSET_EN = 1, this is the left eye image. This is added to DISP_BASE_ADDR to get the full 32 bit address of the graphics surface.  NOTE: Bits 0:2 of this field are hardwired to ZERO.
CRTC_GUI_TRIG_OFFSET (R)	30	0x0	Indicates if visible buffer is last written, or still the previous one. This bit is read only. Goes high when an offset has been written but the corresponding buffer does not appear on screen yet. It goes low again when display starts for that address. 0=Last CRTC_OFFSET or CRTC_OFFSET_RIGHT written is being displayed 1=Last CRTC_OFFSET or CRTC_OFFSET_RIGHT written not yet displayed

CRTC_OFFSET_LOCK	31	0x0	Prevents hardware from internally updating the following fields until cleared: CRTC_OFFSET, CRTC_OFFSET_RIGHT, CRTC_TILE_LINE, CRTC_TILE_LINE_RIGHT. It permits atomic update of CRTC_OFFSET and CRTC_TILE_LINE. Normal operation is with the lock in zero. 0=Unlock these regs 1=Lock'em
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Main graphics visible surface origin. Left eye image for stereo

<b>CRTC_OFFSET_CNTL - RW - 32 bits - [MMReg:0x228]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CRTC_TILE_LINE	3:0	0x0	When CRTC_TILE_EN = 1, this field holds the 4 LSB of the line of the surface where CRTC_OFFSET starts (the 'y' for line 0 of the display, or 'start line'). The display address generator needs to know this to determine the proper pitch to add at the end of each display line. This is normally 0, unless the display is in a virtual desktop mode with tiling enabled. For example, if the surface offset is zero and the display starts in line 3, CRTC_TILE_LINE=0x3 CRTC_OFFSET = 0xC0 Note that tiles are 8 lines high, but this register must contain ((start line) MOD 16) in order to do the checkerboarding correctly. Do not worry about what checkerboarding is, you shouldn't need to know.
CRTC_TILE_LINE_RIGHT	7:4	0x0	When CRTC_TILE_EN_RIGHT = 1, this field holds the 4 LSB of the line of the surface where CRTC_OFFSET_RIGHT starts. Same as for the left eye with CRTC_TILE_LINE and CRTC_OFFSET. Right fields only used when CRTC_STEREO_OFFSET_EN = 1.
CRTC_TILE_EN_RIGHT	14	0x0	Graphics display tiling enable for right eye image. Used only when CRTC_STEREO_OFFSET_EN = 1. 0=Display Surface uses linear addressing 1=Display surface uses tiled addressing
CRTC_TILE_EN	15	0x0	Graphics display tiling enable. When CRTC_STEREO_OFFSET_EN = 1 controls tiling of left eye image only. 0=Display Surface uses linear addressing 1=Display surface uses tiled addressing

CRTC_OFFSET_FLIP_CNTL	16	0x0	<p>Selects position within the frame at which new CRTC_OFFSET will be used.</p> <p>Should be normally zero. If set to one, a new offset will be taken at the end of the line instead of the end of the frame.</p> <p>0=Use new CRTC_OFFSET on vertical blank 1=Use new CRTC_OFFSET on any horizontal blank.</p> <p>Note, this can cause the display to tear.</p>
CRTC_STEREO_OFFSET_EN	17	0x0	<p>Enables the use of the stereo display right eye offset and pitch fields.</p> <p>0=No stereoscopic. RIGHT registers not used 1=Stereoscopic display enabled. Alternate display between normal (left) and right display surfaces</p>
CRTC_STEREO_SYNC_EN	19:18	0x0	<p>Controls function of STEREO_SYNC output signal.</p> <p>0=STEREO_SYNC always low 1=STEREO_SYNC alternates. Low=right, high=left 2=STEREO_SYNC always high 3=STEREO_SYNC alternates. Low=left, high=right</p>
CRTC_STEREO_SYNC_OUT_EN	20	0x0	<p>The output enable for the STEREO_SYNC output signal.</p> <p>0=STEREO_SYNC output tri-stated 1=STEREO_SYNC output enabled</p>
CRTC_STEREO_SYNC (R)	21	0x0	<p>Readback of STEREO_SYNC signal current value.</p>
CRTC_GUI_TRIG_OFFSET_LEFT_EN	28	0x1	<p>Controls whether or not CRTC_OFFSET affects the CRTC_GUI_TRIG_OFFSET to the WAIT_UNTIL register. If enabled, then wait condition is set on writing CRTC_OFFSET, and cleared only if display starts displaying from CRTC_OFFSET (not if display uses CRTC_OFFSET_RIGHT for next frame).</p> <p>0=Writing CRTC_OFFSET (main/left) does not set CRTC_GUI_TRIG_OFFSET 1=Writing CRTC_OFFSET sets CRTC_GUI_TRIG_OFFSET</p>
CRTC_GUI_TRIG_OFFSET_RIGHT_EN	29	0x0	<p>Controls whether or not CRTC_OFFSET_RIGHT affects the CRTC_GUI_TRIG_OFFSET to the WAIT_UNTIL register. If enabled, then wait condition is set on writing CRTC_OFFSET_RIGHT, and cleared only if display starts displaying from CRTC_OFFSET_RIGHT (not if display uses CRTC_OFFSET for next frame).</p> <p>0=Writing CRTC_OFFSET_RIGHT does not set CRTC_GUI_TRIG_OFFSET 1=Writing CRTC_OFFSET_RIGHT sets CRTC_GUI_TRIG_OFFSET</p>
<p>CRTC_GUI_TRIG_OFFSET</p> <p><i>(mirror of CRTC_OFFSET:CRTC_GUI_TRIG_OFFSET)</i> (R)</p>	30	0x0	<p>Indicates if visible buffer is last written, or still the previous one.</p> <p>See CRTC_OFFSET register.</p> <p>0=Last CRTC_OFFSET or CRTC_OFFSET_RIGHT written is being displayed 1=Last CRTC_OFFSET or CRTC_OFFSET_RIGHT written not yet displayed</p>

CRTC_OFFSET_LOCK <i>(mirror of CRTC_OFFSET:CRTC_OFFSET_LOCK)</i>	31	0x0	Prevents hardware from internally updating certain fields until cleared. See CRTC_OFFSET register. 0=Unlock these regs 1=Lock'em
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Graphics Display Address Generator Control

CRTC_PITCH - RW - 32 bits - [MMReg:0x22C]			
Field Name	Bits	Default	Description
CRTC_PITCH	10:0	0x0	Display line pitch in (pixels * 8). Note that for 24bpp the display uses pixels * 8 for the pitch, but the rendering engine uses bytes * 8 for the pitch. For tiled display this is the same pitch as used for the surface in the rendering engine (24bpp not supported for tiled). In tiled the pitch must be a multiple of 256 bytes (the tile width). So for 32bpp tiled, the CRTC_PITCH must be a multiple of 64 pixels. Or 128 pixels for 16bpp, or 256 pixels for 8bpp. For stereo display mode, this is the left image pitch.
CRTC_PITCH_RIGHT	26:16	0x0	Programming details same as for CRTC_PITCH. This field only used in stereo display mode for right image pitch.

Graphics Display Address Pitch

OVR_CLR - RW - 32 bits - [MMReg:0x230]			
Field Name	Bits	Default	Description
OVR_CLR_B	7:0	0x0	Blue component overscan colour.
OVR_CLR_G	15:8	0x0	Green component overscan colour.
OVR_CLR_R	23:16	0x0	Red component overscan colour.

Overscan color. Always 24 bit, independent of pixel depth.

OVR_WID_LEFT_RIGHT - RW - 32 bits - [MMReg:0x234]			
Field Name	Bits	Default	Description
OVR_WID_RIGHT	6:0	0x0	Right overscan width (in pixels * 8).
OVR_WID_LEFT	22:16	0x0	Left overscan width (in pixels * 8).

Overscan border left/right width control.

<b>OVR_WID_TOP_BOTTOM - RW - 32 bits - [MMReg:0x238]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OVR_WID_BOTTOM	9:0	0x0	Bottom overscan width (in scan lines).
OVR_WID_TOP	25:16	0x0	Top overscan width (in scan lines).

Overscan border top/bottom width control.

<b>DISPLAY_BASE_ADDR - RW - 32 bits - [MMReg:0x23C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISPLAY_BASE_ADDR	31:0	0x0	Base address added to all graphics and cursor requests to the internal memory controller. This should normally be set equal to MC_FB_LOCATION.MC_FB_START. It could be set to other places to allow display out of system (e.g. AGP) memory, but this is not recommended. This is a 4 Megabyte aligned base address.  NOTE: Bits 0:21 of this field are hardwired to ZERO.

Graphics & cursor base address

<b>SNAPSHOT_VH_COUNTS - R - 32 bits - [MMReg:0x240]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SNAPSHOT_HCOUNT	9:0	0x0	
SNAPSHOT_VCOUNT	27:16	0x0	

No description available for this register.

<b>SNAPSHOT_F_COUNT - R - 32 bits - [MMReg:0x244]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SNAPSHOT_F_COUNT	20:0	0x0	

No description available for this register.

<b>N_VIF_COUNT - RW - 32 bits - [MMReg:0x248]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
N_VIF_COUNT_VAL	9:0	0x0	
GENLOCK_SOURCE_SEL	31	0x0	

No description available for this register.

<b>SNAPSHOT_VIF_COUNT - RW - 32 bits - [MMReg:0x24C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
LSNAPSHOT_VIF_COUNT (R)	9:0	0x0	
USNAPSHOT_VIF_COUNT (R)	20:10	0x0	
AUTO_SNAPSHOT_TAKEN_RD (R)	24	0x0	
AUTO_SNAPSHOT_TAKEN_WR (W)	24	0x0	
MANUAL_SNAPSHOT_NOW	25	0x0	

No description available for this register.

<b>FP_CRTC_H_TOTAL_DISP - RW - 32 bits - [MMReg:0x250]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
FP_CRTC_H_TOTAL	9:0	0x0	Horizontal total ((pixels * 8)-1). Sum of display width, over-scan right, front porch, sync width, back porch and over-scan left. If horizontal autocentering or horizontal fixed blank is enabled(see CRTC_MORE_CNTL), this field contains the width of the horizontal blanking time(in characters)
FP_CRTC_H_DISP	24:16	0x0	Horizontal display end ((pixels * 8)-1). Determines number of visible pixels, not including overscan.

DFP Shadow Horizontal Display/Horizontal Total.

These values are used when FP\_GEN\_CNTL.FP\_USE\_SHADOW\_EN = 1

FP_CRTC_V_TOTAL_DISP - RW - 32 bits - [MMReg:0x254]			
Field Name	Bits	Default	Description
FP_CRTC_V_TOTAL	11:0	0x0	Vertical total(lines-1). Sum of display height, overscan bottom, front porch, sync width, back porch and overscan top. If vertical autocentering or vertical fixed blank is enabled(see CRTC_MORE_CNTL) this field contains the length of the vertical blanking time(in lines)
FP_CRTC_V_DISP	27:16	0x0	Vertical display end(lines-1). Determines number of visible lines, not including overscan.

DFP Shadow Vertical Display/Vertical Total registers.

These values are used when FP\_GEN\_CNTL.FP\_USE\_SHADOW\_EN = 1

CUR_OFFSET - RW - 32 bits - [MMReg:0x260]			
Field Name	Bits	Default	Description
CUR_OFFSET	26:0	0x0	Hardware cursor address offset. For monochrome cursors (CRTC_CUR_MODE = 00), this vlaue must be a 16 byte aligned address. For color cursor modes it must be a 256 byte aligned address. The CUR_OFFSET is relative to the DISP_BASE_ADDRESS, meaning the active display pointed to by CRTC_OFFSET and the cursor must be in the same region of memory. This value is adjusted to move the cursor off the top edge of the display. See the CUR_VERT_OFF description.  NOTE: Bits 0:3 of this field are hardwired to ZERO.
CUR_LOCK	31	0x0	Locks the HWC_EN, CUR_OFFSET, CUR_HORZ_VERT_POSN and CUR_HORZ_VERT_OFF registers to allow tear free atomic updating of the cursor shape and/or position. Moving the cursor around on the top and/or left edges, or changing the shape, requires multiple register writes. If these were done without setting CUR_LOCK, then flicker could occur. 0=Unlocked 1=Locked

Location of the hardware cursor image.

CUR_HORZ_VERT_POSN - RW - 32 bits - [MMReg:0x264]			
Field Name	Bits	Default	Description
CUR_VERT_POSN	11:0	0x0	Cursor vertical position. To move the cursor off the top edge set CUR_VERT_POSN=0 and see the CUR_VERT_OFF description. When CRTC_GEN_CNTL.CRTC_DBL_SCAN_EN=1 the logical position from the OS must be converted to a physical position to program here by multiplying by 2. i.e. no odd values should be used in double scan mode.
CUR_HORZ_POSN	29:16	0x0	Cursor horizontal position. To move the cursor off the left edge set CUR_HORZ_POSN=0 and see the CUR_HORZ_OFF description.
CUR_LOCK <i>(mirror of CUR_OFFSET:CUR_LOCK)</i>	31	0x0	Locks the HWC_EN, CUR_OFFSET, CUR_HORZ_VERT_POSN and CUR_HORZ_VERT_OFF registers to allow tear free atomic updating of the cursor shape and/or position. Moving the cursor around on the top and/or left edges, or changing the shape, requires multiple register writes. If these were done without setting CUR_LOCK, then flicker could occur. 0=Unlocked 1=Locked

Sets the screen position of the top left pixel of the visible part of the hardware cursor.

CUR_HORZ_VERT_OFF - RW - 32 bits - [MMReg:0x268]			
Field Name	Bits	Default	Description
CUR_VERT_OFF	5:0	0x0	Cursor vertical offset. Height of cursor is (64-CUR_VERT_OFF). To move the cursor off the top of the display, set CUR_VERT_POSN to 0, add 16*(number of lines to move off the top) to CUR_OFFSET, and increase CUR_VERT_OFF by the same number of lines. When is double scan display (CRTC_DBL_SCAN_EN=1) the height of the cursor is limited to 32 logical lines, but 64 physical lines. i.e. the image in memory can be up to 32 lines high, but will cover 64 physical lines of the display. Also in double scan mode the height of the cursor must be even in physical lines. i.e. this field must be even.

CUR_HORZ_OFF	21:16	0x0	Cursor horizontal offset. Width of the cursor is always 64 pixels. CUR_HORZ_OFF controls how far into the cursor map from the left is 'pixel 0'. The horizontal position on the display of 'pixel 0' is set by CUR_HORZ_POSN. Therefore to move the cursor off the left edge of the display, set the CUR_HORZ_POSN to zero, and increase the CUR_HORZ_OFF by the number of pixels off the left edge.
CUR_LOCK <i>(mirror of CUR_OFFSET:CUR_LOCK)</i>	31	0x0	Locks the HWC_EN, CUR_OFFSET, CUR_HORZ_VERT_POSN and CUR_HORZ_VERT_OFF registers to allow tear free atomic updating of the cursor shape and/or position. Moving 0=Unlocked 1=Locked

Controls the size of the hardware cursor mask in memory, and used to move the cursor off the top and/or left edges of the display.

CUR_CLR0 - RW - 32 bits - [MMReg:0x26C]			
Field Name	Bits	Default	Description
CUR_CLR0_B	7:0	0x0	Blue component of cursor color 0.
CUR_CLR0_G	15:8	0x0	Green component of cursor color 0.
CUR_CLR0_R	23:16	0x0	Red component of cursor color 0.

Hardware cursor color 0. Always 24bpp, independent of graphics mode.  
For monochrome cursor only.

CUR_CLR1 - RW - 32 bits - [MMReg:0x270]			
Field Name	Bits	Default	Description
CUR_CLR1_B	7:0	0x0	Blue component of cursor color 1.
CUR_CLR1_G	15:8	0x0	Green component of cursor color 1.
CUR_CLR1_R	23:16	0x0	Red component of cursor color 1.

Hardware cursor color 1. Always 24bpp, independent of graphics mode.  
For monochrome cursor only.

DAC_EXT_CNTL - RW - 32 bits - [MMReg:0x280]			
Field Name	Bits	Default	Description
DAC_FORCE_BLANK_OFF_EN	4	0x0	When doing DAC comparator test this is best set to 1 so horizontal and vertical retraces do not interrupt the testing. 0=Normal DAC BLANK functionality. 1=DAC BLANK forced off. Use this setting with DAC FORCE logic to detect CRT connection.
DAC_FORCE_DATA_EN	5	0x0	Enables DAC force logic. 0=DAC FORCE logic disabled 1=DAC input data forced as per DAC_FORCE_DATA_SEL and DAC_FORCE_DATA fields
DAC_FORCE_DATA_SEL	7:6	0x0	Selects combination of black (0x00) and DAC_FORCE_DATA value forced on red, green and blue DAC channels. 0=R=DAC_FORCE_DATA,G=B=0x00 1=G=DAC_FORCE_DATA,R=B=0x00 2=B=DAC_FORCE_DATA,R=G=0x00 3=R=G=B=DAC_FORCE_DATA
DAC_FORCE_DATA	17:8	0x0	Data forced on DAC channels as per DAC_FORCE_DATA_SEL and DAC_FORCE_DATA_EN.

DAC force control for analog monitor connection detection. This is used in combination with the DAC\_CNTL register comparator fields.

FP_GEN_CNTL - RW - 32 bits - [MMReg:0x284]			
Field Name	Bits	Default	Description
FP_BLANK_EN	1	0x0	0 = Normal operation. 1 = Send black pixel data to TMDS encoder to blank screen. No effect on DE or SYNCs. 0=Normal operation. 1=Black data to TMDS encoder. No effect on DE or SYNCs.
TMDS_EN	2	0x0	0 = TMDS interface is disabled. 1 = TMDS interface is enabled. This bit can be cleared if the hardware detects a hot plug disconnect of the DFP and FP_DETECT_EN=1. 0=TMDS interface is disabled. This bit can be cleared by hot plug disconnect if FP_DETECT_EN=1. 1=TMDS interface is enabled.
PANEL_FORMAT	3	0x1	Panel format: (default=0) 0 = 18 bit per pixel TFT panel - 666 RGB. 1 = 24 bit per pixel TFT panel - 888 RGB 0=18 bit per pixel TFT panel - 666 RGB 1=24 bit per pixel TFT panel - 888 RGB

NO_OF_GREY	5:4	0x0	<p>Grey level select:</p> <p>0 = No frame modulation.  1 = 2 levels of grey support.  2 = 4 levels of grey support.  3 = reserved</p> <p>0=No frame modulation.  1=2 levels of grey support.  2=4 levels of grey support.  3=reserved</p>
FP_RST_FM	6	0x0	<p>Frame modulation reset.</p> <p>0 = EnaFMCir.  1 = ResetFMCir</p> <p>0=Frame modulator ready.  1=Reset frame modualtor circuit.</p>
FP_EN_TMDS (R)	7	0x0	<p>Read-only bit that indicates TMDS status.</p> <p>0 = TMDS interface is disabled. Either by TMDS_EN written with 0, or hot plug disconnect detected.  1 = TMDS interface is enabled. Also requires TMDS macro to be properly set up.</p> <p>0=TMDS interface is disabled. Either by TMDS_EN written with 0, or hot plug disconnect detected.  1=TMDS interface is enabled. Also requires TMDS macro to be properly set up.</p>
FP_DETECT_SENSE (R)	8	0x0	<p>0 = No hot plug panel connected or panel that does not support hot plug is connected.  1 = Hot plug panel is connected.</p> <p>0=No hot plug panel connected or panel that does not support hot plug is connected.  1=Hot plug panel is connected.</p>
FP_DETECT_INT_POL	9	0x0	<p>0 = Generate interrupt on hot plug disconnect.  1 = Generate interrupt on hot plug connect.</p> <p>Requires interrupt to be enabled(GEN_INT_CNTL.FP_DETECT_MASK)</p> <p>0=Generate interrupt on hot plug disconnect.  1=Generate interrupt on hot plug connect.</p>
FP_DETECT_EN	12	0x0	<p>0 = Hot plug detection has no affect on TMDS transmitter enable/disable.  1 = Hot plug detection can disable TMDS transmitter. Transmitter enable only possible by SW.</p> <p>0=Hot plug detection has no affect on TMDS transmitter enable/disable.  1=Hot plug detection can disable TMDS transmitter. Transmitter enable only possible by SW.</p>

FP_USE_VGA_HVSYNC	14	0x1	<p>0 = TMDS H&amp;V SYNC based only on FP_x_SYNC_STRT_WID registers. For VGA modes, this will not be adjusted for pixel data delays through VGA logic.</p> <p>1 = TMDS H&amp;V SYNC adjusted in VGA modes for delays through VGA pixel data logic.</p> <p>0=TMDS H&amp;V SYNC based only on FP_x_SYNC_STRT_WID. For VGA modes, this will not be adjusted for pixel data delays through VGA logic.</p> <p>1=TMDS H&amp;V SYNC adjusted in VGA modes for delays through VGA pixel data logic.</p>
FP_USE_VGA_SYNC_POLARITY	15	0x0	<p>0 = TMDS H&amp;V SYNC polarities determined by FP_x_SYNC_POL fields.</p> <p>1 = TMDS H&amp;V SYNC polarities determined by VGA_xSYNC regs in VGA modes, and FP_x_SYNC_POL fields in non-VGA modes.</p> <p>0=TMDS H&amp;V SYNC polarities determined by FP_x_SYNC_POL fields.</p> <p>1=TMDS H&amp;V SYNC polarities determined by VGA_xSYNC regs in VGA modes, and FP_x_SYNC_POL fields in non-VGA modes.</p>
CRTC_DONT_SHADOW_VPAR	16	0x0	<p>0 = Use Shadowed Vertical CRT values. DFP VSYNC calculated from shadow CRT VSYNC register values. If FP_USE_SHADOW_EN=1 uses shadowed V_BLANK_START, V_BLANK_END, and V_TOTAL.</p> <p>1 = Use non-shadowed vertical CRT values. DFP VSYNC calculated from non-shadowed vertical CRT values. If FP_USE_SHADOW_EN=1, uses non-shadowed V_BLANK_START, V_BLANK_END, and V_TOTAL.</p> <p>0=Use Shadowed</p> <p>1=Use non-shadowed</p>
CRTC_DONT_SHADOW_HEND	17	0x0	<p>0 = If FP_USE_SHADOW_EN=1 then use shadowed versions of H_DISP_END, H_BLANK_START, and H_BLANK_END CRT registers</p> <p>1 = Use non-shadowed CRT register values regardless of value of FP_USE_SHADOW_EN</p> <p>0=Use Shadowed HorzDispEnd</p> <p>1=Use non-shadowed HorzDispEnd</p>
CRTC_USE_SHADOWED_VEND	18	0x0	<p>0 = use non-shadow V_DISP_END register value</p> <p>1 = if FP_USE_SHADOW_EN=1 then use shadow CRT V_DISP_END_S register value, else use non-shadow value</p> <p>0=disable</p> <p>1=use shadowed VEND</p>
CRTC_USE_SHADOWED_ROWCUR	19	0x0	<p>0 = use normal CRT register values</p> <p>1 = use shadowed MAX_ROW_SCAN, CURSOR_START, CURSOR_END, and UNDRLN_LOC CRT registers</p> <p>0=disable</p> <p>1=use shadowed RowCur</p>

RMX_HVSYNC_CONTROL_EN	20	0x0	<p>0 = Use standard syncs generated for CRT and DFP HSYNC and VSYNC outputs</p> <p>1 = Use syncs generated in RMX logic for CRT and DFP HSYNC and VSYNC outputs. While this will also work when RMX is disabled, it should only be used with RMX enabled</p> <p>0=Use standard syncs generated for CRT and DFP HSYNC and VSYNC outputs</p> <p>1=Use syncs generated in RMX logic for CRT and DFP HSYNC and VSYNC outputs</p>
DFP_SYNC_SEL	21	0x0	<p>0=Use standard(non-shadow) values for DFP syncs(with auto-scaling panels or at native resolution)</p> <p>1=Use shadow(DFP) registers for DFP syncs</p> <p>0=Use non-shadow values for DFP syncs</p> <p>1=Use shadow(LCD) values for DFP syncs</p>
CRTC_LOCK_8DOT	22	0x0	<p>0=Normal VGA text is 8 or 9 dot depending on SEQ01.SEQ_DOT8. 1=Force VGA text to 8 dot. Used when Horizontal RMX is enabled</p> <p>0=Normal VGA text 8 or 9 dot.</p> <p>1=Force VGA text to 8 dot.</p>
CRT_SYNC_SEL	23	0x0	<p>0=Use standard (non-shadow) values for CRT syncs in normal operation.</p> <p>1=Use shadow(DFP) values for CRT syncs in centring/RMX modes (registers with FP_ name prefix)</p> <p>0=Use non-shadow values for CRT syncs in centring mode</p> <p>1=Use shadow(LCD) values for CRT syncs in centring mode</p>
FP_USE_SHADOW_EN	24	0x0	<p>0=Use standard CRTC registers to calculate CRT display parameters.</p> <p>1=Use shadow CRT registers (mirrored with the registers with a FP_ name prefix) to calculate CRT parameters.</p> <p>0=Disable</p> <p>1=Enable</p>
DONT_RST_CHAREN	25	0x0	<p>0 = stop CHAREN if SEQ00=0</p> <p>1 = when SEQ00=0 CHAREN is not stopped. Use with RMX.</p> <p>0=stop CHAREN if SEQ00=0</p> <p>1=Don't</p>

CRT_SYNC_ALT_SEL	26	0x0	<p>0 = value of CRT_SYNC_SEL determines which register values are used to generate CRT horz. &amp; vert. sync start and width.</p> <p>1 = Alternate CRT shadow register values (CRT_CRTC_H_SYNC_STRT_WID and CRT_CRTC_V_SYNC_STRT_WID) are used to generate CRT sync start and width in centering/RMX modes.</p> <p>0=Use CRT_SYNC_SEL to choose CRT sync start and width.</p> <p>1=Use alternate CRT shadow values for CRT sync start and width in centering mode (CRT_CRTC_H_SYNC_STRT_WID and CRT_CRTC_V_SYNC_STRT_WID)</p>
CRTC_USE_NONSHADOW_HPARAMS_FOR_BLANK	27	0x0	<p>0 = disabled (normal operation)</p> <p>1 = makes left overscan width in VGA equal the value in non-shadow CRT registers when shadowing is enabled. When FP_USE_SHADOW_EN=1 and in VGA mode, the horizontal blank end(left overscan width) is calculated from the non-shadow CRT values. <math>H\_BLANK\_END = H\_TOTAL(shadow) - (H\_TOTAL(non-shadow) - H\_BLANK\_END(non-shadow))</math></p> <p>0=Left overscan calculated from shadow H parameters.</p> <p>1=Left overscan calculated from non-shadow H parameters.</p>
CRTC_USE_NONSHADOW_VPARAMS_FOR_BLANK	28	0x0	<p>0 = disabled (normal operation)</p> <p>1 = makes top overscan width in VGA equal the value in non-shadow CRT registers when shadowing is enabled. When FP_USE_SHADOW_EN=1 and in VGA mode, the vertical blank end(top overscan width) is calculated from the non-shadow CRT values. <math>V\_BLANK\_END = V\_TOTAL(shadow) - (V\_TOTAL(non-shadow) - V\_BLANK\_END(non-shadow))</math></p> <p>0=Top overscan calculated from shadow V parameters.</p> <p>1=Top overscan calculated from non-shadow V parameters.</p>
CRTC_VGA_XOVERSCAN_COLOR	29	0x0	<p>0 = use extended overscan color (OVR_CLR register) for overscan pixels in VGA mode when extended overscan is enabled(CRTC_VGA_XOVERSCAN = 1).</p> <p>1 = use VGA overscan color for overscan pixels in VGA mode when extended overscan enabled.</p> <p>0=Use extended overscan color when doing extended overscan in VGA mode.</p> <p>1=Use VGA overscan color when doing extended overscan in VGA mode.</p>

CRTC_VGA_XOVERSCAN_DIVBY2_EN	30	0x0	<p>0 = in VGA mode, when CRTC_EXT_CNTL.CRTC_VGA_XOVERSCAN=1 and SEQ_PCLKBY2=1 then OVR_LEFT/RIGHT register values are used.</p> <p>1 = in VGA mode, when CRTC_EXT_CNTL.CRTC_VGA_XOVERSCAN=1 and SEQ_PCLKBY2=1, then OVR_LEFT/RIGHT register values are divided by 2</p> <p>0=When VGA and extended overscan and SEQ_PCLKBY2=1, then OVR_WID_LEFT/RIGHT are used directly.</p> <p>1=When VGA and extended overscan and SEQ_PCLKBY2=1, then OVR_WID_LEFT/RIGHT are divided by 2.</p>
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Digital Flat Panel(DFP) general controls

FP_VERT_STRETCH - RW - 32 bits - [MMReg:0x290]			
Field Name	Bits	Default	Description
FP_VERT_STRETCH_RATIO	11:0	0x0	For both values of FP_VERT_STRETCH_MODE, valid values for the ratio are 1 to 4095. Ratio = ((Active display height in lines (including overscan)) / (Panel height in lines)) x 4096
FP_VERT_PANEL_SIZE	23:12	0x0	DFP height in lines = (panel height in lines - 1)
FP_VERT_STRETCH_EN	25	0x0	0 = Disable Vertical RMX. 1 = Enable Vert. RMX 0=Vertical stretching disabled. 1=Vertical stretching enabled.
FP_VERT_STRETCH_MODE	26	0x0	Panel vertical stretch mode: 0 = line replication. 1 = vertical blending 0=Disables vertical filter, giving line replication. 1=Enables vertical filter blending.
FP_AUTO_VERT_RATIO	27	0x0	0 = Use FP_VERT_STRETCH_RATIO as Vratio for RMX. 1 = use auto-calculated vertical ratio. Works in both VGA and Extended modes. 0=Use FP_VERT_STRETCH_RATIO register field. Required selection for non-VGA modes. 1=Auto calculate vertical ratio. Only available in VGA modes.
RMX_AUTO_RATIO_VERT_INC	31	0x1	0 = Vertical auto ratio result truncated(i.e. rounded down). 1 = Vertical auto ratio result truncated, and then incremented by 1 (i.e. rounded up). 0=Vertical auto ratio result truncated, i.e. rounded down. 1=Vertical auto ratio result truncated, and then incremented by 1.

Panel Vertical Ratiometric(RMX) stretch control register

FP_H_SYNC_STRT_WID - RW - 32 bits - [MMReg:0x2C4]			
Field Name	Bits	Default	Description
FP_H_SYNC_STRT_PIX	2:0	0x0	DFP Horizontal sync start delay in pixels. Allows pixel accurate horizontal positioning by delaying sync position by the specified number of pixels.
FP_H_SYNC_STRT_CHAR	12:3	0x0	Horizontal sync start position (pixels * 8). Sum of display width, overscan right and front porch. If horizontal fixed blank or autocentering (see CRTC_MORE_CNTL) is enabled, this register field contains the offset (from then end of the active display/start of horizontal blank) within the blank time of the start of the horizontal sync signal for the DFP (in characters)
FP_H_SYNC_WID	21:16	0x0	Horizontal sync width (pixels * 8). If horz. fixed blank or autocentering is enabled this register field contains the width (in characters) of the horizontal sync signal for the DFP.
FP_H_SYNC_POL	23	0x0	DFP Horizontal sync polarity 0=Active high 1=Active low 0=Active high 1=Active low

Shadow Horizontal Sync for Digital Flat Panels.

Used for DFP HSYNC when FP\_GEN\_CNTL.DFP\_SYNC\_SEL=1 and used for CRT HSYNC when FP\_GEN\_CNTL.CRT\_SYNC\_SEL=1.

The FP\_H\_SYNC\_STRT\_PIX and FP\_H\_SYNC\_POL always apply to the DFP Horizontal Sync regardless of other control bits.(DFP\_SYNC\_SEL/CRT\_SYNC\_SEL/horizontal blanking mode/horz. autocentering)

FP_V_SYNC_STRT_WID - RW - 32 bits - [MMReg:0x2C8]			
Field Name	Bits	Default	Description
FP_V_SYNC_STRT	11:0	0x0	Vertical sync start position (in lines). Sum of display height, overscan bottom and front porch. If vertical fixed blank or autocentering is enabled(see CRTC_MORE_CNTL) this field contains the offset(from the bottom of the active display/start of vertical blank) within the vertical blank time of the start of the vertical sync signal for the DFP(in lines)
FP_V_SYNC_WID	20:16	0x0	Vertical sync width(in lines). If vert. fixed blank or autocentering is enabled this field contains the length (in lines) of the vertical sync signal for the DFP

FP_V_SYNC_POL	23	0x0	Vertical sync polarity 0=Active high 1=Active low 0=Active high 1=Active low
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Shadow Vertical Sync for Digital Flat Panels

AUX_WINDOW_HORZ_CNTL - RW - 32 bits - [MMReg:0x2D8]			
Field Name	Bits	Default	Description
AUX_WIN_HORZ_START	11:0	0x0	Pixel coordinate of left edge of auxiliary window.
AUX_WIN_HORZ_END	23:12	0x0	Pixel coordinate of right edge of auxiliary window.
AUX_WIN_EN	24	0x0	Auxiliary window enable/disable. 0=Disable 1=Enable
AUX_WIN_OUT_DELAY	28:25	0x5	Pixel accurate adjustment of AUXWIN position. Allows it to delayed relative to the RGB signals from the DAC. Available settings are: 000 = -5 pixels 001 = -4 pixels 010 = -3 pixels 011 = -2 pixels 100 = -1 pixel 101 = 0 pixels 110 = +1 pixels 111 = +2 pixels
RESERVED	30	0x1	Not used in this ASIC
AUX_WIN_LOCK  <i>(mirror of AUX_WINDOW_VERT_CNTL:AUX_WIN_LOCK)</i>	31	0x0	Locks AUX_WIN register fields to allow atomic update of all fields at once when unlocked. 0 = not locked, 1 = locked 0=don't lock 1=lock

Auxiliary window horizontal controls

AUX_WINDOW_VERT_CNTL - RW - 32 bits - [MMReg:0x2DC]			
Field Name	Bits	Default	Description
AUX_WIN_VERT_START	11:0	0x0	Line coordinate of top edge of auxiliary window.
AUX_WIN_VERT_END	27:16	0x0	Line coordinate of bottom edge of auxiliary window.

AUX_WINDOW_POL	30	0x0	Selects whether AUXWIN output is high or low when raster inside window coordinates. 0 = active high 1 = active low 0=Active high 1=Active low
AUX_WIN_LOCK	31	0x0	Locks AUX_WIN register fields to allow atomic update of all fields at once when unlocked. 0 = not locked, 1 = locked 0=don't lock 1=lock

Auxiliary window vertical controls

<b>GRPH_BUFFER_CNTL - RW - 32 bits - [MMReg:0x2F0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
GRPH_START_REQ	6:0	0x7c	Request watermark where display requests to memory controller will start. Normally set to the upper limit.  NOTE: Bits 0:1 of this field are hardwired to ZERO.
GRPH_STOP_REQ	14:8	0x7c	Request watermark where display requests to memory controller will stop. Normally set to the upper limit.  NOTE: Bits 0:1 of this field are hardwired to ZERO.
GRPH_CRITICAL_POINT	22:16	0x20	Read data watermark where pending display requests to the memory controller go to high priority. This forces the memory controller to service the pending display requests ASAP. Setting 0x00 forces all display requests to remain high priority at all times.
GRPH_CRITICAL_CNTL	28	0x0	For debug. Should always be set low. 0=Critical point based on current lowest write point. 1=Critical point based on last write point.
GRPH_BUFFER_SIZE	29	0x1	For debug. Should always be set high. 0=Extended mode graphics buffer is 64 entries maximum. 1=Extended mode graphics buffer is 128 entries maximum.
GRPH_CRITICAL_AT_SOF	30	0x0	For debug. Should always be set low. 0=Wait 1/2 line before going critical at start of each frame. 1=Go critical immediately at the start of each frame.
GRPH_STOP_CNTL	31	0x0	For debug. Should always be set low. 0=GRPH_STOP_REQ and VGA_STOP_REQ are -4 from actual stop point. 1=GRPH_STOP_REQ and VGA_STOP_REQ are exact stop point.

Control of display buffer fill requests for non-VGA modes. This register is programmed by the BIOS or DAL on display mode switches.

## 2.8 OverlayDisplay Registers

### Overlay Display Control Registers

OV0_Y_X_START - RW - 32 bits - [MMReg:0x400]			
Field Name	Bits	Default	Description
OV0_X_START	12:0	0x0	Overlay X ending coordinate relative to ACTIVE screen (0,0)
OV0_Y_START	28:16	0x0	Overlay Y ending coordinate relative to ACTIVE screen (0,0)

X/Y coords relative to active display in pixels

OV0_Y_X_END - RW - 32 bits - [MMReg:0x404]			
Field Name	Bits	Default	Description
OV0_X_END	12:0	0x0	Overlay X ending coordinate relative to ACTIVE screen (0,0)
OV0_Y_END	28:16	0x0	Overlay X ending coordinate relative to ACTIVE screen (0,0)

X/Y ending coordinates (inclusive) relative to active display in pixels

OV0_REG_LOAD_CNTL - RW - 32 bits - [MMReg:0x410]			
Field Name	Bits	Default	Description
OV0_LOCK	0	0x0	<p>If this bit is set, then the start of Display VBlank event that usually updates double buffered registers is ignored. Use this bit to autonomously update scaler and subpicture registers.</p> <p>To use, set this bit, and then poll OV0_LOCK_READBACK until the lock takes effect. In almost all situations the lock should take effect before the first read; however, it is theoretically possible that the lock will not take quickly if various clocks in the chip are programmed to very low frequencies (for power saving for example).</p> <p>Once the lock takes, write registers to update the overlay. Then write the lock bit to zero.</p> <p>The new settings will take effect at the next VBlank rising edge (provided that LOCK is left unset).  0=NOT LOCKED  1=LOCKED</p>
OV0_VBLANK_DURING_LOCK (R)	1	0x0	<p>This bit is updated only when OV0_LOCK transitions from 1 to 0. If VBlank occurred while OV0_LOCK was 1, then this bit will be updated to the value one. Otherwise it is updated to the value zero.  0=DID NOT HAPPEN  1=DID HAPPEN</p>
OV0_STALL_GUI_UNTIL_FLIP	2	0x0	<p>The intent here is for the overlay to be able to tell the GUI that it is using the surface that the GUI wants to render to. The overlay will send an 'OV0_SURFACE_IS_FREE' signal to the GUI. It will make this signal go low when there is a danger of front buffer overwrite as determined by software. If software wants to stall the GUI, then it will set OV0_STALL_GUI_UNTIL_FLIP when it locks, updates, and unlocks overlay and subpicture registers. OV0_SURFACE_IS_FREE will go low at unlock and then high during VBlank (when the hardware double buffering flips the registers). The behavior of OV0_SURFACE_IS_FREE is undefined if OV0_STALL_GUI_UNTIL_FLIP is written to when the lock bit is not set.</p> <p>OV0_SURFACE_IS_FREE is not an event signal. If it is low the WaitUntilEvent command must stall the GUI until it is high. It does not wait until the signal transitions from low to high. (i.e. If it is already high, there is no stall).</p> <p>0=DO NOT STALL  1=DO STALL</p>

OV0_LOCK_READBACK (R)	3	0x0	See OV0_LOCK. This bit indicates whether the lock took effect. 0=NOT LOCKED 1=LOCKED
OV0_FLIP_READBACK (R)	4	0x0	Status indication of whether last submitted overlay flip has occurred yet. 0=Flip not yet occurred. 1=Flip has occurred.

Overlay register load control

OV0_SCALE_CNTL - RW - 32 bits - [MMReg:0x420]			
Field Name	Bits	Default	Description
OV0_HORZ_PICK_NEAREST	2	0x0	Recommend set to zero. If source keying is absolutely needed, then we may need to drop the interpolated scale in order to make the source keyer work. 0=BLEND 1=FIX H_ALPHA = 0
OV0_VERT_PICK_NEAREST	3	0x0	Recommend set to zero. If source keying is absolutely needed, then we may need to drop the interpolated scale in order to make the source keyer work. 0=BLEND 1=FIX V_ALPHA = 0
OV0_SIGNED_UV	4	0x0	Support the signed UV source format needed by Apple. 0=UNSIGNED 1=SIGNED
OV0_GAMMA_SEL	7:5	0x0	Select gamma correction factor: (default=0) 0 = Brightness Enable 1 = Gamma 2.2 2 = Gamma 1.8 3 = Gamma 1.4  0=Linear, G=1.0 1=G=0.85 2=G=1.1 3=G=1.2 4=G=1.45 5=G=1.7 6=G=2.2 7=G=2.5

OV0_SURFACE_FORMAT	11:8	0x0	<p>Scale source pixel format from memory:</p> <p>0-2 = (reserved)            3 = 15 bpp aRGB 1555            4 = 16 bpp RGB 565            5 = (reserved)            6 = 32 bpp aRGB 8888            7-8 = (reserved)            9 = YUV 9            10 = YUV 12            11 = VYUY422            12 = YVYU422            13-15 = (reserved)            3=15BPP ARGB1555            4=16BPP RGB565            6=32BPP ARGB8888            9=Three plane YUV9            10=Three plane YUV12            11=Packed VYUY422            12=Packed YVYU422            13=Two plane YUV12</p>
OV0_ADAPTIVE_DEINT	12	0x0	<p>0=Adaptive de-interlacing is off.            1=Adaptive de-interlacing enabled.</p>
OV0_BURST_PER_PLANE	22:16	0x7f	
OV0_DOUBLE_BUFFER_REGS	24	0x0	<p>Recommend set to 1. Turns on double buffering so that many registers can be updated autonomously in the VBlank. Currently the following fields are double buffered but the list is subject to change as we attempt to reduce the gate count.</p> <p>OV0_V_INC, OV0_P1_V_ACCUM_INIT,            OV0_P23_V_ACCUM_INIT,            OV0_P1_BLNK_LN_AT_TOP_M1,            OV0_P1_ACTIVE_LINES_M1,            OV0_P23_BLNK_LN_AT_TOP_M1,            OV0_P23_ACTIVE_LINES_M1,            OV0_P1_OCTWORDS_PER_LINE_M1,            OV0_P2_OCTWORDS_PER_LINE_M1,            OV0_P3_OCTWORDS_PER_LINE_M1,            OV0_SMART_SWITCH, OV0_BURST_PER_PLANE,            OV0_SOFT_EOF_TOGGLE, OV0_DEINT_PAT,            OV0_DEINT_PAT_LEN_M1, OV0_P1_H_INC,            OV0_P23_H_INC, OV0_P1_H_STEP_BY,            OV0_P23_H_STEP_BY, OV0_P1_H_ACCUM_INIT,            OV0_PRESHIFT_P1_TO, OV0_P23_H_ACCUM_INIT,            OV0_PRESHIFT_P23_TO, OV0_P1_X_START,            OV0_P1_X_END, OV0_P2_X_START, OV0_P2_X_END,            OV0_P3_X_START, OV0_P3_X_END,            OV0_P1_MAX_LN_IN_PER_LN_OUT,            OV0_P23_MAX_LN_IN_PER_LN_OUT.</p> <p>0=OFF            1=ON</p>

OV0_BANDWIDTH (R)	26	0x0	0=NORMAL 1=BANDWIDTH LIMIT/ACK
OV0_INT_EMU	29	0x0	Enables experimental deinterlacing hardware which should make displayed video look sharper than 'bobbed' video, but without the feathering artifacts associated with 'weaved' video. It also makes colours richer. 0=OFF 1=ON
OV0_OVERLAY_EN	30	0x0	0 = Overlay Disable (default=0) 1 = Overlay Enable 0=DISABLE 1=ENABLE
OV0_SOFT_RESET	31	0x1	Resets the scaler. 0=ENABLE 1=RESET

General scaler control

OV0_V_INC - RW - 32 bits - [MMReg:0x424]			
Field Name	Bits	Default	Description
OV0_V_INC	25:8	0x0	Vertical accumulator increment [17:0]. This is a 6.12 fixed point number. It is used to control the vertical scaling ratio.

Vertical accumulator increment

OV0_P1_V_ACCUM_INIT - RW - 32 bits - [MMReg:0x428]			
Field Name	Bits	Default	Description
OV0_P1_MAX_LN_IN_PER_LN_OUT	1:0	0x1	This field supports a new feature which is the ability to read in and blend more than one line for every line output. Using it greatly improves image quality when downscaling vertically. However, memory bandwidth limits the number of lines that can be read in. Do not program the scaler to read in more lines than there is bandwidth to support. The scaler document provides an explanation on determining the available bandwidth.
OV0_P1_V_ACCUM_INIT	25:15	0x0	This is a 6.5 fixed point number. The integer portion indicates how many lines to fetch and cycle into (and possibly through) through the line buffers in preparation for generating the first display line. The fractional portion indicates the blend of source lines the four tap/two tap filter kernel that is used to generate the first display line.

This register is needed to accurately vertically position the source video in the overlay display window, and also to accurately position it relative to the subpicture image.

<b>OV0_P23_V_ACCUM_INIT - RW - 32 bits - [MMReg:0x42C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_P23_MAX_LN_IN_PER_LN_OUT	1:0	0x1	This field supports a new feature which is the ability to read in and blend more than one line for every line output. Using it greatly improves image quality when downscaling vertically. However, memory bandwidth limits the number of lines that can be read in. Do not program the scaler to read in more lines than there is bandwidth to support. The scaler document provides an explanation on determining the available bandwidth.
OV0_P23_V_ACCUM_INIT	24:15	0x0	This is a 6.5 fixed point number. The integer portion indicates how many lines (planer U and V lines) to fetch and cycle into (and possibly through) through the line buffers in preparation for generating the first display line. The fractional portion indicates the blend of source lines the four tap/two tap filter kernel that is used to generate the first display line.

Please refer to P1\_V\_ACCUM\_INIT. This register is used for the UV components in Planer modes.

<b>OV0_P1_BLANK_LINES_AT_TOP - RW - 32 bits - [MMReg:0x430]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_P1_BLNK_LN_AT_TOP_M1	11:0	0xff	This is a signed value. Default it to -1 and don't exceed the maximum positive value.
OV0_P1_ACTIVE_LINES_M1	27:16	0x0	Program this with the surface height minus one. After the hardware scales and displays the blank lines at top and the active lines, it will continue to scale and display blank lines until it reaches the end of the overlay window.

Used for DVD letterboxing (when a wide movie is displayed with black borders at the top and bottom). The problem is that software can't provide the black borders using the primary display because subpicture information can be displayed in the black regions. It also is wasteful to allocate extra off screen memory in the frame buffer and fill it with 'black' pixels. Thus use these fields to create the black borders for DVD letterboxing.

<b>OV0_P23_BLANK_LINES_AT_TOP - RW - 32 bits - [MMReg:0x434]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_P23_BLNK_LN_AT_TOP_M1	10:0	0x7ff	This is a signed value. Default it to -1 and don't exceed the maximum positive value.

OV0_P23_ACTIVE_LINES_M1	26:16	0x0	Program this with the surface height minus one. After the hardware scales and displays the blank lines at top and the active lines, it will continue to scale and display blank lines until it reaches the end of the overlay window.
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Please refer to P1\_BLANK\_LINES\_AT\_TOP. This register is used for the UV components in Planer modes.

OV0_BASE_ADDR - RW - 32 bits - [MMReg:0x43C]			
Field Name	Bits	Default	Description
OV0_BASE_ADDR	31:0	0x0	This base is added to all overlay address requests to the internal memory controller. Setting this register equal to MC_FB_LOCATION.MC_FB_START positions all overlay surfaces in the frame buffer. Alternatively setting it to MC_AGP_LOCATION.MC_AGP_START positions overlay surfaces in AGP memory. The use of the overlay from AGP is supported, but not recommended. This base address must be a 4 Megabyte aligned value.  NOTE: Bits 0:21 of this field are hardwired to ZERO.

Overlay base address

OV0_VID_BUF0_BASE_ADRS - RW - 32 bits - [MMReg:0x440]			
Field Name	Bits	Default	Description
OV0_VID_BUF_PITCH_SEL	0	0x0	Associates either OV0_VID_BUF_PITCH0_VALUE register or OV0_VID_BUF_PITCH1_VALUE register with this surface or plane of a planer surface. 0=SELECT PITCH 0 1=SELECT PITCH 1
RESERVED_BIT1	1	0x0	reserved for tiling info. No overlay tiling in this ASIC.
OV0_VID_BUF_BASE_ADRS	26:4	0x0	BASE_ADRS is actually a poor choice of name. This field points to the octaword that contains the top left corner pixel of the region of the surface that you wish to display.
RESERVED_BIT31_28	31:28	0x0	reserved for tiling info. No overlay tiling in this ASIC.

A surface descriptor register that include the base address (or base offset) of a surface, and some attributes for pitch selection and tiled surface support.

Double buffering (for autonomous overlay updates), or multi-buffering can be achieved by switching between any of the six base address registers using the OV0\_AUTOFLIP\_CNTL register. (Note: for planer surfaces the six registers are interpreted by hardware as two sets of three registers. Thus only OV0\_VID\_BUF0 and OV0\_VID\_BUF3 are valid selections.)

OV0\_VID\_BUF0 can describe any non-planer surface, or it can be used to describe the Y plane of a planer surface.

<b>OV0_VID_BUF1_BASE_ADRS - RW - 32 bits - [MMReg:0x444]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_VID_BUF_PITCH_SEL	0	0x0	Same as in OV0_VID_BUF0_BASE_ADRS. 0=SELECT PITCH 0 1=SELECT PITCH 1
RESERVED_BIT1	1	0x0	reserved for tiling info. No overlay tiling in this ASIC.
OV0_VID_BUF_BASE_ADRS	26:4	0x0	Same as in OV0_VID_BUF0_BASE_ADRS.
RESERVED_BIT31_28	31:28	0x0	reserved for tiling info. No overlay tiling in this ASIC.

OV0\_VID\_BUF1 can describe any non-planer surface, or it can be used to describe the U plane of a planer surface.

<b>OV0_VID_BUF2_BASE_ADRS - RW - 32 bits - [MMReg:0x448]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_VID_BUF_PITCH_SEL	0	0x0	Same as in OV0_VID_BUF0_BASE_ADRS. 0=SELECT PITCH 0 1=SELECT PITCH 1
RESERVED_BIT1	1	0x0	reserved for tiling info. No overlay tiling in this ASIC.
OV0_VID_BUF_BASE_ADRS	26:4	0x0	Same as in OV0_VID_BUF0_BASE_ADRS.
RESERVED_BIT31_28	31:28	0x0	reserved for tiling info. No overlay tiling in this ASIC.

OV0\_VID\_BUF2 can describe any non-planer surface, or it can be used to describe the V plane of a planer surface.

<b>OV0_VID_BUF3_BASE_ADRS - RW - 32 bits - [MMReg:0x44C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_VID_BUF_PITCH_SEL	0	0x0	Same as in OV0_VID_BUF0_BASE_ADRS. 0=SELECT PITCH 0 1=SELECT PITCH 1
RESERVED_BIT1	1	0x0	reserved for tiling info. No overlay tiling in this ASIC.
OV0_VID_BUF_BASE_ADRS	26:4	0x0	Same as in OV0_VID_BUF0_BASE_ADRS.
RESERVED_BIT31_28	31:28	0x0	reserved for tiling info. No overlay tiling in this ASIC.

OV0\_VID\_BUF3 can describe any non-planer surface, or it can be used to describe the Y plane of a planer surface.

<b>OV0_VID_BUF4_BASE_ADRS - RW - 32 bits - [MMReg:0x450]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_VID_BUF_PITCH_SEL	0	0x0	Same as in OV0_VID_BUF0_BASE_ADRS. 0=SELECT PITCH 0 1=SELECT PITCH 1
RESERVED_BIT1	1	0x0	reserved for tiling info. No overlay tiling in this ASIC.
OV0_VID_BUF_BASE_ADRS	26:4	0x0	Same as in OV0_VID_BUF0_BASE_ADRS.
RESERVED_BIT31_28	31:28	0x0	reserved for tiling info. No overlay tiling in this ASIC.

OV0\_VID\_BUF4 can describe any non-planer surface, or it can be used to describe the U plane of a planer surface.

<b>OV0_VID_BUF5_BASE_ADRS - RW - 32 bits - [MMReg:0x454]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_VID_BUF_PITCH_SEL	0	0x0	Same as in OV0_VID_BUF0_BASE_ADRS. 0=SELECT PITCH 0 1=SELECT PITCH 1
RESERVED_BIT1	1	0x0	reserved for tiling info. No overlay tiling in this ASIC.
OV0_VID_BUF_BASE_ADRS	26:4	0x0	Same as in OV0_VID_BUF0_BASE_ADRS.
RESERVED_BIT31_28	31:28	0x0	reserved for tiling info. No overlay tiling in this ASIC.

OV0\_VID\_BUF5 can describe any non-planer surface, or it can be used to describe the V plane of a planer surface.

<b>OV0_VID_BUF_PITCH0_VALUE - RW - 32 bits - [MMReg:0x460]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_PITCH_VALUE	19:4	0x0	For linear (non-tiled) surfaces, the pitch value is the pitch of the surface, or in the case of planer modes, the pitch of a plane in a surface. For tiled modes, the pitch value is not the pitch. It is a number that the hardware needs to get from the beginning of last line that it read in the previous row of tiles to the beginning first line that it must read in the next row of tiles. To understand this concept, you need a solid understanding of how tiled surfaces are organized in memory. (there is code in the ov0setup.cpp sample code that does the necessary calculations).

OV0_PITCH_SKIP_LINES	27:26	0x0	Used only if the surface (or plane in planer surface) is tiled. Ignored otherwise.  When downscaling, or when picking off the even or odd lines of an MPEG frame, it is sometimes desirable to 'double the pitch'. However, unlike linear surfaces, doubling the pitch in a tiled surface doesn't have the desired effect. Therefore, hardware provides a mechanism for skipping lines. Using this field will require that the OV0_PITCH?_VALUE field be changed as well. 0=USE EVERY LINE 1=USE EVERY 2nd LINE 2=USE EVERY 4th LINE 3=USE EVERY 8th LINE
OV0_PITCH_IN_TILES_LSBS	31:28	0x0	Not used. No overlay tiling in this ASIC.

Fields needed for advancing the hardware's line start address pointer from the beginning of one line to the beginning of the next, and for enabling correct checkerboarding in tiled modes.

<b>OV0_VID_BUF_PITCH1_VALUE - RW - 32 bits - [MMReg:0x464]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_PITCH_VALUE	19:4	0x0	See OV0_VID_BUF_PITCH0_VALUE.
OV0_PITCH_SKIP_LINES	27:26	0x0	See OV0_VID_BUF_PITCH0_VALUE. 0=USE EVERY LINE 1=USE EVERY 2nd LINE 2=USE EVERY 4th LINE 3=USE EVERY 8th LINE
OV0_PITCH_IN_TILES_LSBS	31:28	0x0	Not used. No overlay tiling in this ASIC.

A second set of pitch fields that can be used to implement double buffering when changing the pitch, or that can be used to have different pitches for different planes in planer modes (YUV9 and YUV12). Selection of Pitch0/Pitch1 is controlled by the OV0\_VID\_BUF?\_PITCH\_SEL field in the selected OV0\_VID\_BUF?\_BASE\_ADRS register.

<b>OV0_AUTO_FLIP_CNTRL - RW - 32 bits - [MMReg:0x470]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_SOFT_BUF_NUM	2:0	0x0	A pointer to one of the six base address registers. For non-planer modes valid values are from 0 to 5. For planer modes valid values are 0 and 3.
OV0_SOFT_REPEAT_FIELD	3	0x0	0=LAST FIELD NOT REPEAT 1=LAST FIELD IS REPEAT

OV0_SOFT_BUF_ODD	4	0x0	<p>For non-interlaced video (e.g. MPEG frames) this field is don't care, but the SHIFT_EVEN_DOWN and SHIFT_ODD_DOWN register fields should be zero. For interlaced video provided by a software application, this field should indicate if the video field is even or odd. If This value is ignored until the internal version of the _EOF_TOGGLE signal changes state.</p> <p>0=EVEN 1=ODD</p>
OV0_IGNORE_REPEAT_FIELD	5	0x0	<p>If a hardware video capture port is selected, and if the video input stream has embedded repeat field flags, then these can be used to reset the deinterlacing pattern. Specifically, the current pattern will be used to select how the field that just arrived and it's two predecessors are displayed. The next time a field arrives, deinterlacing pattern zero will be used.</p> <p>Setting this bit will cause the repeat field flags to be ignored.</p> <p>If VID_PORT_SELECT is 2 (software), then the hardware assumes that every incoming field has a REPEAT_FIELD attribute. Use this bit to disable that attribute on a field by field basis.</p> <p>0=DON'T IGNORE 1=DO IGNORE</p>
OV0_SOFT_EOF_TOGGLE	6	0x0	<p>After writing SOFT_BUF_NUM and SOFT_BUF_ODD, then change the state of the EOF_TOGGLE bit. The EOF_TOGGLE signal is double buffered, so your change won't happen to the internal version of EOF_TOGGLE (and thus won't be used by hardware) until the start of VBlank, and then only if the LOCK bit is low. However when the internal version does change state, the hardware becomes aware of the new field/frame of video that you describe using SOFT_BUF_NUM and SOFT_BUF_ODD.</p>
OV0_VID_PORT_SELECT	9:8	0x0	<p>Selects one of the two capture engines or a software application as the provider of video.</p> <p>0=PORT 0 1=reserved 2=SOFTWARE</p>
OV0_P1_FIRST_LINE_EVEN	16	0x0	<p>If you are weaving two fields together, then you must indicate if the first line that the scaler will fetch is in the field labeld even or the field labeld odd.</p> <p>0=IS ODD 1=IS EVEN</p>
OV0_SHIFT_EVEN_DOWN	18	0x0	<p>If 'bobbing' video (Called 'Run' Deinterlacing) then this bit allows you to shift the even fields down.</p>
OV0_SHIFT_ODD_DOWN	19	0x0	<p>If 'bobbing' video (Called 'Run' Deinterlacing) then this bit allows you to shift the odd fields down.</p>

OV0_FIELD_POL_SOURCE	23	0x0	0=Video field polarity taken from next source field. Recommended for bob. 1=Video field polarity taken from current source field. Recommended for weave.
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As a video capture port or software application provides new fields or frames of video, information about where these new fields/frames, what they are, and how they should be displayed is passed to the scaler using the AUTO\_FLIP\_CNTRL register.

OV0\_SOFT\_BUF\_NUM, OV0\_SOFT\_BUF\_ODD, and OV0\_IGNORE\_REPEAT\_FIELD are a software application's way of describing new video fields or frames to hardware. These values are ignored until the internal (double buffered) version of the \_EOF\_TOGGLE signal changes state.

If a new video field or frame is created, indicate where it is by writing the address into an unused BASE ADDRESS REGISTER. (If you have already set up a circular buffer then this may already be done). Then write the number of the base address register in OV0\_SOFT\_BUF\_NUM. Also set it's attributes using OV0\_SOFT\_BUF\_ODD and OV0\_IGNORE\_REPEAT\_FIELD. Then change the value of SOFT\_EOF\_TOGGLE to submit the description of the new field to hardware.

The hardware will display some 'combination' of this field and the two previous fields. ('Weave' most recent with next most recent, or 'Weave' the second and third most recent, 'Bob' most recent, or 'Bob' the second most recent)

OV0_DEINTERLACE_PATTERN - RW - 32 bits - [MMReg:0x474]			
Field Name	Bits	Default	Description
OV0_DEINT_PAT	19:0	0x0	Ten two bit values. Values are enumerated as follows: 0) weave the two most recently submitted fields together and display them, 1) weave the second two most recently submitted fields together and display them, 2) display only the most recently submitted field (using 'bob' deinterlacing), 3) display only the second most recently submitted field (using 'bob' deinterlacing), The scaler documentation provides example patterns of two bit values that can be programmed into this field. This field is double buffered. A two bit value is sampled from the position indicated by the OV0_DEINT_PAT_PNTR at the beginning of a display frame after a new video field is submitted. This two bit value remains in use until a new field is submitted.
OV0_DEINT_PAT_PNTR (R)	27:24	0x0	Read this to find out which two bit value in the pattern the video is currently using.
OV0_DEINT_PAT_LEN_M1	31:28	0x0	Set this to 9 if you want to cycle through all ten two bit values, else set it to a lower value.

The scaler remembers the last three fields of video that were provided. There are 10 two bit values in the OV0\_DEINETRACE\_PATTERN register. Each two bit value selects one of four ways that these fields should be displayed.

OV0_H_INC - RW - 32 bits - [MMReg:0x480]			
Field Name	Bits	Default	Description
OV0_P1_H_INC	13:0	0x0	Horizontal scale increment (1/Scale Ratio) for Y, R, G, and B. It is a 2.12 fixed point number.
OV0_P23_H_INC	29:16	0x0	Horizontal scale increment (1/Scale Ratio) for U and V (Actually Cb and Cr). It is a 2.12 fixed point number.

This register indicates how much to scale the Y, R, G, B (P1) or UV (P23) in the horizontal direction. Note that to improve quality when downscaling you should decimate the data first using the 'STEP\_BY' register fields. The decimated data is then scaled by the amount that you indicate using P?\_H\_INC. The CalcH.cpp function provides the decision making code required to do this.

OV0_STEP_BY - RW - 32 bits - [MMReg:0x484]			
Field Name	Bits	Default	Description
OV0_P1_H_STEP_BY	2:0	0x0	P1 refers to the Y in YUV, to G in RGB32, and to RGB in RGB 15/16. In RGB15/16 the value zero (four tap vertical filtering) is not supported. 0=STEP BY 1, 4TAP VBLEND 1=STEP BY 1, 2TAP VBLEND 2=STEP BY 2, 2TAP VBLEND 3=STEP BY 4 or 3/5, 2TAP VBLEND 4=STEP BY 8 or 7/9 or 6/10, 2TAP VBLEND 5=STEP BY 15/17 or 14/18, 2TAP VBLEND
OV0_P1_PREDWNSC_RATIO	4	0x0	Enables horizontal pre-downscaling for use when horizontal downscale ratio of P1 data is less than 2:1. 0=No predownscale, i.e. 1:1 1=Predownscale 2:1
OV0_P23_H_STEP_BY	10:8	0x0	P23 refers to the UV in YUV, and to RB in RGB32. It is not used in RGB15/16 0=PLANER UV STEP BY 1, 4TAP VBLEND 1=PLANER UV STEP BY 1, 2TAP VBLEND 2=PLANER UV STEP BY 2, 2TAP VBLEND 3=PLANER UV STEP BY 4, 2TAP VBLEND 4=PLANER UV STEP BY 8, 2TAP VBLEND 5=PLANER UV STEP BY 14/18, 2TAP VBLEND
OV0_P23_PREDWNSC_RATIO	12	0x0	Enables horizontal pre-downscaling for use when horizontal downscale ratio of P23 data is less than 2:1. In modes where P23 data is already sub-sampled horizontally, this would only be used when the horizontal scale ratio goes below 4:1. 0=No predownscale, i.e. 1:1 1=Predownscale 2:1

Horizontal scaling is performed via a combination of horizontal blending and horizontal decimation. There is a limit to how many source pixels the vertical scalers can provide to the horizontal scalers per output pixel. If H\_STEP\_BY is zero, then the vertical filters perform four tap vertical filtering. If H\_STEP\_BY is greater than zero, then the the vertical scalers reconfigure themselves so that they provide twice as many pixels per clock, but perform only linear two tap vertical filtering to generate those pixels. If H\_STEP\_BY is 2, then the vertical filters fetch only the pixels with and even X coordinate relative to the octword alligned surface base offset. If H\_STEP\_BY is 3, then every 4th pixel is fetched, etc. For ease of implementation reasons, at higher H\_STEP\_BY settings, the spacing between may not be an exact power of two. For example when H\_STEP\_BY is 4, the hardware may step by 7,9,7,9 rather than stepping by 8,8,8,8.

The code to program this field is provided in a function called CalcH.cpp

<b>OV0_P1_H_ACCUM_INIT - RW - 32 bits - [MMReg:0x488]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_P1_H_ACCUM_INIT	19:15	0x0	Indicates the blend of source pixels you want in the four tap filter kernal to provide to generate the first display pixel. The ov0setup.cpp program shows how to calculate the correct value.
OV0_PRESHIFT_P1_TO	31:28	0x2	Indicates how many source pixels you want to preshift into the horizontal Y four tap filter to generate the first display pixel. Please refer to the documentation for sample code on how to program this field. Typically this value is two or three.

This register is needed to accurately horizontally position the source video in the overlay display window, and also to accurately position it relative to the subpicture image.

<b>OV0_P23_H_ACCUM_INIT - RW - 32 bits - [MMReg:0x48C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_P23_H_ACCUM_INIT	19:15	0x0	Indicates the blend of source pixels you want in the four tap filter kernal to provide to generate the first display pixel. The ov0setup.cpp program shows how to calculate the correct value.
OV0_PRESHIFT_P23_TO	30:28	0x2	Indicates how many source pixels you want to preshift into the horizontal U and V four tap filters to generate the first display pixel. Please refer to the documentation for sample code on how to program this field. Typically this value is two or three.

Please refer to P1\_H\_ACCUM\_INIT. This register is used for the UV components in Planer modes.

<b>OV0_P1_X_START_END - RW - 32 bits - [MMReg:0x494]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_P1_X_END	11:0	0x0	End pixel in an octword aligned line for Y, R, G, and B
OV0_P1_X_START	19:16	0x0	Start pixel in an octword aligned line for Y, R, G, and B

Fields in the OV0\_VID\_BUF?\_BASE\_ADRS and OV0\_VID\_BUF\_PITCH?\_VALUE registers are used to determine the address of the start octword for each line. The P?\_X\_START\_END registers indicate more accurately where the lines start and ends relative to that first octword. The P?\_X\_START field indicates exactly which pixel in the first octword to start on. The P?\_X\_END field indicates which pixel to end on relative to pixel zero in the first octword. The hardware uses the P?\_X\_END and the SURFACE\_FORMAT fields to determine how many octwords to fetch.

This register allows pixel accurate windowing of the source surface which was not supported in earlier chips. It is now possible to zoom, pan (for DVD pan and scan), and clip the source.

Refer to ov0setup.cpp for sample code on how to program this register. You will notice the the CalcH.cpp routine returns values, P1StepSize and P23StepSize, that indicate the horizontal step when downscaling. These are used to insure that the start and end values are programmed correctly if pixel dropping occurs during horizontal downscaling.

P1 refers to Y, R, G, and B

<b>OV0_P2_X_START_END - RW - 32 bits - [MMReg:0x498]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_P2_X_END	10:0	0x0	End pixel in an octword aligned line for U.
OV0_P2_X_START	19:16	0x0	Start pixel in an octword aligned line for U

See the P1 description. This register (and its fields) will be renamed OV0\_P23\_X\_START\_END in the near future.

P2 refers to Cb (U)

<b>OV0_P3_X_START_END - RW - 32 bits - [MMReg:0x49C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_P3_X_END	10:0	0x0	End pixel in an octword aligned line for V (program to the same value as OV0_P2_X_END if this register still exists.)
OV0_P3_X_START	19:16	0x0	Start pixel in an octword aligned line for V (program to the same value as OV0_P2_X_START if this register still exists.)

See the P1 description. Note that you can no longer program the P2(U) and P3(V) start and end points to different values. To support planer surfaces where the U and V planes to share a pitch, make sure that the pitch is a multiple of two octwords. This register is now redundant and will be removed at the earliest opportunity.

P3 refers to Cr (U)

<b>OV0_FILTER_CNTL - RW - 32 bits - [MMReg:0x4A0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_HC_COEF_ON_HORZ_Y	0	0x0	Selects the hard coded upscaling filter coefficients for scaling the Y component horizontally. 0=PROGRAMABLE 1=HARD CODED
OV0_HC_COEF_ON_HORZ_UV	1	0x0	Selects the hard coded upscaling filter coefficients for scaling the UV component horizontally. 0=PROGRAMABLE 1=HARD CODED
OV0_HC_COEF_ON_VERT_Y	2	0x0	Selects the hard coded upscaling filter coefficients for scaling the Y component vertically. Applies only if the vertical filter engine is performing four tap filtering on the Y. 0=PROGRAMABLE 1=HARD CODED
OV0_HC_COEF_ON_VERT_UV	3	0x0	Selects the hard coded upscaling filter coefficients for scaling the UV component vertically. Applies only if the vertical filter engine is performing four tap filtering on the UV. 0=PROGRAMABLE 1=HARD CODED

There are five four tap filters. It is expensive to provide each filter with it's own set of programmable coefficients, so there are hard coded coefficients suitable for upscaling built into the hardware. For example, if you have to use the programable coefficients to specify a gaussian curve for downscaling Y horizontally, but you still want to upsample the UV using the sharper upscaling truncated sync function, then use the hard coded coefficients for the horizontal UV.

<b>OV0_FOUR_TAP_COEF_0 - RW - 32 bits - [MMReg:0x4B0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_COEF__0TH_TAP	3:0	0x0	
OV0_COEF__1ST_TAP	14:8	0x0	
OV0_COEF__2ND_TAP	22:16	0x0	
OV0_COEF__3RD_TAP	27:24	0x0	

Coefficients used for phase 0/8. 0TH\_TAP means the left most of top most pixel in a set of four will be multiplied by this coefficient.

<b>OV0_FOUR_TAP_COEF_1 - RW - 32 bits - [MMReg:0x4B4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_COEF__0TH_TAP	3:0	0x0	
OV0_COEF__1ST_TAP	14:8	0x0	
OV0_COEF__2ND_TAP	22:16	0x0	
OV0_COEF__3RD_TAP	27:24	0x0	

Coefficients used for phase 1/8 and 5/8 when swapped. 0TH\_TAP means the left most of top most pixel in a set of four will be multiplied by this coefficient when the coefficients aren't swapped.

<b>OV0_FOUR_TAP_COEF_2 - RW - 32 bits - [MMReg:0x4B8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_COEF__0TH_TAP	3:0	0x0	
OV0_COEF__1ST_TAP	14:8	0x0	
OV0_COEF__2ND_TAP	22:16	0x0	
OV0_COEF__3RD_TAP	27:24	0x0	

Coefficients used for phase 2/8 and 6/8 when swapped. 0TH\_TAP means the left most of top most pixel in a set of four will be multiplied by this coefficient when the coefficients aren't swapped.

<b>OV0_FOUR_TAP_COEF_3 - RW - 32 bits - [MMReg:0x4BC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_COEF__0TH_TAP	3:0	0x0	
OV0_COEF__1ST_TAP	14:8	0x0	
OV0_COEF__2ND_TAP	22:16	0x0	
OV0_COEF__3RD_TAP	27:24	0x0	

Coefficients used for phase 3/8 and 7/8 when swapped. 0TH\_TAP means the left most of top most pixel in a set of four will be multiplied by this coefficient when the coefficients aren't swapped.

<b>OV0_FOUR_TAP_COEF_4 - RW - 32 bits - [MMReg:0x4C0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_COEF__0TH_TAP	3:0	0x0	
OV0_COEF__1ST_TAP	14:8	0x0	
OV0_COEF__2ND_TAP	22:16	0x0	
OV0_COEF__3RD_TAP	27:24	0x0	

Coefficients used for phase 4/8. 0TH\_TAP means the left most of top most pixel in a set of four will be multiplied by this coefficient.

<b>OV0_FLAG_CNTRL - RW - 32 bits - [MMReg:0x4DC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_HI_PRI_MCREQ	3:0	0x8	
OV0_HI_PRI_FORCE	8	0x0	0=NO FORCE 1=FORCE
OV0_LUMA_10BIT_EN	12	0x0	0=H filter produces 8 bits for luma 1=H filter produces 10 bits for luma
OV0_CHROMA_10BIT_EN	13	0x0	0=H filter produces 8 bits for chroma 1=H filter produces 10 bits for chroma

No description available for this register.

<b>OV0_VID_KEY_CLR_LOW - RW - 32 bits - [MMReg:0x4E4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_VID_KEY_Cb_BLUE_LOW	9:0	0x0	Overlay/subpicture keyer Cb or blue component lower limit.
OV0_VID_KEY_Y_GREEN_LOW	19:10	0x0	Overlay/subpicture keyer Y or green component lower limit.
OV0_VID_KEY_Cr_RED_LOW	29:20	0x0	Overlay/subpicture keyer Cr or red component lower limit.

Overlay/subpicture range keyer lower limits. The overlay/subpicture blend unit output where keying is done is 30bpp. This is the data before color conversion or gamma adjustment.

<b>OV0_GRP_KEY_CLR_LOW - RW - 32 bits - [MMReg:0x4EC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_GRP_KEY_BLUE_LOW	7:0	0x0	Graphics keyer blue component lower limit.
OV0_GRP_KEY_GREEN_LOW	15:8	0x0	Graphics keyer green component lower limit.
OV0_GRP_KEY_RED_LOW	23:16	0x0	Graphics keyer red component lower limit.
OV0_GRP_KEY_ALPHA_LOW	31:24	0x0	Graphics keyer alpha component lower limit.

Graphics range keyer lower limits. Note in some modes expansion is needed to create an 8 bit red, green, blue or alpha from the 4, 5, or 6 bits stored in the frame buffer. This is controlled by DAC\_CNTL.DAC\_EXPAND\_MODE. Graphics keying is always done on 8 bit post-expanded data. For pixel depths that do not have alpha, set the ALPHA\_LOW to 0x00. To key on only the alpha channel in 15 or 32 bpp, set the color lower limits to 0x00.

<b>OV0_GRP_KEY_CLR_HIGH - RW - 32 bits - [MMReg:0x4F0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_GRP_KEY_BLUE_HIGH	7:0	0x0	Graphics keyer blue component upper limit.
OV0_GRP_KEY_GREEN_HIGH	15:8	0x0	Graphics keyer green component upper limit.
OV0_GRP_KEY_RED_HIGH	23:16	0x0	Graphics keyer red component upper limit.
OV0_GRP_KEY_ALPHA_HIGH	31:24	0x0	Graphics keyer alpha component upper limit.

Graphics range keyer upper limits. Note in some modes expansion is needed to create an 8 bit red, green, blue or alpha from the 4, 5, or 6 bits stored in the frame buffer. This is controlled by DAC\_CNTL.DAC\_EXPAND\_MODE. Graphics keying is always done on 8 bit post-expanded data. For pixel depths that do not have alpha, set the ALPHA\_HIGH to 0xFF. To key on only the alpha channel in 15 or 32 bpp, set the color high limits to 0xFF.

<b>OV0_KEY_CNTL - RW - 32 bits - [MMReg:0x4F4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_VIDEO_KEY_FN	1:0	0x0	Selects overlay keyer result equation. Result used as stated in OV0_CMP_MIX. 0=VID_KEY = FALSE = 0 1=VID_KEY = TRUE = 1 2=VID_KEY = (VID_Cr_BLUE in range) AND (VID_Cb_GREEN in range) AND (VID_Y_RED in range) 3=VID_KEY = not [(VID_Cr_BLUE in range) AND (VID_Cb_GREEN in range) AND (VID_Y_RED in range)]

OV0_GRAPHICS_KEY_FN	5:4	0x0	Selects graphics keyer result equation. Result used as stated in OV0_CMP_MIX. 0=GRPH_KEY = FALSE = 0 1=GRPH_KEY = TRUE = 1 2=GPPH_KEY = (GRPH_BLUE in range) AND (GRPH_GREEN in range) AND (GRPH_RED in range) AND (GRPH_ALPHA in range) 3=GRPH_KEY = not [(GRPH_BLUE in range) AND (GRPH_GREEN in range) AND (GRPH_RED in range) AND (GRPH_ALPHA in range)]
OV0_CMP_MIX	8	0x0	Selects final mix of graphics and video keys. Result used as stated in DISP_MERGE_CNTL.DISP_ALPHA_MODE. 0=GRPH_VID_KEY = GRPH_KEY or VID_KEY 1=GRPH_VID_KEY = GRPH_KEY and VID_KEY

Graphics/overlay keyer control

OV0_TEST - RW - 32 bits - [MMReg:0x4F8]			
Field Name	Bits	Default	Description
OV0_SUBPIC_ONLY	3	0x0	Forces the subpicture data on. 0=NORMAL 1=PURE SUBPICTURE DATA
OV0_SWAP_UV	5	0x0	This field will swap the U and V components (and also the R and B components in RGB modes). 0=NO SWAP 1=SWAP
OV0_NOROUNDUP	6	0x0	0=ROUND UP HORZ & VERT FIR 1=DO NOT ROUND UP HORZ & VERT FIR
OV0_ADAPTIVE_DEINT_ADJ	13:12	0x0	

Test registers for the scaler.

## 2.9 Display Merge Registers

### Display Merge Control Registers

DISP_MISC_CNTL - RW - 32 bits - [MMReg:0xD00]			
Field Name	Bits	Default	Description
SOFT_RESET_GRP_H_PP	0	0x0	0=Not reset 1=Reset graphics and cursor pixel pipe in pixel clock domain
SOFT_RESET_SUBPIC_PP	1	0x0	0=Not reset 1=Reset sub-picture pixel pipe in pixel clock domain
SOFT_RESET_OV0_PP	2	0x0	0=Not reset 1=Reset ov0scale pixel pipe in pixel clock domain
SOFT_RESET_GRP_H_SCLK	4	0x0	0=Not reset 1=Reset graphics and cursor logic in system clock domain
SOFT_RESET_SUBPIC_SCLK	5	0x0	0=Not reset 1=Reset sub-picture logic in system clock domain
SOFT_RESET_OV0_SCLK	6	0x0	0=Not reset 1=Reset ov0scale logic in system clock domain
SYNC_STRENGTH	9:8	0x2	0=Minimum drive. ~74 ohms. 1=Matched impedance drive. ~63 ohms. 2=Optimal drive. ~47 ohms. 3=Maximum drive. ~42 ohms.
PALETTE_MEM_RD_MARGIN	27:24	0x3	
RMX_BUF_MEM_RD_MARGIN	31:28	0x3	

No description available for this register.

DAC_MACRO_CNTL - RW - 32 bits - [MMReg:0xD04]			
Field Name	Bits	Default	Description
DAC_WHITE_CNTL	3:0	0x8	
DAC_BG_ADJ	11:8	0x8	
DAC_PDWN_R	16	0x0	
DAC_PDWN_G	17	0x0	
DAC_PDWN_B	18	0x0	

No description available for this register.

<b>DISP_TEST_DEBUG_CNTL - RW - 32 bits - [MMReg:0xD10]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_TEST_DISPENG	0	0x0	0=Disable 1=Enable
DISP_TEST_PALETTE	1	0x0	0=Disable 1=Enable
DISP_TEST_DAC	2	0x0	0=Disable 1=Enable
DISP_TEST_SUBPIC	3	0x0	0=Disable 1=Enable
DISP_TEST_OV0SCALE	4	0x0	0=Disable 1=Enable
DISP_TEST_CLK	5	0x0	0=Disable 1=Enable
DISP_GRP_UNDERFLOW (R)	24	0x0	0=No graphics underflow 1=Graphics buffer has underflowed since last cleared
DISP_GRP_UNDERFLOW_CLR (W)	24	0x0	0=Write 0, no effect 1=Write 1, clear graphics buffer underflow flag
DISP_CUR_UNDERFLOW (R)	25	0x0	0=No cursor underflow 1=Cursor buffer has underflowed since last cleared
DISP_CUR_UNDERFLOW_CLR (W)	25	0x0	0=Write 0, no effect 1=Write 1, clear cursor buffer underflow flag
DISP_OV0_UNDERFLOW (R)	26	0x0	0=No overlay underflow 1=Overlay buffer has underflowed since last cleared
DISP_OV0_UNDERFLOW_CLR (W)	26	0x0	0=Write 0, no effect 1=Write 1, clear overlay buffer underflow flag
DISP_SUBPIC_UNDERFLOW (R)	27	0x0	0=No sub-picture underflow 1=Sub-picture buffer has underflowed since last cleared
DISP_SUBPIC_UNDERFLOW_CLR (W)	27	0x0	0=Write 0, no effect 1=Write 1, clear sub-picture buffer underflow flag
DISP_SUBPIC_FORCE_HI_PRI	28	0x0	0=Use hardware circuit to generate high priority bit for memory request 1=Force subpic to be high priority memory requester

Test and debug controls for display block.

DISP_HW_DEBUG - RW - 32 bits - [MMReg:0xD14]			
Field Name	Bits	Default	Description
DISP_HW_0_DEBUG	0	0x0	
DISP_HW_1_DEBUG	1	0x0	
DISP_HW_2_DEBUG	2	0x0	
DISP_HW_3_DEBUG	3	0x0	
DISP_HW_4_DEBUG	4	0x0	
DISP_HW_5_DEBUG	5	0x0	
DISP_HW_6_DEBUG	6	0x0	
DISP_HW_7_DEBUG	7	0x0	
DISP_HW_8_DEBUG	8	0x0	
DISP_HW_9_DEBUG	9	0x0	
DISP_HW_A_DEBUG	10	0x0	
DISP_HW_B_DEBUG	11	0x0	
DISP_HW_C_DEBUG	12	0x0	
DISP_HW_D_DEBUG	13	0x0	
DISP_HW_E_DEBUG	14	0x0	
DISP_HW_F_DEBUG	15	0x0	
DISP_HW_10_DEBUG	16	0x0	
DISP_HW_11_DEBUG	17	0x0	
DISP_HW_12_DEBUG	18	0x0	
DISP_HW_13_DEBUG	19	0x0	
DISP_HW_14_DEBUG	20	0x0	
DISP_HW_15_DEBUG	21	0x0	
DISP_HW_16_DEBUG	22	0x0	
DISP_HW_17_DEBUG	23	0x0	
DISP_HW_18_DEBUG	24	0x0	
DISP_HW_19_DEBUG	25	0x0	
DISP_HW_1A_DEBUG	26	0x0	

DISP_HW_1B_DEBUG	27	0x0	
DISP_HW_1C_DEBUG	28	0x0	
DISP_HW_1D_DEBUG	29	0x0	
DISP_HW_1E_DEBUG	30	0x0	
DISP_HW_1F_DEBUG	31	0x0	

Hardware debug bits for display block. Programmed by BIOS/driver init as needed and not touched again.

<b>DAC_CRC_SIG1 - R - 32 bits - [MMReg:0xD18]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DAC_CRC_SIG_B	9:0	0x0	CRC signature value for blue data. When reset, CRCB(9:0) <= 0x3FF; When CRC is running, CRCB(9:1) <= CRCB(8:0) xor blue(9:1), CRCB(0) <= CRCB(9) xor CRCB(2) xor blue(0)
DAC_CRC_SIG_G	25:16	0x0	CRC signature value for green data. When reset, CRCG(9:0) <= 0x3FF; When CRC is running, CRCG(9:1) <= CRCG(8:0) xor green(9:1), CRCG(0) <= CRCG(9) xor CRCG(2) xor green(0)

CRC signature value for blue and green components. Use DAC\_CRC\_EN to initiate a field or frame analysis. See DAC\_CRC\_EN for details.

<b>DAC_CRC_SIG2 - R - 32 bits - [MMReg:0xD1C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DAC_CRC_SIG_R	9:0	0x0	CRC signature value for red data. When reset, CRCR(9:0) <= 0x3FF; When CRC is running, CRCR(9:1) <= CRCR(8:0) xor red(9:1), CRCR(0) <= CRCR(9) xor CRCR(2) xor red(0)

DAC_CRC_SIG_C	21:16	0x0	<p>CRC signature value for control signals.</p> <p>The control signal input vector is made up as follows:  control(0) &lt;= not blank (0 in retrace, 1 in active or overscan)  control(1) &lt;= Display Enable (0 in retrace or overscan, 1 in active)  control(2) &lt;= HSYNC  control(3) &lt;= VSYNC  control(4) &lt;= AUXWIN  control(5) &lt;= STEREO SYNC</p> <p>When reset,  CRCC(5:0) &lt;= 0x3F;  When CRC is running,  CRCC(5:1) &lt;= CRCC(4:0) xor control(5:1),  CRCC(0) &lt;= CRCC(5) xor CRCC(0) xor control(0)</p>
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CRC signature value for red component and control signals. Use DAC\_CRC\_EN to initiate a field or frame analysis. See DAC\_CRC\_EN for details.

OV0_LIN_TRANS_A - RW - 32 bits - [MMReg:0xD20]			
Field Name	Bits	Default	Description
OV0_LIN_TRANS_Cb_R	15:1	0x0	Overlay linear transform unit coefficient for Cb of R. Format S3.11 (-8.00..+7.99)
OV0_LIN_TRANS_Y_R	31:17	0x951	Overlay linear transform unit coefficient for Y of R. Format S3.11 (-8.00..+7.99)

Overlay linear transform unit coefficient group A

OV0_LIN_TRANS_B - RW - 32 bits - [MMReg:0xD24]			
Field Name	Bits	Default	Description
OV0_LIN_TRANS_OFF_R	12:0	0x190e	Overlay linear transform unit coefficient offset of R. Format S11.1 (-2048.0..+2047.5)
OV0_LIN_TRANS_Cr_R	31:17	0xcc5	Overlay linear transform unit coefficient for Cr of R. Format S3.11 (-8.00..+7.99)

Overlay linear transform unit coefficient group B

OV0_LIN_TRANS_C - RW - 32 bits - [MMReg:0xD28]			
Field Name	Bits	Default	Description
OV0_LIN_TRANS_Cb_G	15:1	0x7cde	Overlay linear transform unit coefficient for Cb of G. Format S3.11 (-8.00..+7.99)

OV0_LIN_TRANS_Y_G	31:17	0x951	Overlay linear transform unit coefficient for Y of G. Format S3.11 (-8.00..+7.99)
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Overlay linear transform unit coefficient group C

OV0_LIN_TRANS_D - RW - 32 bits - [MMReg:0xD2C]			
Field Name	Bits	Default	Description
OV0_LIN_TRANS_OFF_G	12:0	0x442	Overlay linear transform unit coefficient offset of G. Format S11.1 (-2048.0..+2047.5)
OV0_LIN_TRANS_Cr_G	31:17	0x797f	Overlay linear transform unit coefficient for Cr of G. Format S3.11 (-8.00..+7.99)

Overlay linear transform unit coefficient group D

OV0_LIN_TRANS_E - RW - 32 bits - [MMReg:0xD30]			
Field Name	Bits	Default	Description
OV0_LIN_TRANS_Cb_B	15:1	0x1023	Overlay linear transform unit coefficient for Cb of B. Format S3.11 (-8.00..+7.99)
OV0_LIN_TRANS_Y_B	31:17	0x951	Overlay linear transform unit coefficient for Y of B. Format S3.11 (-8.00..+7.99)

Overlay linear transform unit coefficient group E

OV0_LIN_TRANS_F - RW - 32 bits - [MMReg:0xD34]			
Field Name	Bits	Default	Description
OV0_LIN_TRANS_OFF_B	12:0	0x175f	Overlay linear transform unit coefficient offset of B. Format S11.1 (-2048.0..+2047.5)
OV0_LIN_TRANS_Cr_B	31:17	0x0	Overlay linear transform unit coefficient for Cr of B. Format S3.11 (-8.00..+7.99)

Overlay linear transform unit coefficient group F

OV0_GAMMA_0_F - RW - 32 bits - [MMReg:0xD40]			
Field Name	Bits	Default	Description
OV0_GAMMA_0_F_OFFSET	8:0	0x0	Overlay gamma correction non-linear offset for input 0-F. Format 8.1 (0.0..+255.5)

OV0_GAMMA_0_F_SLOPE	26:16	0x100	Overlay gamma correction non-linear slope for input 0-F. Format 3.8 (0.00..+7.99)
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Overlay gamma correction non-linear offset and slope for input 0-F

<b>OV0_GAMMA_10_1F - RW - 32 bits - [MMReg:0xD44]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_GAMMA_10_1F_OFFSET	8:0	0x20	Overlay gamma correction non-linear offset for input 10-1F. Format 8.1 (0.0..+255.5)
OV0_GAMMA_10_1F_SLOPE	26:16	0x100	Overlay gamma correction non-linear slope for input 10-1F. Format 3.8 (0.00..+7.99)

Overlay gamma correction non-linear offset and slope for input 10-1F

<b>OV0_GAMMA_20_3F - RW - 32 bits - [MMReg:0xD48]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_GAMMA_20_3F_OFFSET	9:0	0x40	Overlay gamma correction non-linear offset for input 20-3F. Format 9.1 (0.0..+511.5)
OV0_GAMMA_20_3F_SLOPE	25:16	0x100	Overlay gamma correction non-linear slope for input 20-3F. Format 2.8 (0.00..+3.99)

Overlay gamma correction non-linear offset and slope for input 20-3F

<b>OV0_GAMMA_40_7F - RW - 32 bits - [MMReg:0xD4C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_GAMMA_40_7F_OFFSET	9:0	0x80	Overlay gamma correction non-linear offset for input 40-7F. Format 9.1 (0.0..+511.5)
OV0_GAMMA_40_7F_SLOPE	24:16	0x100	Overlay gamma correction non-linear slope for input 40-7F. Format 1.8 (0.00..+1.99)

Overlay gamma correction non-linear offset and slope for input 40-7F

<b>OV0_GAMMA_380_3BF - RW - 32 bits - [MMReg:0xD50]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_GAMMA_380_3BF_OFFSET	8:0	0x100	Overlay gamma correction non-linear offset for input 380-3BF. Format 8.1 + 0x300 integer added by HW (+768.0..+1023.5)
OV0_GAMMA_380_3BF_SLOPE	24:16	0x100	Overlay gamma correction non-linear slope for input 380-3BF. Format 1.8 (0.00..+1.99)

Overlay gamma correction non-linear offset and slope for input 380-3BF

<b>OV0_GAMMA_3C0_3FF - RW - 32 bits - [MMReg:0xD54]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_GAMMA_3C0_3FF_OFFSET	8:0	0x100	Overlay gamma correction non-linear offset for input 3C0-3FF. Format 8.1 + 0x300 integer added by HW (+768.0..+1023.5)
OV0_GAMMA_3C0_3FF_SLOPE	24:16	0x100	Overlay gamma correction non-linear slope for input 3C0-3FF. Format 1.8 (0.00..+1.99)

Overlay gamma correction non-linear offset and slope for input 3C0-3FF

<b>DISP_MERGE_CNTL - RW - 32 bits - [MMReg:0xD60]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_ALPHA_MODE	1:0	0x0	<p>Graphics and overlay blend mode select. There are three choices of blend mode as described below. Per pixel alpha is really only for graphics modes that have alpha values embedded (32bpp aRGB8888, 16bpp aRGB1555, 16bpp aRGB4444, 16bpp alphaIndex88. When the global alphas are set to 1 (i.e. 0xFF), the key mode works like key mixing in past chips.</p> <p>0=Key mode: For GRPH_VID_KEY = 0, then Pixel = DISP_GRP_ALPHA * Primary Graphics. For KEY = 1, then Pixel = DISP_OV0_ALPHA * Overlay pixel</p> <p>1=Per pixel alpha mode: See DISP_ALPHA_PREMULT and DISP_ALPHA_INV for result</p> <p>2=Global alpha mode: Outside overlay window Pixel = DISP_GRP_ALPHA * Primary Graphics. Inside overlay window Pixel = (1-DISP_OV0_ALPHA * Primary Graphics + DISP_OV0_ALPHA * Overlay pixel</p>

DISP_ALPHA_INV	2	0x0	For use with per pixel alpha blend mode. Applies optional inversion to the alpha value extracted from the graphics surface data. 0=When DISP_ALPHA_MODE = 01, then use per pixel alpha as primary graphics opacity (PIX_ALPHA <= alpha from pixel) 1=When DISP_ALPHA_MODE = 01, then use per pixel alpha as primary graphics transparency (PIX_ALPHA <= 1 - (alpha from pixel))
DISP_ALPHA_PREMULT	3	0x0	For use with per pixel alpha blend mode. Selects whether pre-multiplied alpha or non-pre-multiplied alpha mix equation is used. 0=When DISP_ALPHA_MODE = 01, then Pixel = PIX_ALPHA * graphics pixel + (1-PIX_ALPHA) * overlay pixel 1=When DISP_ALPHA_MODE = 01, then Pixel = graphics pixel + (1-PIX_ALPHA) * overlay pixel
DISP_RGB_OFFSET_EN	8	0x0	Enable for no clamping for YUV input to YUV output. Should always be enabled, unless it doesn't work. When enabled, DISP_LIN_TRANS must not be in bypass mode and the DISP_LIN_TRANS_XXX_C4, C8 and C12 offset values must have a -1536 subtracted from each coefficient. 0=RGB mixing pipe operates in 0 to 1 (i.e. 0..1023) limited RGB space. Overlay pixel values outside this range are clamped to be in range. 1=RGB mixing pipe operates in -1.5 to +1.5 range. No clamping occurs for YCbCr or YPbPr mode outputs. Clamping is applied for RGB mode outputs.
DISP_GRP_ALPHA	23:16	0xff	Global graphics alpha for use in key mode and global alpha modes of DISP_ALPHA_MODE.
DISP_OV0_ALPHA	31:24	0xff	Global video alpha for use in key mode and global alpha modes of DISP_ALPHA_MODE.

Controls for mixing of graphics and video layers

DISP_OUTPUT_CNTL - RW - 32 bits - [MMReg:0xD64]			
Field Name	Bits	Default	Description
DISP_DAC_SOURCE	1:0	0x0	<p>DAC data source select. When doing ratiometric expansion, this should always be set to 10. When pixel clock is above 165 MHz, this MUST be set to 00. The 11 setting is used for YPbPr direct drive of televisions. The 01 setting allows advanced color adjustment for the display, but this will rarely be used.</p> <p>0=DAC output data comes directly from display merger.  1=DAC output data comes from output linear transform unit.  2=DAC output data comes from ratiometric expansion unit.  3=DAC output data comes from display transform unit, and DAC is in YPbPr mode.</p>
DISP_TRANS_MATRIX_SEL	5:4	0x0	<p>Output linear transform unit coefficient select. When set to 00 graphics and video pixels can have independently controlled brightness, saturation and contrast. This allows graphics colors to be less saturated and intense on televisions.</p> <p>0=Display transform unit uses alpha MSB to select matrix coefficients  1=Display transform unit only uses graphics coefficient registers  2=Display transform unit only uses video coefficient registers</p>
DISP_RMX_SOURCE	8	0x0	<p>Ratiometric expansion source select. This is normally set to 0. The 1 setting can be used to improve video brightness on panels and CRTs, but this is normally done better using the overlay contrast and gamma controls.</p> <p>0=Ratiometric expansion data comes directly from display merger.  1=Ratiometric expansion data comes from output linear transform unit.</p>
DISP_RMX_HTAP_SEL	9	0x0	<p>Ratiometric expansion horizontal filter select.</p> <p>0=Ratiometric expansion horizontal filter uses 4 tap filtering.  1=Ratiometric expansion horizontal filter uses 2 tap filtering.</p>
DISP_RMX_DITH_EN	10	0x1	<p>Selects how 30 bit data is converted to 24 bits at input to ratiometric expansion unit.</p> <p>0=Convert 30 bit color data to 24 bits by truncation of lower bits.  1=Convert 30 bit color data to 24 bits by 1-D dithering.</p>

DISP_TV_SOURCE	16	0x0	<p>TV out source select. Recommend always using transform unit setting.</p> <p>0=TV output data source is from output linear transform unit. Can be RGB or YCbCr.</p> <p>1=TV output data comes directly from display merger.</p>
DISP_TV_MODE	18:17	0x0	<p>TV out mode. When display is 640x480 or less triple clocked (00) should always be used for best quality. When greater resolution use double clocked (01) setting. ITU-R BT.656 and YCbCr4:2:2 modes do not work with Rage Theater I, but are reserved for future use. When using triple clocked mode, the output linear transform unit should be programmed to convert RGB to YCbCr and DISP_RGB_OFFSET_EN should be set high. Of course Rage Theater must also be setup to take YCbCr input. When all this is done, the quality of video on the TV will be optimal.</p> <p>0=TV output mode is triple clocked. Either RGB or YCbCr data source may be selected. Both 8 and 10 bit modes supported.</p> <p>1=TV output mode is RGB double clocked. TV output source data must be RGB. If 8 bit mode then RGB565. If 10 bit mode then RGB776.</p> <p>2=TV output mode is ITU-R BT.656 like. Must be double clocked. TV output source data must be YCbCr. Both 8 and 10 bit modes supported.</p> <p>3=TV output mode is YCrCb4:2:2. Must be double clocked. TV output source data must be YCbCr. Both 8 and 10 bit modes supported.</p>
DISP_TV_YG_DITH_EN	19	0x0	<p>TV out dither enable for luma/green (Y/G) component. When doing RGB mode, this should be set the same as DISP_TV_CbB_CrR_DITH_EN.</p> <p>0=No dither on Y or G TV output data.</p> <p>1=Dither Y or G TV output data. No effect in 10 bit modes.</p>
DISP_TV_CbB_CrR_DITH_EN	20	0x0	<p>TV out dither enable for chroma/red/blue (Cr/Cb/R/B) components. When doing RGB mode, this should be set the same as DISP_TV_CbB_CrR_DITH_EN.</p> <p>0=No dither on Cb &amp; Cr or B &amp; R TV output data.</p> <p>1=Dither Cb &amp; Cr or B &amp; R TV output data. No effect in 10 bit modes.</p>
DISP_TV_BIT_WIDTH	21	0x0	<p>TV out word bit width. Always use 8 bit with Rage Theater I. Affects how dithering is done, and how colour components are packed in double clock mode (i.e. RGB565 or RGB776).</p> <p>0=8 bit TV out mode enabled.</p> <p>1=10 bit TV out mode enabled.</p>

DISP_TV_SYNC_MODE	23:22	0x0	<p>Should be set to same as the field sequence length in Rage Theater. This is normally 4. Using this allows the graphics chip to force Rage Theater even/odd field sequence to be in sync with the overlay field polarity. Setting 00 disables this function.</p> <p>0=Send TV out sync line every frame.  DISP_TV_SYNC_FORCE is don't care.  1=Send TV out sync line every 2 frames.  2=Send TV out sync line every 4 frames.  3=Send TV out sync line every 8 frames.</p>
DISP_TV_SYNC_FORCE	24	0x0	<p>Selects which field overlay field polarity forces a sync line to Rage Theater. Should normally be set to 0.</p> <p>0=Force TV out sync line when EVEN field next and out of sequence.  1=Force TV out sync line when ODD field next and out of sequence.</p>
DISP_TV_SYNC_COLOR	26:25	0x0	<p>Sets the color of the TV out sync line to Rage Theater. Set to 00 (light blue) for normal operation. 01 and 10 (white and black) settings are for use during the alignment initialization phase of the Rage Theater interface.</p> <p>0=TV out sync line color is light blue.  1=TV out sync line color is white.  2=TV out sync line color is black.  3=Reserved.</p>
DISP_TV_EVEN_FLAG_CNTL	28:27	0x0	<p>Controls how the overlay generates the next field even/odd polarity flag for the TV out interface.</p> <p>0=TV out even flag inverse of video field polarity. i.e. 1 for even.  1=TV out even flag equal to video field polarity. i.e. 1 for odd.  2=TV out even flag forced to 0.  3=TV out even flag forced to 1.</p>
DISP_TV_SYNC_STATUS (R)	29	0x0	<p>Status bit to indicate whether the TV out interface is sending a sync line in the current frame.</p> <p>0=TV out not sending sync line for current frame.  1=TV out is sending sync line for current frame.</p>
DISP_TV_H_DOWNSCALE	30	0x0	<p>Reserved for future use.</p> <p>Enables the 2:1 horizontal downscaler in the TV out interface block. This is meant for use only in display modes greater than 848 pixels wide (i.e. 1024x768). This option can only be set when DISP_TV_MODE=00 or 01.</p> <p>0=TV out works normally.  1=TV out downscales horizontally by 2.</p>

Display outout control register

<b>DISP_LIN_TRANS_GRP_H_A - RW - 32 bits - [MMReg:0xD80]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_LIN_TRANS_GRP_H_C2	14:3	0x0	Linear transform unit graphics coefficients C2. Format S0.11 (-1.00..+0.99)
DISP_LIN_TRANS_GRP_H_C1	31:19	0x800	Linear transform unit graphics coefficients C1. Format S1.11 (-2.00..+1.99)

Linear transform unit graphics coefficients group A

<b>DISP_LIN_TRANS_GRP_H_B - RW - 32 bits - [MMReg:0xD84]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_LIN_TRANS_GRP_H_C4	12:0	0x0	Linear transform unit graphics coefficients C4. Format S11.1 (-2048.0..+2047.5)
DISP_LIN_TRANS_GRP_H_C3	30:19	0x0	Linear transform unit graphics coefficients C3. Format S0.11 (-1.00..+0.99)

Linear transform unit graphics coefficients group B

<b>DISP_LIN_TRANS_GRP_H_C - RW - 32 bits - [MMReg:0xD88]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_LIN_TRANS_GRP_H_C6	15:3	0x800	Linear transform unit graphics coefficients C6. Format S1.11 (-2.00..+1.99)
DISP_LIN_TRANS_GRP_H_C5	30:19	0x0	Linear transform unit graphics coefficients C5. Format S0.11 (-1.00..+0.99)

Linear transform unit graphics coefficients group C

<b>DISP_LIN_TRANS_GRP_H_D - RW - 32 bits - [MMReg:0xD8C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_LIN_TRANS_GRP_H_C8	12:0	0x0	Linear transform unit graphics coefficients C8. Format S11.1 (-2048.0..+2047.5)
DISP_LIN_TRANS_GRP_H_C7	30:19	0x0	Linear transform unit graphics coefficients C7. Format S0.11 (-1.00..+0.99)

Linear transform unit graphics coefficients group D

<b>DISP_LIN_TRANS_GRPHE - RW - 32 bits - [MMReg:0xD90]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_LIN_TRANS_GRPHE_C10	14:3	0x0	Linear transform unit graphics coefficients C10. Format S0.11 (-1.00..+0.99)
DISP_LIN_TRANS_GRPHE_C9	30:19	0x0	Linear transform unit graphics coefficients C9. Format S0.11 (-1.00..+0.99)

Linear transform unit graphics coefficients group E

<b>DISP_LIN_TRANS_GRPHE - RW - 32 bits - [MMReg:0xD94]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_LIN_TRANS_GRPHE_C12	12:0	0x0	Linear transform unit graphics coefficients C12. Format S11.1 (-2048.0..+2047.5)
DISP_LIN_TRANS_GRPHE_C11	31:19	0x800	Linear transform unit graphics coefficients C11. Format S1.11 (-2.00..+1.99)

Linear transform unit graphics coefficients group F

<b>DISP_LIN_TRANS_VID_A - RW - 32 bits - [MMReg:0xD98]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_LIN_TRANS_VID_A_C2	14:3	0x0	Linear transform unit video coefficients C2. Format S0.11 (-1.00..+0.99)
DISP_LIN_TRANS_VID_A_C1	31:19	0x800	Linear transform unit video coefficients C1. Format S1.11 (-2.00..+1.99)

Linear transform unit video coefficients group A

<b>DISP_LIN_TRANS_VID_B - RW - 32 bits - [MMReg:0xD9C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_LIN_TRANS_VID_B_C4	12:0	0x0	Linear transform unit video coefficients C4. Format S11.1 (-2048.0..+2047.5)
DISP_LIN_TRANS_VID_B_C3	30:19	0x0	Linear transform unit video coefficients C3. Format S0.11 (-1.00..+0.99)

Linear transform unit video coefficients group B

<b>DISP_LIN_TRANS_VID_C - RW - 32 bits - [MMReg:0xDA0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_LIN_TRANS_VID_C6	15:3	0x800	Linear transform unit video coefficients C6. Format S1.11 (-2.00..+1.99)
DISP_LIN_TRANS_VID_C5	30:19	0x0	Linear transform unit video coefficients C5. Format S0.11 (-1.00..+0.99)

Linear transform unit video coefficients group C

<b>DISP_LIN_TRANS_VID_D - RW - 32 bits - [MMReg:0xDA4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_LIN_TRANS_VID_C8	12:0	0x0	Linear transform unit video coefficients C8. Format S11.1 (-2048.0..+2047.5)
DISP_LIN_TRANS_VID_C7	30:19	0x0	Linear transform unit video coefficients C7. Format S0.11 (-1.00..+0.99)

Linear transform unit video coefficients group D

<b>DISP_LIN_TRANS_VID_E - RW - 32 bits - [MMReg:0xDA8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_LIN_TRANS_VID_C10	14:3	0x0	Linear transform unit video coefficients C10. Format S0.11 (-1.00..+0.99)
DISP_LIN_TRANS_VID_C9	30:19	0x0	Linear transform unit video coefficients C9. Format S0.11 (-1.00..+0.99)

Linear transform unit video coefficients group E

<b>DISP_LIN_TRANS_VID_F - RW - 32 bits - [MMReg:0xDAC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_LIN_TRANS_VID_C12	12:0	0x0	Linear transform unit video coefficients C12. Format S11.1 (-2048.0..+2047.5)
DISP_LIN_TRANS_VID_C11	31:19	0x800	Linear transform unit video coefficients C11. Format S1.11 (-2.00..+1.99)

Linear transform unit video coefficients group F

## 2.10 Rmx Registers

### RMX Control Registers

RMX_HORZ_FILTER_0TAP_COEF - RW - 32 bits - [MMReg:0xDB0]			
Field Name	Bits	Default	Description
RMX_COEF_0POS_0TAP_HORZ	4:0	0x1f	Tap 0 position 0 coefficient
RMX_COEF_1POS_0TAP_HORZ	9:5	0x1f	Tap 0 position 1 coefficient. Position 7 coefficients internally derived from position 1 coefficients.
RMX_COEF_2POS_0TAP_HORZ	14:10	0x1f	Tap 0 position 2 coefficient. Position 6 coefficients internally derived from position 2 coefficients.
RMX_COEF_3POS_0TAP_HORZ	19:15	0x1f	Tap 0 position 3 coefficient. Position 5 coefficients internally derived from position 3 coefficients.
RMX_COEF_4POS_0TAP_HORZ	24:20	0x1f	Tap 0 position 4 coefficient

Ratiometric expander horizontal filter tap0 coefficients for 4 tap filter. If filter is  $Y=a*Y0+b*Y1+c*Y2+d*Y3$ ; then tap0 coefficient= $b/a+b$ .

RMX_HORZ_FILTER_1TAP_COEF - RW - 32 bits - [MMReg:0xDB4]			
Field Name	Bits	Default	Description
RMX_COEF_0POS_1TAP_HORZ	4:0	0x1f	Tap 1 position 0 coefficient
RMX_COEF_1POS_1TAP_HORZ	9:5	0x1f	Tap 1 position 1 coefficient. Position 7 coefficients internally derived from position 1 coefficients.
RMX_COEF_2POS_1TAP_HORZ	14:10	0x1f	Tap 1 position 2 coefficient. Position 6 coefficients internally derived from position 2 coefficients.
RMX_COEF_3POS_1TAP_HORZ	19:15	0x1f	Tap 1 position 3 coefficient. Position 5 coefficients internally derived from position 3 coefficients.
RMX_COEF_4POS_1TAP_HORZ	24:20	0x1f	Tap 1 position 4 coefficient

Ratiometric expander horizontal filter tap1 coefficients for 4 tap filter. If filter is  $Y=a*Y0+b*Y1+c*Y2+d*Y3$ ; then tap1 coefficient= $d/c+d$ .

RMX_HORZ_FILTER_2TAP_COEF - RW - 32 bits - [MMReg:0xDB8]			
Field Name	Bits	Default	Description
RMX_COEF_0POS_2TAP_HORZ	4:0	0x0	Tap 2 position 0 coefficient

RMX_COEF_1POS_2TAP_HORZ	9:5	0x0	Tap 2 position 1 coefficient. Position 7 coefficients internally derived from position 1 coefficients.
RMX_COEF_2POS_2TAP_HORZ	14:10	0x0	Tap 2 position 2 coefficient. Position 6 coefficients internally derived from position 2 coefficients.
RMX_COEF_3POS_2TAP_HORZ	19:15	0x0	Tap 2 position 3 coefficient. Position 5 coefficients internally derived from position 3 coefficients.
RMX_COEF_4POS_2TAP_HORZ	24:20	0x0	Tap 2 position 4 coefficient

Ratiometric expander horizontal filter tap2 coefficients for 4 tap filter. If filter is  $Y=a*Y0+b*Y1+c*Y2+d*Y3$ ; then tap2 coefficient=c+d.

RMX_HORZ_PHASE - RW - 32 bits - [MMReg:0xDBC]			
Field Name	Bits	Default	Description
RMX_HORZ_START_PHASE	11:0	0x0	Ratiometric expander horizontal accumulator start phase. Horizontal filter accumulator resets to this value at the start of each line. This is normally set to zero, but can be used to fix certain large expansion cases where the expanded image otherwise comes out one pixel too large.
RMX_VERT_START_PHASE	27:16	0x0	Ratiometric expander vertical accumulator start phase. Vertical filter accumulator resets to this value at the start of each frame. This is normally set to zero, but can be used to fix certain large expansion cases where the expanded image otherwise comes out one pixel too large.

Ratiometric expander accumulator horizontal and vertical start phases

## 2.11 FeatureBlock Registers

### Feature Block Control Registers.

TMDS_CNTL - RW - 32 bits - [MMReg:0x294]			
Field Name	Bits	Default	Description
TMDS_CTL0	0	0x0	Control signal for TMDS (encoded in Green channel)
TMDS_CTL1	1	0x0	Control signal for TMDS (encoded in Green channel)
TMDS_CTL2	2	0x0	Control signal for TMDS (encoded in Red channel)
TMDS_CTL3	3	0x0	Control signal for TMDS (encoded in Red channel)
TMDS_DEBUG_HSYNC	4	0x0	Debug mode HSYNC control
TMDS_DEBUG_VSYNC	5	0x0	Debug mode VSYNC control
TMDS_DEBUG_DE	6	0x0	Debug mode Display Enable
TMDS_DEBUG_EN	7	0x0	Debug mode enable
TMDS_CTL_FB_SEL	9:8	0x0	Select input of CTL0 for TMDS
TMDS_CTL_FB_DEL	11:10	0x0	Select delay of CTL0 for TMDS
TMDS_CTL3_SEL	12	0x0	Select the source for CTL3. 0 - from control register; 1 - From STEREO SYNC 0=Use control register 1=Use STEREO SYNC
TMDS_SYNC_CHAR_EN	19:16	0x0	SYNC character enable. Each of the bit represents use of register defined sync character. Bit x= 1 means SYNC_CHARx is defined by register
TMDS_SYNC_CONT	24	0x1	TMDS synchronization control
TMDS_DPCUM_TST	25	0x0	Dcbalancer test enable
TMDS_DPCUM_IN	29:26	0x0	Dcbalancer test input
TMDS_CRC_EN	30	0x0	Enable CRC calculation
TMDS_RB_SWITCH_EN	31	0x0	Switch Red and Blue encoding position

Control register for TMDS encoder timing and others

TMDS_SYNC_CHAR_SETA - RW - 32 bits - [MMReg:0x298]			
Field Name	Bits	Default	Description
TMDS_SYNC_CHAR0	9:0	0x354	TMDS SYNC Character 0 (Default 1101010100)

TMDS_SYNC_CHAR1	25:16	0x154	TMDS SYNC Character 1 (Default 0101010100)
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TMDS SYNC Character set A

<b>TMDS_SYNC_CHAR_SETB - RW - 32 bits - [MMReg:0x29C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
TMDS_SYNC_CHAR2	9:0	0xab	TMDS SYNC Character 2 (Default 0010101011)
TMDS_SYNC_CHAR3	25:16	0x2ab	TMDS SYNC Character 3 (Default 1010101011)

TMDS SYNC character set b

<b>TMDS_CRC - R - 32 bits - [MMReg:0x2A0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
TMDS_CRCRGB	29:0	0x0	30bits RGB combined CRC result

TMDS CRC read back

<b>TMDS_TRANSMITTER_CNTL - RW - 32 bits - [MMReg:0x2A4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
TMDS_PLEN	0	0x0	TMDS transmitter's PLL enable. This can power down the PLL
TMDS_PLLRST	1	0x1	TMDS transmitter's PLL reset. PLL will start the locking acquisition process once this signal becomes LOW
TMDS_MODE_SEL	3:2	0x0	TMDS transmitter mode select. 00-outputs encoded data to macro, this can be encoded normal data or encoded random data, depending on TMDS_RAN_PAT_SEL. 11-outputs 1/2 clock test pattern. 10-outputs TMDS_TSTPIX.
TMDS_REGSEL	5:4	0x0	TMDS_REG output select one of the four channels
TMDS_HALF_CLK_RST	6	0x0	Resets 1/2 clock test pattern to 0 when = 1
TMDS_RAN_PAT_RST	7	0x1	Resets the pseudo-random pattern to seed value when = 0
TMDS_TSTPIX	17:8	0x0	TMDS transmitter test pixel. This signal is transmitted when TMDS_MODE_SEL is 10
TMDS_REG (R)	27:18	0x0	Output of shift registers. These are the outputs of the 10 shift registers from one of the channels during test mode (Read only)

ICHSEL	28	0x1	TMDS Channel C clock source select. Reserved for debugging only. Should always be held high
ITCLKSEL	29	0x0	Test clock select. 0-Normal operation; 1-PLL bypassed with test clocks
TMDS_RAN_PAT_SEL	30	0x0	Select between normal incoming data or 24-bit pseudo-random data. 0-Normal data; 1-random data generated by TMDS block

TMDS transmitter control register

<b>TMDS_PLL_CNTL - RW - 32 bits - [MMReg:0x2A8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
TMDS_PLLPCP	2:0	0x4	TMDS PLL charge-pump gain control
TMDS_PLLPVG	5:3	0x4	TMDS PLL VCO gain control
TMDS_PLLPDC	7:6	0x2	TMDS PLL duty cycle control
TMDS_PLLPVS	11:8	0x6	TMDS driver voltage swing control. Select the Rext from 300ohm to 1000ohm in 50ohm step which is equivalent to 250 to 720 mV swing.

TMDS PLL control register

## 2.12 I2C Registers

### I2C Description.

I2C_CNTL_0 - RW - 32 bits - [IOReg,MMReg:0x90]			
Field Name	Bits	Default	Description
I2C_DONE	0	0x0	Read only. Indicate whether current I2C request is finished or not 0=I2c is busy 1=transfer is complete
I2C_NACK	1	0x0	Read only. Status bit indicate whether I2C slave did not acknowledge. 1=Slave did not issue acknowledge
I2C_HALT	2	0x0	Read only. Status bit indicate where I2C bus transfer is time out. 1=Time-out condition, transfer is halted
I2C_SOFT_RST	5	0x0	Software reset I2C interface block 0=Normal 1=Resets i2c controller
I2C_DRIVE_EN	6	0x0	Enable I2C pad driving pull-up action 0=Pullup by external resistor 1=I2C pads drive SDA
I2C_DRIVE_SEL	7	0x0	If DRIVE_EN is HIGH, select drive time 0=Drive for 10MCLKs 1=20MCLKS
I2C_START	8	0x0	Indicate whether use the start condition in I2C protocol. 0=No start 1=Start
I2C_STOP	9	0x0	Indicate whether use the stop condition in I2C protocol. 0=No stop 1=Stop
I2C_RECEIVE	10	0x0	Master receive/transmit mode selection 0=Send 1=Receive
I2C_ABORT	11	0x0	If 1, abort the current I2C operation by sending STOP bit. 0=No abort 1=Abort
I2C_GO	12	0x0	Write this bit initiate I2C operation. Read this bit indicate the I2C operation is finished or not.
I2C_PRESCALE	31:16	0x0	I2C clock divider to generate I2C SCL output. It also indirectly control the sampling rate.

I2C control registers

<b>I2C_CNTL_1 - RW - 32 bits - [IOReg,MMReg:0x94]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
I2C_DATA_COUNT	3:0	0x0	Byte count for data to be transferred through I2C interface. The data should be in the 16 bytes I2C buffer
I2C_ADDR_COUNT	10:8	0x0	Byte count for I2C addresses. Maximum 3 bytes of address can be transferred.
I2C_SEL	16	0x0	Not used in Rage5 0=Pullup by external resistor 1=I2C pads drive SCL
I2C_EN	17	0x0	Enable I2C
I2C_TIME_LIMIT	31:24	0x0	Time out limit. Total wait time = TIME_LIMIT * 4 * PRESCLAE(15:8) cycles for SCL to be LOW

I2C control registers

<b>I2C_DATA - RW - 32 bits - [IOReg,MMReg:0x98]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
I2C_DATA	7:0	0x0	I2C data interface. Programmers use this 8bits interface to write and read I2C bus data.

I2C data registers. Programmers use this 8bits interface to write and read I2C bus data.

## 2.13 VIP Registers

### Video Interface Port Description.

VIPH_CH0_DATA - RW - 32 bits - [MMReg:0xC00]			
Field Name	Bits	Default	Description
VIPH_CH0_DT	31:0	0x0	VIPH0 data interface

VIPH0 data interface

VIPH_CH1_DATA - RW - 32 bits - [MMReg:0xC04]			
Field Name	Bits	Default	Description
VIPH_CH1_DT	31:0	0x0	VIPH0 data interface

VIPH0 data interface

VIPH_CH2_DATA - RW - 32 bits - [MMReg:0xC08]			
Field Name	Bits	Default	Description
VIPH_CH2_DT	31:0	0x0	VIPH0 data interface

VIPH0 data interface

VIPH_CH3_DATA - RW - 32 bits - [MMReg:0xC0C]			
Field Name	Bits	Default	Description
VIPH_CH3_DT	31:0	0x0	VIPH0 data interface

VIPH0 data interface

VIPH_CH0_ADDR - RW - 32 bits - [MMReg:0xC10]			
Field Name	Bits	Default	Description
VIPH_CH0_AD	7:0	0x0	Bit(3:0): FIFO address Bit(4): 0= register access, 1 = FIFO access. Bit(5): 0= register write, 1= register read. Bits(7:6): Slave device ID.

VIPH0 command + address.

VIPH_CH1_ADDR - RW - 32 bits - [MMReg:0xC14]			
Field Name	Bits	Default	Description
VIPH_CH1_AD	7:0	0x0	Bit(3:0): FIFO address Bit(4): 0= register access, 1 = FIFO access. Bit(5): 0= register write, 1= register read. Bits(7:6): Slave device ID.

VIPH1 command + address.

VIPH_CH2_ADDR - RW - 32 bits - [MMReg:0xC18]			
Field Name	Bits	Default	Description
VIPH_CH2_AD	7:0	0x0	Bit(3:0): FIFO address Bit(4): 0= register access, 1 = FIFO access. Bit(5): 0= register write, 1= register read. Bits(7:6): Slave device ID.

VIPH2 command + address.

VIPH_CH3_ADDR - RW - 32 bits - [MMReg:0xC1C]			
Field Name	Bits	Default	Description
VIPH_CH3_AD	7:0	0x0	Bit(3:0): FIFO address Bit(4): 0= register access, 1 = FIFO access. Bit(5): 0= register write, 1= register read. Bits(7:6): Slave device ID.

VIPH3 command + address.

VIPH_CH0_SBCNT - RW - 32 bits - [MMReg:0xC20]			
Field Name	Bits	Default	Description
VIPH_CH0_SCNT	19:0	0x0	Write non-zero byte count will trigger DMA. Maximum 2 jobs can be loaded into the queue any one time.

Byte count of transfer requested.

<b>VIPH_CH1_SBCNT - RW - 32 bits - [MMReg:0xC24]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
VIPH_CH1_SCNT	19:0	0x0	Write non-zero byte count will trigger DMA. Maximum 2 jobs can be loaded into the queue any one time.

Byte count of transfer requested.

<b>VIPH_CH2_SBCNT - RW - 32 bits - [MMReg:0xC28]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
VIPH_CH2_SCNT	19:0	0x0	Write non-zero byte count will trigger DMA. Maximum 2 jobs can be loaded into the queue any one time.

Byte count of transfer requested.

<b>VIPH_CH3_SBCNT - RW - 32 bits - [MMReg:0xC2C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
VIPH_CH3_SCNT	19:0	0x0	Write non-zero byte count will trigger DMA. Maximum 2 jobs can be loaded into the queue any one time.

Byte count of transfer requested.

<b>VIPH_CH0_ABCNT - R - 32 bits - [MMReg:0xC30]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
VIPH_CH0_ACNT	19:0	0x0	Keep track of active byte-count remaining.

Read back of remaining byte count.

<b>VIPH_CH1_ABCNT - R - 32 bits - [MMReg:0xC34]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
VIPH_CH1_ACNT	19:0	0x0	Keep track of active byte-count remaining.

Read back of remaining byte count.

**VIPH\_CH2\_ABCNT - R - 32 bits - [MMReg:0xC38]**

Field Name	Bits	Default	Description
VIPH_CH2_ACNT	19:0	0x0	Keep track of active byte-count remaining.

Read back of remaining byte count.

**VIPH\_CH3\_ABCNT - R - 32 bits - [MMReg:0xC3C]**

Field Name	Bits	Default	Description
VIPH_CH3_ACNT	19:0	0x0	Keep track of active byte-count remaining.

Read back of remaining byte count.

**VIPH\_CONTROL - RW - 32 bits - [MMReg:0xC40]**

Field Name	Bits	Default	Description
VIPH_CLK_SEL	7:0	0x0	VIPH clock select, only even divider is permitted. Which means VIPH_CLK_SEL(0) must be set to 1. 0=reserved 1=reserved 2=reserved 3=xclkby4 4=reserved 5=xclkby6 6=... (Only EVEN divider is permitted)
VIPH_REG_RDY (R)	13	0x0	0= VIPH is ready for next register access. 1= VIPH is busy for current VIPH register access.
VIPH_MAX_WAIT	19:16	0x0	Number of VIP phases before issuing time out. Set to zero means no time out
VIPH_DMA_MODE	20	0x0	0= No DMA. 1= DMA
VIPH_EN	21	0x0	VIP Host port Enable
VIPH_DV0_WID	24	0x0	VIPH0 bus width 0=2-bit vipbus 1=4-bit vipbus
VIPH_DV1_WID	25	0x0	VIPH1 bus width 0=2-bit vipbus 1=4-bit vipbus
VIPH_DV2_WID	26	0x0	VIPH2 bus width 0=2-bit vipbus 1=4-bit vipbus

VIPH_DV3_WID	27	0x0	VIPH3 bus width 0=2-bit vipbus 1=4-bit vipbus
VIPH_PWR_DOWN (R)	28	0x0	'1' to wake up PCICLK. 0=Normal 1=STARTUP PCICLK
VIPH_PWR_DOWN_AK (W)	28	0x0	Clear PWR_DOWN by writing a 1. In order to support PCI-CLK power down mode, it is important to clear this bit every time there is an interrupt from any part of VIP 0=Normal 1=Allow the host bus to go back to power down state
VIPH_VIPCLK_DIS	29	0x0	'0' will supply VIP clock to slave. '1' will stops VIP clock to save power. 0= 1=turn off VIPCLK for power saving

VIP Host Port Control

<b>VIPH_DV_LAT - RW - 32 bits - [MMReg:0xC44]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
VIPH_TIME_UNIT	11:0	0x0	Basic time slice
VIPH_DV0_LAT	19:16	0x0	How many time slice port 0 gets
VIPH_DV1_LAT	23:20	0x0	How many time slice port 1 gets
VIPH_DV2_LAT	27:24	0x0	How many time slice port 2 gets
VIPH_DV3_LAT	31:28	0x0	How many time slice port 3 gets

Time slice partition

<b>VIPH_DMA_CHUNK - RW - 32 bits - [MMReg:0xC48]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
VIPH_CH0_CHUNK	3:0	0x0	Chunk size between VIP host port and DMA for port 0
VIPH_CH1_CHUNK	5:4	0x0	Chunk size between VIP host port and DMA for port 1
VIPH_CH2_CHUNK	7:6	0x0	Chunk size between VIP host port and DMA for port 2
VIPH_CH3_CHUNK	9:8	0x0	Chunk size between VIP host port and DMA for port 3
VIPH_CH0_ABORT	16	0x0	Abort DMA operation through port 0
VIPH_CH1_ABORT	17	0x0	Abort DMA operation through port 1
VIPH_CH2_ABORT	18	0x0	Abort DMA operation through port 2

VIPH_CH3_ABORT	19	0x0	Abort DMA operation through port 3
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DMA transfer chunk size and abort control

VIPH_DV_INT - RW - 32 bits - [MMReg:0xC4C]			
Field Name	Bits	Default	Description
VIPH_DV0_INT_EN	0	0x0	Interrupt polling enable for VIP slave device 0
VIPH_DV1_INT_EN	1	0x0	Interrupt polling enable for VIP slave device 1
VIPH_DV2_INT_EN	2	0x0	Interrupt polling enable for VIP slave device 2
VIPH_DV3_INT_EN	3	0x0	Interrupt polling enable for VIP slave device 3
VIPH_DV0_INT (R)	4	0x0	Interrupt
VIPH_DV0_AK (W)	4	0x0	Clear interrupt with a '1'
VIPH_DV1_INT (R)	5	0x0	Interrupt
VIPH_DV1_AK (W)	5	0x0	Clear interrupt with a '1'
VIPH_DV2_INT (R)	6	0x0	Interrupt
VIPH_DV2_AK (W)	6	0x0	Clear interrupt with a '1'
VIPH_DV3_INT (R)	7	0x0	Interrupt
VIPH_DV3_AK (W)	7	0x0	Clear interrupt with a '1'

VIP Host port interrupt control

VIPH_TIMEOUT_STAT - RW - 32 bits - [MMReg:0xC50]			
Field Name	Bits	Default	Description
VIPH_FIFO0_STAT (R)	0	0x0	'1' if port 0 time out or hung.
VIPH_FIFO0_AK (W)	0	0x0	Clear FIFO0_STAT with a '1'
VIPH_FIFO1_STAT (R)	1	0x0	'1' if port 1 time out or hung.
VIPH_FIFO1_AK (W)	1	0x0	Clear FIFO1_STAT with a '1'
VIPH_FIFO2_STAT (R)	2	0x0	'1' if port 2 time out or hung.
VIPH_FIFO2_AK (W)	2	0x0	Clear FIFO2_STAT with a '1'
VIPH_FIFO3_STAT (R)	3	0x0	'1' if port 3 time out or hung.
VIPH_FIFO3_AK (W)	3	0x0	Clear FIFO3_STAT with a '1'
VIPH_REG_STAT (R)	4	0x0	'1' if register port time out or hung.

## VIP Registers

VIPH_REG_AK (W)	4	0x0	Clear REG_STAT with a '1'
VIPH_AUTO_INT_STAT (R)	5	0x0	'1' if auto interrupt polling time out or hung.
VIPH_AUTO_INT_AK (W)	5	0x0	Clear AUTO_INT_STAT with a '1'
VIPH_FIFO0_MASK	8	0x0	'0' disable interrupt.
VIPH_FIFO1_MASK	9	0x0	'0' disable interrupt.
VIPH_FIFO2_MASK	10	0x0	'0' disable interrupt.
VIPH_FIFO3_MASK	11	0x0	'0' disable interrupt.
VIPH_REG_MASK	12	0x0	'0' disable interrupt.
VIPH_AUTO_INT_MASK	13	0x0	'0' disable interrupt.
VIPH_DV0_INT_MASK	16	0x0	'0' disable interrupt.
VIPH_DV1_INT_MASK	17	0x0	'0' disable interrupt.
VIPH_DV2_INT_MASK	18	0x0	'0' disable interrupt.
VIPH_DV3_INT_MASK	19	0x0	'0' disable interrupt.
VIPH_INTPIN_EN	20	0x0	'0' means no physical pins used for VIP interrupt. 1= physical pins used.
VIPH_INTPIN_INT (R)	21	0x0	'1' if physical pins has interrupt.
VIPH_REGR_DIS	24	0x0	'0'= any host read from VIPH_REG_DATA will trigger VIP register cycle. 1= Read from VIPH_REG_DATA will not trigger VIP register cycle.

VIP Host Port Time Out Status

VIPH_REG_ADDR - RW - 32 bits - [IOReg,MMReg:0x80]			
Field Name	Bits	Default	Description
VIPH_REG_AD	15:0	0x0	Bits (11:0): Slave registers address. Bits(12): 0 = register access, 1= FIFO access. Bits(13): 0= register write, 1 = register read. Bits(15:14): Slave device ID.

VIP Host register access command and address.

VIPH_REG_DATA - RW - 32 bits - [IOReg,MMReg:0x84]			
Field Name	Bits	Default	Description
VIPH_REG_DT_R (R)	31:0	0x0	Read from VIP Host Port register data port
VIPH_REG_DT_W (W)	31:0	0x0	Write to VIP Host Port register data port

VIP Host Port register data port

FCP_CNTL - RW - 32 bits - [MMReg:0x910]			
Field Name	Bits	Default	Description
FCP0_SRC_SEL	2:0	0x4	PCICLK,PCLK, PCLKb, HREF, GND, HREFb. 0=PCICLK 1=PCLK 2=PCLKb 3=HREF 4=GND 5=HREFb

Capture Port FCP clock mux control

## 2.14 Capture Registers

Registers to facilitate the capture of input video data

FCP_CNTL - RW - 32 bits - [MMReg:0x910]			
Field Name	Bits	Default	Description
FCP0_SRC_SEL	2:0	0x4	PCICLK, PCLK, PCLKb, HREF, GND, HREFb. 0=PCICLK 1=PCLK 2=PCLKb 3=HREF 4=GND 5=HREFb

Capture Port FCP clock mux control

GEN_INT_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]			
Field Name	Bits	Default	Description
CRTC_VBLANK_STAT (R) (DISPLAY)	0	0x0	Vertical blank interrupt. Set when display in vertical retrace. 0=No event 1=Event has occurred, interrupting if enabled
CRTC_VBLANK_STAT_AK (W) (DISPLAY)	0	0x0	Vertical blank interrupt acknowledge. 0=No effect 1=Clear status
CRTC_VLINE_STAT (R) (DISPLAY)	1	0x0	Vertical line interrupt. Set on display line on programmed by the CRTC_VLINE_CRNT_VLINE.CRTC_VLINE register. 0=No event 1=Event has occurred, interrupting if enabled
CRTC_VLINE_STAT_AK (W) (DISPLAY)	1	0x0	Vertical line interrupt acknowledge. 0=No effect 1=Clear status
CRTC_VSYNC_STAT (R) (DISPLAY)	2	0x0	Vertical sync interrupt. Set on start of VSYNC at the DAC. 0=No event 1=Event has occurred, interrupting if enabled
CRTC_VSYNC_STAT_AK (W) (DISPLAY)	2	0x0	Vertical sync interrupt acknowledge. 0=No effect 1=Clear status
SNAPSHOT_STAT (R) (DISPLAY)	3	0x0	Snapshot interrupt. Set as controlled by SNAPSHOT_VIF_COUNT register. 0=No event 1=Event has occurred, interrupting if enabled

SNAPSHOT_STAT_AK (W) (DISPLAY)	3	0x0	Snapshot interrupt acknowledge. 0=No effect 1=Clear status
FP_DETECT_STAT (R) (DISPLAY)	4	0x0	Hot plug detect (HPD) interrupt. Set on HPD connect or disconnect as controlled by FP_GEN_CNTL.FP_DETECT_INT_POL. 0=No event 1=Event has occurred, interrupting if enabled
FP_DETECT_STAT_AK (W) (DISPLAY)	4	0x0	Hot plug detect (HPD) interrupt acknowledge. 0=No effect 1=Clear status
CAP0_INT_ACTIVE (R) (VIP)	8	0x0	Capture port 0 has active interrupt(s). 0=Capture port 0 not source of any active interrupt 1=Capture port 0 has active interrupt(s)
DMA_VIPH0_INT (R) (VIP)	12	0x0	VIP host port channel 0 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH0_INT_AK (W) (VIP)	12	0x0	VIP host port channel 0 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH1_INT (R) (VIP)	13	0x0	VIP host host channel 1 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH1_INT_AK (W) (VIP)	13	0x0	VIP host port channel 1 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH2_INT (R) (VIP)	14	0x0	VIP host port channel 2 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH2_INT_AK (W) (VIP)	14	0x0	VIP host port channel 2 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH3_INT (R) (VIP)	15	0x0	VIP host port channel 3 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH3_INT_AK (W) (VIP)	15	0x0	VIP host port channel 3 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
I2C_INT (R) (VIP)	17	0x0	I2C interrupt. 0=No event 1=Event has occurred, interrupting if enabled
I2C_INT_AK (W) (VIP)	17	0x0	I2C interrupt acknowledge/reset. 0=No effect 1=Clear status

Capture Registers

GUI_IDLE_STAT (R) (RBBM)	19	0x1	GUI idle interrupt. 0=No event 1=Event has occurred, interrupting if enabled
GUI_IDLE_STAT_AK (W) (RBBM)	19	0x0	GUI idle interrupt acknowledge. 0=No effect 1=Clear status
VIPH_INT (R) (VIP)	24	0x0	VIP host port interrupt. 0=No event 1=Event has occurred, interrupting if enabled
SW_INT (R) (HDP)	25	0x0	Software interrupt. General purpose interrupt that can only be set by software event by writing to SW_INT_SET. 0=No event 1=Event has occurred, interrupting if enabled
SW_INT_AK (W) (HDP)	25	0x0	Software interrupt acknowledge. 0=No effect 1=Clear SW_INT (set low)
SW_INT_SET (W) (HDP)	26	0x0	Software interrupt trigger. 0=No effect 1=Set SW_INT active (high)
GUIDMA_STAT (R) (CP)	30	0x0	GUI DMA channel interrupt. 0=No event 1=Event has occurred, interrupting if enabled
GUIDMA_AK (W) (CP)	30	0x0	GUI DMA channel interrupt acknowledge. 0=No effect 1=Clear status
VIDDMA_STAT (R) (CP)	31	0x0	Video capture DMA channel interrupt. 0=No event 1=Event has occurred, interrupting if enabled
VIDDMA_AK (W) (CP)	31	0x0	Video capture DMA channel interrupt acknowledge. 0=No effect 1=Clear status

General Interrupt Status register.

These fields can be polled and acknowledged even if interrupts are disabled, or the respective fields are masked in the GEN\_INT\_CNTL register.

<b>CAPO_BUF0_OFFSET - RW - 32 bits - [MMReg:0x920]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_BUF0_OFFSET	31:0	0x0	Capture Port 0 Buffer 0 starting address  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture Port 0 Buffer 0 starting address

**CAP0\_BUF1\_OFFSET - RW - 32 bits - [MMReg:0x924]**

Field Name	Bits	Default	Description
CAP_BUF1_OFFSET	31:0	0x0	Capture Port 0 Buffer 1 starting address  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture Port 0 Buffer 1 starting address

**CAP0\_BUF0\_EVEN\_OFFSET - RW - 32 bits - [MMReg:0x928]**

Field Name	Bits	Default	Description
CAP_BUF0_EVEN_OFFSET	31:0	0x0	Capture Port 0 Buffer 0 even frame starting address  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture Port 0 Buffer 0 even frame starting address

**CAP0\_BUF1\_EVEN\_OFFSET - RW - 32 bits - [MMReg:0x92C]**

Field Name	Bits	Default	Description
CAP_BUF1_EVEN_OFFSET	31:0	0x0	Capture Port 0 Buffer 1 even frame starting address  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture Port 0 Buffer 1 even frame starting address

**CAP0\_BUF\_PITCH - RW - 32 bits - [MMReg:0x930]**

Field Name	Bits	Default	Description
CAP_BUF_PITCH	11:0	0x0	Capture 0 buffer's pitch.  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 buffer's pitch.

**CAP0\_V\_WINDOW - RW - 32 bits - [MMReg:0x934]**

Field Name	Bits	Default	Description
CAP_V_START	11:0	0x0	Vertical window starting line number.

CAP_V_END	27:16	0x0	Vertical window end line number.
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Capture 0's Vertical window.

CAP0_H_WINDOW - RW - 32 bits - [MMReg:0x938]			
Field Name	Bits	Default	Description
CAP_H_START	11:0	0x0	Horizontal window's start.
CAP_H_WIDTH	27:16	0x0	Horizontal window's width.  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0's Horizontal window.

CAP0_VBI0_OFFSET - RW - 32 bits - [MMReg:0x93C]			
Field Name	Bits	Default	Description
CAP_VBI0_OFFSET	31:0	0x0	Capture 0 VBI 0 buffer's starting address.  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 VBI 0 buffer's starting address.

CAP0_VBI1_OFFSET - RW - 32 bits - [MMReg:0x940]			
Field Name	Bits	Default	Description
CAP_VBI1_OFFSET	31:0	0x0	Capture 0 VBI 1 buffer's starting address.  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 VBI 1 buffer's starting address.

CAP0_VBI_V_WINDOW - RW - 32 bits - [MMReg:0x944]			
Field Name	Bits	Default	Description
CAP_VBI_V_START	11:0	0x0	Capture 0 VBI's Vertical start.
CAP_VBI_V_END	27:16	0x0	Capture 0 VBI's Vertical End.

Capture 0 VBI's vertical window

<b>CAP0_VBI_H_WINDOW - RW - 32 bits - [MMReg:0x948]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_VBI_H_START	11:0	0x0	Capture 0 VBI's Horizontal start.
CAP_VBI_H_WIDTH	27:16	0x0	Capture 0 VBI's Horizontal Width.  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 VBI's horizontal window

<b>CAP0_PORT_MODE_CNTL - RW - 32 bits - [MMReg:0x94C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_PORT_WIDTH	1	0x0	Capture 0 port width. 0=8 bits 1=16 bits
CAP_PORT_BYTE_USED	2	0x0	In 8 bit width mode, which byte used. 0=lower byte used 1=upper byte used

Capture 0 mode control register.

<b>CAP0_TRIG_CNTL - RW - 32 bits - [MMReg:0x950]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_TRIGGER_R (R)	1:0	0x0	Read only. Capture status. 0=capture complete 1=capture pending 2=capture in progress
CAP_TRIGGER_W (W)	0	0x0	Write only. Start capture next frame. 0=no action 1=capture next field/frame
CAP_EN	4	0x0	Capture 0 enable. 0=disable 1=enable
CAP_VSYNC_CNT (R)	15:8	0x0	Read only. VSYNC counter.
CAP_VSYNC_CLR	16	0x0	Reset the VSYNC counter.

Capture 0 trigger control.

<b>CAP0_DEBUG - R - 32 bits - [MMReg:0x954]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_H_STATUS	11:0	0x0	Capture 0 Horizontal status.
CAP_V_STATUS	27:16	0x0	Capture 0 vertical status.
CAP_V_SYNC	28	0x0	Capture 0 VSYNC status.

Capture 0 debug status register.

<b>CAP0_CONFIG - RW - 32 bits - [MMReg:0x958]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_INPUT_MODE	0	0x0	Input mode. 0=OneShot trigger mode 1=Enable continuous capture
CAP_START_FIELD	1	0x0	Starting field. 0=Odd 1=Even
CAP_START_BUF_R (R)	2	0x0	Read only. Current starting buffer. 0=Buffer 0 1=Buffer 1
CAP_START_BUF_W (W)	3	0x0	Write only. Control starting buffer. 0=Buffer 0 1=Buffer 1
CAP_BUF_TYPE	5:4	0x0	Buffer type. 0=Field 1=Alternating 2=Frame
CAP_ONESHOT_MODE	6	0x0	ONESHOT mode. 0=FIELD 1=FRAME
CAP_BUF_MODE	8:7	0x0	Capture 0 buffer mode. 0=Single 1=Double 2=Triple
CAP_MIRROR_EN	9	0x0	Capture 0 mirroring function enable. 0=Normal 1=Mirror
CAP_ONESHOT_MIRROR_EN	10	0x0	ONESHOT buffer mirroring function enable. 0=Normal 1=Mirror

CAP_VIDEO_SIGNED_UV	11	0x0	Enable conversion to signed value. 1=Convert to signed
CAP_ANC_DECODE_EN	12	0x0	ANC enable. 0=disable 1=enable
CAP_VBI_EN	13	0x0	VBI enable. 0=disable 1=enable
CAP_SOFT_PULL_DOWN_EN	14	0x0	Software pull down enable. 0=disable 1=enable
CAP_VIP_EXTEND_FLAG_EN	15	0x0	Extended flag enable. 0=DISABLE 1=ENABLE
CAP_FAKE_FIELD_EN	16	0x1	Fake field enable. 0=DISABLE 1=ENABLE
CAP_FIELD_START_LINE_DIFF	18:17	0x0	Odd, Even frame line number differences. 0=EQUAL 1=ODD_ONE_MORE_LINE 2=EVEN_ONE_MORE_LINE
CAP_HORZ_DOWN	20:19	0x0	Horizontal decimation. 0=Normal 1=x2 2=x4
CAP_VERT_DOWN	22:21	0x0	Vertical decimation. 0=Normal 1=x2 2=x4
CAP_STREAM_FORMAT	25:23	0x0	Video stream format. 0=Brooktree 1=CCIR 656 2=ZV 3=16bit VIP 4=TRANSPORT STREAM
CAP_HDWNS_DEC	26	0x1	Horizontal downscaler or decimator. 0=downscaler 1=decimator
CAP_VIDEO_IN_FORMAT	29	0x0	Input format. 0=YVYU422 1=VYUY422
VBI_HORZ_DOWN	31:30	0x0	0=Normal 1=x2 2=x4

Capture 0 configuration register.

<b>CAPO_ANC0_OFFSET - RW - 32 bits - [MMReg:0x95C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_ANC0_OFFSET	31:0	0x0	Starting address  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 ANC 0 starting address.

<b>CAPO_ANC1_OFFSET - RW - 32 bits - [MMReg:0x960]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_ANC1_OFFSET	31:0	0x0	Starting address  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 ANC 1 starting address.

<b>CAPO_ANC_H_WINDOW - RW - 32 bits - [MMReg:0x964]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_ANC_WIDTH	11:0	0x0	Window width.  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 ANC horizontal window.

<b>CAPO_VIDEO_SYNC_TEST - RW - 32 bits - [MMReg:0x968]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_TEST_VID_SOF	0	0x0	Start of field.
CAP_TEST_VID_EOF	1	0x0	End of field.
CAP_TEST_VID_EOL	2	0x0	End of line.
CAP_TEST_VID_FIELD	3	0x0	Odd/Even field. 0=Even Field 1=Odd Field
CAP_TEST_SYNC_EN	5	0x0	Test sync enable. 0=Normal 1=Test Mode

Capture port 0 sync test.

<b>CAP0_ONESHOT_BUF_OFFSET - RW - 32 bits - [MMReg:0x96C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_ONESHOT_BUF_OFFSET	31:0	0x0	ONESHOT buffer starting address.  NOTE: Bits 0:1 of this field are hardwired to ZERO.

ONESHOT buffer starting address.

<b>CAP0_BUF_STATUS - R - 32 bits - [MMReg:0x970]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_PRE_VID_BUF	1:0	0x0	Read only. Previous capture buffer.
CAP_CUR_VID_BUF	3:2	0x0	Read only. Current Capture buffer.
CAP_PRE_FIELD	4	0x0	Read only. Previous field.
CAP_CUR_FIELD	5	0x0	Read only. Current field.
CAP_PRE_VBI_BUF	7:6	0x0	Read only. Previous VBI buffer.
CAP_CUR_VBI_BUF	9:8	0x0	Read only. Current VBI buffer.
CAP_VBI_BUF_STATUS	10	0x0	Read only. VBI busy status. 0=done 1=busy
CAP_PRE_ANC_BUF	12:11	0x0	Read only. Previous ANC buffer.
CAP_CUR_ANC_BUF	14:13	0x0	Read only. Current ANC buffer.
CAP_ANC_BUF_STATUS	15	0x0	Read only. Buffer busy status. 0=done 1=busy
CAP_ANC_PRE_BUF_CNT	27:16	0x0	Read only. Buffer count.
CAP_VIP_INC	28	0x0	Read only. Interlaced or not. 0=INTERLACED 1=NON_INTERLACED
CAP_VIP_PRE_REPEAT_FIELD	29	0x0	Read only. Previous buffer is new/repeat field. 0=new_field 1=repeated_field
CAP_CAP_BUF_STATUS	30	0x0	Read only. Capture buffer busy status. 0=done 1=busy

Capture 0 buffer status.

<b>CAPO_VBI2_OFFSET - RW - 32 bits - [MMReg:0x980]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_VBI2_OFFSET	31:0	0x0	Capture 0 VBI 2 buffer's starting address.  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 VBI 2 buffer's starting address.

<b>CAPO_VBI3_OFFSET - RW - 32 bits - [MMReg:0x984]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_VBI3_OFFSET	31:0	0x0	Capture 0 VBI 3 buffer's starting address.  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 VBI 3 buffer's starting address.

<b>CAPO_ANC2_OFFSET - RW - 32 bits - [MMReg:0x988]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_ANC2_OFFSET	31:0	0x0	Starting address  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 ANC 2 starting address.

<b>CAPO_ANC3_OFFSET - RW - 32 bits - [MMReg:0x98C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_ANC3_OFFSET	31:0	0x0	Starting address  NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 ANC 3 starting address.

<b>VID_BUFFER_CONTROL - RW - 32 bits - [MMReg:0x900]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAPO_BUFFER_WATER_MARK	4:0	0x1	Capture 0 buffer water mark.

FULL_BUFFER_EN	16	0x0	1= The shared buffer is dedicated to one capture only. 0=DISABLE 1=ENABLE
CAP0_ANC_VBI_QUAD_BUF	17	0x0	0=Dual buffer 1=Quaduple buffer
VID_BUFFER_RESET	20	0x0	Reset the buffer pointers. 0=NOT RESET 1=RESET
CAP_SWAP	22:21	0x0	Capture Port Swap control.
CAP0_BUFFER_EMPTY (R)	24	0x0	Capture 0's buffer empty status. 0=EMPTY 1=NOT EMPTY

Video Capture port buffer control.

<b>CAP_INT_CNTL - RW - 32 bits - [MMReg:0x908]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP0_BUF0_INT_EN	0	0x0	Capture 0 Buffer 0 Interrupt enable. 0=Disable 1=Enable
CAP0_BUF0_EVEN_INT_EN	1	0x0	Capture 0 Buffer 0 even frame Interrupt enable. 0=Disable 1=Enable
CAP0_BUF1_INT_EN	2	0x0	Capture 0 Buffer 1 Interrupt enable. 0=Disable 1=Enable
CAP0_BUF1_EVEN_INT_EN	3	0x0	Capture 0 Buffer 1 even frame Interrupt enable. 0=Disable 1=Enable
CAP0_VBI0_INT_EN	4	0x0	Capture 0 VBI Buffer 0 Interrupt enable. 0=Disable 1=Enable
CAP0_VBI1_INT_EN	5	0x0	Capture 0 VBI Buffer 1 Interrupt enable. 0=Disable 1=Enable
CAP0_ONESHOT_INT_EN	6	0x0	Capture 0 ONESHOT Buffer Interrupt enable. 0=Disable 1=Enable
CAP0_ANC0_INT_EN	7	0x0	Capture 0 ANC Buffer 0 Interrupt enable. 0=Disable 1=Enable

CAP0_ANC1_INT_EN	8	0x0	Capture 0 ANC Buffer 1 Interrupt enable. 0=Disable 1=Enable
CAP0_VBI2_INT_EN	9	0x0	Capture 0 VBI Buffer 2 Interrupt enable. 0=Disable 1=Enable
CAP0_VBI3_INT_EN	10	0x0	Capture 0 VBI Buffer 3 Interrupt enable. 0=Disable 1=Enable
CAP0_ANC2_INT_EN	11	0x0	Capture 0 ANC Buffer 2 Interrupt enable. 0=Disable 1=Enable
CAP0_ANC3_INT_EN	12	0x0	Capture 0 ANC Buffer 3 Interrupt enable. 0=Disable 1=Enable

Video Capture port interrupt control register

<b>CAP_INT_STATUS - RW - 32 bits - [MMReg:0x90C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP0_BUF0_INT (R)	0	0x0	Read only. Buffer 0 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_BUF0_INT_AK (W)	0	0x0	Buf0 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_BUF0_EVEN_INT (R)	1	0x0	Read only. Buffer 0 even frame interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_BUF0_EVEN_INT_AK (W)	1	0x0	Buf0 even frame buffer interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_BUF1_INT (R)	2	0x0	Read only. Buffer 1 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_BUF1_INT_AK (W)	2	0x0	Buf1 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_BUF1_EVEN_INT (R)	3	0x0	Read only. Buffer 1 even frame interrupt status. 0=No event 1=Event has occurred, interrupting if enabled

CAP0_BUF1_EVEN_INT_AK (W)	3	0x0	Buf1 even frame buffer interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_VBI0_INT (R)	4	0x0	Read only. VBI buffer 0 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_VBI0_INT_AK (W)	4	0x0	VBI buffer 0 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_VBI1_INT (R)	5	0x0	Read only. VBI buffer 1 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_VBI1_INT_AK (W)	5	0x0	VBI buffer 1 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_ONESHOT_INT (R)	6	0x0	Read only. ONESHOT buffer interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_ONESHOT_INT_AK (W)	6	0x0	ONESHOT buffer interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_ANC0_INT (R)	7	0x0	Read only. ANC buffer 0 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_ANC0_INT_AK (W)	7	0x0	ANC buffer 0 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_ANC1_INT (R)	8	0x0	Read only. ANC buffer 1 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_ANC1_INT_AK (W)	8	0x0	ANC buffer 1 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_VBI2_INT (R)	9	0x0	Read only. VBI buffer 2 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_VBI2_INT_AK (W)	9	0x0	VBI buffer 2 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_VBI3_INT (R)	10	0x0	Read only. VBI buffer 3 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled

## Capture Registers

CAP0_VBI3_INT_AK (W)	10	0x0	VBI buffer 3 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_ANC2_INT (R)	11	0x0	Read only. ANC buffer 2 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_ANC2_INT_AK (W)	11	0x0	ANC buffer 2 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_ANC3_INT (R)	12	0x0	Read only. ANC buffer 3 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_ANC3_INT_AK (W)	12	0x0	ANC buffer 3 interrupt acknowledgment. 0=No effect 1=Clear status

Capture port interrupt control.

## 2.15 DMA Registers

### Direct Memory Access Description.

DMA_VIPH0_COMMAND - R - 32 bits - [MMReg:0xA00]			
Field Name	Bits	Default	Description
BYTE_COUNT	20:0	0x0	Byte Count of transfer size.
SWAP_CONTROL	25:24	0x0	Endian's swap control. 0=No Swaping 1=[15:0] = [31:16], [31:16] = [15:0] 2=[7:0] = [31:24], [15:8] = [23:16], [23:16] = [15:8], [31:24] = [7:0] 3=Undefined
TRANSFER_SOURCE	26	0x0	Address space of source data. 0=Transfer from memory 1=Transfer from VIPH
TRANSFER_DEST	27	0x0	Address space of destination data. 0=Transfer to memory 1=Transfer to VIPH
SOURCE_OFFSET_HOLD	28	0x0	Hold the source address without increase. 0=Increment 1=Hold
DEST_OFFSET_HOLD	29	0x0	Hold the destination address without increase. 0=Increment 1=Hold
INTERRUPT_DIS	30	0x0	End of DMA command table interrupt control. 0=Normal 1=Disable the end of list interrupt
END_OF_LIST_STATUS	31	0x0	Status bit show the last command of the DMA table. 0=Normal 1=End of Descriptor List

VIPH channel0 DMA command read back.

DMA_VIPH1_COMMAND - R - 32 bits - [MMReg:0xA04]			
Field Name	Bits	Default	Description
BYTE_COUNT	20:0	0x0	Byte Count of transfer size.

SWAP_CONTROL	25:24	0x0	Endian's swap control. 0=No Swaping 1=[15:0] = [31:16], [31:16] = [15:0] 2=[7:0] =[31:24], [15:8] = [23:16], [23:16] = [15:8], [31:24] = [7:0] 3=Undefined
TRANSFER_SOURCE	26	0x0	Address space of source data. 0=Transfer from memory 1=Transfer from VIPH
TRANSFER_DEST	27	0x0	Address space of destination data. 0=Transfer to memory 1=Transfer to VIPH
SOURCE_OFFSET_HOLD	28	0x0	Hold the source address without increase. 0=Increment 1=Hold
DEST_OFFSET_HOLD	29	0x0	Hold the destination address without increase. 0=Increment 1=Hold
INTERRUPT_DIS	30	0x0	End of DMA command table interrupt control. 0=Normal 1=Disable the end of list interrupt
END_OF_LIST_STATUS	31	0x0	Status bit show the last command of the DMA table. 0=Normal 1=End of Descriptor List

VIPH channel1 DMA command read back.

<b>DMA_VIPH2_COMMAND - R - 32 bits - [MMReg:0xA08]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BYTE_COUNT	20:0	0x0	Byte Count of transfer size.
SWAP_CONTROL	25:24	0x0	Endian's swap control. 0=No Swaping 1=[15:0] = [31:16], [31:16] = [15:0] 2=[7:0] =[31:24], [15:8] = [23:16], [23:16] = [15:8], [31:24] = [7:0] 3=Undefined
TRANSFER_SOURCE	26	0x0	Address space of source data. 0=Transfer from memory 1=Transfer from VIPH
TRANSFER_DEST	27	0x0	Address space of destination data. 0=Transfer to memory 1=Transfer to VIPH

SOURCE_OFFSET_HOLD	28	0x0	Hold the source address without increase. 0=Increment 1=Hold
DEST_OFFSET_HOLD	29	0x0	Hold the destination address without increase. 0=Increment 1=Hold
INTERRUPT_DIS	30	0x0	End of DMA command table interrupt control. 0=Normal 1=Disable the end of list interrupt
END_OF_LIST_STATUS	31	0x0	Status bit show the last command of the DMA table. 0=Normal 1=End of Descriptor List

VIPH channel2 DMA command read back.

<b>DMA_VIPH3_COMMAND - R - 32 bits - [MMReg:0xA0C]</b>			
Field Name	Bits	Default	Description
BYTE_COUNT	20:0	0x0	Byte Count of transfer size.
SWAP_CONTROL	25:24	0x0	Endian's swap control. 0=No Swaping 1=[15:0] = [31:16], [31:16] = [15:0] 2=[7:0] = [31:24], [15:8] = [23:16], [23:16] = [15:8], [31:24] = [7:0] 3=Undefined
TRANSFER_SOURCE	26	0x0	Address space of source data. 0=Transfer from memory 1=Transfer from VIPH
TRANSFER_DEST	27	0x0	Address space of destination data. 0=Transfer to memory 1=Transfer to VIPH
SOURCE_OFFSET_HOLD	28	0x0	Hold the source address without increase. 0=Increment 1=Hold
DEST_OFFSET_HOLD	29	0x0	Hold the destination address without increase. 0=Increment 1=Hold
INTERRUPT_DIS	30	0x0	End of DMA command table interrupt control. 0=Normal 1=Disable the end of list interrupt
END_OF_LIST_STATUS	31	0x0	Status bit show the last command of the DMA table. 0=Normal 1=End of Descriptor List

VIPH channel3 DMA command read back.

<b>DMA_VIPH_STATUS - R - 32 bits - [MMReg:0xA10]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DMA_VIPH0_AVAIL	3:0	0x3	VIPH DMA channel 0 available job queue number.
DMA_VIPH1_AVAIL	7:4	0x3	VIPH DMA channel 1 available job queue number.
DMA_VIPH2_AVAIL	11:8	0x3	VIPH DMA channel 2 available job queue number.
DMA_VIPH3_AVAIL	15:12	0x3	VIPH DMA channel 3 available job queue number.
DMA_VIPH0_CURRENT	17:16	0x0	VIPH DMA channel 0 current active job queue number
DMA_VIPH1_CURRENT	19:18	0x0	VIPH DMA channel 1 current active job queue number
DMA_VIPH2_CURRENT	21:20	0x0	VIPH DMA channel 2 current active job queue number
DMA_VIPH3_CURRENT	23:22	0x0	VIPH DMA channel 3 current active job queue number
DMA_VIPH0_ACTIVE	24	0x0	VIPH DMA channel 0 active status. 0=All VIP0 queue transfers are all done 1=A VIP0 queue transfer is active
DMA_VIPH1_ACTIVE	25	0x0	VIPH DMA channel 1 active status. 0=All VIP1 queue transfers are all done 1=A VIP1 queue transfer is active
DMA_VIPH2_ACTIVE	26	0x0	VIPH DMA channel 2 active status. 0=All VIP2 queue transfers are all done 1=A VIP2 queue transfer is active
DMA_VIPH3_ACTIVE	27	0x0	VIPH DMA channel 3 active status. 0=All VIP3 queue transfers are all done 1=A VIP3 queue transfer is active

VIPH DMA channels status register.

<b>DMA_VIPH_CHUNK_0 - RW - 32 bits - [MMReg:0xA18]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DMA_VIPH3_TABLE_SWAP	1:0	0x0	VIPH DMA Channel 3 Endian swap control. 0=No swap 1=8bit swap 2=16bit swap 3=reserved
DMA_VIPH2_TABLE_SWAP	3:2	0x0	VIPH DMA Channel 2 Endian swap control. 0=No swap 1=8bit swap 2=16bit swap 3=reserved

DMA_VIPH1_TABLE_SWAP	5:4	0x0	VIPH DMA Channel 1 Endian swap control. 0=No swap 1=8bit swap 2=16bit swap 3=reserved
DMA_VIPH0_TABLE_SWAP	7:6	0x0	VIPH DMA Channel 0 Endian swap control. 0=No swap 1=8bit swap 2=16bit swap 3=reserved
DMA_VIPH3_NOCHUNK	28	0x0	VIPH DMA Channel 3 disregard chunk size 0=Use chunk value 1=Use infinity for the chunk value
DMA_VIPH2_NOCHUNK	29	0x0	VIPH DMA Channel 2 disregard chunk size 0=Use chunk value 1=Use infinity for the chunk value
DMA_VIPH1_NOCHUNK	30	0x0	VIPH DMA Channel 1 disregard chunk size 0=Use chunk value 1=Use infinity for the chunk value
DMA_VIPH0_NOCHUNK	31	0x0	VIPH DMA Channel 0 disregard chunk size 0=Use chunk value 1=Use infinity for the chunk value

VIP Host Port DMA Chunk control register.

<b>DMA_VIPH_CHUNK_1_VAL - RW - 32 bits - [MMReg:0xA1C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DMA_VIP0_CHUNK	7:0	0xf	VIP Host Port DMA channel 0 Chunk size
DMA_VIP1_CHUNK	15:8	0xf	VIP Host Port DMA channel 1 Chunk size
DMA_VIP2_CHUNK	23:16	0xf	VIP Host Port DMA channel 2 Chunk size
DMA_VIP3_CHUNK	31:24	0xf	VIP Host Port DMA channel 3 Chunk size

VIP Host Port DMA Chunk size

<b>DMA_VIP0_TABLE_ADDR - W - 32 bits - [MMReg:0xA20]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DMA_VIPH_TABLE_ADDR	31:0	0x0	This points to first entry in the DMA table.

VIP Port 0 DMA table starting address

<b>DMA_VIP1_TABLE_ADDR - W - 32 bits - [MMReg:0xA30]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DMA_VIPH_TABLE_ADDR	31:0	0x0	This points to first entry in the DMA table.

VIP Port 1 DMA table starting address

<b>DMA_VIP2_TABLE_ADDR - W - 32 bits - [MMReg:0xA40]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DMA_VIPH_TABLE_ADDR	31:0	0x0	This points to first entry in the DMA table.

VIP Port 2 DMA table starting address

<b>DMA_VIP3_TABLE_ADDR - W - 32 bits - [MMReg:0xA50]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DMA_VIPH_TABLE_ADDR	31:0	0x0	This points to first entry in the DMA table.

VIP Port 3 DMA table starting address

<b>DMA_VIPH0_ACTIVE - R - 32 bits - [MMReg:0xA24]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DMA_VIPH_TABLE_ADDR_ACT	31:0	0x0	This points to the current active entry in the DMA table.

VIP Port 0 DMA Current table address

<b>DMA_VIPH1_ACTIVE - R - 32 bits - [MMReg:0xA34]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DMA_VIPH_TABLE_ADDR_ACT	31:0	0x0	This points to the current active entry in the DMA table.

VIP Port 1 DMA Current table address

**DMA\_VIPH2\_ACTIVE - R - 32 bits - [MMReg:0xA44]**

Field Name	Bits	Default	Description
DMA_VIPH_TABLE_ADDR_ACT	31:0	0x0	This points to the current active entry in the DMA table.

VIP Port 2 DMA Current table address

**DMA\_VIPH3\_ACTIVE - R - 32 bits - [MMReg:0xA54]**

Field Name	Bits	Default	Description
DMA_VIPH_TABLE_ADDR_ACT	31:0	0x0	This points to the current active entry in the DMA table.

VIP Port 3 DMA Current table address

**DMA\_VIPH\_ABORT - RW - 32 bits - [MMReg:0xA88]**

Field Name	Bits	Default	Description
DMA_VIPH0_ABORT_QUE	2:0	0x0	Select which job in the queue of VIP Host Port DMA channel 0 is going to be aborted 0=queue number to abort
DMA_VIPH0_ABORT_EN	3	0x0	Enable abort action 0=Normal 1=Enable queue abort
DMA_VIPH1_ABORT_QUE	6:4	0x0	Select which job in the queue of VIP Host Port DMA channel 1 is going to be aborted 0=queue number to abort
DMA_VIPH1_ABORT_EN	7	0x0	Enable abort action 0=Normal 1=Enable queue abort
DMA_VIPH2_ABORT_QUE	10:8	0x0	Select which job in the queue of VIP Host Port DMA channel 2 is going to be aborted 0=queue number to abort
DMA_VIPH2_ABORT_EN	11	0x0	Enable abort action 0=Normal 1=Enable queue abort
DMA_VIPH3_ABORT_QUE	14:12	0x0	Select which job in the queue of VIP Host Port DMA channel 3 is going to be aborted 0=queue number to abort
DMA_VIPH3_ABORT_EN	15	0x0	Enable abort action 0=Normal 1=Enable queue abort

*DMA Registers*

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DMA_VIPH0_RESET	20	0x0	Soft reset. Reset the DMA and job queue.
DMA_VIPH1_RESET	21	0x0	Soft reset. Reset the DMA and job queue.
DMA_VIPH2_RESET	22	0x0	Soft reset. Reset the DMA and job queue.
DMA_VIPH3_RESET	23	0x0	Soft reset. Reset the DMA and job queue.

VIP Host Port DMA abort control registers

## 2.16 CommandProcessor Registers

### Command Processor Control Registers.

CP_RB_CNTL - RW - 32 bits - [MMReg:0x704]			
Field Name	Bits	Default	Description
RB_BUFSZ	5:0	0x0	Ring Buffer Size. This size is expressed in log2 of the actual size (in 64-bit 'quadwords' ). For example, for a buffer of 1024 quadwords, you would program this field to 10(decimal). Default = 0
RB_BLKSZ	13:8	0x0	Ring Buffer Block Size. This defines the number of quadwords that the Command Processor will read between updates to the host's copy of the Read Pointer. This size is expressed in log2 of the actual size (in 64-bit 'quadwords' ). For example, for a block of 1024 quadwords, you would program this field to 10(decimal). Default = 0
BUF_SWAP	17:16	0x0	Endian Swap Control for Ring Buffer and Indirect Buffer. Only affects the chip behavior if the buffer resides in system memory. 0 = No swap 1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC 2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA 3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB Default = 0
MAX_FETCH	19:18	0x0	Maximum Fetch Size for any read request that the CP makes to memory. 0 = 1 octword. (16 bytes) 1 = 2 octwords. (32 bytes) 2 = 4 octwords. (64 bytes) 3 = reserved Default = 0
RB_NO_UPDATE	27	0x0	Ring Buffer No Write to Read Pointer 0= Write to Host's copy of Read Pointer in system memory. 1= Do not write to Host's copy of Read pointer. The purpose of this control bit is to have a fall-back position if the bus-mastered write to system memory doesn't work, in which case the driver will have to read the Graphics Controller's copy of the Read Pointer directly, with some performance penalty. Default = 0

Ring Buffer Control

<b>CP_RB_BASE - RW - 32 bits - [MMReg:0x700]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
RB_BASE	31:2	0x0	Ring Buffer Base. Address of the beginning of the ring buffer.

Ring Buffer Base

<b>CP_RB_RPTR_ADDR - RW - 32 bits - [MMReg:0x70C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
RB_RPTR_SWAP	1:0	0x0	
RB_RPTR_ADDR	31:2	0x0	Ring Buffer Read Pointer Address. Address of the Host's copy of the Read Pointer. CP_RB_RPTR (RO) Ring Buffer Read Pointer

Ring Buffer Read Pointer Address

<b>CP_RB_RPTR - R - 32 bits - [MMReg:0x710]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
RB_RPTR	22:0	0x0	Ring Buffer Read Pointer. This is an index (in dwords) of the current element being read from the ring buffer. Read Only.

Ring Buffer Read Pointer Address

<b>CP_RB_WPTR - RW - 32 bits - [MMReg:0x714]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
RB_WPTR	22:0	0x0	Ring Buffer Write Pointer. This is an index (in dwords) of the last known element to be written to the ring buffer (by the host).

Ring Buffer Write Pointer

<b>CP_RB_WPTR_DELAY - RW - 32 bits - [MMReg:0x718]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
PRE_WRITE_TIMER	27:0	0x0	Pre-Write Timer. The number of clocks that a write to the CP_RB_WPTR register will be delayed until actually taking effect. Default = 0
PRE_WRITE_LIMIT	31:28	0x0	Pre-Write Limit. The number of times that the CP_RB_WPTR register can be written (while the PRE_WRITE_TIMER has not expired) before the CP_RB_WPTR register is forced to be updated with the most recently written value. Default = 0

Ring Buffer Write Pointer Delay

<b>CP_IB_BASE - RW - 32 bits - [MMReg:0x738]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
IB_BASE	31:2	0x0	Indirect Buffer Base. Address of the beginning of the indirect buffer.

Indirect Buffer Base

<b>CP_IB_BUFSZ - RW - 32 bits - [MMReg:0x73C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
IB_BUFSZ	22:0	0x0	Indirect Buffer Size. This size is expressed in dwords. This field is an initiator to begin fetching commands from the Indirect Buffer. Default = 0

Indirect Buffer Size

<b>CP_CSQ_CNTL - RW - 32 bits - [MMReg:0x740]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CSQ_CNT_PRIMARY (R)	7:0	0x0	Count of available dwords in the queue for the Primary Stream. Read Only.

CSQ_CNT_INDIRECT (R)	15:8	0x0	Count of available dwords in the queue for the Indirect Stream. Read Only.
CSQ_MODE	31:28	0x0	Command Stream Queue Mode. Controls whether each command stream is enabled, and whether it is in push mode (Programmed I/O), or pull mode (Bus-Master). Encodings are chosen to be compatible with Rage128. 0= Primary Disabled, Indirect Disabled. 1= Primary PIO, Indirect Disabled. 2= Primary BM, Indirect Disabled. 3,5,7= Primary PIO, Indirect BM. 4,6,8= Primary BM, Indirect BM. 9-14= Reserved. 15= Primary PIO, Indirect PIO Default = 0

Command Stream Queue Control

CP_CSQ_APER_PRIMARY - RW - 32 bits - [MMReg:0x1000-0x11FC]			
Field Name	Bits	Default	Description
CP_CSQ_APER_PRIMARY	31:0	0x0	

No description available for this register.

CP_CSQ_APER_INDIRECT - RW - 32 bits - [MMReg:0x1300-0x13FC]			
Field Name	Bits	Default	Description
CP_CSQ_APER_INDIRECT	31:0	0x0	

No description available for this register.

SCRATCH_REG0 - RW - 32 bits - [MMReg:0x15E0]			
Field Name	Bits	Default	Description
SCRATCH_REG0	31:0	0x0	ScratchPad Register.

ScratchPad Register.

<b>SCRATCH_REG1 - RW - 32 bits - [MMReg:0x15E4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SCRATCH_REG1	31:0	0x0	ScratchPad Register.

ScratchPad Register.

<b>SCRATCH_REG2 - RW - 32 bits - [MMReg:0x15E8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SCRATCH_REG2	31:0	0x0	ScratchPad Register.

ScratchPad Register.

<b>SCRATCH_REG3 - RW - 32 bits - [MMReg:0x15EC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SCRATCH_REG3	31:0	0x0	ScratchPad Register.

ScratchPad Register.

<b>SCRATCH_REG4 - RW - 32 bits - [MMReg:0x15F0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SCRATCH_REG4	31:0	0x0	ScratchPad Register.

ScratchPad Register.

<b>SCRATCH_REG5 - RW - 32 bits - [MMReg:0x15F4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SCRATCH_REG5	31:0	0x0	ScratchPad Register.

ScratchPad Register.

<b>SCRATCH_UMSK - RW - 32 bits - [MMReg:0x770]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SCRATCH_UMSK	5:0	0x0	Update Mask for ScratchPad Registers. One bit for each of the scratchpad registers. 1 = Write the contents of the respective ScratchPad register to Memory (using the SCRATCH_ADDR register as a base) whenever that ScratchPad register is written. 0 = No write to memory. Default = 0
SCRATCH_SWAP	17:16	0x0	

ScratchPad Register Update Mask

<b>SCRATCH_ADDR - RW - 32 bits - [MMReg:0x774]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SCRATCH_ADDR	31:5	0x0	Memory Address to which the contents of scratchpad registers should be written. Reg 0 is written to address: SCRATCH_ADDR + 0 Reg 1 is written to address: SCRATCH_ADDR + 4 Reg 2 is written to address: SCRATCH_ADDR + 8 ... etc...

ScratchPad Register Address

<b>DMA_GUI_TABLE_ADDR - W - 32 bits - [MMReg:0x780]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CP_SYNC	0	0x0	Synchronize with the Command Processor. Indicates that the MicroEngine cannot proceed to write anything to the register backbone while this DMA is running.
TABLE_ADDR	31:4	0x0	Memory Address of the most recently active descriptor.

No description available for this register.

<b>DMA_GUI_SRC_ADDR - R - 32 bits - [MMReg:0x784]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SRC_ADDR	31:0	0x0	Memory Address or Register-space Address where Source data begins, for the currently active descriptor that is being processed by the DMA engine. Read Only.

No description available for this register.

<b>DMA_GUI_DST_ADDR - R - 32 bits - [MMReg:0x788]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DST_ADDR	31:0	0x0	Memory Address or Register-space Address where Source data is being written, for the currently active descriptor that is being processed by the DMA engine. Read Only.

No description available for this register.

<b>DMA_GUI_COMMAND - R - 32 bits - [MMReg:0x78C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BYTE_COUNT	20:0	0x0	Number of Bytes remaining to be transferred from Source to Destination.
SRC_SWAP	23:22	0x0	Source Endian Swap Control. 0 = No swap 1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC 2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA 3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB
DST_SWAP	25:24	0x0	Destination Endian Swap Control. 0 = No swap 1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC 2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA 3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB
SAS	26	0x0	Source Address Space. 0 = Source Address is a memory-space address 1 = Source Address is a register-space address
DAS	27	0x0	Destination Address Space. 0 = Destination Address is a memory-space address 1 = Destination Address is a register-space address

SAIC	28	0x0	Source Address Increment Control. 0 = Increment the internal Source Address with each data transfer. 1 = No increment.
DAIC	29	0x0	Destination Address Increment Control. 0 = Increment the internal Destination Address with each data transfer. 1 = No increment.
INTDIS	30	0x0	Interrupt Disable. This value is a don't care if the EOL bit is '0'. 1= Disable the EndOfList interrupt. 0= Don't disable interrupt.
EOL	31	0x0	End Of List. Indicates that the currently active descriptor is the last one in the Descriptor Table.

(RO)

<b>DMA_GUI_STATUS - RW - 32 bits - [MMReg:0x790]</b>			
Field Name	Bits	Default	Description
DTAQ_AVAIL (R)	4:0	0x0	The number of available entries in the Descriptor Table Address Queue. Read Only.
LAST_TABLE_NUM (R)	11:8	0x0	This is a pointer into the Descriptor Table Address Queue, indicating which queue entry was the last one to be written. Read Only.
CURRENT_TABLE_NUM (R)	15:12	0x0	This is a pointer into the Descriptor Table Address Queue, indicating which queue entry the DMA engine is currently processing. Read Only.
ABORT_EN	20	0x0	1 = Abort the Descriptor Table Address Queue entry indicated by the CURRENT_TABLE_NUM field, and halt operation. 0 = No Abort, or when following a value of '1', re-initialize (invalidate all entries in) the Descriptor Table Address Queue, and allow the DMA to accept new commands. Note that the programmer must wait for the ACTIVE bit to be '0' before writing a zero to the ABORT_EN bit; otherwise the DMA engine might hang.
ACTIVE (R)	21	0x0	Indicates that the DMA engine is currently working on a descriptor. It indicates whether the CURRENT_TABLE_NUM field is a valid entry in the Descriptor Table Address Queue. Read Only.

SWAP	23:22	0x0	Endian Swap Control for fetching the Descriptor Table. 0 = No swap 1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC 2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA 3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB
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No description available for this register.

<b>DMA_GUI_ACT_DSCRPTR - R - 32 bits - [MMReg:0x794]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
TABLE_ADDR	31:4	0x0	Memory Address of the most recently active descriptor.

(RO)

<b>DMA_VID_TABLE_ADDR - W - 32 bits - [MMReg:0x7A0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CP_SYNC	0	0x0	Synchronize with the Command Processor. Indicates that the MicroEngine cannot proceed to write anything to the register backbone while this DMA is running.
TABLE_ADDR	31:4	0x0	Memory Address of the most recently active descriptor.

No description available for this register.

<b>DMA_VID_SRC_ADDR - R - 32 bits - [MMReg:0x7A4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SRC_ADDR	31:0	0x0	Memory Address or Register-space Address where Source data begins, for the currently active descriptor that is being processed by the DMA engine. Read Only.

No description available for this register.

DMA_VID_DST_ADDR - R - 32 bits - [MMReg:0x7A8]			
Field Name	Bits	Default	Description
DST_ADDR	31:0	0x0	Memory Address or Register-space Address where Source data is being written, for the currently active descriptor that is being processed by the DMA engine. Read Only.

No description available for this register.

DMA_VID_COMMAND - R - 32 bits - [MMReg:0x7AC]			
Field Name	Bits	Default	Description
BYTE_COUNT	20:0	0x0	Number of Bytes remaining to be transferred from Source to Destination.
SRC_SWAP	23:22	0x0	Source Endian Swap Control. 0 = No swap 1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC 2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA 3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB
DST_SWAP	25:24	0x0	Destination Endian Swap Control. 0 = No swap 1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC 2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA 3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB
SAS	26	0x0	Source Address Space. 0 = Source Address is a memory-space address 1 = Source Address is a register-space address
DAS	27	0x0	Destination Address Space. 0 = Destination Address is a memory-space address 1 = Destination Address is a register-space address
SAIC	28	0x0	Source Address Increment Control. 0 = Increment the internal Source Address with each data transfer. 1 = No increment.
DAIC	29	0x0	Destination Address Increment Control. 0 = Increment the internal Destination Address with each data transfer. 1 = No increment.
INTDIS	30	0x0	Interrupt Disable. This value is a don't care if the EOL bit is '0'. 1 = Disable the EndOfList interrupt. 0 = Don't disable interrupt.

EOL	31	0x0	End Of List. Indicates that the currently active descriptor is the last one in the Descriptor Table.
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(RO)

<b>DMA_VID_STATUS - RW - 32 bits - [MMReg:0x7B0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DTAQ_AVAIL (R)	4:0	0x0	The number of available entries in the Descriptor Table Address Queue. Read Only.
LAST_TABLE_NUM (R)	11:8	0x0	This is a pointer into the Descriptor Table Address Queue, indicating which queue entry was the last one to be written. Read Only.
CURRENT_TABLE_NUM (R)	15:12	0x0	This is a pointer into the Descriptor Table Address Queue, indicating which queue entry the DMA engine is currently processing. Read Only.
ABORT_EN	20	0x0	1 = Abort the Descriptor Table Address Queue entry indicated by the CURRENT_TABLE_NUM field, and halt operation. 0 = No Abort, or when following a value of '1', re-initialize (invalidate all entries in) the Descriptor Table Address Queue, and allow the DMA to accept new commands. Note that the programmer must wait for the ACTIVE bit to be '0' before writing a zero to the ABORT_EN bit; otherwise the DMA engine might hang.
ACTIVE (R)	21	0x0	Indicates that the DMA engine is currently working on a descriptor. It indicates whether the CURRENT_TABLE_NUM field is a valid entry in the Descriptor Table Address Queue. Read Only.
SWAP	23:22	0x0	Endian Swap Control for fetching the Descriptor Table. 0 = No swap 1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC 2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA 3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB

No description available for this register.

<b>DMA_VID_ACT_DSCRPTR - R - 32 bits - [MMReg:0x7B4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
TABLE_ADDR	31:4	0x0	Memory Address of the most recently active descriptor.

(RO)

<b>CP_CSQ_ADDR - W - 32 bits - [MMReg:0x7F0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CSQ_ADDR	9:2	0x0	Address into the Command Stream Queue which is to be read from. Used for debug, to read the contents of the Command Stream Queue.

(WO) Command Stream Queue Address

<b>CP_CSQ_DATA - R - 32 bits - [MMReg:0x7F4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CSQ_DATA	31:0	0x0	Data from the Command Stream Queue, from location pointed to by the CP_CSQ_ADDR register. Used for debug, to read the contents of the Command Stream Queue.

(RO) Command Stream Queue Data

<b>CP_CSQ_STAT - R - 32 bits - [MMReg:0x7F8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CSQ_RPTR_PRIMARY	7:0	0x0	Current Read Pointer into the Primary Queue. Default = 0.
CSQ_WPTR_PRIMARY	15:8	0x0	Current Write Pointer into the Primary Queue. Default = 0.
CSQ_RPTR_INDIRECT	23:16	0x0	Current Read Pointer into the Indirect Queue. Default = 0.
CSQ_WPTR_INDIRECT	31:24	0x0	Current Write Pointer into the Indirect Queue. Default = 0.

(RO) Command Stream Queue Status

<b>CP_ME_CNTL - RW - 32 bits - [MMReg:0x7D0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ME_STAT (R)	15:0	0x0	Status of MicroEngine internal registers. This value depends on the current value of the ME_STATMUX field. Read Only.
ME_STATMUX	20:16	0x0	Selects which status is to be returned on the ME_STAT field.

ME_BUSY (R)	29	0x0	Busy indicator for the MicroEngine. 0 = MicroEngine not busy. 1 = MicroEngine is active. Read Only.
ME_MODE	30	0x1	Run-Mode of MicroEngine. 0 = Single-Step Mode. 1 = Free-running Mode. Default = 1
ME_STEP (W)	31	0x0	Step the MicroEngine by one instruction. Writing a '1' to this field causes the MicroEngine to step by one instruction, if and only if the ME_MODE bit is a '0'. Write Only.

Micro Engine Control

CP_ME_RAM_ADDR - RW - 32 bits - [MMReg:0x7D4]			
Field Name	Bits	Default	Description
ME_RAM_ADDR	7:0	0x0	MicroEngine RAM Address (Write Mode) Writing this register puts the RAM access circuitry into 'Write Mode', which allows the address to auto-increment as data is written into the RAM.

MicroEngine RAM Address

CP_ME_RAM_RADDR - W - 32 bits - [MMReg:0x7D8]			
Field Name	Bits	Default	Description
ME_RAM_RADDR <i>(mirror of CP_ME_RAM_ADDR:ME_RAM_ADDR)</i>	7:0	0x0	MicroEngine RAM Address (Read Mode) Writing this register puts the RAM access circuitry into 'Read Mode', which allows the address to auto-increment as data is read from the RAM. Write Only.

MicroEngine RAM Read Address

CP_ME_RAM_DATAH - RW - 32 bits - [MMReg:0x7DC]			
Field Name	Bits	Default	Description
ME_RAM_DATAH	5:0	0x0	MicroEngine RAM Data High Used to load the MicroEngine RAM.

MicroEngine RAM Data High

<b>CP_ME_RAM_DATA1 - RW - 32 bits - [MMReg:0x7E0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ME_RAM_DATA1	31:0	0x0	MicroEngine RAM Data Low Used to load the MicroEngine RAM.

MicroEngine RAM Data Low

## **2.17 DrawingEngine Registers**

### **Drawing Engine**

## 2.18 DrawingEngine2D Registers

### Drawing Engine 2D Control Registers.

DST_OFFSET - RW - 32 bits - [MMReg:0x1404]			
Field Name	Bits	Default	Description
DST_OFFSET	31:0	0x0	Destination Offset in Units of 1KB, 0 to (4GB-1KB). When a write to this register occurs, bits 9: 0 of destination offset will be set to 0.  NOTE: Bits 0:3 of this field are hardwired to ZERO.

Destination Offset in Units of 1KB, 0 to (4GB-1KB). When a write to this register occurs, bits 9: 0 of destination offset will be set to 0.

DST_PITCH - RW - 32 bits - [MMReg:0x1408]			
Field Name	Bits	Default	Description
DST_PITCH	13:0	0x0	Pitch in units of 64 bytes, 0 to 16320 bytes across. DST_TILE 31: 30 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) 2: microtiled 3: tiled and microtiled Write bits 31: 30 to E2_DST_TILE, 29: 22 to E2_DST_PITCH and 21: 0 to E2_DST_OFFSET  NOTE: Bits 0:3 of this field are hardwired to ZERO.

Pitch in units of 64 bytes, 0 to 16320 bytes across. DST\_TILE 31: 30 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) 2: microtiled 3: tiled and microtiled Write bits 31: 30 to E2\_DST\_TILE, 29: 22 to E2\_DST\_PITCH and 21: 0 to E2\_DST\_OFFSET

DST_WIDTH - RW - 32 bits - [MMReg:0x140C]			
Field Name	Bits	Default	Description
DST_WIDTH	13:0	0x0	Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete

Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2\_DST\_X, Write 31: 16 to E2\_DST\_WIDTH, then signal blit\_start. E2\_DST\_Y = E2\_DEST\_Y (+/-) E2\_DST\_HEIGHT as function of direction after blit is complete

<b>DST_HEIGHT - RW - 32 bits - [MMReg:0x1410]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DST_HEIGHT	13:0	0x0	Destination Height Write 15: 0 to E2_DST_Y, Write 31: 16 to E2_DST_HEIGHT

Destination Height Write 15: 0 to E2\_DST\_Y, Write 31: 16 to E2\_DST\_HEIGHT

<b>SRC_X - RW - 32 bits - [MMReg:0x1414]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SRC_X	13:0	0x0	Source X coordinate: range -8192 to 8191

Source X coordinate: range -8192 to 8191

<b>SRC_Y - RW - 32 bits - [MMReg:0x1418]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SRC_Y	13:0	0x0	Source Y coordinate: range -8192 to 8191 Write 13: 0 to E2_SRC_X, Write 29: 16 to E2_SRC_Y

Source Y coordinate: range -8192 to 8191 Write 13: 0 to E2\_SRC\_X, Write 29: 16 to E2\_SRC\_Y

<b>DST_X - RW - 32 bits - [MMReg:0x141C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DST_X	13:0	0x0	Destination X

Destination X

<b>DST_Y - RW - 32 bits - [MMReg:0x1420]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DST_Y	13:0	0x0	Destination Y

Destination Y

SRC_PITCH_OFFSET - W - 32 bits - [MMReg:0x1428]			
Field Name	Bits	Default	Description
SRC_OFFSET <i>(mirror bits 10:31 of SRC_OFFSET:SRC_OFFSET)</i>	21:0	0x0	Source Offset in Units of 1KB, 0 to (4GB-1KB). When a write to this register occurs, bits 9: 0 of source offset will be set to 0.
SRC_PITCH <i>(mirror bits 6:13 of SRC_PITCH:SRC_PITCH)</i>	29:22	0x0	Pitch in units of 64 bytes, 0 to 16320 bytes across. SRC_TILE 30 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) Write bit 30 to E2_SRC_TILE, 29: 22 to E2_SRC_PITCH and 21: 0 to E2_SRC_OFFSET
SRC_TILE <i>(mirror of SRC_TILE:SRC_TILE)</i>	30	0x0	0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) Write 0 to E2_SRC_TILE SRC_PITCH_OFFSET[ W/R]

No description available for this register.

DST_PITCH_OFFSET - W - 32 bits - [MMReg:0x142C]			
Field Name	Bits	Default	Description
DST_OFFSET <i>(mirror bits 10:31 of DST_OFFSET:DST_OFFSET)</i>	21:0	0x0	Destination Offset in Units of 1KB, 0 to (4GB-1KB). When a write to this register occurs, bits 9: 0 of destination offset will be set to 0.
DST_PITCH <i>(mirror bits 6:13 of DST_PITCH:DST_PITCH)</i>	29:22	0x0	Pitch in units of 64 bytes, 0 to 16320 bytes across. DST_TILE 31: 30 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) 2: microtiled 3: tiled and microtiled Write bits 31: 30 to E2_DST_TILE, 29: 22 to E2_DST_PITCH and 21: 0 to E2_DST_OFFSET
DST_TILE <i>(mirror of DST_TILE:DST_TILE)</i>	31:30	0x0	0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) 2: microtiled 3: tiled and microtiled Write 9: 0 to E2_DST_TILE DST_PITCH_OFFSET[ W/R]

No description available for this register.

SRC_Y_X - W - 32 bits - [MMReg:0x1434]			
Field Name	Bits	Default	Description
SRC_X <i>(mirror of SRC_X:SRC_X)</i>	13:0	0x0	Source X coordinate: range -8192 to 8191

SRC_Y <i>(mirror of SRC_Y:SRC_Y)</i>	29:16	0x0	Source Y coordinate: range -8192 to 8191 Write 13: 0 to E2_SRC_X, Write 29: 16 to E2_SRC_Y
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(aliased to SRC\_X, SRC\_Y) [ W] (MM: 5\_0D)

DST_Y_X - W - 32 bits - [MMReg:0x1438]			
Field Name	Bits	Default	Description
DST_X <i>(mirror of DST_X:DST_X)</i>	13:0	0x0	Destination X
DST_Y <i>(mirror of DST_Y:DST_Y)</i>	29:16	0x0	Destination Y

No description available for this register.

DST_HEIGHT_WIDTH - W - 32 bits - [MMReg:0x143C]			
Field Name	Bits	Default	Description
DST_WIDTH <i>(mirror of DST_WIDTH:DST_WIDTH)</i>	13:0	0x0	Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete
DST_HEIGHT <i>(mirror of DST_HEIGHT:DST_HEIGHT)</i>	29:16	0x0	Destination Height Write 15: 0 to E2_DST_Y, Write 31: 16 to E2_DST_HEIGHT

[ W] Destination Height and Width

DP_GUI_MASTER_CNTL - W - 32 bits - [MMReg:0x146C]			
Field Name	Bits	Default	Description
GMC_SRC_PITCH_OFFSET_CNTL	0	0x0	If 0: use E2_DEFAULT_OFFSET for source offset use E2_DEFAULT_PITCH for source pitch use E2_DEFAULT_TILE for source tiling if 1: use E2_SRC_OFFSET for source offset use E2_SRC_PITCH for source pitch use E2_SRC_TILE for source tiling 0=(SRC_OFFSET, SRC_PITCH) = (DEFAULT_PITCH_OFFSET) 1=Leave Alone

GMC_DST_PITCH_OFFSET_CNTL	1	0x0	<p>If 0: use E2_DEFAULT_OFFSET for destination offset use E2_DEFAULT_PITCH for destination pitch use E2_DEFAULT_TILE for destination tiling if 1: use E2_DST_OFFSET for destination offset use E2_DST_PITCH for destination pitch use E2_DST_TILE for destination tiling GMC_SRC_CLIPPING If 0: use E2_DEFAULT_SCISSOR_BOTTOM for source scissor bottom use E2_DEFAULT_SCISSOR_RIGHT for source scissor right if 1: use E2_SRC_SCISSOR_BOTTOM for source scissor bottom use E2_SRC_SCISSOR_RIGHT for source scissor right</p> <p>0=(DST_OFFSET, DST_PITCH) = (DEFAULT_PITCH_OFFSET) 1=Leave Alone</p>
GMC_SRC_CLIPPING	2	0x0	<p>0=(SC_RIGHT, SC_BOTTOM) = (DEFAULT_SC_BOTTOM_RIGHT) 1=no default</p>
GMC_DST_CLIPPING	3	0x0	<p>If 0: use E2_DEFAULT_SCISSOR_BOTTOM for destination scissor bottom use E2_DEFAULT_SCISSOR_RIGHT for destination scissor right use 0 for destination scissor top use 0 for destination scissor left if 1: use E2_DST_SCISSOR_BOTTOM for destination scissor bottom use E2_DST_SCISSOR_RIGHT for destination scissor right use E2_DST_SCISSOR_TOP for destination scissor top use E2_DST_SCISSOR_LEFT for destination scissor left GMC_BRUSH_DATATYPE Write to E2_BAGU_BRUSHTYPE 0=(SC_LEFT, SC_TOP) = (0,0), (SC_BOTTOM, SC_RIGHT) = DEF_SC_BOTTOM_RIGHT) 1=no default</p>
GMC_BRUSH_DATATYPE  <i>(mirror of DP_DATATYPE:DP_BRUSH_DATATYPE)</i>	7:4	0x0	<p>0=8X8 mono pattern (expanded to frgd, bkgd) 1=8X8 mono pattern (expanded to frgd, leave_alone) 2=RESERVED 3=RESERVED 4=RESERVED 5=RESERVED 6=32X1 mono pattern for lines (expanded to frgd, bkgd) 7=32X1 mono pattern for lines (expanded to frgd,leave_alone) 8=RESERVED 9=RESERVED 10=8X8 color (pixel type same as DST) 11=RESERVED 12=RESERVED 13=solid color for blits (use frgd) 14=solid color for lines (use frgd) 15=solid color for blits (use frgd)</p>

GMC_DST_DATATYPE <i>(mirror of DP_DATATYPE:DP_DST_DATATYPE)</i>	11:8	0x0	0=RESERVED 1=RESERVED 2=8 bpp pseudocolor 3=16 bpp aRGB 1555 4=16 bpp RGB 565 5=RESERVED 6=32 aRGB 8888
GMC_SRC_DATATYPE <i>(mirror bits 0:1 of DP_DATATYPE:DP_SRC_DATATYPE)</i>	13:12	0x0	0=mono (expanded to frgd, bkgd) 1=mono (expanded to frgd, leave_alone) 2=RESERVED 3=color (pixel type same as DST)=3
GMC_BYTE_PIX_ORDER <i>(mirror of DP_DATATYPE:DP_BYTE_PIX_ORDER)</i>	14	0x0	0=pixel order from MSBit to LSBit 1=pixel order from LSBit to MSBit
GMC_ROP3 <i>(mirror of DP_MIX:DP_ROP3)</i>	23:16	0x0	0=ROP3 function
GMC_DP_SRC_SOURCE <i>(mirror of DP_MIX:DP_SRC_SOURCE)</i>	26:24	0x0	2=loaded from memory (rectangular trajectory) 3=loaded thru hostadata (linear trajectory) 4=loaded thru hosdata (linear trajectory & byte-aligned)
GMC_SRC_DATATYPE2 <i>(mirror bits 2:2 of DP_DATATYPE:DP_SRC_DATATYPE)</i>	27	0x0	0=mono (expanded to frgd, bkgd) 1=RESERVED
GMC_CLR_CMP_FCN_DIS	28	0x0	
GMC_WR_MSK_DIS	30	0x0	

[ W] (MM: 5\_1B)

BRUSH_Y_X - RW - 32 bits - [MMReg:0x1474]			
Field Name	Bits	Default	Description
BRUSH_X	2:0	0x0	and BRUSH_Y to E2_BAGU_X and E2_BAGU_Y BRUSH_DATA [ 63: 0] [ R/W] (MM: 5_20 - 5_5F)
BRUSH_Y	10:8	0x0	

No description available for this register.

<b>DP_BRUSH_BKGD_CLR - RW - 32 bits - [MMReg:0x1478]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DP_BRUSH_BKGD_CLR	31:0	0x0	Background color Write to RB2D_BRUSHDATA[ 3] SRC_OFFSET[ W/R] Source Offset

Background color Write to RB2D\_BRUSHDATA[ 3] SRC\_OFFSET[ W/R] Source Offset

<b>DP_BRUSH_FRGD_CLR - RW - 32 bits - [MMReg:0x147C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DP_BRUSH_FRGD_CLR	31:0	0x0	Foreground color. Write to RB2D_BRUSHDATA[ 2] DP_BRUSH_BKGD_CLR [ R/W] (MM: 5_1E)

No description available for this register.

<b>BRUSH_DATA0 - W - 32 bits - [MMReg:0x1480]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA1 - W - 32 bits - [MMReg:0x1484]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA2 - W - 32 bits - [MMReg:0x1488]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA3 - W - 32 bits - [MMReg:0x148C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA4 - W - 32 bits - [MMReg:0x1490]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA5 - W - 32 bits - [MMReg:0x1494]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA6 - W - 32 bits - [MMReg:0x1498]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA7 - W - 32 bits - [MMReg:0x149C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA8 - W - 32 bits - [MMReg:0x14A0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA9 - W - 32 bits - [MMReg:0x14A4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA10 - W - 32 bits - [MMReg:0x14A8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA11 - W - 32 bits - [MMReg:0x14AC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA12 - W - 32 bits - [MMReg:0x14B0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA13 - W - 32 bits - [MMReg:0x14B4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA14 - W - 32 bits - [MMReg:0x14B8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA15 - W - 32 bits - [MMReg:0x14BC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA16 - W - 32 bits - [MMReg:0x14C0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA17 - W - 32 bits - [MMReg:0x14C4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA18 - W - 32 bits - [MMReg:0x14C8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA19 - W - 32 bits - [MMReg:0x14CC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA20 - W - 32 bits - [MMReg:0x14D0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA21 - W - 32 bits - [MMReg:0x14D4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA22 - W - 32 bits - [MMReg:0x14D8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA23 - W - 32 bits - [MMReg:0x14DC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA24 - W - 32 bits - [MMReg:0x14E0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA25 - W - 32 bits - [MMReg:0x14E4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA26 - W - 32 bits - [MMReg:0x14E8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA27 - W - 32 bits - [MMReg:0x14EC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA28 - W - 32 bits - [MMReg:0x14F0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA29 - W - 32 bits - [MMReg:0x14F4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA30 - W - 32 bits - [MMReg:0x14F8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA31 - W - 32 bits - [MMReg:0x14FC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA32 - W - 32 bits - [MMReg:0x1500]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA33 - W - 32 bits - [MMReg:0x1504]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA34 - W - 32 bits - [MMReg:0x1508]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA35 - W - 32 bits - [MMReg:0x150C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA36 - W - 32 bits - [MMReg:0x1510]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA37 - W - 32 bits - [MMReg:0x1514]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA38 - W - 32 bits - [MMReg:0x1518]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA39 - W - 32 bits - [MMReg:0x151C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA40 - W - 32 bits - [MMReg:0x1520]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA41 - W - 32 bits - [MMReg:0x1524]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA42 - W - 32 bits - [MMReg:0x1528]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA43 - W - 32 bits - [MMReg:0x152C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA44 - W - 32 bits - [MMReg:0x1530]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA45 - W - 32 bits - [MMReg:0x1534]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA46 - W - 32 bits - [MMReg:0x1538]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA47 - W - 32 bits - [MMReg:0x153C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA48 - W - 32 bits - [MMReg:0x1540]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA49 - W - 32 bits - [MMReg:0x1544]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA50 - W - 32 bits - [MMReg:0x1548]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA51 - W - 32 bits - [MMReg:0x154C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA52 - W - 32 bits - [MMReg:0x1550]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA53 - W - 32 bits - [MMReg:0x1554]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA54 - W - 32 bits - [MMReg:0x1558]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA55 - W - 32 bits - [MMReg:0x155C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA56 - W - 32 bits - [MMReg:0x1560]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA57 - W - 32 bits - [MMReg:0x1564]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA58 - W - 32 bits - [MMReg:0x1568]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA59 - W - 32 bits - [MMReg:0x156C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA60 - W - 32 bits - [MMReg:0x1570]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA61 - W - 32 bits - [MMReg:0x1574]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

<b>BRUSH_DATA62 - W - 32 bits - [MMReg:0x1578]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BRUSH_DATA	31:0	0x0	

No description available for this register.

BRUSH_DATA63 - W - 32 bits - [MMReg:0x157C]			
Field Name	Bits	Default	Description
BRUSH_DATA	31:0	0x0	

No description available for this register.

DST_WIDTH_X - W - 32 bits - [MMReg:0x1588]			
Field Name	Bits	Default	Description
DST_X <i>(mirror of DST_X:DST_X)</i>	13:0	0x0	Destination X
DST_WIDTH <i>(mirror of DST_WIDTH:DST_WIDTH)</i>	29:16	0x0	Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete

[ W ] Destination X and Width coordinate

DST_HEIGHT_WIDTH_8 - W - 32 bits - [MMReg:0x158C]			
Field Name	Bits	Default	Description
DST_WIDTH <i>(mirror bits 0:7 of DST_WIDTH:DST_WIDTH)</i>	23:16	0x0	Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete
DST_HEIGHT <i>(mirror bits 0:7 of DST_HEIGHT:DST_HEIGHT)</i>	31:24	0x0	Destination Height Write 15: 0 to E2_DST_Y, Write 31: 16 to E2_DST_HEIGHT

[ W ] (Reserved) 15: 0 DST\_WIDTH 23: 16 Destination width: range 0 to 256 (ZERO extent)

SRC_X_Y - W - 32 bits - [MMReg:0x1590]			
Field Name	Bits	Default	Description
SRC_Y <i>(mirror of SRC_Y:SRC_Y)</i>	13:0	0x0	Source Y coordinate: range -8192 to 8191 Write 13: 0 to E2_SRC_X, Write 29: 16 to E2_SRC_Y

SRC_X <i>(mirror of SRC_X:SRC_X)</i>	29:16	0x0	13: 0 Source X coordinate: range -8192 to 8191
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(aliased to SRC\_X, SRC\_Y) [ W] (MM: 5\_64)

DST_X_Y - W - 32 bits - [MMReg:0x1594]			
Field Name	Bits	Default	Description
DST_Y <i>(mirror of DST_Y:DST_Y)</i>	13:0	0x0	Destination Y
DST_X <i>(mirror of DST_X:DST_X)</i>	29:16	0x0	Destination X

No description available for this register.

DST_WIDTH_HEIGHT - W - 32 bits - [MMReg:0x1598]			
Field Name	Bits	Default	Description
DST_HEIGHT <i>(mirror of DST_HEIGHT:DST_HEIGHT)</i>	13:0	0x0	Destination Height Write 15: 0 to E2_DST_Y, Write 31: 16 to E2_DST_HEIGHT
DST_WIDTH <i>(mirror of DST_WIDTH:DST_WIDTH)</i>	29:16	0x0	Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete

Destination Width and Height

DST_WIDTH_X_INCY - W - 32 bits - [MMReg:0x159C]			
Field Name	Bits	Default	Description
DST_X <i>(mirror of DST_X:DST_X)</i>	13:0	0x0	Destination X
DST_WIDTH <i>(mirror of DST_WIDTH:DST_WIDTH)</i>	29:16	0x0	Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete

[ W] Destination Width and X coordinate

<b>DST_HEIGHT_Y - W - 32 bits - [MMReg:0x15A0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DST_Y <i>(mirror of DST_Y:DST_Y)</i>	13:0	0x0	Destination Y
DST_HEIGHT <i>(mirror of DST_HEIGHT:DST_HEIGHT)</i>	29:16	0x0	Destination Height Write 15: 0 to E2_DST_Y, Write 31: 16 to E2_DST_HEIGHT

No description available for this register.

<b>SRC_OFFSET - RW - 32 bits - [MMReg:0x15AC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SRC_OFFSET	31:0	0x0	Source Offset in Units of 1KB, 0 to (4GB-1KB). When a write to this register occurs, bits 9: 0 of source offset will be set to 0.  NOTE: Bits 0:3 of this field are hardwired to ZERO.

Source Offset in Units of 1KB, 0 to (4GB-1KB). When a write to this register occurs, bits 9: 0 of source offset will be set to 0.

<b>SRC_PITCH - RW - 32 bits - [MMReg:0x15B0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SRC_PITCH	13:0	0x0	Pitch in units of 64 bytes, 0 to 16320 bytes across. SRC_TILE 30 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) Write bit 30 to E2_SRC_TILE, 29: 22 to E2_SRC_PITCH and 21: 0 to E2_SRC_OFFSET  NOTE: Bits 0:3 of this field are hardwired to ZERO.

Pitch in units of 64 bytes, 0 to 16320 bytes across. SRC\_TILE 30 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) Write bit 30 to E2\_SRC\_TILE, 29: 22 to E2\_SRC\_PITCH and 21: 0 to E2\_SRC\_OFFSET

CLR_CMP_CNTL - W - 32 bits - [MMReg:0x15C0]			
Field Name	Bits	Default	Description
CLR_CMP_FCN_SRC	2:0	0x0	Color comparison function (Mnemonic, action): 0 = False (CMP_FALSE, always draw) 1 = True (CMP_TRUE, never draw) 2-3 = (reserved) 4 = SRC_CLR != CLR_CMP_CLR_SRC (CMP_EQ_COLOR, draw when eq) 5 = SRC_CLR = CLR_CMP_CLR_SRC (CMP_NEQ_COLOR, draw when neq) 6 = (reserved) 7 = SRC_CLR = CLR_CMP_CLR_SRC (CMP_EQ_FLIP, flip using expanded SRC_FRGD_CLR as flip mask when eq) (Reserved) 7: 3 CLR_CMP_FCN_DST 10: 8 Color comparison function (Mnemonic, action): 0 = False (CMP_FALSE, always draw) 1 = True (CMP_TRUE, never draw) 2-3 = (reserved) 4 = DST_CLR != CLR_CMP_CLR_DST (CMP_NEQ_COLOR, draw when eq) 5 = DST_CLR = CLR_CMP_CLR_DST (CMP_EQ_COLOR, draw when neq) 6-7 = (reserved) (Reserved) 23: 11 CLR_CMP_SRC 25: 24 Defines source for color keying: 0 = Destination 1 = Source 2 = Src and Dst 3 = reserved (Reserved) 31: 26 Write to RB2D_CLRCMP_CNTL 0=False (always draw) 1=True (never draw) 4=SRC_CLR !=CLR_CMP_CLR_SRC (draw on eq) 5=SRC_CLR = CLR_CMP_CLR_SRC (draw on neq) 7=SRC_CLR = CLR_CMP_CLR_SRC (flip on eq)
CLR_CMP_FCN_DST	10:8	0x0	0=False (always draw) 1=True (never draw) 4=DST_CLR !=CLR_CMP_CLR_DST (draw on eq) 5=DST_CLR = CLR_CMP_CLR_DST (draw on neq)
CLR_CMP_SRC	25:24	0x0	0=Destination 1=Source 2=Src and Dst

[ R/W] (MM: 5\_70)

CLR_CMP_CLR_SRC - W - 32 bits - [MMReg:0x15C4]			
Field Name	Bits	Default	Description
CLR_CMP_CLR_SRC	31:0	0x0	Color comparison color of source Write to RB2D_CLRCMP_CLR_SRC

Color comparison color of source Write to RB2D\_CLRCMP\_CLR\_SRC

<b>CLR_CMP_CLR_DST - W - 32 bits - [MMReg:0x15C8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CLR_CMP_CLR_DST	31:0	0x0	Color comparison color of destination Write to RB2D_CLRCMP_CLR_DST

Color comparison color of destination Write to RB2D\_CLRCMP\_CLR\_DST

<b>CLR_CMP_MSK - W - 32 bits - [MMReg:0x15CC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CLR_CMP_MSK	31:0	0x0	Color comparison color Write to RB2D_CLRCMP_MSK DEFAULT_PITCH_OFFSET[ W/R]

No description available for this register.

<b>DP_SRC_FRGD_CLR - RW - 32 bits - [MMReg:0x15D8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DP_SRC_FRGD_CLR	31:0	0x0	Foreground color. When color compare src eq flip is enabled, a '1' in bit location n means enable flipping on bit n. Write to E2_SRC_FRGD_CLR, And write to RB2D_CLRCMP_FLIPE

No description available for this register.

<b>DP_SRC_BKGD_CLR - RW - 32 bits - [MMReg:0x15DC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DP_SRC_BKGD_CLR	31:0	0x0	Background color. Write to E2_SRC_BKGD_CLR

Background color. Write to E2\_SRC\_BKGD\_CLR

<b>DST_LINE_START - RW - 32 bits - [MMReg:0x1600]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DST_START_X	13:0	0x0	Start X
DST_START_Y	29:16	0x0	Start Y Write 13: 0 to E2_LINE_START_X; Write 29: 16 to E2_LINE_START_Y; Write 0 to E2_LINE_PATCOUNT

No description available for this register.

<b>DST_LINE_END - RW - 32 bits - [MMReg:0x1604]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DST_END_X	13:0	0x0	End X
DST_END_Y	29:16	0x0	End Y Write 15: 0 to E2_LINE_END_X; Write 31: 16 to E2_LINE_END_Y; signal line_start; then copy E2_LINE_END_X into E2_LINE_START_X and E2_LINE_END_Y into E2_LINE_START_Y.

No description available for this register.

<b>DST_LINE_PATCOUNT - RW - 32 bits - [MMReg:0x1608]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
LINE_PATCOUNT	4:0	0x0	Line pattern counter Write 4: 0 to E2_LINE_PATCOUNT. When DST_LINE_START register is written into the line pattern counter is reset to 0. If a non-zero starting value is desired, this register must be written in after writing to DST_LINE_START register. BRUSH_Y_X [ W/R] (MM: 5_1D)

No description available for this register.

<b>SC_LEFT - RW - 32 bits - [MMReg:0x1640]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SC_LEFT	13:0	0x0	Range -8192 to 8191.

Range -8192 to 8191.

<b>SC_RIGHT - RW - 32 bits - [MMReg:0x1644]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SC_RIGHT	13:0	0x0	Range -8192 to 8191.

Range -8192 to 8191.

<b>SC_TOP - RW - 32 bits - [MMReg:0x1648]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SC_TOP	13:0	0x0	Range -8192 to 8191. (Reserved) Write 23: 16 to E2_DST_SCISSOR_TOP, Write 13: 0 to E2_DST_SCISSOR_LEFT

Range -8192 to 8191. (Reserved) Write 23: 16 to E2\_DST\_SCISSOR\_TOP, Write 13: 0 to E2\_DST\_SCISSOR\_LEFT

<b>SC_BOTTOM - RW - 32 bits - [MMReg:0x164C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SC_BOTTOM	13:0	0x0	Range -8192 to 8191. (Reserved) Write 23: 16 to E2_SRC_SCISSOR_BOTTOM, Write 13: 0 to E2_SRC_SCISSOR_RIGHT

Range -8192 to 8191. (Reserved) Write 23: 16 to E2\_SRC\_SCISSOR\_BOTTOM, Write 13: 0 to E2\_SRC\_SCISSOR\_RIGHT

<b>SRC_SC_RIGHT - RW - 32 bits - [MMReg:0x1654]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SC_RIGHT	13:0	0x0	Range -8192 to 8191.

[ R/W] (MM: 5\_95)

<b>SRC_SC_BOTTOM - RW - 32 bits - [MMReg:0x165C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SC_BOTTOM	13:0	0x0	Range -8192 to 8191. (Reserved) Write 23: 16 to E2_SRC_SCISSOR_BOTTOM, Write 13: 0 to E2_SRC_SCISSOR_RIGHT

[ R/W] (MM: 5\_97)

DP_CNTL - RW - 32 bits - [MMReg:0x16C0]			
Field Name	Bits	Default	Description
DST_X_DIR  <i>(mirror of DP_CNTL_XDIR_YDIR_YMAJOR:DST_X_DIR)</i>	0	0x0	Destination X0 direction 0 = right to left 1 = left to right Reserved (Must be unused ---. Used by parser to set only xdir/ydir of blits) Write 31 to E2_CNTL_DIRECTION bit 1, Write bit 15 to E2_CNTL_DIRECTION bit 0 0=right to left 1=left to right
DST_Y_DIR  <i>(mirror of DP_CNTL_XDIR_YDIR_YMAJOR:DST_Y_DIR)</i>	1	0x0	1 Destination Y direction 0 = bottom to top 1 = top to bottom This bit is written during setup engine initiated operations. Note that this bit is assumed to be '1' for all triangles. This bit is set to '1' by a GUI_MASTER_CNTL write DST_TILE 4: 3 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) 3: tiled and microtiled Write 0: 1 to E2_CNTL_DIRECTION and 4: 3 to E2_DST_TILE 0=bottom to top 1=top to bottom
DST_TILE  <i>(mirror of DST_TILE:DST_TILE)</i>	4:3	0x0	

[ R/W] (MM: 5\_B0)

DP_DATATYPE - RW - 32 bits - [MMReg:0x16C4]			
Field Name	Bits	Default	Description
DP_DST_DATATYPE	3:0	0x0	in DP_DATATYPE 0=RESERVED 1=RESERVED 2=8 bpp pseudocolor 3=16 bpp aRGB 1555 4=16 bpp RGB 565 5=RESERVED 6=32 aRGB 8888

DP_BRUSH_DATATYPE	11:8	0x0	0=8X8 mono pattern (expanded to frgd, bkgd) 1=8X8 mono pattern (expanded to frgd, leave_alone) 2=RESERVED 3=RESERVED 4=RESERVED 5=RESERVED 6=32X1 mono pattern for lines (expanded to frgd, bkgd) 7=32X1 mono pattern for lines (expanded to frgd,leave_alone) 8=RESERVED 9=RESERVED 10=8X8 color (pixel type same as DST) 11=RESERVED 12=RESERVED 13=solid color for blits (use frgd) 14=solid color for lines (use frgd) 15=solid color for blits (use frgd)
DP_SRC_DATATYPE	18:16	0x0	0=mono (expanded to frgd, bkgd) 1=mono (expanded to frgd, leave_alone) 2=RESERVED 3=color (pixel type same as DST)=3 4=RESERVED 5=8bpp, use clut to translate 6=32bpp, use clut to translate 7=Obuffer(64 bit in, 32 bit out)
DP_BYTE_PIX_ORDER	30	0x0	0=pixel order from MSBit to LSBit 1=pixel order from LSBit to MSBit

[ R/W] (MM: 5\_B1)

DP_MIX - RW - 32 bits - [MMReg:0x16C8]			
Field Name	Bits	Default	Description
DP_SRC_SOURCE	10:8	0x0	2=loaded from memory (rectangular trajectory) 3=loaded thru hostdata (linear trajectory) 4=loaded thru hosdata (linear trajectory & byte-aligned)
DP_ROP3	23:16	0x0	Windows 3.1 ROP3 code. Ternary Raster Operations 0=ROP3 function

[ R/W] (MM: 5\_B2) (Reserved) 7: 0 DP\_SRC\_SOURCE 10: 8 Src source: 2 = loaded from memory (rectangular trajectory) 3 = loaded thru hostdata (linear trajectory) 4 = loaded thru hostdata (linear trajectory & byte-aligned) Note that during 3D/Scaler Operations (whenever SCALE\_3D\_FCN is non-zero) the DP\_SRC\_SOURCE field is ignored and data is always loaded from the 3D/Scaler pipeline

DP_WRITE_MSK - W - 32 bits - [MMReg:0x16CC]			
Field Name	Bits	Default	Description
DP_WRITE_MSK	31:0	0x0	Write mask Write to RB2D_WRITEMASK

Write mask Write to RB2D\_WRITEMASK

DEFAULT_SC_BOTTOM_RIGHT - RW - 32 bits - [MMReg:0x16E8]			
Field Name	Bits	Default	Description
DEFAULT_SC_RIGHT	13:0	0x0	Range -8192 to 8191.
DEFAULT_SC_BOTTOM	29:16	0x0	Range -8192 to 8191. (Reserved) 31: 10 Write 13: 0 to E2_DEFAULT_SCISSOR_RIGHT Write 29: 16 to E2_DEFAULT_SCISSOR_BOTTOM

[ R/W] (MM: 5\_BA)

SC_TOP_LEFT - W - 32 bits - [MMReg:0x16EC]			
Field Name	Bits	Default	Description
SC_LEFT <i>(mirror of SC_LEFT:SC_LEFT)</i>	13:0	0x0	Range -8192 to 8191.
SC_TOP <i>(mirror of SC_TOP:SC_TOP)</i>	29:16	0x0	Range -8192 to 8191. (Reserved) Write 23: 16 to E2_DST_SCISSOR_TOP, Write 13: 0 to E2_DST_SCISSOR_LEFT

No description available for this register.

SC_BOTTOM_RIGHT - W - 32 bits - [MMReg:0x16F0]			
Field Name	Bits	Default	Description
SC_RIGHT <i>(mirror of SC_RIGHT:SC_RIGHT)</i>	13:0	0x0	Range -8192 to 8191.
SC_BOTTOM <i>(mirror of SC_BOTTOM:SC_BOTTOM)</i>	29:16	0x0	Range -8192 to 8191. (Reserved) Write 23: 16 to E2_SRC_SCISSOR_BOTTOM, Write 13: 0 to E2_SRC_SCISSOR_RIGHT

(aliased to SC\_BOTTOM, SC\_RIGHT) [ W] (MM: 5\_BC)

SRC_SC_BOTTOM_RIGHT - W - 32 bits - [MMReg:0x16F4]			
Field Name	Bits	Default	Description
SC_RIGHT <i>(mirror of SRC_SC_RIGHT:SC_RIGHT)</i>	13:0	0x0	Range -8192 to 8191.
SC_BOTTOM <i>(mirror of SRC_SC_BOTTOM:SC_BOTTOM)</i>	29:16	0x0	Range -8192 to 8191. (Reserved) Write 23: 16 to E2_SRC_SCISSOR_BOTTOM, Write 13: 0 to E2_SRC_SCISSOR_RIGHT

(aliased to SRC\_SC\_BOTTOM, SRC\_SC\_RIGHT) [ W ] (MM: 5\_BD)

DST_TILE - RW - 32 bits - [MMReg:0x1700]			
Field Name	Bits	Default	Description
DST_TILE	1:0	0x0	

0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) 2: microtiled 3: tiled and microtiled Write 9: 0 to E2\_DST\_TILE DST\_PITCH\_OFFSET[ W/R]

SRC_TILE - RW - 32 bits - [MMReg:0x1704]			
Field Name	Bits	Default	Description
SRC_TILE	0	0x0	0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) Write 0 to E2_SRC_TILE SRC_PITCH_OFFSET[ W/R]

0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) Write 0 to E2\_SRC\_TILE SRC\_PITCH\_OFFSET[ W/R]

SRC_CLUT_ADDRESS - RW - 32 bits - [MMReg:0x1780]			
Field Name	Bits	Default	Description
SRC_CLUT_ADDRESS	7:0	0x0	to E2_SRC_CLUT_ADDRESS

to E2\_SRC\_CLUT\_ADDRESS

SRC_CLUT_DATA - W - 32 bits - [MMReg:0x1784]			
Field Name	Bits	Default	Description
SRC_CLUT_DATA	31:0	0x0	CLUT data. Read

CLUT data. Read

SRC_CLUT_DATA_RD - R - 32 bits - [MMReg:0x1788]			
Field Name	Bits	Default	Description
SRC_CLUT_DATA	31:0	0x0	CLUT data. Read

No description available for this register.

HOST_DATA0 - RW - 32 bits - [MMReg:0x17C0]			
Field Name	Bits	Default	Description
HOST_DATA	31:0	0x0	

No description available for this register.

HOST_DATA1 - W - 32 bits - [MMReg:0x17C4]			
Field Name	Bits	Default	Description
HOST_DATA <i>(mirror of HOST_DATA0:HOST_DATA)</i>	31:0	0x0	

No description available for this register.

HOST_DATA2 - W - 32 bits - [MMReg:0x17C8]			
Field Name	Bits	Default	Description
HOST_DATA <i>(mirror of HOST_DATA0:HOST_DATA)</i>	31:0	0x0	

No description available for this register.

HOST_DATA3 - W - 32 bits - [MMReg:0x17CC]			
Field Name	Bits	Default	Description
HOST_DATA <i>(mirror of HOST_DATA0:HOST_DATA)</i>	31:0	0x0	

No description available for this register.

HOST_DATA4 - W - 32 bits - [MMReg:0x17D0]			
Field Name	Bits	Default	Description
HOST_DATA <i>(mirror of HOST_DATA0:HOST_DATA)</i>	31:0	0x0	

No description available for this register.

HOST_DATA5 - W - 32 bits - [MMReg:0x17D4]			
Field Name	Bits	Default	Description
HOST_DATA <i>(mirror of HOST_DATA0:HOST_DATA)</i>	31:0	0x0	

No description available for this register.

HOST_DATA6 - W - 32 bits - [MMReg:0x17D8]			
Field Name	Bits	Default	Description
HOST_DATA <i>(mirror of HOST_DATA0:HOST_DATA)</i>	31:0	0x0	

No description available for this register.

HOST_DATA7 - W - 32 bits - [MMReg:0x17DC]			
Field Name	Bits	Default	Description
HOST_DATA <i>(mirror of HOST_DATA0:HOST_DATA)</i>	31:0	0x0	

No description available for this register.

HOST_DATA_LAST - W - 32 bits - [MMReg:0x17E0]			
Field Name	Bits	Default	Description
HOST_DATA_LAST <i>(mirror of HOST_DATA0:HOST_DATA)</i>	31:0	0x0	Host Data Last. This register is here for R128 compatibility. Write to E2_HOST_DATA

No description available for this register.

DP_XOP - W - 32 bits - [MMReg:0x17F8]			
Field Name	Bits	Default	Description
XOP_A	7:0	0x0	Depends on XOP selected by XOP_OP
XOP_B	15:8	0x0	Depends on XOP selected by XOP_OP
XOP_C	23:16	0x0	Depends on XOP selected by XOP_OP
XOP_OP	25:24	0x0	Extended operations code, overrides ROP 0 - Normal 1 - D3D/OpenGL blend 2 - Alpha blend (32-bit only) (Reserved) 31: 26 Write to RB2D_XOP

[ R/W] (MM: 0x0244)

DEFAULT_PITCH_OFFSET - RW - 32 bits - [MMReg:0x16E0]			
Field Name	Bits	Default	Description
DEFAULT_OFFSET	21:0	0x0	Default Offset in Units of 1KB, 0 to (4GB-1KB). When a write to this register occurs, bits 9: 0 of default offset will be set to 0.

DEFAULT_PITCH	29:22	0x0	Pitch in units of 64 bytes, 0 to 16320 bytes across. DEFAULT_TILE 31: 30 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) 2: microtiled(destination only) 3: tiled and microtiled(destination only) Write bits 31: 30 to E2_DEFAULT_TILE, 29: 22 to E2_DEFAULT_PITCH and 21: 0 to E2_DEFAULT_OFFSET
DEFAULT_TILE	31:30	0x0	

No description available for this register.

## 2.19 RenderBackend2D Registers

### Render Backend 2D Control Registers.

RB2D_ROP - R - 32 bits - [MMReg:0x3400]			
Field Name	Bits	Default	Description
ROP	23:16	0x0	3D ROP, ROP2 code for 3D fragments. This value is replicated into 2 nibbles to form the equivalent ROP3 code to control the ROP3 logic.

ROP control register , Windows 3.1 ROP code.

RB2D_CLRCMP_SRC - R - 32 bits - [MMReg:0x3408]			
Field Name	Bits	Default	Description
CLRCMP_SRC	31:0	0x0	Color Compare Source , Comparison color for source. The format of this color is based on the 2D destination data format.

Color Compare Source , Comparison color for source.

RB2D_CLRCMP_DST - R - 32 bits - [MMReg:0x340C]			
Field Name	Bits	Default	Description
CLRCMP_DST	31:0	0x0	Color Compare Dest , Comparison color for destination. The format of this color is based on the 2D destination data format.

Color Compare Dest , Comparison color for destination.

RB2D_CLRCMP_FLIPE - R - 32 bits - [MMReg:0x3410]			
Field Name	Bits	Default	Description
CLRCMP_FLIPE	31:0	0x0	Color Compare Flip, This shadows E2_SRC_FRGD_CLR and is written via the DP_SRC_FRGD_CLR register location. This is the foreground color. When RB2D_CLRCMP_CNTL.FCN_SRC = 7, a '1' in bit location n means enable flipping on bit n.

Color Compare Flip, Color Compare flip register.

<b>RB2D_CLRCMP_CNTL - R - 32 bits - [MMReg:0x3414]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
FCN_SRC	2:0	0x0	Color Compare Source Function, Specifies the function to perform on the source color compare. 0=False (cmp_false, always draw) 1=True (cmp_true, never draw) 2=RESERVED 3=RESERVED 4=SRC == CLRCMP_SRC (do not draw if equal) 5=SRC != CLRCMP_SRC (draw if equal) 6=RESERVED 7=SRC == CLRCMP_SRC and FLIP
FCN_DST	10:8	0x0	Color Compare Destination Function, Specifies the function to perform on the source color compare. 0=False (cmp_false, always draw) 1=True (cmp_true, never draw) 2=RESERVED 3=RESERVED 4=SRC == CLRCMP_SRC (do not draw if equal) 5=SRC != CLRCMP_SRC (draw if equal) 6=RESERVED 7=RESERVED
SRC	25:24	0x0	Color Compare Function Select, Selects which color compare results to use in the final compare results. 0=Destination 1=Source 2=Src AND Dst 3=Hilite

Color Compare Control, Controls the color compare logic.

<b>RB2D_CLRCMP_MSK - R - 32 bits - [MMReg:0x3418]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CLRCMP_MSK	31:0	0x0	Color Compare Mask, This is ANDed with source and destination before compare.

Color Compare Mask, This is ANDed with source and destination before compare.

RB2D_WRITEMASK - R - 32 bits - [MMReg:0x341C]			
Field Name	Bits	Default	Description
WRITEMASK	31:0	0x0	Write Mask, This is a bit mask that should be set with byte alignment for better performance.

Write Mask, This is a bit mask.

RB2D_DATATYPE - R - 32 bits - [MMReg:0x3420]			
Field Name	Bits	Default	Description
DP_DST_DATATYPE	3:0	0x0	2D Destination Datatype, Shadow of the E2_DST_DATATYPE field in 2D pipe. Written via DP_DATATYPE register address in the 2D pipe.
DP_BRUSH_DATATYPE	11:8	0x0	Brush Datatype, Shadow of the E2_DST_DATATYPE field in 2D pipe. Written via DP_DATATYPE register address in the 2D pipe.

2D Data Formats, Denotes format of 2D destination and brush.

RB2D_GUI_MASTER_CNTL - R - 32 bits - [MMReg:0x3424]			
Field Name	Bits	Default	Description
GMC_BRUSH_DATATYPE <i>(mirror of RB2D_DATATYPE:DP_BRUSH_DATATYPE)</i>	7:4	0x0	GMC_BRUSH_DATATYPE shadow, Shadow of GMC_BRUSH_DATATYPE field of DP_GUI_MASTER_CNTL register in 2D pipe. Value of this field is loaded into RB2D_DATATYPE.DP_BRUSH_DATATYPE.
GMC_DST_DATATYPE <i>(mirror of RB2D_DATATYPE:DP_DST_DATATYPE)</i>	11:8	0x0	GMC_DST_DATATYPE shadow, Shadow of GMC_DST_DATATYPE field of DP_GUI_MASTER_CNTL register in 2D pipe. Value of this field is loaded into RB2D_DATATYPE.DP_DST_DATATYPE.
GMC_ROP <i>(mirror of RB2D_ROP:ROP)</i>	23:16	0x0	
GMC_CLR_CMP_FCN_DIS	28	0x0	GMC_CLR_CMP_FCN_DIS shadow, Clear RB2D_CLRCMP_CNTL if set, else does nothing. Shadow of GMC_CLR_CMP_FCN_DIS field of DP_GUI_MASTER_CNTL register in 2D pipe.
GMC_WR_MSK_DIS	30	0x0	GMC_WR_MASK_DIS shadow, Sets RB2D_WRITEMASK to 0xFFFFFFFF if set, else does nothing. Shadow of GMC_WR_MASK_DIS field of DP_GUI_MASTER_CNTL register in 2D pipe.

GUI Master Control, Master control register for 2D operations

## 2.20 RasterEngineRegisters Registers

Basic raster engine description.

RE_SOLID_COLOR - RW - 32 bits - [MMReg:0x1C1C] [MMReg:0x261C]			
Field Name	Bits	Default	Description
SOLID_COLOR	31:0	0x0	32-bit color used for solid shading. Organized as 8: 8: 8: 8 ARGB.

[ R/W] (MM: X\_XX)

RE_WIDTH_HEIGHT - RW - 32 bits - [MMReg:0x1C44] [MMReg:0x2644]			
Field Name	Bits	Default	Description
WIDTH	10:0	0x0	Width-1 of primary scissor plane
HEIGHT	26:16	0x0	Height-1 of primary scissor plane

[ R/W] (MM: X\_XX)

RE_MISC - RW - 32 bits - [MMReg:0x1CC4] [MMReg:0x26C4]			
Field Name	Bits	Default	Description
STIPPLE_X_OFFSET	4:0	0x0	X offset to apply to X index of stipple RAM
STIPPLE_Y_OFFSET	12:8	0x0	Y offset to apply to Y index of stipple RAM
STIPPLE_BIT_ORDER	16	0x0	0 : Little Bit Order (x= 0 on the right of stipple data) 1 : Big Bit Order (x = 0 on the left of stipple data) 0=Little Bit Order 1=Big Bit Order

No description available for this register.

RE_STIPPLE_ADDR - RW - 32 bits - [MMReg:0x1CC8] [MMReg:0x26C8]			
Field Name	Bits	Default	Description
STIPPLE_ADDR	4:0	0x0	5-bit index into the 32 x 32 RAM. It is self incrementing with every access to RE_STIPPLE_DATA.

No description available for this register.

RE_STIPPLE_DATA - RW - 32 bits - [MMReg:0x1CCC] [MMReg:0x26CC]			
Field Name	Bits	Default	Description
STIPPLE_DATA	31:0	0x0	Row of stipple data indexed by RE_STIPPLE_ADDR.

[ R/W] (MM: X\_XX)

RE_LINE_PATTERN - RW - 32 bits - [MMReg:0x1CD0] [MMReg:0x26D0]			
Field Name	Bits	Default	Description
LINE_PATTERN	15:0	0x0	0 : Don't Draw Pixel 1 : Draw Pixel
REPEAT_COUNT	23:16	0x0	16 Pattern Repeat Count 0x00 : 256x 0x01 : 1x 0x02 : 2x : 0xFF : 255x
PATTERN_START	27:24	0x0	Indicates starting state of pattern pointer 0x0 : Points to pattern bit 0 0x1 : Points to pattern bit 1 : 0xF : Points to pattern bit 15
PATTERN_BIT_ORDER	28	0x0	0 : Little Bit Order (Pointer = 0 is on the right of the pattern) 1 : Big Bit Order (Pointer = 0 is on the left of the pattern) 0=Little Bit Order 1=Big Bit Order
AUTO_RESET_ENABLE	29	0x0	0 : Do not reset the counter and pointer at EndOfLinePattern 1 : Automatically reset the counter and pointer at EndOfLinePattern 0=disable 1=enable

[ R/W] (MM: X\_XX)

RE_LINE_STATE - RW - 32 bits - [MMReg:0x1CD4] [MMReg:0x26D4]			
Field Name	Bits	Default	Description
CURRENT_PTR	3:0	0x0	Indicates current state of pattern pointer (can be set w/ a register write) 0x0 : Points to pattern bit 0 0x1 : Points to pattern bit 1 : 0xF : Points to pattern bit 15 At the end of a line this value will reset to Pattern Start if EndOfPacket is set by the setup engine and AUTO_RESET_ENABLE is on.
CURRENT_COUNT	15:8	0x0	Current state of the repeat counter (can be set w/ a register write). At the end of a line this value will reset to 1 if EndOfLinePattern is set by the setup engine and AUTO_RESET_ENABLE is on.

[ R/W] (MM: X\_XX)

<b>RE_SCISSOR_TL_0 - RW - 32 bits - [MMReg:0x1CD8] [MMReg:0x26D8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
X_LEFT	10:0	0x0	Positive Integer X value of left scissor plane
Y_TOP	26:16	0x0	Positive Integer Y value of top scissor plane

[ R/W] (MM: X\_XX)

<b>RE_SCISSOR_BR_0 - RW - 32 bits - [MMReg:0x1CDC] [MMReg:0x26DC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
X_RIGHT	10:0	0x0	Positive Integer X value of right scissor plane
Y_BOTTOM	26:16	0x0	Positive Y value of bottom scissor plane

No description available for this register.

<b>RE_SCISSOR_TL_1 - RW - 32 bits - [MMReg:0x1CE0] [MMReg:0x26E0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
X_LEFT	10:0	0x0	Positive Integer X value of left scissor plane
Y_TOP	26:16	0x0	Positive Integer Y value of top scissor plane

[ R/W] (MM: X\_XX)

<b>RE_SCISSOR_BR_1 - RW - 32 bits - [MMReg:0x1CE4] [MMReg:0x26E4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
X_RIGHT	10:0	0x0	Positive Integer X value of right scissor plane
Y_BOTTOM	26:16	0x0	Positive Y value of bottom scissor plane

No description available for this register.

<b>RE_SCISSOR_TL_2 - RW - 32 bits - [MMReg:0x1CE8] [MMReg:0x26E8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
X_LEFT	10:0	0x0	Positive Integer X value of left scissor plane

Y_TOP	26:16	0x0	Positive Integer Y value of top scissor plane
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[ R/W] (MM: X\_XX)

RE_SCISSOR_BR_2 - RW - 32 bits - [MMReg:0x1CEC] [MMReg:0x26EC]			
Field Name	Bits	Default	Description
X_RIGHT	10:0	0x0	Positive Integer X value of right scissor plane
Y_BOTTOM	26:16	0x0	Positive Y value of bottom scissor plane

No description available for this register.

## 2.21 AGP Registers

### AGP Interface Control Registers

## 2.22 VGA Registers

The complete set of Video Graphics Accelerator Registers

GENMO_WT - W - 8 bits - VGA_IO:0x3C2			
Field Name	Bits	Default	Description
GENMO_MONO_ADDRESS_B (BIF)	0	0x0	VGA addressing mode. 0=Monochrome emulation, regs at 0x3Bx 1=Color/Graphic emulation, regs at 0x3Dx
VGA_RAM_EN (BIF)	1	0x0	Enables/Disables CPU access to video RAM at VGA aperture. 0=Disable 1=Enable
VGA_CKSEL (DISPLAY)	3:2	0x0	Selects pixel clock frequency to use in VGA modes. Used when CRTC_GEN_CNTL.CRTC_EXT_DISP_EN=0. See CLOCK_CNTL_INDEX.PPLL_DIV_SEL for non-VGA mode pixel clock selection. 0=25.1744MHz (640 Pels) 1=28.3212MHz (720 Pels) 2=Reserved 3=Reserved
ODD_EVEN_MD_PGSEL (HDP)	5	0x0	This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled. Used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory. 0=Selects odd (high) memory locations 1=Selects even (low) memory locations
VGA_HSYNC_POL (DISPLAY)	6	0x0	Determines polarity of horizontal sync (HSYNC) for VGA modes. 0 = HSYNC pulse active high 1 = HSYNC pulse active low The covention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes.
VGA_VSYNC_POL (DISPLAY)	7	0x0	Determines polarity of vertical sync (VSYNC) for VGA modes. 0 = VSYNC pulse active high 1 = VSYNC pulse active low The covention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes.

Miscellaneous Output Register (Write)

GENMO_RD - R - 8 bits - VGA_IO:0x3CC			
Field Name	Bits	Default	Description
GENMO_MONO_ADDRESS_B  <i>(mirror of GENMO_WT:GENMO_MONO_ADDRESS_B)</i>  (BIF)	0	0x0	VGA addressing mode.
VGA_RAM_EN  <i>(mirror of GENMO_WT:VGA_RAM_EN)</i>  (BIF)	1	0x0	Enables/Disables CPU access to video RAM at VGA aperture.
VGA_CKSEL  <i>(mirror of GENMO_WT:VGA_CKSEL)</i>  (DISPLAY)	3:2	0x0	Selects pixel clock frequency to use.
ODD_EVEN_MD_PGSEL  <i>(mirror of GENMO_WT:ODD_EVEN_MD_PGSEL)</i>  (HDP)	5	0x0	This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled. Used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory.
VGA_HSYNC_POL  <i>(mirror of GENMO_WT:VGA_HSYNC_POL)</i>  (DISPLAY)	6	0x0	Determines polarity of horizontal sync (HSYNC) for VGA modes. 0 = HSYNC pulse active high 1 = HSYNC pulse active low The covention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes.
VGA_VSYNC_POL  <i>(mirror of GENMO_WT:VGA_VSYNC_POL)</i>  (DISPLAY)	7	0x0	Determines polarity of vertical sync (VSYNC) for VGA modes. 0 = VSYNC pulse active high 1 = VSYNC pulse active low The covention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes.

Miscellaneous Output Register (Read)

GENFC_WT - W - 8 bits - [VGA_IO:0x3BA] [VGA_IO:0x3DA]			
Field Name	Bits	Default	Description
VSYNC_SEL_W	3	0x0	Vertical sync select (write). 0=Normal vertical sync 1=Sync is 'vertical sync' ORed with 'vertical display enable'

Feature Control Register (Read)

GENFC_RD - R - 8 bits - VGA_IO:0x3CA			
Field Name	Bits	Default	Description
VSYNC_SEL_R <i>(mirror of GENFC_WT:VSYNC_SEL_W)</i>	3	0x0	Vertical sync select (read). 0=Normal vertical sync 1=Sync is 'vertical sync' ORed with 'vertical display enable'

Feature Control Register (Read)

GENS0 - R - 8 bits - VGA_IO:0x3C2			
Field Name	Bits	Default	Description
SENSE_SWITCH	4	0x0	DAC comparator read back. Used for monitor detection. Mirror of DAC_CMP_OUTPUT@DAC_CNTL. See description there.
CRT_INTR	7	0x0	CRT Interrupt: 0=Vertical retrace interrupt is cleared 1=Vertical retrace interrupt is pending

Input Status 0 Register

GENS1 - R - 8 bits - [VGA_IO:0x3BA] [VGA_IO:0x3DA]			
Field Name	Bits	Default	Description
NO_DISPLAY	0	0x0	Display enable. 0=Enable 1=Disable
VGA_VSTATUS	3	0x0	Vertical Retrace Status. 0=Vertical retrace not active 1=Vertical retrace active

PIXEL_READ_BACK	5:4	0x0	Diagnostic bits 0, 1 respectively. These two bits are connected to two of the eight colour outputs (P7:P0) of the attribute controller. Connections are controlled by ATTR12(5,4) as follows: 0=P2,P0 1=P5,P4 2=P3,P1 3=P7,P6
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Input Status 1 Register

<b>MEM_VGA_WP_SEL - RW - 32 bits - [IOReg,MMReg:0x38]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
MEM_VGA_WPS0	11:0	0x0	Write page pointer for lower 32 KByte aperture into 128 MByte video memory.
MEM_VGA_WPS1	27:16	0x0	Write page pointer for upper 32 KByte aperture into 128 MByte video memory.

Two write page pointers used for the two small 32K apertures at 0xA000 and 0xA800. Pages are selectable only on 32K boundaries.

<b>MEM_VGA_RP_SEL - RW - 32 bits - [IOReg,MMReg:0x3C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
MEM_VGA_RPS0	11:0	0x0	Read page pointer for lower 32 KByte aperture into 128 MByte video memory.
MEM_VGA_RPS1	27:16	0x0	Read page pointer for upper 32 KByte aperture into 128 MByte video memory.

Two read page pointers used for the two small 32K apertures at 0xA000 and 0xA800. Pages are selectable only on 32K boundaries.

## 2.23 CRTC Registers

### CRT Control Registers

CRTC8_IDX - RW - 8 bits - [VGA_IO:0x3B4] [VGA_IO:0x3D4]			
Field Name	Bits	Default	Description
VCRTC_IDX  <i>(mirror bits 0:5 of CRTC_EXT_CNTL:VCRTC_IDX_MASTER)</i>  (HDP) (DISPLAY)	5:0	0x0	This index points to one of the internal registers of the CRT controller (CRTC) at address 0x3?5, for the next CRTC read/write operation.

CRT Index Register

CRTC8_DATA - RW - 8 bits - [VGA_IO:0x3B5] [VGA_IO:0x3D5]			
Field Name	Bits	Default	Description
VCRTC_DATA  (HDP) (DISPLAY)	7:0	0x0	CRTC data indirect access

CRTC Data Register

CRT00 - RW - 8 bits - VGACRTIND:0x0			
Field Name	Bits	Default	Description
H_TOTAL  <i>(mirror bits 0:7 of CRTC_H_TOTAL_DISP:CRTC_H_TOTAL)</i>	7:0	0x0	These bits define the active horizontal display in a scan line, including the retrace period. The value is five less than the total number of displayed characters in a scan line.

Horizontal Total Register

**CRT01 - RW - 8 bits - VGACRTIND:0x1**

Field Name	Bits	Default	Description
H_DISP_END <i>(mirror bits 0:7 of CRTC_H_TOTAL_DISP:CRTC_H_DISP)</i>	7:0	0x0	These bits define the active horizontal display in a scan line. The value is one less than the total number of displayed characters in a scan line.

Horizontal Display Enable End Register

**CRT02 - RW - 8 bits - VGACRTIND:0x2**

Field Name	Bits	Default	Description
H_BLANK_START	7:0	0x0	These bits define the horizontal character count that represents the character count in the active display area plus the right border. In other words, the count is from the start of active display to the start of triggering of the H blanking pulse.

Start Horizontal Blanking Register

**CRT03 - RW - 8 bits - VGACRTIND:0x3**

Field Name	Bits	Default	Description
H_BLANK_END	4:0	0x0	H blanking bits 4-0 respectively. These are the five low-order bits (of six bits in total) of horizontal character count for triggering the end of the horizontal blanking pulse.
H_DE_SKEW	6:5	0x0	Display-enable skew: 0=0Skew 1=1Skew 2=2Skew 3=3Skew
CR10CR11_R_DIS_B	7	0x0	Comptibility Read: 0=WrtOnlyToCRT10-11 1=WrtRdToCRT10-11

End Horizontal Blanking Register

CRT04 - RW - 8 bits - VGACRTIND:0x4			
Field Name	Bits	Default	Description
H_SYNC_START <i>(mirror bits 0:7 of CRTC_H_SYNC_STRT_WID:CRTC_H_SYNC_STRT_CHAR)</i>	7:0	0x0	These bits define the horizontal character count at which the horizontal retrace pulse becomes active.

Start Horizontal Retrace Register

CRT05 - RW - 8 bits - VGACRTIND:0x5			
Field Name	Bits	Default	Description
H_SYNC_END <i>(mirror bits 0:4 of CRTC_H_SYNC_STRT_WID:CRTC_H_SYNC_WID)</i>	4:0	0x0	H Retrace Bits (these are the 5-bit result from the sum of CRT0 plus the width of the horizontal retrace pulse, in character clock units).
H_SYNC_SKEW	6:5	0x0	H Retrace Delay bits (these two bits skew the horizontal retrace pulse).
H_BLANK_END_B5	7	0x0	H blocking end bit 5 (this is the bit of the 6-bit character count for the H blanking end pulse). The other five low-order bits are CRT03[4:0].

End Horizontal Retrace Register

CRT06 - RW - 8 bits - VGACRTIND:0x6			
Field Name	Bits	Default	Description
V_TOTAL <i>(mirror bits 0:7 of CRTC_V_TOTAL_DISP:CRTC_V_TOTAL)</i>	7:0	0x0	These are the eight low-order bits of the 10-bit vertical total register. The 2 high-order bits are CRT07[5:0] in the CRTC overflow register. The value of this register represents the total number of H raster scans plus vertical retrace (active display, blanking), minus two scan lines.

Vertical Total Register

CRT07 - RW - 8 bits - VGACRTIND:0x7			
Field Name	Bits	Default	Description
V_TOTAL_B8 <i>(mirror bits 8:8 of CRTC_V_TOTAL_DISP:CRTC_V_TOTAL)</i>	0	0x0	V Total Bit 8 (CRT06). Bit 8 of 10 bit vertical count for V Total. For functional description see CRT06 register.
V_DISP_END_B8 <i>(mirror bits 8:8 of CRTC_V_TOTAL_DISP:CRTC_V_DISP)</i>	1	0x0	End V Display Bit 8 (CRT12). Bit 8 of 10-bit vertical count for V Display enable. For functional description see CRT12 register.
V_SYNC_START_B8 <i>(mirror bits 8:8 of CRTC_V_SYNC_STRT_WID:CRTC_V_SYNC_STRT)</i>	2	0x0	Start V Retrace Bit 8 (CRT10). Bit 8 of 10-bit vertical count for V Retrace start. For functional description see CRT10 register.
V_BLANK_START_B8	3	0x0	Start V Blanking Bit 8 (CRT15). Bit 8 of the 10-bit vertical count for V Blanking start. For functional description see CRT15 register.
LINE_CMP_B8 <i>(mirror bits 8:8 of CRTC_VLINE_CRNT_VLINE:CRTC_VLINE)</i>	4	0x0	Line compare bit 8 (CRT18). Bit 8 of the 10-bit vertical count for line compare. For functional description see CRT18 register.
V_TOTAL_B9 <i>(mirror bits 9:9 of CRTC_V_TOTAL_DISP:CRTC_V_TOTAL)</i>	5	0x0	V Total Bit 9 (CRT06). Bit 9 of 10-bit vertical count for V Total. For functional description see CRT06 register.
V_DISP_END_B9 <i>(mirror bits 9:9 of CRTC_V_TOTAL_DISP:CRTC_V_DISP)</i>	6	0x0	End V Display Bit 9 (CRT12). Bit 9 of 10-bit vertical count for V Display enable end (for functional description see CRT12 register).
V_SYNC_START_B9 <i>(mirror bits 9:9 of CRTC_V_SYNC_STRT_WID:CRTC_V_SYNC_STRT)</i>	7	0x0	Start V Retrace Bit (CRT10). Bit 9 of 10-bit vertical count for V Retrace start. For functional description see CRT10 register.

CRTC Overflow Register

CRT08 - RW - 8 bits - VGACRTIND:0x8			
Field Name	Bits	Default	Description
ROW_SCAN_START	4:0	0x0	Preset row scan bit 4:0. This register is used for software-controlled vertical scrolling in text or graphics modes. The value specifies the first line to be scanned after a V retrace (in the next frame). Each H Retrace pulse increments the counter by 1, up to the maximum scan line value programmed by CRT09, then the counter is cleared.
BYTE_PAN	6:5	0x0	Byte panning control bits 1 and 0 (respectively). Bits 6 and 5 extend the capability of byte panning (shifting) by up to three characters (for description H_PEL Panning register ATTR13).

Preset Row Scan Register

CRT09 - RW - 8 bits - VGACRTIND:0x9			
Field Name	Bits	Default	Description
MAX_ROW_SCAN	4:0	0x0	Maximum scan line bits. These bits define a value that is the actual number of scan line per character minus 1.
V_BLANK_START_B9	5	0x0	Start V Blanking bit 9 (CRT15). Bit 9 of 10-bit vertical count for line compare. For functional description see CRT18 register.
LINE_CMP_B9 <i>(mirror bits 9:9 of CRTC_VLINE_CRNT_VLINE:CRTC_VLINE)</i>	6	0x0	Line Compare Bit 9 (CRT18). Bit 9 of 10-bit vertical count for line compare. For functional description see CRT18 register.
DOUBLE_CHAR_HEIGHT	7	0x0	200/400 line scan. NOTE H/V display and blanking timings etc. (in CRT00-CRT06 registers) are not affected. 0=200LineScan 1=400LineScan

Maximum Scan Line Register

<b>CRT0A - RW - 8 bits - VGACRTIND:0xA</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CURSOR_START	4:0	0x0	Cursor start bits 4:0 (respectively). These bits define a value that is the starting scan line (on a character row) for the line cursor. The 5-bit value is equal to the actual number minus one. This value is used together with the Cursor End Bits CRT0B[4:0] to determine the height of the cursor. The cursor height in VGA does not wrap around (as in EGA) and is actually absent when the 'end' value is less than the 'start' value. In EGA when the 'end' value is less, the cursor is a full block cursor the same height as the character cell.
CURSOR_DISABLE	5	0x0	Cursor on/off. 0=on 1=off

Cursor Start Register

<b>CRT0B - RW - 8 bits - VGACRTIND:0xB</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CURSOR_END	4:0	0x0	Cursor End Bits 4-0, respectively.- These bits define the ending scan row (on a character line) for the line cursor. In EGA, this 5-bit value is equal to the actual number of lines plus one.- The cursor height in VGA does not wrap around (as in EGA) and is actually absent when the 'end' value is less than the 'start' value. In EGA when the 'end' value is less, the cursor is a full block cursor the same height as the character cell.
CURSOR_SKEW	6:5	0x0	Cursor Skew Bits 1 and 0, respectively.- These bits define the number of characters the cursor is to be shifted to the right (skewed) from the character pointed at by the cursor location (registers CRT0E and CRT0F), in VGA mode. Skew values when in EGA mode are enclosed in brackets.

Cursor End Register

CRT0C - RW - 8 bits - VGACRTIND:0xC			
Field Name	Bits	Default	Description
DISP_START  <i>(mirror bits 11:18 of CRTC_OFFSET:CRTC_OFFSET)</i>	7:0	0x0	SA bits 15:8-These are the eight high-order bits of the 16-bit display buffer start location. The low order bits are contained in CRT0D.-In split screen mode, CRT0C = CRT0D point to the starting location of screen A (top half.) The starting address for screen B is always zero.

Start Address (High Byte) Register

CRT0D - RW - 8 bits - VGACRTIND:0xD			
Field Name	Bits	Default	Description
DISP_START  <i>(mirror bits 3:10 of CRTC_OFFSET:CRTC_OFFSET)</i>	7:0	0x0	SA bits 7:0- These are the eight low-order bits of the 16-bit display buffer start location. The high-order bits are contained in CRT0C. - In split creen mode, CRT0C + CRT0D points to the starting location of screen A (top half.) The starting address for screen B is always zero.

Start Address (Low Byte) Register

CRT0E - RW - 8 bits - VGACRTIND:0xE			
Field Name	Bits	Default	Description
CURSOR_LOC_HI	7:0	0x0	CA bits 15:8- These are the eight high-order bits of the 16 bit cursor start address. The low-order CA bits are contained in CRT0F. This address is relative to the start of physical display memory address pointed to by CRT0C + CRT0D. In other words, if CRT0C + CRT0D is changed, the cursor still pints to the same character as before.

Cursor Location (High Byte) Register

CRT0F - RW - 8 bits - VGACRTIND:0xF			
Field Name	Bits	Default	Description
CURSOR_LOC_LO	7:0	0x0	CA bits 7:0- These are the eight low-order bits of the 16 bit cursor start address. The high-order CA bits are contained in CRT0E. This address is relative to the start of physical display memory address pointed to by CRT0C + CRT0D. In other words, if CRT0C + T0D is changed, the cursor still points to the same character as before

Cursor Location (Low Byte) Register

CRT10 - RW - 8 bits - VGACRTIND:0x10			
Field Name	Bits	Default	Description
V_SYNC_START  <i>(mirror bits 0:7 of CRTC_V_SYNC_STRT_WID:CRTC_V_SYNC_STRT)</i>	7:0	0x0	Bits CRT10[7:0] are the eight low-order bits of the 10-bit vertical retrace start count. The two high-order bits are CRT10[2:7], located in the CRTC overflow register.- These bits define the horizontal scan count that triggers the V retrace pulse.

Start Vertical Retrace Register

CRT11 - RW - 8 bits - VGACRTIND:0x11			
Field Name	Bits	Default	Description
V_SYNC_END  <i>(mirror bits 0:3 of CRTC_V_SYNC_STRT_WID:CRTC_V_SYNC_WID)</i>	3:0	0x0	V Retrace End Bits 3-0- Bits CRT11[0:3] define the horizontal scan count that triggers the end of the V Retrace pulse.
V_INTR_CLR	4	0x0	V Retrace Interrupt Set: 0=VRetraceIntCleared 1=Not Cleared
V_INTR_EN	5	0x0	V Retrace Interrupt Disabled: 0=VRetraceIntEna 1=Disable
SEL5_REFRESH_CYC	6	0x0	0=3 DRAM Refresh/Horz Line 1=5 DRAM Refresh/Horz Line
C0T7_WR_ONLY	7	0x0	Write Protect (CRT00-CRT06). All register bits except CRT07[4] are write protected. 0=EnaWrtToCRT00-07 1=C0T7B4WrtOnly

End Vertical Retrace Register

CRT12 - RW - 8 bits - VGACRTIND:0x12			
Field Name	Bits	Default	Description
V_DISP_END  <i>(mirror bits 0:7 of CRTC_V_TOTAL_DISP:CRTC_V_DISP)</i>	7:0	0x0	These are the eight low-order bits of the 10-bit register containing the horizontal scan count indicating where the active display on the screen should end. The high-order bits are CRT07 [1:6] in the CRT overflow register.

Vertical Display Enable End Register

CRT13 - RW - 8 bits - VGACRTIND:0x13			
Field Name	Bits	Default	Description
DISP_PITCH <i>(mirror bits 0:7 of CRTC_PITCH:CRTC_PITCH)</i>	7:0	0x0	- These bits define an offset value, equal to the logical line width of the screen (from the first character of the current line to the first character of the next line).- Memory organization is dependent on the video mode. Bit CRT17[6] selects byte or word mode. Bit CRT14[6], which overrides the byte/word mode setting, selects Double-Word mode when it is logical one.- The first character of the next line is specified by the start address (CRT0C + CRT0D) plus the offset. The offset for byte mode is 2x CRT13; for word mode, 4x; for double word mode 8x.

Offset Register

CRT14 - RW - 8 bits - VGACRTIND:0x14			
Field Name	Bits	Default	Description
UNDRLN_LOC (DISPLAY)	4:0	0x0	H Row Scan Bits 4-0.- These bits define the horizontal scan row, from the top of the characterline, that should be used for underlining. The 5-bit value is equal to the actual number minus one.
ADDR_CNT_BY4 (DISPLAY)	5	0x0	Count-by-4: 0=Char. Clock 1=CountBy4
DOUBLE_WORD (HDP) (DISPLAY)	6	0x0	Double-Word Mode: 0=Disable 1=DoubleWordMdEna

Underline Location Register

CRT15 - RW - 8 bits - VGACRTIND:0x15			
Field Name	Bits	Default	Description
V_BLANK_START	7:0	0x0	These are the eight low-order bits of the 10-bit vertical blanking start register. Bit 9 is CRT09[5]; bit 8 is CRT07[3]- The 10 bits specify the starting location of the vertical blanking pulse, in units of horizontal scan lines. The value is equal to the actual number of displayed lines minus one.

Start Vertical Blanking Register

CRT16 - RW - 8 bits - VGACRTIND:0x16			
Field Name	Bits	Default	Description
V_BLANK_END	7:0	0x0	These bits define the point at which to trigger the end of the vertical blanking pulse. The location is specified in units of horizontal scan lines.- The value to be stored in this register is the seven low-order bits of the sum of 'pulse width count' plus the content of Start Vertical Blanking register (CRT15) minus one.

End Vertical Blanking Register

CRT17 - RW - 8 bits - VGACRTIND:0x17			
Field Name	Bits	Default	Description
RA0_AS_A13B (DISPLAY)	0	0x0	Compatibility Mode:
RA1_AS_A14B (DISPLAY)	1	0x0	Select Row Scan Counter:
VCOUNT_BY2 (DISPLAY)	2	0x0	Vertical_by_2 NOTE: When bit 2 is logical one, other vertical register values should be adjusted as well (CRT06, CRT10, CRT12, CRT15, and CRT18).
ADDR_CNT_BY2 (DISPLAY)	3	0x0	Count_by_2: ENGINEERING NOTE: Bit can be written and read, but has no effect.
WRAP_A15TOA0 (DISPLAY)	5	0x0	Address Wrap: ENGINEERING NOTE: Bit can be written and read, but has no effect.
BYTE_MODE (HDP) (DISPLAY)	6	0x0	Byte/Word Mode: 0=WordMode 1=ByteMode
CRTC_SYNC_EN (DISPLAY)	7	0x0	H/V Retrace Enable: 0=Disable HVSynC 1=EnaHVSynC

CRT Mode Register

CRT18 - RW - 8 bits - VGACRTIND:0x18			
Field Name	Bits	Default	Description
LINE_CMP <i>(mirror bits 0:7 of CRTC_VLINE_CRNT_VLINE:CRTC_VLINE)</i>	7:0	0x0	- These bits are the eight low-order of the 10-bit line compare register. Bit 8 is CRT07[4], bit 9 is CRT09[6]. The value of this register is used to disable scrolling on a portion of the display screen, as when split screen is active. When the vertical counter reaches this value, the memory address and row scan counters are cleared.- The screen area above the line specified by the register is commonly called screen A. The screen below is screen B. Screen B cannot be scrolled, but it can panned only together with screen A, controlled by the PEL panning compatibility bit ATTR10[5]. (For a description of this control bit see ATTR10[5].)

Line Compare Register

CRT1E - R - 8 bits - VGACRTIND:0x1E			
Field Name	Bits	Default	Description
GRPH_DEC_RD1	1	0x0	This register is used to read back the graphics controller index decode.

Graphics Controller Index Decode Register

CRT1F - R - 8 bits - VGACRTIND:0x1F			
Field Name	Bits	Default	Description
GRPH_DEC_RD0	7:0	0x0	This register is used to read back the graphics controller index decode.

Graphics Controller Index Decode Register

CRT22 - R - 8 bits - VGACRTIND:0x22			
Field Name	Bits	Default	Description
GRPH_LATCH_DATA	7:0	0x0	This register is used to read the data in the Graphics Controller CPU data latches. The Graphics Controller Read Map Select register bits 0 and 1 determines which byte is read back.

RAM Data Latch Readback Register

## 2.24 CRTCSshadow Registers

### CRT Control Shadow Registers

CRT00_S - RW - 8 bits - VGACRTIND:0x40			
Field Name	Bits	Default	Description
H_TOTAL_S  <i>(mirror bits 0:7 of FP_CRTC_H_TOTAL_DISP:FP_CRTC_H_TO TAL)</i>	7:0	0x0	

No description available for this register.

CRT01_S - RW - 8 bits - VGACRTIND:0x41			
Field Name	Bits	Default	Description
H_DISP_END_S  <i>(mirror bits 0:7 of FP_CRTC_H_TOTAL_DISP:FP_CRTC_H_DIS P)</i>	7:0	0x0	

No description available for this register.

CRT02_S - RW - 8 bits - VGACRTIND:0x42			
Field Name	Bits	Default	Description
H_BLANK_START_S	7:0	0x0	

No description available for this register.

CRT03_S - RW - 8 bits - VGACRTIND:0x43			
Field Name	Bits	Default	Description
H_BLANK_END_S	4:0	0x0	

H_DE_SKEW_S	6:5	0x0	0=0Skew 1=1Skew 2=2Skew 3=3Skew
CR10CR11_R_DIS_B_M <i>(mirror of CRT03:CR10CR11_R_DIS_B)</i>	7	0x0	0=WrtOnlyToCRT10-11 1=WrtRdToCRT10-11

No description available for this register.

CRT04_S - RW - 8 bits - VGACRTIND:0x44			
Field Name	Bits	Default	Description
H_SYNC_START_S <i>(mirror bits 0:7 of FP_H_SYNC_STRT_WID:FP_H_SYNC_STRT_CHAR)</i>	7:0	0x0	

No description available for this register.

CRT05_S - RW - 8 bits - VGACRTIND:0x45			
Field Name	Bits	Default	Description
H_SYNC_END_S <i>(mirror bits 0:4 of FP_H_SYNC_STRT_WID:FP_H_SYNC_WID)</i>	4:0	0x0	
H_SYNC_SKEW_S	6:5	0x0	
H_BLANK_END_B5_S	7	0x0	

No description available for this register.

CRT06_S - RW - 8 bits - VGACRTIND:0x46			
Field Name	Bits	Default	Description
V_TOTAL_S <i>(mirror bits 0:7 of FP_CRTC_V_TOTAL_DISP:FP_CRTC_V_TOTAL)</i>	7:0	0x0	

No description available for this register.

CRT07_S - RW - 8 bits - VGACRTIND:0x47			
Field Name	Bits	Default	Description
V_TOTAL_B8_S <i>(mirror bits 8:8 of FP_CRTC_V_TOTAL_DISP:FP_CRTC_V_TO TAL)</i>	0	0x0	
V_DISP_END_B8_S <i>(mirror bits 8:8 of FP_CRTC_V_TOTAL_DISP:FP_CRTC_V_DIS P)</i>	1	0x0	
V_SYNC_START_B8_S <i>(mirror bits 8:8 of FP_V_SYNC_STRT_WID:FP_V_SYNC_STRT )</i>	2	0x0	
V_BLANK_START_B8_S	3	0x0	
LINE_CMP_B8_M <i>(mirror bits 8:8 of CRTC_VLINE_CRNT_VLINE:CRTC_VLINE)</i>	4	0x0	
V_TOTAL_B9_S <i>(mirror bits 9:9 of FP_CRTC_V_TOTAL_DISP:FP_CRTC_V_TO TAL)</i>	5	0x0	
V_DISP_END_B9_S <i>(mirror bits 9:9 of FP_CRTC_V_TOTAL_DISP:FP_CRTC_V_DIS P)</i>	6	0x0	
V_SYNC_START_B9_S <i>(mirror bits 9:9 of FP_V_SYNC_STRT_WID:FP_V_SYNC_STRT )</i>	7	0x0	

No description available for this register.

CRT08_S - RW - 8 bits - VGACRTIND:0x48			
Field Name	Bits	Default	Description
ROW_SCAN_START_M <i>(mirror of CRT08:ROW_SCAN_START)</i>	4:0	0x0	
BYTE_PAN_M <i>(mirror of CRT08:BYTE_PAN)</i>	6:5	0x0	

No description available for this register.

CRT09_S - RW - 8 bits - VGACRTIND:0x49			
Field Name	Bits	Default	Description
MAX_ROW_SCAN_S	4:0	0x0	
V_BLANK_START_B9_S	5	0x0	
LINE_CMP_B9_M <i>(mirror bits 9:9 of CRTC_VLINE_CRNT_VLINE:CRTC_VLINE)</i>	6	0x0	
DOUBLE_CHAR_HEIGHT_M <i>(mirror of CRT09:DOUBLE_CHAR_HEIGHT)</i>	7	0x0	0=200LineScan 1=400LineScan

No description available for this register.

CRT0A_S - RW - 8 bits - VGACRTIND:0x4A			
Field Name	Bits	Default	Description
CURSOR_START_S	4:0	0x0	
CURSOR_DISABLE_M <i>(mirror of CRT0A:CURSOR_DISABLE)</i>	5	0x0	0=on 1=off

No description available for this register.

CRT0B_S - RW - 8 bits - VGACRTIND:0x4B			
Field Name	Bits	Default	Description
CURSOR_END_S	4:0	0x0	
CURSOR_SKEW_M	6:5	0x0	
<i>(mirror of CRT0B:CURSOR_SKEW)</i>			

No description available for this register.

CRT0C_S - RW - 8 bits - VGACRTIND:0x4C			
Field Name	Bits	Default	Description
DISP_START_M	7:0	0x0	
<i>(mirror bits 11:18 of CRTC_OFFSET:CRTC_OFFSET)</i>			

No description available for this register.

CRT0D_S - RW - 8 bits - VGACRTIND:0x4D			
Field Name	Bits	Default	Description
DISP_START_M	7:0	0x0	
<i>(mirror bits 3:10 of CRTC_OFFSET:CRTC_OFFSET)</i>			

No description available for this register.

CRT0E_S - RW - 8 bits - VGACRTIND:0x4E			
Field Name	Bits	Default	Description
CURSOR_LOC_HI_M	7:0	0x0	
<i>(mirror of CRT0E:CURSOR_LOC_HI)</i>			

No description available for this register.

CRT0F_S - RW - 8 bits - VGACRTIND:0x4F			
Field Name	Bits	Default	Description
CURSOR_LOC_LO_M <i>(mirror of CRT0F:CURSOR_LOC_LO)</i>	7:0	0x0	

No description available for this register.

CRT10_S - RW - 8 bits - VGACRTIND:0x50			
Field Name	Bits	Default	Description
V_SYNC_START_S <i>(mirror bits 0:7 of FP_V_SYNC_STRT_WID:FP_V_SYNC_STRT)</i>	7:0	0x0	

No description available for this register.

CRT11_S - RW - 8 bits - VGACRTIND:0x51			
Field Name	Bits	Default	Description
V_SYNC_END_S <i>(mirror bits 0:3 of FP_V_SYNC_STRT_WID:FP_V_SYNC_WID)</i>	3:0	0x0	
V_INTR_CLR_M <i>(mirror of CRT11:V_INTR_CLR)</i>	4	0x0	0=VRetraceIntCleared 1=Not Cleared
V_INTR_EN_M <i>(mirror of CRT11:V_INTR_EN)</i>	5	0x0	0=VRetraceIntEna 1=Disable
SEL5_REFRESH_CYC_M <i>(mirror of CRT11:SEL5_REFRESH_CYC)</i>	6	0x0	0=3 DRAM Refresh/Horz Line 1=5 DRAM Refresh/Horz Line
C0T7_WR_ONLY_M <i>(mirror of CRT11:C0T7_WR_ONLY)</i>	7	0x0	0=EnaWrtToCRT00-07 1=C0T7B4WrtOnly

No description available for this register.

CRT12_S - RW - 8 bits - VGACRTIND:0x52			
Field Name	Bits	Default	Description
V_DISP_END_S  <i>(mirror bits 0:7 of FP_CRTC_V_TOTAL_DISP:FP_CRTC_V_DISP)</i>	7:0	0x0	

No description available for this register.

CRT13_S - RW - 8 bits - VGACRTIND:0x53			
Field Name	Bits	Default	Description
DISP_PITCH_M  <i>(mirror bits 0:7 of CRTC_PITCH:CRTC_PITCH)</i>	7:0	0x0	

No description available for this register.

CRT14_S - RW - 8 bits - VGACRTIND:0x54			
Field Name	Bits	Default	Description
UNDRLN_LOC_S  (DISPLAY)	4:0	0x0	Shadow copy UNDRLN_N_LOC
ADDR_CNT_BY4_M  <i>(mirror of CRT14:ADDR_CNT_BY4)</i>  (DISPLAY)	5	0x0	Mirror of ADDR_CNT_BY4
DOUBLE_WORD_M  <i>(mirror of CRT14:DOUBLE_WORD)</i>  (HDP) (DISPLAY)	6	0x0	Mirror of DOUBLE_WORD

Shadow of Underline Location Register

CRT15_S - RW - 8 bits - VGACRTIND:0x55			
Field Name	Bits	Default	Description
V_BLANK_START_S	7:0	0x0	

No description available for this register.

CRT16_S - RW - 8 bits - VGACRTIND:0x56			
Field Name	Bits	Default	Description
V_BLANK_END_S	7:0	0x0	

No description available for this register.

CRT17_S - RW - 8 bits - VGACRTIND:0x57			
Field Name	Bits	Default	Description
RA0_AS_A13B_M <i>(mirror of CRT17:RA0_AS_A13B)</i> (DISPLAY)	0	0x0	Mirror of RA0_AS_A13B
RA1_AS_A14B_M <i>(mirror of CRT17:RA1_AS_A14B)</i> (DISPLAY)	1	0x0	Mirror of RA1_AS_A14B
VCOUNT_BY2_S (DISPLAY)	2	0x0	Shadow copy of VCOUNT_BY2
ADDR_CNT_BY2_M <i>(mirror of CRT17:ADDR_CNT_BY2)</i> (DISPLAY)	3	0x0	Mirror of ADDR_CNT_BY2
WRAP_A15TOA0_M <i>(mirror of CRT17:WRAP_A15TOA0)</i> (DISPLAY)	5	0x0	Mirror of WRAP_A15TOA0

BYTE_MODE_M <i>(mirror of CRT17:BYTE_MODE)</i> (HDP) (DISPLAY)	6	0x0	Mirror of BYTE_MODE
CRTC_SYNC_EN_M <i>(mirror of CRT17:CRTC_SYNC_EN)</i> (DISPLAY)	7	0x0	Mirror of CRTC_SYNC_EN

Shadow of CRT Mode Register

CRT18_S - RW - 8 bits - VGACRTIND:0x58			
Field Name	Bits	Default	Description
LINE_CMP_M <i>(mirror bits 0:7 of CRTC_VLINE_CRNT_VLINE:CRTC_VLINE)</i>	7:0	0x0	

No description available for this register.

CRT1E_S - R - 8 bits - VGACRTIND:0x5E			
Field Name	Bits	Default	Description
GRPH_DEC_RD1_M <i>(mirror of CRT1E:GRPH_DEC_RD1)</i>	1	0x0	Mirror of GRPH_DEC_RD1

Shadow of CRT1E

CRT1F_S - R - 8 bits - VGACRTIND:0x5F			
Field Name	Bits	Default	Description
GRPH_DEC_RD0_M <i>(mirror of CRT1F:GRPH_DEC_RD0)</i>	7:0	0x0	Mirror of GRPH_DEC_RD0

Shadow of CRT1F

CRT22_S - R - 8 bits - VGACRTIND:0x62			
Field Name	Bits	Default	Description
GRPH_LATCH_DATA_M <i>(mirror of CRT22:GRPH_LATCH_DATA)</i>	7:0	0x0	Mirror of GRPH_LATCH_DATA

Shadow of CRT22

## 2.25 SEQ Registers

### Sequencer Control Registers

SEQ8_IDX - RW - 8 bits - VGA_IO:0x3C4			
Field Name	Bits	Default	Description
SEQ_IDX (HDP) (DISPLAY)	2:0	0x0	This index points to one of the sequencer registers (SEQ_) at I/O port address 0x3C5, for the next SEQ read/write operation.

SEQ Index Register

SEQ8_DATA - RW - 8 bits - VGA_IO:0x3C5			
Field Name	Bits	Default	Description
SEQ_DATA (HDP) (DISPLAY)	7:0	0x0	SEQ data indirect access

SEQ Data Register

SEQ00 - RW - 8 bits - VGASEQIND:0x0			
Field Name	Bits	Default	Description
SEQ_RST0B	0	0x1	Synchronous reset bit 0: 0=Follows SEQ_RST1B 1=Sequencer runs unless SEQ_RST1B=0
SEQ_RST1B	1	0x1	Synchronous reset bit 1: 0=Disable character clock, display requests, and H/V syncs 1=Sequencer runs unless SEQ_RST0B=0

Reset Register

SEQ01 - RW - 8 bits - VGASEQIND:0x1			
Field Name	Bits	Default	Description
SEQ_DOT8	0	0x1	8/9 Dot Clocks (Modes 1, 2, 3, and 7 use 9-dot characters. To change bit 0, GENVS(0) must be logical 0). 0=9 dot char clock. Modes 0, 1, 2, 3 & 7 1=8 dot char clock.
SEQ_SHIFT2	2	0x0	Shift load bits. 0=Load video serializer every clock, if SEQ_SHIFT4=0 1=Load video serializer every other clock, if SEQ_SHIFT4=0
SEQ_PCLKBY2	3	0x0	Dot Clock (typically, 320 and 360 horizontal modes use divide-by-2 to provide 40 column displays. To change this bit SEQ00[0:0] must be first set to zero.)). 0=Dot clock is normal 1=Dot clock is divided by 2
SEQ_SHIFT4	4	0x0	Shift load bits. 0=SEQ_SHIFT2 determines serializer loading 1=Load video serializer every fourth clock. Ignore SEQ_SHIFT2
SEQ_MAXBW	5	0x1	Screen off: 0=Normal. Screen on 1=Screen off and blanked. CPU has uninterrupted access to frame buffer

Clock Mode Register

SEQ02 - RW - 8 bits - VGASEQIND:0x2			
Field Name	Bits	Default	Description
SEQ_MAP0_EN	0	0x0	Enable map 0 0=Disable write to memory map 0 1=Enable write to memory map 0
SEQ_MAP1_EN	1	0x0	Enable map 1 0=Disable write to memory map 1 1=Enable write to memory map 1
SEQ_MAP2_EN	2	0x0	Enable map 2 0=Disable write to memory map 2 1=Enable write to memory map 2
SEQ_MAP3_EN	3	0x0	Enable map 3 0=Disable write to memory map 3 1=Enable write to memory map 3

Map Mask Register

<b>SEQ03 - RW - 8 bits - VGASEQIND:0x3</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SEQ_FONT_B1	0	0x0	Character Map Select B Bit 1
SEQ_FONT_B2	1	0x0	Character Map Select B Bit 2
SEQ_FONT_A1	2	0x0	Character Map Select A Bit 1
SEQ_FONT_A2	3	0x0	Character Map Select A Bit 2
SEQ_FONT_B0	4	0x0	Character Map Select B Bit 0
SEQ_FONT_A0	5	0x0	Character Map Select A Bit 0

Character Map Select Register

<b>SEQ04 - RW - 8 bits - VGASEQIND:0x4</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SEQ_256K	1	0x0	Extended memory - 1 indicates 256 KB of video memory is present. It also enables the character map selection in SEQ03. 0=64KB memory present. Has no effect since 256KB always available 1=256KB memory present
SEQ_ODDEVEN	2	0x0	Odd/Even 0=Even CPU address (A0=0) accesses maps 0 and 2. Odd address accesses maps 1 and 3 1=Enables sequential access to maps for odd/even modes. SEQ02 (Map Mask) selects which maps are used
SEQ_CHAIN	3	0x0	Chain (when logical 1, it takes priority over off/even mode bits SEQ04[2] and GRA05[4]. Unlike odd/even mode, SEQ04[2] is the only bit used to enable chain mode (double odd/even). Chain does not affect CRTC access to video memory. Odd/even bit SEQ04[2] should be the opposite of GRA05[4]. 0=Enables sequential access to maps. SEQ02 (Map Mask) selects which maps are used 1=For 256 color modes. Map select by CPU address bits A1:A0

Memory Mode Register

## 2.26 ATTR Registers

### Attribute Controller Registers

ATTR00 - RW - 8 bits - VGAATTRIND:0x0			
Field Name	Bits	Default	Description
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 0

ATTR01 - RW - 8 bits - VGAATTRIND:0x1			
Field Name	Bits	Default	Description
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 1

ATTR02 - RW - 8 bits - VGAATTRIND:0x2			
Field Name	Bits	Default	Description
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 2

ATTR03 - RW - 8 bits - VGAATTRIND:0x3			
Field Name	Bits	Default	Description
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 3

<b>ATTR04 - RW - 8 bits - VGAATTRIND:0x4</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 4

<b>ATTR05 - RW - 8 bits - VGAATTRIND:0x5</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 5

<b>ATTR06 - RW - 8 bits - VGAATTRIND:0x6</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 6

<b>ATTR07 - RW - 8 bits - VGAATTRIND:0x7</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 7

<b>ATTR08 - RW - 8 bits - VGAATTRIND:0x8</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 8

<b>ATTR09 - RW - 8 bits - VGAATTRIND:0x9</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 9

<b>ATTR0A - RW - 8 bits - VGAATTRIND:0xA</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register Ah (10)

<b>ATTR0B - RW - 8 bits - VGAATTRIND:0xB</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register Bh (11)

<b>ATTR0C - RW - 8 bits - VGAATTRIND:0xC</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register Ch (12)

<b>ATTR0D - RW - 8 bits - VGAATTRIND:0xD</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register Dh (13)

<b>ATTR0E - RW - 8 bits - VGAATTRIND:0xE</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register Eh (14)

<b>ATTR0F - RW - 8 bits - VGAATTRIND:0xF</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register Fh (15)

<b>ATTR10 - RW - 8 bits - VGAATTRIND:0x10</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_GRP_MODE	0	0x0	Graphics/Alphanumeric Mode. 0=Alphanumeric Mode 1=Graphic Mode
ATTR_MONO_EN	1	0x0	Monochrome/Colour Attributes Select: 0=Color Disp 1=MonoChrome Disp
ATTR_LGRP_EN	2	0x0	Line Graphics Enable. Must be 0 for character fonts that do not use line graphics character codes for graphics. Zero will force the 9th dot to the background colour. One will allow the 8th bit of the line graphics characters to be stretched to the 9th dot. 0=Disable line graphics 8th dot stretch 1=Enable line graphics 8th dot stretch
ATTR_BLINK_EN	3	0x0	Blink Enable/Background Intensity: Selects whether bit 7 of the attribute controls intensity or blinking.  0=Intensity control 1=Blink control
ATTR_PANTOPONLY	5	0x0	PEL Panning Compatibility: 0=Panning both 1=Panning only the top half screen
ATTR_PCLKBY2	6	0x0	PEL Clock Select: 0=Shift register clocked every dot clock 1=For mode 13 (256 colour), 8 bits packed to form a pixel
ATTR_CSEL_EN	7	0x0	Alternate Colour Source: 0=Select ATTR00-0F bit 5:4 as P5 and P4 1=Select ATTR14 bit 1:0 as P5 and P4

Mode Control Register

<b>ATTR11 - RW - 8 bits - VGAATTRIND:0x11</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_OVSC	7:0	0x0	Overscan Colour

Overscan Colour Register

ATTR12 - RW - 8 bits - VGAATTRIND:0x12			
Field Name	Bits	Default	Description
ATTR_MAP_EN	3:0	0x0	Enable Colour Map bits. 0 = Disables data from respective map from being used for video output. 1 = Enables data from respective map for use in video output.
ATTR_VSMUX	5:4	0x0	Video Status Mux bits 1:0. These are control bits for the multiplexer on colour bits P0-P7. The bit selection is also indicated at GENS1[5:4]: 00 = P2, P0 01 = P5, P4 10 = P3, P1 11 = P7, P6

Colour Map Enable Register

ATTR13 - RW - 8 bits - VGAATTRIND:0x13			
Field Name	Bits	Default	Description
ATTR_PPAN	3:0	0x0	Shift Count Bits 3:0. The shift count value (0-8) indicates how many pixel positions to shift left.  Shift in respective modes Count 0+, 1+, 2+, 13 All other Value 3+, 7, 7+ 0 1 0 0 1 2 - 1 2 3 1 2 3 4 - 3 4 5 2 4 5 6 - 5 6 7 3 6 7 8 - 7 8 0 - -

Horizontal PEL Panning Register

<b>ATTR14 - RW - 8 bits - VGAATTRIND:0x14</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
ATTR_CSEL1	1:0	0x0	Colour bits P5 and P4, respectively. These are the colour output bits (instead of bits 5 and 4 of the internal palette registers ATTR00-0F) when alternate colour source, bit ATTR10[7] is logical 1.
ATTR_CSEL2	3:2	0x0	Colour bits P7 and P6, respectively. These two bits are the two high-order bits of the 8-bit colour, used for rapid colour set switching (addressing different parts of the DAC colour lookup table). The lower order bits are in registers ATTR00-0F.

Colour Select Register

## 2.27 GRPH Registers

### Graphics Control Registers

GRPH8_IDX - RW - 8 bits - VGA_IO:0x3CE			
Field Name	Bits	Default	Description
GRPH_IDX (HDP) (DISPLAY)	3:0	0x0	This index is used to address one of the internal registers of the graphics controller (GRAC) at I/O port 0x3CRF.

GRPH Index Register

GRPH8_DATA - RW - 8 bits - VGA_IO:0x3CF			
Field Name	Bits	Default	Description
GRPH_DATA (HDP) (DISPLAY)	7:0	0x0	GRPH data indirect access

GRPH Data Register

GRA00 - RW - 8 bits - VGAGRPHIND:0x0			
Field Name	Bits	Default	Description
GRPH_SET_RESET0	0	0x0	Set/Reset Map 0
GRPH_SET_RESET1	1	0x0	Set/Reset Map 1
GRPH_SET_RESET2	2	0x0	Set/Reset Map 2
GRPH_SET_RESET3	3	0x0	Set/Reset Map 3

Set/Reset Register

GRA01 - RW - 8 bits - VGAGRPHIND:0x1			
Field Name	Bits	Default	Description
GRPH_SET_RESET_ENA0	0	0x0	Enable Set/Reset Map 0
GRPH_SET_RESET_ENA1	1	0x0	Enable Set/Reset Map 1
GRPH_SET_RESET_ENA2	2	0x0	Enable Set/Reset Map 2

GRPH_SET_RESET_ENA3	3	0x0	Enable Set/Reset Map 3
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Enable Set/Reset Register

GRA02 - RW - 8 bits - VGAGRPHIND:0x2			
Field Name	Bits	Default	Description
GRPH_CCOMP	3:0	0x0	Colour Compare Map bits 3:0. In Read mode (GRA05[3] being logical 1), the 4 bits from this register are compared with the 4-bit PEL value (made up of one bit from each map), from bit positions 0 through 7. As long as the colour don't care bits (GRA07[0:3]) for the respective maps are logical 1's, the compare takes place only on those bits of the PEL value, and the CPU reads a one for a match in that bit position. If Colour Don't Care bit for one map is a logical zero, the latched data from the map is excluded from the compare, and only the remaining three bits are compared to generate bus data.

Colour Compare Register

GRA03 - RW - 8 bits - VGAGRPHIND:0x3			
Field Name	Bits	Default	Description
GRPH_ROTATE	2:0	0x0	Rotate Count Bits 2-0. Specifies the number of bit positions that the CPU data is to be rotated to the right, before doing the function selected by bits 3 and 4 above and subsequence bit mask select and write operations. Rotation is carried out only in write modes 0 and 3. In these two modes, the CPU data is rotated first, the operated only the function bits GRA03[4:3], the updated by the bit mask register GRA05.
GRPH_FN_SEL	4:3	0x0	Function Select Bits 1 and 2. These functions are performed on the CPU data before the selected bits are updated by the bit mask register, and then written to the display buffers. 0=Replace 1=AND 2=OR 3=XOR

Data Rotate Register

GRA04 - RW - 8 bits - VGAGRPHIND:0x4			
Field Name	Bits	Default	Description
GRPH_RMAP	1:0	0x0	Read Mode 0 Only: GRA controller returns the contents of one of the four latched buffer bytes to CPU each time a CPU read loads these latches. The 2 bits (0 and 1) define a value that represents the bit map where CPU is to read data - usefull in transferring bit map data between the maps and system RAM.

Read Map Select Register

GRA05 - RW - 8 bits - VGAGRPHIND:0x5			
Field Name	Bits	Default	Description
GRPH_WRITE_MODE (HDP)	1:0	0x0	Write Mode: 0=Write mode 0 1=Write mode 1 2=Write mode 2 3=Write mode 3
GRPH_READ1 (HDP)	3	0x0	Read Mode: 0=Read mode 0, byte oriented 1=Read mode 1, pixel oriented
CGA_ODDEVEN (HDP)	4	0x0	Odd/Even Addressing Enable. Used to enable CGA emulation, this bit enables off/even addressing mode when it is logical one. Normally, this bit and memory mode bit SEQ04[2] are set to agree with each other in enabling odd/even mode emulation. 0=Disable Odd/Even Addressing 1=Enable Odd/Even Addressing
GRPH_OES (HDP) (DISPLAY)	5	0x0	Shift Register Mode: This bit controls how data from memory is loaded into the shift registers M0D0:M0D7, M1D0:M1D7; M2D0:M2D7, and M3D0:M3D7 are representations of this data. 0=Linear shift mode 1=Tiled shift mode
GRPH_PACK (HDP) (DISPLAY)	6	0x0	256 Colour Mode. This bit also contros how data from memory is loaded into the shift registers. 0=Use shift register mode as per GRPH_OES 1=256 color mode, read as packed pixels, ignore GRPH_OES

Graphics Mode Register

<b>GRA06 - RW - 8 bits - VGAGRPHIND:0x6</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
GRPH_GRAPHICS	0	0x0	Graphics/Alphanumeric Mode 0=Alpha Numeric Mode 1=Graphics Mode
GRPH_ODDEVEN	1	0x0	Chains Odd Maps to Even 0=Normal 1=Chain Odd maps to Even
GRPH_ADRSEL	3:2	0x0	Memory Map Read Bits 1 and 0, respectively. 0=A0000-128K 1=A0000-64K 2=B0000-32K 3=B8000-32K

Graphics Miscellaneous Register

<b>GRA07 - RW - 8 bits - VGAGRPHIND:0x7</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
GRPH_XCARE0	0	0x0	Ignore Map 0 0=Ignore map 0 1=Use map 0 for read mode 1
GRPH_XCARE1	1	0x0	Ignore Map 1 0=Ignore map 1 1=Use map 1 for read mode 1
GRPH_XCARE2	2	0x0	Ignore Map 2 0=Ignore map 2 1=Use map 2 for read mode 1
GRPH_XCARE3	3	0x0	Ignore Map 3 0=Ignore map 3 1=Use map 3 for read mode 1

Colour Don't Care Register

<b>GRA08 - RW - 8 bits - VGAGRPHIND:0x8</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
GRPH_BMSK	7:0	0x0	Bit Mask

Bit Mask Register

## 2.28 Miscellaneous Registers

<b>GENENB - R - 8 bits - VGA_IO:0x3C3</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BLK_IO_BASE	7:0	0x0	

No description available for this register.

<b>MM_INDEX - RW - 32 bits - [IOReg,MMReg:0x0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
MM_ADDR	30:0	0x0	
MM_APER	31	0x0	0=Register Aperture 1=Linear Aperture 0

No description available for this register.

<b>MM_DATA - RW - 32 bits - [IOReg,MMReg:0x4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
MM_DATA	31:0	0x0	

No description available for this register.

<b>BUS_CNTL - RW - 32 bits - [IOReg,MMReg:0x30]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BUS_DBL_RESYNC	0	0x1	0=Normal 1=Add extra resynchronizing clock
BUS_MSTR_RESET (W)	1	0x0	0=Normal 1=Reset
BUS_FLUSH_BUF (W)	2	0x0	0=Normal 1=Flush
BUS_STOP_REQ_DIS	3	0x0	0=Normal 1=Disable

Miscellaneous Registers

BUS_READ_COMBINE_EN	4	0x0	0=Disable 1=Enable
BUS_WRT_COMBINE_EN	5	0x0	0=Disable 1=Enable
BUS_MASTER_DIS	6	0x1	0=Enable 1=Disable
BIOS_ROM_WRT_EN	7	0x0	0=Disable 1=Enable
BUS_PREFETCH_MODE	9:8	0x0	0=HI prefetching disabled 1=HI prefetches during active bus requests only 2=HI always prefetches continuously 3=Hi attempts to hold 1 DW of read data for a delayed read completion
BUS_VGA_PREFETCH_EN	10	0x0	0=Disable 1=Enable
BUS_SGL_READ_DISABLE	11	0x0	0=Enable 1=Disable
BIOS_DIS_ROM	12	0x0	0=Enable 1=Disable
BUS_PCI_READ_RETRY_EN	13	0x0	0=Normal 1=Enable
BUS_AGP_AD_STEPPING_EN	14	0x1	0=No stepping in AGP 1=AD Stepping in AGP and PCI
BUS_PCI_WRT_RETRY_EN	15	0x0	0=Normal 1=Enable
BUS_RETRY_WS	19:16	0xf	
BUS_MSTR_RD_MULT	20	0x0	0=Read line 1=Read multiple
BUS_MSTR_RD_LINE	21	0x0	0=Read multiple 1=Read line
BUS_SUSPEND	22	0x0	0=Resume BM transfer 1=Suspend BM transfer
LAT_16X	23	0x0	0=1X 1=16X
BUS_RD_DISCARD_EN	24	0x0	0=Disable 1=Enable
ENFRCWRDY	25	0x0	0=Disable 1=Enable
BUS_MSTR_WS	26	0x0	0=8 wait states 1=32 wait states

BUS_PARKING_DIS	27	0x1	0=Enable 1=Disable
BUS_MSTR_DISCONNECT_EN	28	0x0	0=Disable 1=Enable
SERR_EN	29	0x0	0=Disable 1=Enable
BUS_READ_BURST	30	0x0	0=Disable 1=Enable
BUS_RDY_READ_DLY	31	0x1	0=no RDY delay 1=RDY delayed 1 mem clk

No description available for this register.

<b>HI_STAT - RW - 32 bits - [IOReg,MMReg:0x4C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
HI_STAT	2:0	0x0	
AGP_BUSY (R)	3	0x0	

No description available for this register.

<b>BUS_CNTL1 - RW - 32 bits - [IOReg,MMReg:0x34]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
PMI_IO_DISABLE	0	0x0	0=Normal 1=Disable
PMI_MEM_DISABLE	1	0x0	0=Normal 1=Disable
PMI_BM_DISABLE	2	0x0	0=Normal 1=Disable
PMI_INT_DISABLE	3	0x0	0=Normal 1=Disable
BUS2_STALE_DATA_TIMER	7:4	0xf	
BUS2_VGA_REG_COHERENCY_DIS	8	0x0	0=Enable 1=Disable
BUS2_VGA_MEM_COHERENCY_DIS	9	0x0	0=Enable 1=Disable
BUS2_HDP_REG_COHERENCY_DIS	10	0x0	0=Enable 1=Disable

BUS2_GUI_INITIATOR_COHERENCY_DIS	11	0x0	0=Enable 1=Disable
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No description available for this register.

CONFIG_CNTL - RW - 32 bits - [IOReg,MMReg:0xE0]			
Field Name	Bits	Default	Description
APER_REG_ENDIAN	5:4	0x0	
CFG_VGA_RAM_EN <i>(mirror of GENMO_WT:VGA_RAM_EN)</i>	8	0x0	0=Disable 1=Enable
CFG_VGA_IO_DIS	9	0x0	
CFG_ATI_REV_ID (R)	19:16	0x0	

No description available for this register.

CONFIG_MEMSIZE - RW - 32 bits - [IOReg,MMReg:0xF8]			
Field Name	Bits	Default	Description
CONFIG_MEMSIZE	28:24	0x0	

No description available for this register.

CONFIG_APER_0_BASE - R - 32 bits - [MMReg:0x100]			
Field Name	Bits	Default	Description
APER_0_BASE	31:25	0x0	

No description available for this register.

CONFIG_APER_1_BASE - R - 32 bits - [MMReg:0x104]			
Field Name	Bits	Default	Description
APER_1_BASE	31:24	0x0	

No description available for this register.

<b>CONFIG_APER_SIZE - R - 32 bits - [MMReg:0x108]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
APER_SIZE	27:24	0x0	

No description available for this register.

<b>CONFIG_REG_1_BASE - R - 32 bits - [MMReg:0x10C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
REG_APER_1_SELECT	18	0x1	
REG_1_BASE	31:19	0x0	

No description available for this register.

<b>CONFIG_REG_APER_SIZE - R - 32 bits - [MMReg:0x110]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
REG_APER_SIZE	18:0	0x40000	

No description available for this register.

<b>PAD_AGPINPUT_DELAY - RW - 32 bits - [MMReg:0x164]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
PAD_AGPINPUT_DELAY	31:0	0x0	

No description available for this register.

<b>PAD_CTLR_STRENGTH - RW - 32 bits - [MMReg:0x168]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
PAD_N_STRENGTH_READ_BACK (R)	3:0	0x0	
PAD_P_STRENGTH_READ_BACK (R)	7:4	0x0	
PAD_N_MANUAL_STRENGTH	11:8	0x0	
PAD_P_MANUAL_STRENGTH	15:12	0x0	

PAD_MANUAL_OVERRIDE	16	0x1	0=Allow normal impedance compensation operation 1=Default to manual settings
PAD_TEST_OUT (R)	17	0x0	
PAD_DUMMY_OUT (R)	18	0x0	
PAD_HI_IO_DFR	19	0x0	
PAD_HI_IO_SCHMEN	20	0x0	
PAD_HI_IO_DREN	21	0x0	
PAD_HI_IO_SLEW	22	0x0	
PAD_HI_IO_VDIFF	23	0x0	
PAD_HI_IO_DFR_OVERRIDE	24	0x0	
PAD_HI_IO_SCHMEN_OVERRIDE	25	0x0	
PAD_HI_IO_DREN_OVERRIDE	26	0x0	
PAD_HI_IO_SLEW_OVERRIDE	27	0x0	
PAD_HI_IO_VDIFF_OVERRIDE	28	0x0	

No description available for this register.

<b>PAD_CTLR_UPDATE - RW - 32 bits - [MMReg:0x16C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
PAD_UPDATE_RATE	4:0	0x16	
PAD_SAMPLE_DELAY	12:8	0x6	
PAD_INC_THRESHOLD	20:16	0x18	
PAD_DEC_THRESHOLD	28:24	0x8	

No description available for this register.

<b>AGP_CNTL - RW - 32 bits - [MMReg:0x174]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
MAX_IDLE_CLK	7:0	0x0	
HOLD_RD_FIFO	8	0x0	
HOLD_RQ_FIFO	9	0x0	

EN_2X_STBB	10	0x0	
FORCE_FULL_SBA	11	0x0	
SBA_DIS	12	0x0	
AGP_REV_ID	13	0x0	
REG_CRIPPLE_AGP4X	14	0x0	
REG_CRIPPLE_AGP2X4X	15	0x0	
FORCE_INT_VREF	16	0x0	
PENDING_SLOTS_VAL	18:17	0x0	
PENDING_SLOTS_SEL	19	0x0	
EN_EXTENDED_AD_STB_2X	20	0x0	
DIS_QUEUED_GNT_FIX	21	0x0	0=Enable 1=Disable
EN_RDATA2X4X_MULTIRESET	22	0x0	
EN_RBFCALM	23	0x0	
FORCE_EXT_VREF	24	0x0	
DIS_RBF	25	0x0	0=Allow normal RBF operation 1=Disable RBF generation
AGP_MISC	31:26	0x0	

No description available for this register.

<b>BM_STATUS - R - 32 bits - [MMReg:0x160]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BUS_MASTER_STATUS	31:0	0x0	

No description available for this register.

<b>VENDOR_ID - R - 16 bits - [MMReg:0xF00] [pciConfig:0x0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
VENDOR_ID	15:0	0x1002	

No description available for this register.

<b>DEVICE_ID - R - 16 bits - [MMReg:0xF02] [pciConfig:0x2]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DEVICE_ID	15:0	0x3541	

No description available for this register.

<b>COMMAND - RW - 16 bits - [MMReg:0xF04]:R [pciConfig:0x4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
IO_ACCESS_EN	0	0x0	0=Disable 1=Enable
MEM_ACCESS_EN	1	0x0	0=Disable 1=Enable
BUS_MASTER_EN	2	0x0	0=Disable 1=Enable
SPECIAL_CYCLE_EN (R)	3	0x0	0=Disable 1=Enable
MEM_WRITE_INVALIDATE_EN (R)	4	0x0	0=Disable 1=Enable
PAL_SNOOP_EN	5	0x0	0=Disable 1=Enable
PARITY_ERROR_EN (R)	6	0x0	0=Disable 1=Enable
AD_STEPPING (R)	7	0x1	0=Disable 1=Enable
SERR_EN	8	0x0	0=Disable 1=Enable
FAST_B2B_EN	9	0x0	0=Disable 1=Enable

No description available for this register.

<b>STATUS - RW - 16 bits - [MMReg:0xF06]:R [pciConfig:0x6]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_LIST (R)	4	0x1	
PCI_66_EN (R)	5	0x1	

UDF_EN (R)	6	0x0	0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x1	
DEVSEL_TIMING (R)	10:9	0x1	
SIGNAL_TARGET_ABORT (R)	11	0x0	
RECEIVED_TARGET_ABORT	12	0x0	0=Inactive 1=Active
RECEIVED_MASTER_ABORT	13	0x0	0=Inactive 1=Active
SIGNALLED_SYSTEM_ERROR	14	0x0	
PARITY_ERROR_DETECTED (R)	15	0x0	

No description available for this register.

<b>REVISION_ID - R - 8 bits - [MMReg:0xF08] [pciConfig:0x8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
MINOR_REV_ID	3:0	0x0	
MAJOR_REV_ID	7:4	0x0	

No description available for this register.

<b>REGPROG_INF - R - 8 bits - [MMReg:0xF09] [pciConfig:0x9]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
REG_LEVEL_PROG_INF	7:0	0x0	

No description available for this register.

<b>SUB_CLASS - R - 8 bits - [MMReg:0xF0A] [pciConfig:0xA]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SUB_CLASS_INF	7	0x0	0=00 - VGA device 1=80 - extended graphics

No description available for this register.

<b>BASE_CODE - R - 8 bits - [MMReg:0xF0B] [pciConfig:0xB]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BASE_CLASS_CODE	7:0	0x3	

No description available for this register.

<b>CACHE_LINE - RW - 8 bits - [MMReg:0xF0C]:R [pciConfig:0xC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CACHE_LINE_SIZE	7:0	0x0	

No description available for this register.

<b>LATENCY - RW - 8 bits - [MMReg:0xF0D]:R [pciConfig:0xD]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
LATENCY_TIMER	7:0	0x0	

No description available for this register.

<b>HEADER - R - 8 bits - [MMReg:0xF0E] [pciConfig:0xE]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
HEADER_TYPE	6:0	0x0	
DEVICE_TYPE	7	0x0	0=Single-Function Device 1=Multi-Function Device

No description available for this register.

<b>BIST - R - 8 bits - [MMReg:0xF0F] [pciConfig:0xF]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BIST_COMP	3:0	0x0	
BIST_STRT	6	0x0	
BIST_CAP	7	0x0	

No description available for this register.

<b>MEM_BASE - RW - 32 bits - [MMReg:0xF10]:R [pciConfig:0x10]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
PREFETCH_EN (R)	3	0x1	
MEM_BASE	31:25	0x0	

No description available for this register.

<b>IO_BASE - RW - 32 bits - [MMReg:0xF14]:R [pciConfig:0x14]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BLOCK_IO_BIT (R)	7:0	0x1	
IO_BASE	31:8	0x0	

No description available for this register.

<b>REG_BASE - RW - 32 bits - [MMReg:0xF18]:R [pciConfig:0x18]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
REG_BASE	31:19	0x0	

No description available for this register.

<b>ADAPTER_ID - R - 32 bits - [MMReg:0xF2C] [pciConfig:0x2C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SUBSYSTEM_VENDOR_ID <i>(mirror of ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)</i>	15:0	0x0	
SUBSYSTEM_ID <i>(mirror of ADAPTER_ID_W:SUBSYSTEM_ID)</i>	31:16	0x0	

No description available for this register.

<b>BIOS_ROM - RW - 32 bits - [MMReg:0xF30]:R [pciConfig:0x30]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
BIOS_ROM_EN	0	0x0	0=Disable 1=Enable
BIOS_BASE_ADDR	31:17	0x0	

No description available for this register.

<b>CAPABILITIES_PTR - R - 32 bits - [MMReg:0xF34] [pciConfig:0x34]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_PTR	7:0	0x50	

No description available for this register.

<b>INTERRUPT_LINE - RW - 8 bits - [MMReg:0xF3C]:R [pciConfig:0x3C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
INTERRUPT_LINE	7:0	0xff	

No description available for this register.

<b>INTERRUPT_PIN - R - 8 bits - [MMReg:0xF3D] [pciConfig:0x3D]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
INTERRUPT_PIN	0	0x0	

No description available for this register.

<b>MIN_GRANT - R - 8 bits - [MMReg:0xF3E] [pciConfig:0x3E]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
MIN_GNT	7:0	0x8	

No description available for this register.

**MAX\_LATENCY - R - 8 bits - [MMReg:0xF3F] [pciConfig:0x3F]**

Field Name	Bits	Default	Description
MAX_LAT	7:0	0x0	

No description available for this register.

**ADAPTER\_ID\_W - RW - 32 bits - [MMReg:0xF4C]:R [pciConfig:0x4C]**

Field Name	Bits	Default	Description
SUBSYSTEM_VENDOR_ID	15:0	0x0	
SUBSYSTEM_ID	31:16	0x0	

No description available for this register.

**PMI\_CAP\_ID - R - 8 bits - [MMReg:0xF50] [pciConfig:0x50]**

Field Name	Bits	Default	Description
PMI_CAP_ID	7:0	0x1	1=PCI Bus Power Management Interface (PMI) register section

No description available for this register.

**PMI\_NXT\_CAP\_PTR - R - 8 bits - [MMReg:0xF51] [pciConfig:0x51]**

Field Name	Bits	Default	Description
PMI_NXT_CAP_PTR	7:0	0x0	

No description available for this register.

**PMI\_PMC\_REG - R - 16 bits - [MMReg:0xF52] [pciConfig:0x52]**

Field Name	Bits	Default	Description
PMI_VERSION	2:0	0x2	2=Compliant with PMI Specification verison 1.1
PMI_PME_CLOCK	3	0x0	
PMI_DEV_SPECIFIC_INIT	5	0x0	

PMI_D1_SUPPORT	9	0x1	
PMI_D2_SUPPORT	10	0x1	
PMI_PME_SUPPORT	15:11	0x0	

No description available for this register.

<b>PM_STATUS - RW - 16 bits - [MMReg:0xF54]:R [pciConfig:0x54]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
PMI_POWER_STATE	1:0	0x0	
PMI_PME_EN (R)	8	0x0	
PMI_DATA_SELECT (R)	12:9	0x0	
PMI_DATA_SCALE (R)	14:13	0x0	
PMI_PME_STATUS (R)	15	0x0	

No description available for this register.

<b>PMI_DATA - R - 8 bits - [MMReg:0xF57] [pciConfig:0x57]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
PMI_DATA	7:0	0x0	

No description available for this register.

<b>AGP_CAP_ID - R - 32 bits - [MMReg:0xF58] [pciConfig:0x58]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CAP_ID	7:0	0x2	
NEXT_PTR	15:8	0x50	
AGP_MINOR	19:16	0x0	
AGP_MAJOR	23:20	0x2	

No description available for this register.

<b>AGP_STATUS - R - 32 bits - [MMReg:0xF5C] [pciConfig:0x5C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
RATE1X	0	0x1	
RATE2X	1	0x1	
RATE4X	2	0x1	
SBA	9	0x1	
RQ	31:24	0x2f	

No description available for this register.

<b>AGP_COMMAND - RW - 32 bits - [MMReg:0xF60]:R [pciConfig:0x60]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DATA_RATE	2:0	0x0	
AGP_EN	8	0x0	0=disable 1=enable
SBA_EN (R)	9	0x1	0=Disable 1=Enable
RQ_DEPTH	31:24	0x0	

No description available for this register.

<b>AIC_CTRL - RW - 32 bits - [MMReg:0x1D0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
TRANSLATE_EN	0	0x0	0=disable pci gart 1=enable pci gart
HW_0_DEBUG	1	0x0	
HW_1_DEBUG	2	0x0	
HW_2_DEBUG	3	0x0	
HW_3_DEBUG	4	0x0	
HW_4_DEBUG	5	0x0	
HW_5_DEBUG	6	0x0	
HW_6_DEBUG	7	0x0	

HW_7_DEBUG	8	0x0	
HW_8_DEBUG	9	0x0	
HW_9_DEBUG	10	0x0	
HW_A_DEBUG	11	0x0	
HW_B_DEBUG	12	0x0	
HW_C_DEBUG	13	0x0	
HW_D_DEBUG	14	0x0	
HW_E_DEBUG	15	0x0	
HW_F_DEBUG	16	0x0	
HW_10_DEBUG	17	0x0	
HW_11_DEBUG	18	0x0	
HW_12_DEBUG	19	0x0	
HW_13_DEBUG	20	0x0	
HW_14_DEBUG	21	0x0	
HW_15_DEBUG	22	0x0	
HW_16_DEBUG	23	0x0	
HW_17_DEBUG	24	0x0	
HW_18_DEBUG	25	0x0	
HW_19_DEBUG	26	0x0	
HW_1A_DEBUG	27	0x0	
HW_1B_DEBUG	28	0x0	
HW_1C_DEBUG	29	0x0	
HW_1D_DEBUG	30	0x0	
HW_1E_DEBUG	31	0x0	

No description available for this register.

<b>AIC_STAT - R - 32 bits - [MMReg:0x1D4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
AIC_TLB_VLD	0	0x0	

AIC_STAT1	1	0x0	
AIC_STAT0	2	0x0	

No description available for this register.

<b>AIC_PT_BASE - RW - 32 bits - [MMReg:0x1D8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
AIC_PT_BASE	31:12	0x0	

PCI GART page table base address in system memory

<b>AIC_LO_ADDR - RW - 32 bits - [MMReg:0x1DC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
AIC_LO_ADDR	31:12	0x0	

Lower boundary of PCI addresses responded to by the PCI GART; addresses lower than this are not translated

<b>AIC_HI_ADDR - RW - 32 bits - [MMReg:0x1E0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
AIC_HI_ADDR	31:12	0x0	

Upper boundary of PCI addresses responded to by the PCI GART; addresses higher than this are not translated

<b>AIC_TLB_ADDR - R - 32 bits - [MMReg:0x1E4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
AIC_TLB_ADDR	31:12	0x0	

Current page address before translation by the PCI GART

<b>AIC_TLB_DATA - R - 32 bits - [MMReg:0x1E8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
AIC_TLB_DATA	31:12	0x0	

Current page address after translation by the PCI GART

<b>SURFACE_ACCESS_FLAGS - R - 32 bits - [MMReg:0xBF8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SURF0_WRITE_FLAG	0	0x0	Indicates if write to surface 0 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF1_WRITE_FLAG	1	0x0	Indicates if write to surface 1 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF2_WRITE_FLAG	2	0x0	Indicates if write to surface 2 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF3_WRITE_FLAG	3	0x0	Indicates if write to surface 3 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF4_WRITE_FLAG	4	0x0	Indicates if write to surface 4 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF5_WRITE_FLAG	5	0x0	Indicates if write to surface 5 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF6_WRITE_FLAG	6	0x0	Indicates if write to surface 6 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF7_WRITE_FLAG	7	0x0	Indicates if write to surface 7 since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
NONSURF_WRITE_FLAG	8	0x0	Indicates if write to address that missed all surfaces since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
LINEAR_WRITE_FLAG	9	0x0	Indicates if write to anywhere in linear memory aperture since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
VGA_WRITE_FLAG	10	0x0	Indicates if write to anywhere in VGA memory aperture since last cleared. 0=No write since last cleared. 1=Write occurred since last cleared.
SURF0_READ_FLAG	16	0x0	Indicates if read to surface 0 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.

SURF1_READ_FLAG	17	0x0	Indicates if read to surface 1 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.
SURF2_READ_FLAG	18	0x0	Indicates if read to surface 2 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.
SURF3_READ_FLAG	19	0x0	Indicates if read to surface 3 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.
SURF4_READ_FLAG	20	0x0	Indicates if read to surface 4 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.
SURF5_READ_FLAG	21	0x0	Indicates if read to surface 5 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.
SURF6_READ_FLAG	22	0x0	Indicates if read to surface 6 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.
SURF7_READ_FLAG	23	0x0	Indicates if read to surface 7 since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.
NONSURF_READ_FLAG	24	0x0	Indicates if read to address that missed all surfaces since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.
LINEAR_READ_FLAG	25	0x0	Indicates if read to anywhere in linear memory aperture since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.
VGA_READ_FLAG	26	0x0	Indicates if read to anywhere in VGA memory aperture since last cleared. 0=No read since last cleared. 1=Read occurred since last cleared.

Flags to indicate write or read access to memory surfaces

<b>SURFACE_ACCESS_CLR - W - 32 bits - [MMReg:0xBFC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SURF0_WRITE_FLAG_CLR	0	0x0	Used to clear SURF0_WRITE_FLAG. 0=Do not clear this write flag. 1=Clear this write flag.

SURF1_WRITE_FLAG_CLR	1	0x0	Used to clear SURF1_WRITE_FLAG. 0=Do not clear this write flag. 1=Clear this write flag.
SURF2_WRITE_FLAG_CLR	2	0x0	Used to clear SURF2_WRITE_FLAG. 0=Do not clear this write flag. 1=Clear this write flag.
SURF3_WRITE_FLAG_CLR	3	0x0	Used to clear SURF3_WRITE_FLAG. 0=Do not clear this write flag. 1=Clear this write flag.
SURF4_WRITE_FLAG_CLR	4	0x0	Used to clear SURF4_WRITE_FLAG. 0=Do not clear this write flag. 1=Clear this write flag.
SURF5_WRITE_FLAG_CLR	5	0x0	Used to clear SURF5_WRITE_FLAG. 0=Do not clear this write flag. 1=Clear this write flag.
SURF6_WRITE_FLAG_CLR	6	0x0	Used to clear SURF6_WRITE_FLAG. 0=Do not clear this write flag. 1=Clear this write flag.
SURF7_WRITE_FLAG_CLR	7	0x0	Used to clear SURF7_WRITE_FLAG. 0=Do not clear this write flag. 1=Clear this write flag.
NONSURF_WRITE_FLAG_CLR	8	0x0	Used to clear NONSURF_WRITE_FLAG. 0=Do not clear this write flag. 1=Clear this write flag.
LINEAR_WRITE_FLAG_CLR	9	0x0	Used to clear LINEAR_WRITE_FLAG. 0=Do not clear this write flag. 1=Clear this write flag.
VGA_WRITE_FLAG_CLR	10	0x0	Used to clear VGA_WRITE_FLAG. 0=Do not clear this write flag. 1=Clear this write flag.
SURF0_READ_FLAG_CLR	16	0x0	Used to clear SURF0_READ_FLAG. 0=Do not clear this read flag. 1=Clear this read flag.
SURF1_READ_FLAG_CLR	17	0x0	Used to clear SURF1_READ_FLAG. 0=Do not clear this read flag. 1=Clear this read flag.
SURF2_READ_FLAG_CLR	18	0x0	Used to clear SURF2_READ_FLAG. 0=Do not clear this read flag. 1=Clear this read flag.
SURF3_READ_FLAG_CLR	19	0x0	Used to clear SURF3_READ_FLAG. 0=Do not clear this read flag. 1=Clear this read flag.
SURF4_READ_FLAG_CLR	20	0x0	Used to clear SURF4_READ_FLAG. 0=Do not clear this read flag. 1=Clear this read flag.

SURF5_READ_FLAG_CLR	21	0x0	Used to clear SURF5_READ_FLAG. 0=Do not clear this read flag. 1=Clear this read flag.
SURF6_READ_FLAG_CLR	22	0x0	Used to clear SURF6_READ_FLAG. 0=Do not clear this read flag. 1=Clear this read flag.
SURF7_READ_FLAG_CLR	23	0x0	Used to clear SURF7_READ_FLAG. 0=Do not clear this read flag. 1=Clear this read flag.
NONSURF_READ_FLAG_CLR	24	0x0	Used to clear NONSURF_READ_FLAG. 0=Do not clear this read flag. 1=Clear this read flag.
LINEAR_READ_FLAG_CLR	25	0x0	Used to clear LINEAR_READ_FLAG. 0=Do not clear this read flag. 1=Clear this read flag.
VGA_READ_FLAG_CLR	26	0x0	Used to clear VGA_READ_FLAG. 0=Do not clear this read flag. 1=Clear this read flag.

Clear bits for SURFACE\_ACCESS\_FLAGS register

<b>GPIO_VGA_DDC - RW - 32 bits - [IOReg,MMReg:0x60]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
VGA_DCC_DATA_OUTPUT	0	0x0	Ouput data bit if output enabled by VGA_DDC_DATA_EN. 0=Drive VGA_DDC_DATA low, if enabled. 1=Drive VGA_DDC_DATA high, if enabled.
VGA_DDC_CLK_OUTPUT	1	0x0	Ouput clock bit if output enabled by VGA_DDC_CLK_EN. 0=Drive VGA_DDC_CLK low, if enabled. 1=Drive VGA_DDC_CLK high, if enabled.
VGA_DDC_DATA_INPUT (R)	8	0x0	Data bit input. 0=VGA_DDC_DATA pin input is low. 1=VGA_DDC_DATA pin input is high.
VGA_DDC_CLK_INPUT (R)	9	0x0	Clock bit input. 0=VGA_DDC_CLK pin input is low. 1=VGA_DDC_CLK pin input is high.
VGA_DDC_DATA_OUT_EN	16	0x0	Data pin output enable. 0=VGA_DDC_DATA output disabled. 1=VGA_DDC_DATA output enabled.
VGA_DDC_CLK_OUT_EN	17	0x0	Clock pin output enable. 0=VGA_DDC_CLK output disabled. 1=VGA_DDC_CLK output enabled.

Control and read of DDC clock and data lines for analog VGA connector.

<b>GPIO_DVI_DDC - RW - 32 bits - [IOReg,MMReg:0x64]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DVI_DDC_DATA_OUTPUT	0	0x0	Output data bit if output enabled by DVI_DDC_DATA_EN. 0=Drive DVI_DDC_DATA low, if enabled. 1=Drive DVI_DDC_DATA high, if enabled.
DVI_DDC_CLK_OUTPUT	1	0x0	Output clock bit if output enabled by DVI_DDC_CLK_EN. 0=Drive DVI_DDC_CLK low, if enabled. 1=Drive DVI_DDC_CLK high, if enabled.
DVI_DDC_DATA_INPUT (R)	8	0x0	Data bit input. 0=DVI_DDC_DATA pin input is low. 1=DVI_DDC_DATA pin input is high.
DVI_DDC_CLK_INPUT (R)	9	0x0	Clock bit input. 0=DVI_DDC_CLK pin input is low. 1=DVI_DDC_CLK pin input is high.
DVI_DDC_DATA_OUT_EN	16	0x0	Data pin output enable. 0=DVI_DDC_DATA output disabled. 1=DVI_DDC_DATA output enabled.
DVI_DDC_CLK_OUT_EN	17	0x0	Clock pin output enable. 0=DVI_DDC_CLK output disabled. 1=DVI_DDC_CLK output enabled.

Control and read of DDC clock and data lines for digital connector.

<b>CRT_CRTC_H_SYNC_STRT_WID - RW - 32 bits - [MMReg:0x258]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CRT_CRTC_H_SYNC_STRT_CHAR	12:3	0x0	Horizontal sync start position in characters(pixels * 8). Sum of display width, overscan right and front porch. If horizontal autocentering or fixed blank is enabled(see CRTC_MORE_CNTL) this field contains the offset (from the end of the active display/start of horizontal blank) within the blank time of the start of the horizontal sync signal for the CRT (in characters)
CRT_CRTC_H_SYNC_WID	21:16	0x0	Horizontal sync width in characters(pixels * 8) If horz. autocentering or fixed blank is enabled, this field contains the width (in characters) of the horizontal sync signal for the CRT.

Alternate Horizontal CRT Sync.

CRT HSync generated using this value when FP\_GEN\_CNTL.CRT\_ALT\_SYNC\_SEL = 1

<b>CRT_CRTC_V_SYNC_STRT_WID - RW - 32 bits - [MMReg:0x25C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CRT_CRTC_V_SYNC_STRT	11:0	0x0	Vertical sync start. Sum of display height, overscan bottom and front porch. If vertical auto-centering or fixed blank is enabled(see CRTC_MORE_CNTL) this field contains the offset (from the bottom of the active display/start of vertical blank) within the vertical blank time of the start of the vertical sync signal for the CRT (in lines)
CRT_CRTC_V_SYNC_WID	20:16	0x0	Vertical sync width (in lines). If vertical auto-centering or fixed blank is enabled this field contains the length (in lines) of the vertical sync signal for the CRT

Alternate Vertical CRT Sync.

CRT VSync generated using this value when FP\_GEN\_CNTL.CRT\_ALT\_SYNC\_SEL = 1

<b>FP_HORZ_VERT_ACTIVE - RW - 32 bits - [MMReg:0x278]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
FP_VERT_ACTIVE_SIZE	11:0	0x0	Vertical Active Display size (usually panel native height) in lines when vert. auto-centering is enabled.
FP_HORZ_ACTIVE_SIZE	24:16	0x0	Horizontal Active Display size (usually panel native width) in characters (8 pixels per character) when horz. auto-centering is enabled.

Active Display Size registers for auto-centering.

Using auto-centering in combination with ratiometric expansion and auto-ratio calculation should enable ratiometric expansion while preserving the aspect ratio of the original image.

<b>CRTC_MORE_CNTL - RW - 32 bits - [MMReg:0x27C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
CRTC_HORZ_BLANK_MODE_SEL	0	0x0	Selects horizontal retrace mode. Either traditional (0) or fixed blank (1). 0=CRTC H blank timings are relative to start of active. 1=CRTC H blank timings are relative to end of active.
CRTC_VERT_BLANK_MODE_SEL	1	0x0	Selects vertical retrace mode. Either traditional (0) or fixed blank (1). 0=CRTC V blank timings are relative to start of active. 1=CRTC V blank timings are relative to end of active.

CRTC_AUTO_HORZ_CENTER_EN	2	0x0	Enables horizontal auto-centering circuit. See FP_CRTC_H_TOTAL_DISP, FP_CRTC_V_TOTAL_DISP, CRT_CRTC_H_SYNC_STRT_WID, CRT_CRTC_V_SYNC_STRT_WID, FP_H_SYNC_STRT_WID, and FP_V_SYNC_STRT_WID. 0=H centering is manual. 1=H centering is automatic based on H_DISP and FP_HORZ_PANEL_SIZE.
CRTC_AUTO_VERT_CENTER_EN	3	0x0	Enables vertical auto-centering circuit. 0=V centering is manual. 1=V centering is automatic based on V_DISP and FP_VERT_PANEL_SIZE.
CRTC_H_CUTOFF_ACTIVE_EN	4	0x0	Enables horizontal active size forcing circuit. Uses FP_HORZ_STRETCH.FP_HORZ_PANEL_SIZE 0=No corrections to CRTC and/or RMX horizontal tim- ings. 1=Horizontal active forced to FP_HORZ_PANEL_SIZE by stretching or cutting off CRTC timings as needed.
CRTC_V_CUTOFF_ACTIVE_EN	5	0x0	Enables vertical active size forcing circuit. Uses FP_VERT_STRETCH.FP_VERT_PANEL_SIZE 0=No corrections to CRTC and/or RMX vertical timings. 1=Vertical active forced to FP_VERT_PANEL_SIZE by stretching or cutting off CRTC timings as needed.

## More CRTC controls

For 'fixed blank' and 'autocentering' modes, refer to registers FP\_CRTC\_H\_TOTAL\_DISP, FP\_CRTC\_V\_TOTAL\_DISP, FP\_H\_SYNC\_STRT\_WID, FP\_V\_SYNC\_STRT\_WID, CRT\_CRTC\_H\_SYNC\_STRT\_WID, and CRT\_CRTC\_V\_SYNC\_STRT\_WID. For 'autocentering' please also refer to FP\_HORZ\_VERT\_ACTIVE. When autocentering is enabled, fixed blanking is also enabled.

FP_HORZ_STRETCH - RW - 32 bits - [MMReg:0x28C]			
Field Name	Bits	Default	Description
FP_HORZ_STRETCH_RATIO	15:0	0x0	Horizontal RMX Stretch Ratio. When FP_HORZ_STRETCH_MODE = 0 (pixel replication), the value in this register is shifted out serially (LSB first, i.e. bit 0). If the value of the bit shifted out is a '0' then the next real (pre-replication) display pixel is loaded and displayed. If the bit shifted out is a '1' then the last pixel loaded will be duplicated and displayed. The bit shifter is looped back to bit 0 after either bit 9, 11, 12, 14, or 15 depending on the value of FP_LOOP_STRETCH. In pixel-replication mode, bit 0 of the ratio must always be set to '0'. When FP_HORZ_STRETCH_MODE = 1 (blending), valid values for the ratio are 1 to 4095. Ratio = ( (Active display width in characters (including overscan)) / (Panel width in characters)) x 4096 )

FP_HORZ_PANEL_SIZE	24:16	0x0	Digital Flat Panel (DFP) width in characters = ((panel width in pixels/8) - 1). Used when Automatic RMX Horizontal Ratio enabled
FP_HORZ_STRETCH_EN	25	0x0	0 = Disable Horizontal RMX. 1 = Enable Horz. RMX. 0=Horizontal stretching disabled. 1=Horizontal stretching enabled.
FP_HORZ_STRETCH_MODE	26	0x0	Panel horizontal stretch mode: 0 = pixel replication. 1 = horizontal blending. 0=Disables horizontal filter, giving pixel replication. 1=Enables horizontal filter blending.
FP_AUTO_HORZ_RATIO	27	0x0	0=Use FP_HORZ_STRETCH_RATIO as Hratio for RMX. 1=Use auto-calculated ratio for Hratio. Works in both VGA and Extended modes. 0=Use FP_HORZ_STRETCH_RATIO as Hratio for RMX. Required selection for non-VGA modes. 1=Use auto-calculated ratio for Hratio. Only available in VGA modes.
FP_LOOP_STRETCH	30:28	0x0	Panel horizontal 'pixel replication' loop back select: 0 = after bit 9 loop back to bit 0. 1 = after bit 11 loop back to bit 0. 2 = after bit 12 loop back to bit 0. 3 = after bit 14 loop back to bit 0. 4 = after bit 15 loop back to bit 0 0=Loop bit 0 back to bit 9 1=Loop bit 0 back to bit 11 2=Loop bit 0 back to bit 12 3=Loop bit 0 back to bit 14 4=Loop bit 0 back to bit 15
RMX_AUTO_RATIO_HORZ_INC	31	0x1	0=Horizontal auto ratio result truncated, i.e. rounded down. 1=Horizontal auto ratio result truncated, and then incremented by 1 i.e. rounded up. 0=Horizontal auto ratio result truncated, i.e. rounded down. 1=Horizontal auto ratio result truncated, and then incremented by 1.

Panel Horizontal Ratiometric(RMX) stretch control register

<b>VGA_BUFFER_CNTL - RW - 32 bits - [MMReg:0x2F4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
VGA_START_REQ	5:0	0x3c	Request watermark where display requests to memory controller will start.  NOTE: Bits 0:1 of this field are hardwired to ZERO.

VGA_STOP_REQ	13:8	0x3c	Request watermark where display requests to memory controller will stop.  NOTE: Bits 0:1 of this field are hardwired to ZERO.
VGA_CRITICAL_POINT	21:16	0x20	Read data watermark where pending display requests to the memory controller go to high priority. Setting 0x00 forces all display requests to remain high priority at all times.

Control of display buffer fill requests for VGA modes. This register is programmed by the BIOS on VGA mode switches.

<b>OV0_PIPELINE_CNTL - RW - 32 bits - [MMReg:0x408]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_DISP_PIPE_DELAY	3:0	0x8	Debug field used to adjust overlay window position. Leave at default unless hardware problem requires adjustment as instructed.

Debug adjustments for overlay window control

<b>OV0_SUBMIT_HISTORY - R - 32 bits - [MMReg:0x478]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_NEXT_BUF_NUM	2:0	0x0	
OV0_NEXT_IS_ODD	4	0x0	0=EVEN 1=ODD
OV0_CURR_BUF_NUM	10:8	0x0	
OV0_CURR_IS_ODD	12	0x0	0=EVEN 1=ODD
OV0_PREV_BUF_NUM	18:16	0x0	
OV0_PREV_IS_ODD	20	0x0	0=EVEN 1=ODD

No description available for this register.

<b>OV0_SLICE_CNTL - RW - 32 bits - [MMReg:0x4E0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_SLICE_LAST_LINE	6:0	0x0	

OV0_SLICEDONE_STAT (R)	30	0x0	0=Not done with slice. 1=Slice is done.
OV0_MPEG_EOF_TOGGLE	31	0x0	

No description available for this register.

<b>OV0_VID_KEY_CLR_HIGH - RW - 32 bits - [MMReg:0x4E8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
OV0_VID_KEY_Cb_BLUE_HIGH	9:0	0x0	Overlay/subpicture keyer Cb or blue component upper limit.
OV0_VID_KEY_Y_GREEN_HIGH	19:10	0x0	Overlay/subpicture keyer Y or green component upper limit.
OV0_VID_KEY_Cr_RED_HIGH	29:20	0x0	Overlay/subpicture keyer Cr or red component upper limit.

Overlay/subpicture range keyer upper limits. The overlay/subpicture blend unit output where keying is done is 30bpp. This is the data before color conversion or gamma adjustment.

<b>DISP_PWR_MAN - RW - 32 bits - [MMReg:0xD08]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DISP_PWR_MAN_D3_CRTC_EN	0	0x1	0=Resume display at previous CRTC settings on D3hot to D0 power state transition. 1=Leave CRTC idle on D3hot to D0 power transition until BIOS/driver re-initializes.
DISP_PWR_MAN_DPMS	9:8	0x0	0=DPMS On. HSYNC and VSYNC not blocked. 1=DPMS Standby. HSYNC blocked, VSYNC not blocked. 2=DPMS Suspend. VSYNC blocked, HSYNC not blocked. 3=DPMS Off. HSYNC and VSYNC blocked.
DISP_D3_RST	16	0x1	0=D3hot to D0 does not reset display. 1=D3hot to D0 resets all display blocks.
DISP_D3_REG_RST	17	0x1	0=D3hot to D0 does not reset display registers. 1=D3hot to D0 resets all display registers.
DISP_D3_GRP_H_RST	18	0x1	0=D3hot to D0 does not reset graphics logic. 1=D3hot to D0 resets graphics logic, but not registers.
DISP_D3_SUBPIC_RST	19	0x1	0=D3hot to D0 does not reset sub-picture logic. 1=D3hot to D0 resets sub-picture logic, but not registers.
DISP_D3_OV0_RST	20	0x1	0=D3hot to D0 does not reset ov0scale logic. 1=D3hot to D0 resets ov0scale logic, but not registers.
DISP_D1D2_GRP_H_RST	21	0x1	0=D1 or D2 to D0 does not reset graphics logic. 1=D1 or D2 to D0 resets graphics logic, but not registers.

Miscellaneous Registers

DISP_D1D2_SUBPIC_RST	22	0x1	0=D1 or D2 to D0 does not reset sub-picture logic. 1=D1 or D2 to D0 resets sub-picture logic, but not registers.
DISP_D1D2_OV0_RST	23	0x1	0=D1 or D2 to D0 does not reset ov0scale logic. 1=D1 or D2 to D0 resets ov0scale logic, but not registers.

No description available for this register.

<b>DAC_EMBEDDED_SYNC_CNTL - RW - 32 bits - [MMReg:0xDC0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DAC_EMBED_SYNC_EN_Y_G	0	0x0	0=Disable embedded sync on Y/G 1=Enable embedded sync on Y/G
DAC_EMBED_SYNC_EN_Cb_B	1	0x0	0=Disable embedded sync on Cb/B 1=Enable embedded sync on Cb/B
DAC_EMBED_SYNC_EN_Cr_R	2	0x0	0=Disable embedded sync on Cr/R 1=Enable embedded sync on Cr/R
DAC_TRILEVEL_SYNC_EN	3	0x0	0=Embedded sync only negative, if enabled 1=Embedded sync neg. and pos., if enabled

No description available for this register.

<b>DAC_BROAD_PULSE - RW - 32 bits - [MMReg:0xDC4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DAC_BROAD_PULSE_START	12:0	0x0	
DAC_BROAD_PULSE_END	28:16	0x0	

No description available for this register.

<b>DAC_SKEW_CLKS - RW - 32 bits - [MMReg:0xDC8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DAC_SKEW_CLKS	7:0	0x0	

No description available for this register.

<b>DAC_INCR - RW - 32 bits - [MMReg:0xDCC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DAC_INCR_Y_G	9:0	0x0	
DAC_INCR_CrCb_RB	25:16	0x0	

No description available for this register.

<b>DAC_NEG_SYNC_LEVEL - RW - 32 bits - [MMReg:0xDD0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DAC_NEG_SYNC_LEVEL_Y_G	9:0	0x0	
DAC_NEG_SYNC_LEVEL_CrCb_RB	25:16	0x0	

No description available for this register.

<b>DAC_POS_SYNC_LEVEL - RW - 32 bits - [MMReg:0xDD4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DAC_POS_SYNC_LEVEL_Y_G	9:0	0x0	
DAC_POS_SYNC_LEVEL_CrCb_RB	25:16	0x0	

No description available for this register.

<b>DAC_BLANK_LEVEL - RW - 32 bits - [MMReg:0xDD8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DAC_BLANK_LEVEL_Y_G	9:0	0x0	
DAC_BLANK_LEVEL_CrCb_RB	25:16	0x0	

No description available for this register.

CLOCK_CNTL_INDEX - RW - 32 bits - [IOReg,MMReg:0x8]			
Field Name	Bits	Default	Description
PLL_ADDR (DISPLAY) (CG) (CGM)	4:0	0x0	Indirect CG and PLL register index
PLL_WR_EN (DISPLAY) (CG) (CGM)	7	0x0	Indirect CG and PLL register write enable 0=Disable writes to CLOCK_CNTL_DATA 1=Enable writing to CLOCK_CNTL_DATA
PPLL_DIV_SEL (DISPLAY) (CG) (CGM)	9:8	0x0	Pixel clock PLL feedback division selection for non-VGA modes. Used when CRTC_GEN_CNTL.CRTC_EXT_DISP_EN=1. See GENMO_WT.VGA_CKSEL for pixel clock selection when VGA mode active. 0=PPLL_DIV0 1=PPLL_DIV1 2=PPLL_DIV2 3=PPLL_DIV3

CG and PLL indirect register control

CLOCK_CNTL_DATA - RW - 32 bits - [IOReg,MMReg:0xC]			
Field Name	Bits	Default	Description
PLL_DATA (DISPLAY) (CG) (CGM)	31:0	0x0	Data for write to CG and PLL indirect registers

Data for write to CG and PLL indirect registers

PPLL_DIV_0 - RW - 32 bits - CLKIND:0x4			
Field Name	Bits	Default	Description
PPLL_FB0_DIV (CG)	10:0	0x1bb	Feedback divider for pixel clock PLL. PLL output to post divider is PPIIClk = PPLL_REF * PPLL_FBx_DIV / PPLL_REF_DIV. PPIIClk required to always run in the 350 MHz >= PPIIClk >= 125 MHz range. For slower pixel clocks use the PPLL_POSTx_DIV field. The PPLL_FBx_DIV setting must be >= 4.

PPLL_ATOMIC_UPDATE_W <i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i> (W) (CG)	15	0x0	If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.
PPLL_ATOMIC_UPDATE_R <i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i> (R) (CG)	15	0x0	Readback of atomic update status.
PPLL_POST0_DIV (DISPLAY)	18:16	0x0	Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided. 0=/1 1=/2 2=/4 3=/8 4=/3 5=/16 6=/6 7=/12

Pixel clock PLL feedback and post division selection 0

PPLL_DIV_1 - RW - 32 bits - CLKIND:0x5			
Field Name	Bits	Default	Description
PPLL_FB1_DIV (CG)	10:0	0x1f2	Feedback divider for pixel clock PLL. PLL output to post divider is PPIIClk = PPLL_REF * PPLL_FBx_DIV / PPLL_REF_DIV. PPIIClk required to always run in the 350 MHz >= PPIIClk >= 125 MHz range. For slower pixel clocks us the PPLL_POSTx_DIV field. The PPLL_FBx_DIV setting must be >= 4.
PPLL_ATOMIC_UPDATE_W <i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i> (W) (CG)	15	0x0	If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.

PPLL_ATOMIC_UPDATE_R  <i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i> (R)  (CG)	15	0x0	Readback of atomic update status.
PPLL_POST1_DIV  (DISPLAY)	18:16	0x0	Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided. 0=/1 1=/2 2=/4 3=/8 4=/3 5=/16 6=/6 7=/12

Pixel clock PLL feedback and post division selection 1

PPLL_DIV_2 - RW - 32 bits - CLKIND:0x6			
Field Name	Bits	Default	Description
PPLL_FB2_DIV  (CG)	10:0	0x1bb	Feedback divider for pixel clock PLL. PLL output to post divider is PPIIClk = PPLL_REF * PPLL_FBx_DIV / PPLL_REF_DIV. PPIIClk required to always run in the 350 MHz >= PPIIClk >= 125 MHz range. For slower pixel clocks us the PPLL_POSTx_DIV field. The PPLL_FBx_DIV setting must be >= 4.
PPLL_ATOMIC_UPDATE_W  <i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i> (W)  (CG)	15	0x0	If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.
PPLL_ATOMIC_UPDATE_R  <i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i> (R)  (CG)	15	0x0	Readback of atomic update status.

PPLL_POST2_DIV (DISPLAY)	18:16	0x0	Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided. 0=/1 1=/2 2=/4 3=/8 4=/3 5=/16 6=/6 7=/12
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Pixel clock PLL feedback and post division selection 2

PPLL_DIV_3 - RW - 32 bits - CLKIND:0x7			
Field Name	Bits	Default	Description
PPLL_FB3_DIV (CG)	10:0	0x1bb	Feedback divider for pixel clock PLL. PLL output to post divider is $PPIIClk = PPLL\_REF * PPLL\_FBx\_DIV / PPLL\_REF\_DIV$ . PPIIClk required to always run in the 350 MHz $\geq$ PPIIClk $\geq$ 125 MHz range. For slower pixel clocks use the PPLL_POSTx_DIV field. The PPLL_FBx_DIV setting must be $\geq$ 4.
PPLL_ATOMIC_UPDATE_W <i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i> (W) (CG)	15	0x0	If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.
PPLL_ATOMIC_UPDATE_R <i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i> (R) (CG)	15	0x0	Readback of atomic update status.
PPLL_POST3_DIV (DISPLAY)	18:16	0x0	Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided. 0=/1 1=/2 2=/4 3=/8 4=/3 5=/16 6=/6 7=/12

Pixel clock PLL feedback and post division selection 3

VCLK_ECP_CNTL - RW - 32 bits - CLKIND:0x8			
Field Name	Bits	Default	Description
VCLK_SRC_SEL (DISPLAY)	1:0	0x0	Selects source of PIXCLK. The output of this mux selection is post divided by PPLL_POSTx_DIV to create the final PIXCLK. If set to BYTE_CLK, then see BYTE_CLK_POST_DIV below to select the PIXCLK source. Both the clock source you are switching to and from must be running, or the switch will not occur. 0=CPUCLK 1=PSCANCLK 2=BYTE_CLK 3=PPIIClk
VCLK_INVERT (DISPLAY)	4	0x0	Used to invert PPIIClk to get opposite duty cycle. Only takes effect when VCLK_SRC_SEL is using PPIIClk, and PPLL_POSTx_DIV is divide-by-1. Don't care in other cases. 0=Not Invert 1=Invert
ECP_DIV (DISPLAY)	9:8	0x0	OV0CLK clock speed select. Should always be set to 00 for PIXCLK <= 175 MHz and to 01 for PIXCLK > 175 MHz. When set to 01, the overlay and subpic horizontal scale parameters must be adjusted for the extra horizontal replication this causes. Settings 10 and 11 are reserved. 0=OV0CLK = PIXCLK 1=OV0CLK = PIXCLK/2
BYTE_CLK_POST_DIV (DISPLAY)	17:16	0x0	Selects the source of BYTE_CLK when TV output port is enabled. Select BYTCLK input pin when ImpactTV/Rage Theater are to be the dot clock source. Select the appropriate post-divider when Rage graphics chip is to supply the dot clock source. In this case, this post-divider determines the speed of BYTE_CLK to the ImpactTV/Rage Theater, and the PPLL_POSTx_DIV determines if 16 or 24 data bits per pixel are sent over. Don't care if VCLK_SRC_SEL <> 10. 0=BYTE_CLK = BYTCLK (input pin) 1=BYTE_CLK = PPIIClk/2 2=BYTE_CLK = PPIIClk/3 3=BYTE_CLK = PPIIClk/4
ECP_FORCE_ON (DISPLAY)	18	0x0	Controls the dynamic clock control for the back-end overlay/scaler. Set to low for power reduction. 0=SCALER ACTIVITY 1=CONTINUOUS

BYTE_CLK_OUT_EN (DISPLAY)	20	0x0	Controls the function of the BYTCLK pin. When BYTE_CLK_POST_DIV = 00 (BYTCLK input), then this bit should be low (tri state). For other settings of BYTE_CLK_POST_DIV, this bit should be high to drive the clock to the TV encoder chip. 0=Disable 1=Enable
BYTE_CLK_SKEW (DISPLAY)	26:24	0x0	Selects phase of internally generated BYTE_CLK to PIX-CLK. Don't care if BYTE_CLK_POST_DIV = 00 (external input). Used to do alignment of TV out data with clock when Rage graphics chip is generating the dot clock for TV output. Selects phase in 1/2 PPIIClk increments. Valid range depends on BYTE_CLK_POST_DIV setting, and may not exceed (2*byte clock post divider)-1. e.g. for byte clock post divider of 3 (BYTE_CLK_POST_DIV=10), then (2*3)-1=5, so BYTE_CLK_SKEW has range 0 to 5.

General controls for the display clocks.  
VCLK is the pixel, or dot, clock.  
ECP is the overlay/scaler clock.

HTOTAL_CNTL - RW - 32 bits - CLKIND:0x9			
Field Name	Bits	Default	Description
HTOT_PIX_SLIP (DISPLAY)	3:0	0x0	Pixel accurate control of horizontal total. Selects the extra number of pixels to add to each display line. Valid range is 0 to 15. For VGA modes with SEQ_PCLKBY2 = 1 each increment adds one physical pixel or 1/2 a logical pixel to the line total. For 9-dot 40 column VGA text modes, it is not possible to add 16/18ths or 17/18ths of a character extra to the display line times.
HTOT_VCLK_SLIP (DISPLAY)	11:8	0x0	Reserved for future use. No affect in this ASIC.
HTOT_PPLL_SLIP (DISPLAY) (CG)	18:16	0x0	Select the number of 1/5 PPIIClk phase slips to do in the PLL at every HSYNC. This is used as a sub-pixel accurate adjustment of the frame rate for TV out or video gen-locking.
HTOT_CNTL_EDGE (DISPLAY) (CG)	24	0x0	Select which HSYNC edge the slip correction based on HTOT_PPLL_SLIP is done. 0=Falling edge of DAC HSYNC 1=Rising edge of DAC HSYNC

HTOT_CNTL_VGA_EN (DISPLAY) (CG)	28	0x0	Select if the slip controls based on HTOT_PIX_SLIP, HTOT_VCLK_SLIP and HTOT_PPLL_SLIP are enabled for VGA mode. These are always enabled for non-VGA modes when the respective fields are non-zero. 0=Disable 1=Enable
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Horizontal total control. Used to fine-tune the horizontal total. This lengthens the time of each display line by sub-character and/or sub-pixel amounts. The purpose is fine adjustment of the overall frame refresh rate for applications that require it (e.g. TV output, GEN-lock to video input).

PLL_TEST_CNTL - RW - 32 bits - CLKIND:0x13			
Field Name	Bits	Default	Description
TST_SRC_SEL (CG) (CGM)	4:0	0x0	Select different clock source to readable counter and as test clock output
TST_SRC_INV (CG) (CGM)	7	0x0	Invert test clock output
TST_DIVIDERS (CG) (CGM)	8	0x0	Enable driver test
PLL_MASK_READ_B (CG) (CGM)	9	0x1	Mask test clock output and 3 LSBs of readable counter
TESTCLK_MUX_SEL (CG)	12	0x0	0=cg 1=cgm
ANALOG_MON (DISPLAY)	19:16	0x0	
TEST_COUNT (R) (CG) (CGM)	31:24	0x0	Readable counter read back

CG and PLL test control

CP_STAT - R - 32 bits - [MMReg:0x7C0]			
Field Name	Bits	Default	Description
MRU_BUSY	0	0x0	
MWU_BUSY	1	0x0	

RSIU_BUSY	2	0x0	
RCIU_BUSY	3	0x0	
CSF_PRIMARY_BUSY	9	0x0	
CSF_INDIRECT_BUSY	10	0x0	
CSQ_PRIMARY_BUSY	11	0x0	
CSQ_INDIRECT_BUSY	12	0x0	
CSI_BUSY	13	0x0	
GUIDMA_BUSY	28	0x0	
VIDDMA_BUSY	29	0x0	
CMDSTRM_BUSY	30	0x0	
CP_BUSY	31	0x0	

No description available for this register.

<b>RE_TOP_LEFT - RW - 32 bits - [MMReg:0x26C0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
X_LEFT	10:0	0x0	
Y_TOP	26:16	0x0	

No description available for this register.

<b>RE_AUX_SCISSOR_CNTL - RW - 32 bits - [MMReg:0x26F0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
EXCLUSIVE_SCISSOR_0	24	0x0	0=Inclusive 1=Exclusive
EXCLUSIVE_SCISSOR_1	25	0x0	0=Inclusive 1=Exclusive
EXCLUSIVE_SCISSOR_2	26	0x0	0=Inclusive 1=Exclusive
SCISSOR_ENABLE_0	28	0x0	0=Disable Scissor Plane 1=Enable Scissor Plane
SCISSOR_ENABLE_1	29	0x0	0=Disable Scissor Plane 1=Enable Scissor Plane

SCISSOR_ENABLE_2	30	0x0	0=Disable Scissor Plane 1=Enable Scissor Plane
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No description available for this register.

RE_NULL_PRIM - W - 32 bits - [MMReg:0x29E0]			
Field Name	Bits	Default	Description

No description available for this register.

RE_Z_MINMAX_0 - W - 32 bits - [MMReg:0x29F0]			
Field Name	Bits	Default	Description
Z_MINMAX_LO	31:0	0x0	

No description available for this register.

RE_Z_MINMAX_1 - W - 32 bits - [MMReg:0x29F4]			
Field Name	Bits	Default	Description
Z_MINMAX_HI	8:0	0x0	

No description available for this register.

RE_Z_MINMAX_3 - W - 32 bits - [MMReg:0x29FC]			
Field Name	Bits	Default	Description
ZEXPO	31:24	0x0	

No description available for this register.

RE_DDA_RHW_0 - W - 32 bits - [MMReg:0x2730]			
Field Name	Bits	Default	Description
RHWSTART_LO	31:0	0x0	

No description available for this register.

<b>RE_DDA_RHW_1 - W - 32 bits - [MMReg:0x2734]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
RHWSTART_H	8:0	0x0	
DRHWDX_L	31:9	0x0	

No description available for this register.

<b>RE_DDA_RHW_2 - W - 32 bits - [MMReg:0x2738]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DRHWDX_H	15:0	0x0	
DRHWDY_L	31:16	0x0	

No description available for this register.

<b>RE_DDA_RHW_3 - W - 32 bits - [MMReg:0x273C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DRHWDY_H	22:0	0x0	
RHWEXPO	31:24	0x0	

No description available for this register.

<b>RE_DDA_S3_0 - W - 32 bits - [MMReg:0x2880]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
S3START_L	31:0	0x0	

No description available for this register.

<b>RE_DDA_S3_1 - W - 32 bits - [MMReg:0x2884]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
S3START_H	8:0	0x0	
DS3DX_L	31:9	0x0	

No description available for this register.

<b>RE_DDA_S3_2 - W - 32 bits - [MMReg:0x2888]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DS3DX_H	15:0	0x0	
DS3DY_L	31:16	0x0	

No description available for this register.

<b>RE_DDA_S3_3 - W - 32 bits - [MMReg:0x288C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DS3DY_H	22:0	0x0	
NON_PARAMETRIC	23	0x0	
S3EXPO	31:24	0x0	

No description available for this register.

<b>RE_DDA_T3_0 - W - 32 bits - [MMReg:0x2890]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
T3START_L	31:0	0x0	

No description available for this register.

<b>RE_DDA_T3_1 - W - 32 bits - [MMReg:0x2894]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
T3START_H	8:0	0x0	
DT3DX_L	31:9	0x0	

No description available for this register.

<b>RE_DDA_T3_2 - W - 32 bits - [MMReg:0x2898]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DT3DX_H	15:0	0x0	
DT3DY_L	31:16	0x0	

No description available for this register.

<b>RE_DDA_T3_3 - W - 32 bits - [MMReg:0x289C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DT3DY_H	22:0	0x0	
T3EXPO	31:24	0x0	

No description available for this register.

<b>RE_DDA_Q3_0 - W - 32 bits - [MMReg:0x28B0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
Q3START_L	31:0	0x0	

No description available for this register.

<b>RE_DDA_Q3_1 - W - 32 bits - [MMReg:0x28B4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
Q3START_H	8:0	0x0	
DQ3DX_L	31:9	0x0	

No description available for this register.

<b>RE_DDA_Q3_2 - W - 32 bits - [MMReg:0x28B8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
DQ3DX_H	15:0	0x0	

DQ3DY_L	31:16	0x0	
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No description available for this register.

RE_DDA_Q3_3 - W - 32 bits - [MMReg:0x28BC]			
Field Name	Bits	Default	Description
DQ3DY_H	22:0	0x0	
Q3EXPO	31:24	0x0	

No description available for this register.

RE_DDA_DS3_0 - W - 32 bits - [MMReg:0x2940]			
Field Name	Bits	Default	Description
DS3XSTART	31:0	0x0	

No description available for this register.

RE_DDA_DS3_1 - W - 32 bits - [MMReg:0x2944]			
Field Name	Bits	Default	Description
DS3YSTART	31:0	0x0	

No description available for this register.

RE_DDA_DS3_2 - W - 32 bits - [MMReg:0x2948]			
Field Name	Bits	Default	Description
DS3INC	31:0	0x0	

No description available for this register.

RE_DDA_DS3_3 - W - 32 bits - [MMReg:0x294C]			
Field Name	Bits	Default	Description
DS3EXPO	31:24	0x0	

No description available for this register.

**RE\_DDA\_DT3\_0 - W - 32 bits - [MMReg:0x2960]**

Field Name	Bits	Default	Description
DT3XSTART	31:0	0x0	

No description available for this register.

**RE\_DDA\_DT3\_1 - W - 32 bits - [MMReg:0x2964]**

Field Name	Bits	Default	Description
DT3YSTART	31:0	0x0	

No description available for this register.

**RE\_DDA\_DT3\_2 - W - 32 bits - [MMReg:0x2968]**

Field Name	Bits	Default	Description
DT3INC	31:0	0x0	

No description available for this register.

**RE\_DDA\_DT3\_3 - W - 32 bits - [MMReg:0x296C]**

Field Name	Bits	Default	Description
DT3EXPO	31:24	0x0	

No description available for this register.

**PP\_CUBIC\_OFFSET\_T0\_0 - RW - 32 bits - [MMReg:0x1DD0] [MMReg:0x2DD0]**

Field Name	Bits	Default	Description
FACE_OFFSET	31:5	0x0	

No description available for this register.

<b>PP_CUBIC_OFFSET_T0_1 - RW - 32 bits - [MMReg:0x1DD4] [MMReg:0x2DD4]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
FACE_OFFSET	31:5	0x0	

No description available for this register.

<b>PP_CUBIC_OFFSET_T0_2 - RW - 32 bits - [MMReg:0x1DD8] [MMReg:0x2DD8]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
FACE_OFFSET	31:5	0x0	

No description available for this register.

<b>PP_CUBIC_OFFSET_T0_3 - RW - 32 bits - [MMReg:0x1DDC] [MMReg:0x2DDC]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
FACE_OFFSET	31:5	0x0	

No description available for this register.

<b>PP_CUBIC_OFFSET_T0_4 - RW - 32 bits - [MMReg:0x1DE0] [MMReg:0x2DE0]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
FACE_OFFSET	31:5	0x0	

No description available for this register.

<b>PP_CUBIC_OFFSET_T1_0 - RW - 32 bits - [MMReg:0x1E00] [MMReg:0x2E00]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
FACE_OFFSET	31:5	0x0	

No description available for this register.

**PP\_CUBIC\_OFFSET\_T1\_1 - RW - 32 bits - [MMReg:0x1E04] [MMReg:0x2E04]**

Field Name	Bits	Default	Description
FACE_OFFSET	31:5	0x0	

No description available for this register.

**PP\_CUBIC\_OFFSET\_T1\_2 - RW - 32 bits - [MMReg:0x1E08] [MMReg:0x2E08]**

Field Name	Bits	Default	Description
FACE_OFFSET	31:5	0x0	

No description available for this register.

**PP\_CUBIC\_OFFSET\_T1\_3 - RW - 32 bits - [MMReg:0x1E0C] [MMReg:0x2E0C]**

Field Name	Bits	Default	Description
FACE_OFFSET	31:5	0x0	

No description available for this register.

**PP\_CUBIC\_OFFSET\_T1\_4 - RW - 32 bits - [MMReg:0x1E10] [MMReg:0x2E10]**

Field Name	Bits	Default	Description
FACE_OFFSET	31:5	0x0	

No description available for this register.

**PP\_CUBIC\_OFFSET\_T2\_0 - RW - 32 bits - [MMReg:0x1E14] [MMReg:0x2E14]**

Field Name	Bits	Default	Description
FACE_OFFSET	31:5	0x0	

No description available for this register.

<b>PP_CUBIC_OFFSET_T2_1 - RW - 32 bits - [MMReg:0x1E18] [MMReg:0x2E18]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
FACE_OFFSET	31:5	0x0	

No description available for this register.

<b>PP_CUBIC_OFFSET_T2_2 - RW - 32 bits - [MMReg:0x1E1C] [MMReg:0x2E1C]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
FACE_OFFSET	31:5	0x0	

No description available for this register.

<b>PP_CUBIC_OFFSET_T2_3 - RW - 32 bits - [MMReg:0x1E20] [MMReg:0x2E20]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
FACE_OFFSET	31:5	0x0	

No description available for this register.

<b>PP_CUBIC_OFFSET_T2_4 - RW - 32 bits - [MMReg:0x1E24] [MMReg:0x2E24]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
FACE_OFFSET	31:5	0x0	

No description available for this register.

<b>PP_CUBIC_OFFSET_T3_0 - RW - 32 bits - [MMReg:0x2E28]</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
FACE_OFFSET	31:5	0x0	

No description available for this register.

**PP\_CUBIC\_OFFSET\_T3\_1 - RW - 32 bits - [MMReg:0x2E2C]**

Field Name	Bits	Default	Description
FACE_OFFSET	31:5	0x0	

No description available for this register.

**PP\_CUBIC\_OFFSET\_T3\_2 - RW - 32 bits - [MMReg:0x2E30]**

Field Name	Bits	Default	Description
FACE_OFFSET	31:5	0x0	

No description available for this register.

**PP\_CUBIC\_OFFSET\_T3\_3 - RW - 32 bits - [MMReg:0x2E34]**

Field Name	Bits	Default	Description
FACE_OFFSET	31:5	0x0	

No description available for this register.

**PP\_CUBIC\_OFFSET\_T3\_4 - RW - 32 bits - [MMReg:0x2E38]**

Field Name	Bits	Default	Description
FACE_OFFSET	31:5	0x0	

No description available for this register.

**PP\_ROT\_MATRIX\_0 - RW - 32 bits - [MMReg:0x1D58] [MMReg:0x2D58]**

Field Name	Bits	Default	Description
M00_MAN	10:0	0x0	
M10_MAN	26:16	0x0	
Mx0_EXPO	30:27	0x0	

No description available for this register.

PP_ROT_MATRIX_1 - RW - 32 bits - [MMReg:0x1D5C] [MMReg:0x2D5C]			
Field Name	Bits	Default	Description
M01_MAN	10:0	0x0	
M11_MAN	26:16	0x0	
Mx1_EXPO	30:27	0x0	

No description available for this register.

PP_LUM_MATRIX - RW - 32 bits - [MMReg:0x1D00] [MMReg:0x2D00]			
Field Name	Bits	Default	Description
LSCALE	7:0	0x0	
LOFFSET	15:8	0x0	

No description available for this register.

PP_TRI_JUICE - RW - 32 bits - [MMReg:0x2D64]			
Field Name	Bits	Default	Description
TRI_JUICE	4:0	0x0	

No description available for this register.

RB2D_DSTCACHE_MODE - RW - 32 bits - [MMReg:0x3428]			
Field Name	Bits	Default	Description
DC_BYPASS <i>(mirror of RB3D_DSTCACHE_MODE:DC_BYPASS)</i>	1:0	0x0	Dst Cache Bypass, Disables cache when set. This field is cleared to 0 on reset so that by default, both destination caches are enabled. 0=3D cache enabled, 2D cache enabled (Default) 1=3D cache enabled, 2D cache disabled 2=3D cache disabled, 2D cache enabled 3=3D cache disabled, 2D cache disabled
DC_LINE_SIZE <i>(mirror of RB3D_DSTCACHE_MODE:DC_LINE_SIZE)</i>	3:2	0x0	0=256-bit 3D, 256-bit 2D lines (Default) 1=256-bit 3D, 128-bit 2D lines 2=128-bit 3D, 256-bit 2D lines 3=128-bit 3D, 128-bit 2D lines

DC_AUTOFLUSH_ENABLE <i>(mirror of RB3D_DSTCACHE_MODE:DC_AUTOFLUSH_ENABLE)</i>	9:8	0x0	0=No autoflush 3D, no autoflush 2D 1=No autoflush 3D, autoflush 2D 2=Autoflush 3D, no autoflush 2D 3=Autoflush 3D, autoflush 2D (Default)
DC_FORCE_RMW <i>(mirror of RB3D_DSTCACHE_MODE:DC_FORCE_RMW)</i>	16	0x0	Dst Cache Force Read-Modify-Write, Controls whether or not to optimize for write-only Dst modes. This bit is reset to 0 and is intended for debug purposes only. 0=Write-only Enabled 1=Write-only Disabled
DC_DISABLE_RI_FILL <i>(mirror of RB3D_DSTCACHE_MODE:DC_DISABLE_RI_FILL)</i>	24	0x0	0=Enabled 1=Disabled
DC_DISABLE_RI_READ <i>(mirror of RB3D_DSTCACHE_MODE:DC_DISABLE_RI_READ)</i>	25	0x0	0=Enabled 1=Disabled

Dst Cache Mode, Alias to RB3D\_CACHE\_MODE Dst Cache Bypass , Alias to RB3D\_CACHE\_MODE.DC\_BYPASS Dst Cache Force Read-Modify-Write , Alias to RB3D\_CACHE\_MODE.DC\_FORCE\_RMW Dst Cache Disable Fill Check , Alias to RB3D\_CACHE\_MODE.DC\_RI\_FILL Dst Cache Disable Read Check, Alias to RB3D\_CACHE\_MODE.DC\_RI\_READ

RB2D_DSTCACHE_CTLSTAT - RW - 32 bits - [MMReg:0x342C]			
Field Name	Bits	Default	Description
DC_FLUSH <i>(mirror of RB3D_DSTCACHE_CTLSTAT:DC_FLUSH)</i>	1:0	0x0	Dst Cache Flush, Setting this bit flushes dirty data from the 2D and/or 3D Dst Cache. Unless the DC_FREE bits are also set, the tags in the cache remain valid. A purge is achieved by setting both DC_FLUSH and DC_FREE. These are sticky bits that clear themselves at the end of the flush operation. 0=No effect 1=Flush dirty 2D Dst Data 2=Flush dirty 2D Dst Data 3=Flush all dirty Dst Data
DC_FREE <i>(mirror of RB3D_DSTCACHE_CTLSTAT:DC_FREE)</i>	3:2	0x0	Dst Cache Free, Setting this bit invalidates the 2D and/or 3D Dst Cache tags. Unless the DC_FLUSH bit is also set, the cache lines are not written to memory. A purge is achieved by setting both DC_FLUSH and DC_FREE. These are sticky bits that clear themselves at the end of the flush operation. 0=No effect 1=Free 2D Dst tags 2=Free 3D Dst tags 3=Free all Dst tags

DC_BUSY  <i>(mirror of RB3D_DSTCACHE_CTLSTAT:DC_BUSY)</i>	31	0x0	Dst Cache Busy. 0=Idle 1=Busy
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Dst Cache Control and Status, Alias to RB3D\_CACHE\_MODE Dst Cache Flush , Alias to RB3D\_CACHE\_MODE.DC\_FLUSH  
 Dst Cache Free, Alias to RB3D\_CACHE\_MODE.DC\_FREE Dst Cache Read Invalidate, Alias to RB3D\_CACHE\_MODE.DC\_RI  
 Dst Cache Busy, Alias to RB3D\_CACHE\_MODE.DC\_BUSY

RB2D_SRC_ENDIAN - R - 32 bits - [MMReg:0x3430]			
Field Name	Bits	Default	Description
SRC_ENDIAN	1:0	0x0	0=No swap 1=Word swap 2=Dword swap 3=RESERVED

No description available for this register.

RB2D_DST_ENDIAN - R - 32 bits - [MMReg:0x3434]			
Field Name	Bits	Default	Description
DST_ENDIAN	1:0	0x0	0=No swap 1=Word swap 2=Dword swap 3=RESERVED

No description available for this register.

RB2D_PD1_DATA - RW - 32 bits - [MMReg:0x3438]			
Field Name	Bits	Default	Description
PD1_DATA	31:0	0x0	

No description available for this register.

RB2D_PD1_ADDR - RW - 32 bits - [MMReg:0x343C]			
Field Name	Bits	Default	Description
PD1_ADDR	2:0	0x0	

No description available for this register.

**RB2D\_WRITEBACK\_DATA\_LO - RW - 32 bits - [MMReg:0x3450]**

Field Name	Bits	Default	Description
WRITEBACK_DATA_LO <i>(mirror of RB3D_WRITEBACK_DATA_LO:WRITEBACK_DATA_LO)</i>	31:0	0x0	Write-back Data Register Lo , Lower DWORD for write-back. The transfer to memory occurs when WRITEBACK_ADDR is written.

Write-back Data Register Lo, Alias to RB3D\_WRITEBACK\_DATA\_LO. Write-back Data Register Lo, Alias to RB3D\_WRITEBACK\_DATA\_LO.WRITEBACK\_DATA\_LO.

**RB2D\_WRITEBACK\_DATA\_HI - RW - 32 bits - [MMReg:0x3454]**

Field Name	Bits	Default	Description
WRITEBACK_DATA_HI <i>(mirror of RB3D_WRITEBACK_DATA_HI:WRITEBACK_DATA_HI)</i>	31:0	0x0	Write-back Data Register Hi , Upper DWORD for registers write-back. The transfer to memory occurs when WRITEBACK_ADDR is written.

Write-back Data Register Hi , Alias to RB3D\_WRITEBACK\_DATA\_HI Write-back Data Register Hi , Alias to RB3D\_WRITEBACK\_DATA\_HI.WRITEBACK\_DATA\_HI.

**RB2D\_WRITEBACK\_ADDR - RW - 32 bits - [MMReg:0x3458]**

Field Name	Bits	Default	Description
WRITEBACK_ADDR <i>(mirror of RB3D_WRITEBACK_ADDR:WRITEBACK_ADDR)</i>	31:3	0x0	Write-back Address Register , Address to write DWORDS to. The transfer to memory occurs when WRITEBACK_ADDR is written. The 64-bits pointed to by this address is written with WRITEBACK_DATA_HI and WRITEBACK_DATA_LO.

Write-back Address Register , Alias to RB3D\_WRITEBACK\_ADDR. Write-back Address Register , Alias to RB3D\_WRITEBACK\_ADDR.WRITEBACK\_ADDR.

**RB3D\_DEPTHXY\_OFFSET - RW - 32 bits - [MMReg:0x1D60]**

Field Name	Bits	Default	Description
DEPTHX_OFFSET	11:0	0x0	
DEPTY_OFFSET	27:16	0x0	

No description available for this register.

DP_DST_ENDIAN - W - 32 bits - [MMReg:0x15D0]			
Field Name	Bits	Default	Description
DST_ENDIAN	1:0	0x0	0=no swap 1=16 bit swap 2=32 bit swap 3=half dword swap

00 = No swap (the default after reset, for all the endian converters) 01 = 16bit swap: 0xAABBCCDD becomes 0xBBAADDCC 10 = 32bit swap: 0xAABBCCDD becomes 0xDDCCBBAA 11 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB Write to E2\_DP\_DST\_ENDIAN

DP_SRC_ENDIAN - W - 32 bits - [MMReg:0x15D4]			
Field Name	Bits	Default	Description
SRC_ENDIAN	1:0	0x0	0=no swap 1=16 bit swap 2=32 bit swap 3=half dword swap

00 = No swap (the default after reset, for all the endian converters) 01 = 16bit swap: 0xAABBCCDD becomes 0xBBAADDCC 10 = 32bit swap: 0xAABBCCDD becomes 0xDDCCBBAA 11 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB Write to E2\_DP\_SRC\_ENDIAN

DP_CNTL_XDIR_YDIR_YMAJOR - W - 32 bits - [MMReg:0x16D0]			
Field Name	Bits	Default	Description
DST_Y_DIR	15	0x0	0=bottom to top 1=top to bottom
DST_X_DIR	31	0x0	0=right to left 1=left to right

No description available for this register.

DSTCACHE_MODE - W - 32 bits - [MMReg:0x1710]			
Field Name	Bits	Default	Description
DSTCACHE_MODE	31:0	0x0	

No description available for this register.

**DSTCACHE\_CTLSTAT - W - 32 bits - [MMReg:0x1714]**

Field Name	Bits	Default	Description
DSTCACHE_CTLSTAT	31:0	0x0	

No description available for this register.

**TVOUT\_0\_SCRATCH - RW - 32 bits - [IOReg,MMReg:0x88]**

Field Name	Bits	Default	Description
TVOUT_0_SCRATCH	31:0	0x0	

No description available for this register.

**TVOUT\_1\_SCRATCH - RW - 32 bits - [IOReg,MMReg:0x8C]**

Field Name	Bits	Default	Description
TVOUT_1_SCRATCH	31:0	0x0	

No description available for this register.

**VIPPAD\_STRENGTH - RW - 32 bits - [MMReg:0x194]**

Field Name	Bits	Default	Description
I2C_STRENGTH	1:0	0x2	0=Minimum drive. ~74 ohms. 1=Matched impedance drive. ~63 ohms. 2=Optimal drive. ~47 ohms. 3=Maximum drive. ~42 ohms.
TVDAT_STRENGTH	9:8	0x2	0=Minimum drive. ~74 ohms. 1=Matched impedance drive. ~63 ohms. 2=Optimal drive. ~47 ohms. 3=Maximum drive. ~42 ohms.
TVCLK_STRENGTH	13:12	0x2	0=Minimum drive. ~74 ohms. 1=Matched impedance drive. ~63 ohms. 2=Optimal drive. ~47 ohms. 3=Maximum drive. ~42 ohms.
VIPHDAT_STRENGTH	17:16	0x2	0=Minimum drive. ~74 ohms. 1=Matched impedance drive. ~63 ohms. 2=Optimal drive. ~47 ohms. 3=Maximum drive. ~42 ohms.

Miscellaneous Registers

VIPCLK_STRENGTH	21:20	0x2	0=Minimum drive. ~74 ohms. 1=Matched impedance drive. ~63 ohms. 2=Optimal drive. ~47 ohms. 3=Maximum drive. ~42 ohms.
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No description available for this register.

VIPPAD1_MASK - RW - 32 bits - [MMReg:0x1A8]			
Field Name	Bits	Default	Description
VIPPAD1_MASK	17:0	0x0	

No description available for this register.

VIPPAD1_Y - R - 32 bits - [MMReg:0x1B4]			
Field Name	Bits	Default	Description
VIPPAD1_Y	17:0	0x0	

No description available for this register.

EXTERN_TRIG_CNTL - RW - 32 bits - [MMReg:0x1BC]			
Field Name	Bits	Default	Description
EXTERN_TRIG_CLR (W)	0	0x0	0=Write 0 has no affect. 1=Write 1 sets EXTERN_TRIG to 0. This can then be used with WAIT_UNTIL(19) to stall until external signal pulses.
EXTERN_TRIG_READ (R)	1	0x0	0=Read 1 indicates WAIT condition not active. 1=Read 0 indicates WAIT condition active.

No description available for this register.

MEDIA_0_SCRATCH - RW - 32 bits - [MMReg:0x1F0]			
Field Name	Bits	Default	Description
MEDIA_0_SCRATCH	31:0	0x0	

No description available for this register.

**MEDIA\_1\_SCRATCH - RW - 32 bits - [MMReg:0x1F4]**

Field Name	Bits	Default	Description
MEDIA_1_SCRACH	31:0	0x0	

No description available for this register.

**CAP0\_ANC\_BUF01\_BLOCK\_CNT - R - 32 bits - [MMReg:0x974]**

Field Name	Bits	Default	Description
CAP0_ANC_BUF0_BLOCK_CNT	11:0	0x0	
CAP0_ANC_BUF1_BLOCK_CNT	27:16	0x0	

No description available for this register.

**CAP0\_ANC\_BUF23\_BLOCK\_CNT - R - 32 bits - [MMReg:0x97C]**

Field Name	Bits	Default	Description
CAP0_ANC_BUF2_BLOCK_CNT	11:0	0x0	
CAP0_ANC_BUF3_BLOCK_CNT	27:16	0x0	

No description available for this register.

**TMDS\_PATTERN\_GEN\_SEED - RW - 32 bits - [MMReg:0x2AC]**

Field Name	Bits	Default	Description
PATTERN_SEED	23:0	0x222222 2	24-bit seed value for random number generator

Random number generator seed register

**CLK\_PIN\_CNTL - RW - 32 bits - CLKIND:0x1**

Field Name	Bits	Default	Description
OSC_EN (CG)	0	0x1	Oscillation enable 0=Disable 1=Enable

XTL_LOW_GAIN (CG)	2	0x1	Oscillator high gain or low gain control 0=High Gain 1=Low Gain
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Clock pin control

PPLL_CNTL - RW - 32 bits - CLKIND:0x2			
Field Name	Bits	Default	Description
PPLL_RESET (CG)	0	0x1	Power down pixel clock PLL 0=Not Reset 1=Reset
PPLL_SLEEP (CG)	1	0x1	Reset pixel clock PLL 1=Powerdown
PPLL_TST_EN (CG)	2	0x0	Enable pixel clock PLL test mode
PPLL_REFCLK_SEL (CG)	4	0x0	0=not flopped 1=flopped
PPLL_FBCLK_SEL (CG)	5	0x0	0=not flopped 1=flopped
PPLL_TCPOFF (CG)	6	0x0	0=normal 1=test mode: Hi-Z
PPLL_TVCOMAX (CG)	7	0x0	0=normal 1=test mode: runaway
PPLL_PCP (CG)	10:8	0x4	Pixel clock PLL charge pump gain. Programmed by BIOS. Do not change.
PPLL_PVG (CG)	13:11	0x4	Pixel clock PLL VCO gain. Programmed by BIOS. Do not change.
PPLL_PDC (CG)	15:14	0x1	Pixel clock PLL duty cycle. Programmed by BIOS. Do not change.

PPLL_ATOMIC_UPDATE_EN (CG)	16	0x0	Pixel clock PLL atomic update enable for non-VGA modes. Reference and feedback dividers are double buffered and updated concurrently when a PPLL_ATOMIC_UPDATE_W field is set. 0=Atomic Update Disabled 1=Atomic Update Enabled
PPLL_VGA_ATOMIC_UPDATE_EN (CG)	17	0x0	Same as PPLL_ATOMIC_UPDATE_EN, but for VGA modes. 0=VGA Atomic Update Disabled 1=VGA Atomic Update Enabled
PPLL_ATOMIC_UPDATE_SYNC (CG)	18	0x0	Selects pixel clock PLL atomic update trigger position. Using VSYNC delays update, but allows clock frequency change to be hidden in the vertical retrace. 0=Update ASAP 1=Update in VSYNC

Pixel clock PLL control

PPLL_REF_DIV - RW - 32 bits - CLKIND:0x3			
Field Name	Bits	Default	Description
PPLL_REF_DIV (CG)	9:0	0x3f	Pixel clock PLL reference divider. Must be set so reference frequency is between 1MHz and 400kHz. i.e. $1\text{MHz} \geq (\text{PPLL\_REF}) / \text{PPLL\_REF\_DIV} \geq 400\text{kHz}$ . Also 0 and 1 are not legal settings for this register field.
PPLL_ATOMIC_UPDATE_W (W) (CG)	15	0x0	If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers. 0=No Update 1=Update
PPLL_ATOMIC_UPDATE_R (R) (CG)	15	0x0	Readback of atomic update status. 0=Update done 1=Update Pending
PPLL_REF_DIV_SRC (CG)	17:16	0x0	Pixel clock PLL reference divider input source selection. 0=PPLL_REF = XTALIN 1=PPLL_REF = PLLSCLK/2

Pixel clock PLL reference division configuration

<b>M_SPLL_REF_FB_DIV - RW - 32 bits - CLKIND:0xA</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
M_SPLL_REF_DIV (CG) (CGM)	7:0	0x0	Memory/System PLL reference division
MPLL_FB_DIV (CGM)	15:8	0x0	Memory PLL feedback division
SPLL_FB_DIV (CG)	23:16	0x0	System PLL feedback division
MPLL_REF_SRC_SEL (CGM)	24	0x0	0=Normal 1=Cleaner one through I/O

Memory/System PLL reference/feedback division configuration

<b>SPLL_CNTL - RW - 32 bits - CLKIND:0xC</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SPLL_SLEEP (CG)	0	0x1	Power down S domain PLL 1=Powerdown
SPLL_RESET (CG)	1	0x1	Reset S domain PLL 0=Not Reset 1=Reset
SPLL_TST_EN (CG)	2	0x0	Enable S domain PLL test mode
SPLL_REFCLK_SEL (CG)	4	0x0	0=not flopped 1=flopped
SPLL_FBCLK_SEL (CG)	5	0x0	0=not flopped 1=flopped
SPLL_TCPOFF (CG)	6	0x0	0=normal 1=test mode: Hi-Z
SPLL_TVCOMAX (CG)	7	0x0	0=normal 1=test mode: runaway

SPLL_PCP (CG)	10:8	0x4	Program S domain PLL charge pump
SPLL_PVG (CG)	13:11	0x4	Program S domain PLL VCO gain
SPLL_PDC (CG)	15:14	0x1	Program S domain clock duty cycle
SPLL_X1_CLK_SKEW (CG)	18:16	0x0	
SPLL_X2_CLK_SKEW (CG)	22:20	0x0	
SPLL_MODE (CG)	27:24	0x4	

S domain PLL control

<b>SCLK_CNTL - RW - 32 bits - CLKIND:0xD</b>			
<b>Field Name</b>	<b>Bits</b>	<b>Default</b>	<b>Description</b>
SCLK_SRC_SEL (CG)	2:0	0x0	S domain clock source selection 0=not PCICLK 1=SCLK/1 2=SCLK/2 3=SCLK/4 4=SCLK/8 5=External Source/Scan Clock (XTALIN pin) 6=Test Clock from Test Controller 7=MCLK
TCLK_SRC_SEL (CG)	10:8	0x0	0=PCICLK 1=TCLK/1 2=TCLK/2 3=TCLK/4 4=TCLK/8 5=REFCLK 7=Stopped
FORCE_CP (CG)	16	0x1	CP block dynamic power management off 0=Dynamic 1=ForceOn

FORCE_HDP (CG)	17	0x1	HDP block dynamic power management off 0=Dynamic 1=ForceOn
FORCE_DISP (CG)	18	0x1	DISP block dynamic power management off 0=Dynamic 1=ForceOn
FORCE_TOP (CG)	19	0x1	0=Dynamic 1=ForceOn
FORCE_E2 (CG)	20	0x1	E2 block dynamic power management off 0=Dynamic 1=ForceOn
FORCE_SE (CG)	21	0x1	SE block dynamic power management off 0=Dynamic 1=ForceOn
FORCE_IDCT (CG)	22	0x1	IDCT block dynamic power management off 0=Dynamic 1=ForceOn
FORCE_VIP (CG)	23	0x1	VIP block dynamic power management off 0=Dynamic 1=ForceOn
FORCE_RE (CG)	24	0x1	RE block dynamic power management off 0=Dynamic 1=ForceOn
FORCE_PB (CG)	25	0x1	PB block dynamic power management off 0=Dynamic 1=ForceOn
FORCE_TAM (CG)	26	0x1	TAM block dynamic power management off 0=Dynamic 1=ForceOn
FORCE_TDM (CG)	27	0x1	TDM block dynamic power management off 0=Dynamic 1=ForceOn
FORCE_RB (CG)	28	0x1	RB block dynamic power management off 0=Dynamic 1=ForceOn

Clock source selection and dynamic power management control

AGP_PLL_CNTL - RW - 32 bits - CLKIND:0xB			
Field Name	Bits	Default	Description
APLL_SLEEP (CG)	0	0x0	Power down AGP PLL
APLL_RESET (CG)	1	0x0	Reset AGP PLL
APLL_XSEL (CG)	3:2	0x0	Select different AGP mode for testing 0=TESTMODE REFCLK 1=TESTMODE AGP1X 2=TESTMODE AGP2X 3=TESTMODE AGP4X
APLL_TST_EN (CG)	4	0x0	Enable AGP PLL test mode 0=normal 1=test mode
APLL_TCPOFF (CG)	5	0x0	0=normal 1=test mode: Hi-Z
APLL_TVCOMAX (CG)	6	0x0	0=normal 1=test mode: runaway
APLL_REF_SKEW (CG)	9:7	0x4	
APLL_FB_SKEW (CG)	12:10	0x0	
APLL_X0_CLK_SKEW (CG)	15:13	0x0	
APLL_X1_CLK_SKEW (CG)	18:16	0x0	Program AGP1X mode clock skew
APLL_X2_CLK_SKEW (CG)	21:19	0x0	Program AGP2X mode clock skew
APLL_X4_CLK_SKEW (CG)	24:22	0x0	Program AGP4X mode clock skew
APLL_PUMP_GAIN (CG)	27:25	0x4	Program AGP PLL charge pump

APLL_VCO_GAIN (CG)	30:28	0x5	
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AGP PLL control

MPLL_CNTL - RW - 32 bits - CLKIND:0xE			
Field Name	Bits	Default	Description
MPLL_RESET (CGM)	0	0x1	Reset M domain PLL 0=Not Reset 1=Reset
MPLL_SLEEP (CGM)	1	0x1	Power down M domain PLL 1=Powerdown
MPLL_TST_EN (CGM)	2	0x0	Enable M domain PLL test mode
MPLL_REFCLK_SEL (CGM)	4	0x0	0=not flopped 1=flopped
MPLL_FBCLK_SEL (CGM)	5	0x0	0=not flopped 1=flopped
MPLL_TCPOFF (CGM)	6	0x0	0=normal 1=test mode: Hi-Z
MPLL_TVCOMAX (CGM)	7	0x0	0=normal 1=test mode: runaway
MPLL_PCP (CGM)	10:8	0x4	Program M domain PLL charge pump
MPLL_PVG (CGM)	13:11	0x4	Program M domain PLL VCO gain
MPLL_PDC (CGM)	15:14	0x1	Program M domain clock duty cycle
MPLL_X1_CLK_SKEW (CGM)	18:16	0x0	

MPLL_X2_CLK_SKEW (CGM)	22:20	0x0	
MPLL_MODE (CGM)	27:24	0x4	

M domain PLL control

MDLL_CKO - RW - 32 bits - CLKIND:0xF			
Field Name	Bits	Default	Description
MCKOA_SLEEP (CGM)	0	0x1	0=Enabled 1=PowerDown
MCKOA_RESET (CGM)	1	0x1	0=Enabled 1=Reset
MCKOA_RANGE (CGM)	3:2	0x2	
ERSTA_SOUTSEL (CGM)	5:4	0x1	1=no delay 2=2 elements 3=4 elements
MCKOA_FB_SEL (CGM)	7:6	0x1	0=raw feedback 1=delayed feedback 2=internal feedback
MCKOA_REF_SKEW (CGM)	10:8	0x0	
MCKOA_FB_SKEW (CGM)	14:12	0x0	
MCKOA_BP_SEL (CGM)	15	0x1	0=DLL clock 1=MCLK
MCKOB_SLEEP (CGM)	16	0x1	0=Enabled 1=PowerDown
MCKOB_RESET (CGM)	17	0x1	0=Enabled 1=Reset

MCKOB_RANGE (CGM)	19:18	0x2	
ERSTB_SOUTSEL (CGM)	21:20	0x1	1=no delay 2=2 elements 3=4 elements
MCKOB_FB_SEL (CGM)	23:22	0x1	0=raw feedback 1=delayed feedback 2=internal feedback
MCKOB_REF_SKEW (CGM)	26:24	0x0	
MCKOB_FB_SKEW (CGM)	30:28	0x0	
MCKOB_BP_SEL (CGM)	31	0x1	0=DLL clock 1=MCLK

No description available for this register.

<b>MDLL_RDCKA - RW - 32 bits - CLKIND:0x10</b>			
Field Name	Bits	Default	Description
MRDCKA0_SLEEP (CGM)	0	0x1	0=Enabled 1=PowerDown
MRDCKA0_RESET (CGM)	1	0x1	0=Enabled 1=Reset
MRDCKA0_RANGE (CGM)	3:2	0x2	
MRDCKA0_REF_SEL (CGM)	5:4	0x0	0=MCLK 1=QSA0 pad 2=delayed HCLK1 feedback
MRDCKA0_FB_SEL (CGM)	7:6	0x0	0=strobe leaf node 1=logic zero 2=internal feedback
MRDCKA0_REF_SKEW (CGM)	10:8	0x0	

MRDCKA0_SINSEL (CGM)	11	0x0	0=read strobe per 32 bits 1=read strobe per 8 bits
MRDCKA0_FB_SKEW (CGM)	14:12	0x0	
MRDCKA0_BP_SEL (CGM)	15	0x1	0=DLL clock 1=MCLK
MRDCKA1_SLEEP (CGM)	16	0x1	0=Enabled 1=PowerDown
MRDCKA1_RESET (CGM)	17	0x1	0=Enabled 1=Reset
MRDCKA1_RANGE (CGM)	19:18	0x2	
MRDCKA1_REF_SEL (CGM)	21:20	0x0	0=MCLK 1=QSA4 pad 2=delayed HCLK1 feedback
MRDCKA1_FB_SEL (CGM)	23:22	0x0	0=strobe leaf node 1=logic zero 2=internal feedback
MRDCKA1_REF_SKEW (CGM)	26:24	0x0	
MRDCKA1_SINSEL (CGM)	27	0x0	0=read strobe per 32 bits 1=read strobe per 8 bits
MRDCKA1_FB_SKEW (CGM)	30:28	0x0	
MRDCKA1_BP_SEL (CGM)	31	0x1	0=DLL clock 1=MCLK

No description available for this register.

MDLL_RDCKB - RW - 32 bits - CLKIND:0x11			
Field Name	Bits	Default	Description
MRDCKB0_SLEEP (CGM)	0	0x1	0=Enabled 1=PowerDown
MRDCKB0_RESET (CGM)	1	0x1	0=Enabled 1=Reset
MRDCKB0_RANGE (CGM)	3:2	0x2	
MRDCKB0_REF_SEL (CGM)	5:4	0x0	0=MCLK 1=QSB0 pad 2=delayed HCLK1 feedback
MRDCKB0_FB_SEL (CGM)	7:6	0x0	0=strobe leaf node 1=logic zero 2=internal feedback
MRDCKB0_REF_SKEW (CGM)	10:8	0x0	
MRDCKB0_SINSEL (CGM)	11	0x0	0=read strobe per 32 bits 1=read strobe per 8 bits
MRDCKB0_FB_SKEW (CGM)	14:12	0x0	
MRDCKB0_BP_SEL (CGM)	15	0x1	0=DLL clock 1=MCLK
MRDCKB1_SLEEP (CGM)	16	0x1	0=Enabled 1=PowerDown
MRDCKB1_RESET (CGM)	17	0x1	0=Enabled 1=Reset
MRDCKB1_RANGE (CGM)	19:18	0x2	
MRDCKB1_REF_SEL (CGM)	21:20	0x0	0=MCLK 1=QSB4 pad 2=delayed HCLK1 feedback

MRDCKB1_FB_SEL (CGM)	23:22	0x0	0=strobe leaf node 1=logic zero 2=internal feedback
MRDCKB1_REF_SKEW (CGM)	26:24	0x0	
MRDCKB1_SINSEL (CGM)	27	0x0	0=read strobe per 32 bits 1=read strobe per 8 bits
MRDCKB1_FB_SKEW (CGM)	30:28	0x0	
MRDCKB1_BP_SEL (CGM)	31	0x1	0=DLL clock 1=MCLK

No description available for this register.

<b>MCLK_CNTL - RW - 32 bits - CLKIND:0x12</b>			
Field Name	Bits	Default	Description
MCLKA_SRC_SEL (CGM)	2:0	0x0	0=PCICLK 1=MPLLCLK/1 2=MPLLCLK/2 3=MPLLCLK/4 4=MPLLCLK/8 5=External Source/Scan Clock (CLKAFB pin) 6=Test clock from test controller 7=Stopped
YCLKA_SRC_SEL (CGM)	6:4	0x0	0=PCICLK 1=MPLLCLK/1 2=MPLLCLK/2 3=MPLLCLK/4 4=MPLLCLK/8 5=External Source/Scan Clock (CLKBFB pin) 6=Test clock from test controller 7=Stopped
MCLKB_SRC_SEL (CGM)	10:8	0x0	0=PCICLK 1=MPLLCLK/1 2=MPLLCLK/2 3=MPLLCLK/4 4=MPLLCLK/8 5=External Source/Scan Clock (CLKAFB pin) 6=Test clock from test controller 7=Stopped

Miscellaneous Registers

YCLKB_SRC_SEL (CGM)	14:12	0x0	0=PCICLK 1=MPLLCLK/1 2=MPLLCLK/2 3=MPLLCLK/4 4=MPLLCLK/8 5=External Source/Scan Clock (CLKBFB pin) 6=Test clock from test controller 7=Stopped
FORCE_MCLKA (CGM)	16	0x1	0=Dynamic 1=ForceOn
FORCE_MCLKB (CGM)	17	0x1	0=Dynamic 1=ForceOn
FORCE_YCLKA (CGM)	18	0x1	0=Dynamic 1=ForceOn
FORCE_YCLKB (CGM)	19	0x1	0=Dynamic 1=ForceOn
FORCE_MC (CGM)	20	0x1	0=Dynamic 1=ForceOn
FORCE_AIC (CGM)	21	0x1	0=Dynamic 1=ForceOn
MRDCKA0_SOUTSEL (CGM)	25:24	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKA1_SOUTSEL (CGM)	27:26	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKB0_SOUTSEL (CGM)	29:28	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKB1_SOUTSEL (CGM)	31:30	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements

No description available for this register.

# Appendix A

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## A.2 MMR Registers Sorted by Name

Table 2-2 MMR Registers Sorted by Name

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<i>AIC_LO_ADDR</i>		<i>MMReg:0x1DC</i>		2-253
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<i>AIC_STAT</i>		<i>MMReg:0x1D4</i>		2-252
<i>AIC_TLB_ADDR</i>		<i>MMReg:0x1E4</i>		2-253
<i>AIC_TLB_DATA</i>		<i>MMReg:0x1E8</i>		2-253
<i>AUX_WINDOW_HORZ_CNTL</i>		<i>MMReg:0x2D8</i>		2-66
<i>AUX_WINDOW_VERT_CNTL</i>		<i>MMReg:0x2DC</i>		2-66
<i>BM_STATUS</i>		<i>MMReg:0x160</i>		2-243
<i>BRUSH_DATA0</i>		<i>MMReg:0x1480</i>		2-162
<i>BRUSH_DATA1</i>		<i>MMReg:0x1484</i>		2-162
<i>BRUSH_DATA10</i>		<i>MMReg:0x14A8</i>		2-164
<i>BRUSH_DATA11</i>		<i>MMReg:0x14AC</i>		2-164
<i>BRUSH_DATA12</i>		<i>MMReg:0x14B0</i>		2-164
<i>BRUSH_DATA13</i>		<i>MMReg:0x14B4</i>		2-165
<i>BRUSH_DATA14</i>		<i>MMReg:0x14B8</i>		2-165
<i>BRUSH_DATA15</i>		<i>MMReg:0x14BC</i>		2-165
<i>BRUSH_DATA16</i>		<i>MMReg:0x14C0</i>		2-165
<i>BRUSH_DATA17</i>		<i>MMReg:0x14C4</i>		2-165
<i>BRUSH_DATA18</i>		<i>MMReg:0x14C8</i>		2-166
<i>BRUSH_DATA19</i>		<i>MMReg:0x14CC</i>		2-166
<i>BRUSH_DATA2</i>		<i>MMReg:0x1488</i>		2-162
<i>BRUSH_DATA20</i>		<i>MMReg:0x14D0</i>		2-166
<i>BRUSH_DATA21</i>		<i>MMReg:0x14D4</i>		2-166
<i>BRUSH_DATA22</i>		<i>MMReg:0x14D8</i>		2-166
<i>BRUSH_DATA23</i>		<i>MMReg:0x14DC</i>		2-167
<i>BRUSH_DATA24</i>		<i>MMReg:0x14E0</i>		2-167
<i>BRUSH_DATA25</i>		<i>MMReg:0x14E4</i>		2-167
<i>BRUSH_DATA26</i>		<i>MMReg:0x14E8</i>		2-167
<i>BRUSH_DATA27</i>		<i>MMReg:0x14EC</i>		2-167
<i>BRUSH_DATA28</i>		<i>MMReg:0x14F0</i>		2-168
<i>BRUSH_DATA29</i>		<i>MMReg:0x14F4</i>		2-168
<i>BRUSH_DATA3</i>		<i>MMReg:0x148C</i>		2-163
<i>BRUSH_DATA30</i>		<i>MMReg:0x14F8</i>		2-168
<i>BRUSH_DATA31</i>		<i>MMReg:0x14FC</i>		2-168
<i>BRUSH_DATA32</i>		<i>MMReg:0x1500</i>		2-168
<i>BRUSH_DATA33</i>		<i>MMReg:0x1504</i>		2-169
<i>BRUSH_DATA34</i>		<i>MMReg:0x1508</i>		2-169
<i>BRUSH_DATA35</i>		<i>MMReg:0x150C</i>		2-169

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<i>BRUSH_DATA38</i>		<i>MMReg:0x1518</i>		2-170
<i>BRUSH_DATA39</i>		<i>MMReg:0x151C</i>		2-170
<i>BRUSH_DATA4</i>		<i>MMReg:0x1490</i>		2-163
<i>BRUSH_DATA40</i>		<i>MMReg:0x1520</i>		2-170
<i>BRUSH_DATA41</i>		<i>MMReg:0x1524</i>		2-170
<i>BRUSH_DATA42</i>		<i>MMReg:0x1528</i>		2-170
<i>BRUSH_DATA43</i>		<i>MMReg:0x152C</i>		2-171
<i>BRUSH_DATA44</i>		<i>MMReg:0x1530</i>		2-171
<i>BRUSH_DATA45</i>		<i>MMReg:0x1534</i>		2-171
<i>BRUSH_DATA46</i>		<i>MMReg:0x1538</i>		2-171
<i>BRUSH_DATA47</i>		<i>MMReg:0x153C</i>		2-171
<i>BRUSH_DATA48</i>		<i>MMReg:0x1540</i>		2-172
<i>BRUSH_DATA49</i>		<i>MMReg:0x1544</i>		2-172
<i>BRUSH_DATA5</i>		<i>MMReg:0x1494</i>		2-163
<i>BRUSH_DATA50</i>		<i>MMReg:0x1548</i>		2-172
<i>BRUSH_DATA51</i>		<i>MMReg:0x154C</i>		2-172
<i>BRUSH_DATA52</i>		<i>MMReg:0x1550</i>		2-172
<i>BRUSH_DATA53</i>		<i>MMReg:0x1554</i>		2-173
<i>BRUSH_DATA54</i>		<i>MMReg:0x1558</i>		2-173
<i>BRUSH_DATA55</i>		<i>MMReg:0x155C</i>		2-173
<i>BRUSH_DATA56</i>		<i>MMReg:0x1560</i>		2-173
<i>BRUSH_DATA57</i>		<i>MMReg:0x1564</i>		2-173
<i>BRUSH_DATA58</i>		<i>MMReg:0x1568</i>		2-174
<i>BRUSH_DATA59</i>		<i>MMReg:0x156C</i>		2-174
<i>BRUSH_DATA6</i>		<i>MMReg:0x1498</i>		2-163
<i>BRUSH_DATA60</i>		<i>MMReg:0x1570</i>		2-174
<i>BRUSH_DATA61</i>		<i>MMReg:0x1574</i>		2-174
<i>BRUSH_DATA62</i>		<i>MMReg:0x1578</i>		2-174
<i>BRUSH_DATA63</i>		<i>MMReg:0x157C</i>		2-175
<i>BRUSH_DATA7</i>		<i>MMReg:0x149C</i>		2-163
<i>BRUSH_DATA8</i>		<i>MMReg:0x14A0</i>		2-164
<i>BRUSH_DATA9</i>		<i>MMReg:0x14A4</i>		2-164
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<i>BUS_CNTL</i>	<i>IOWReg:0x30</i>	<i>MMReg:0x30</i>		2-237
<i>BUS_CNTL1</i>	<i>IOWReg:0x34</i>	<i>MMReg:0x34</i>		2-239
<i>CAPO_ANC0_OFFSET</i>		<i>MMReg:0x95C</i>		2-126
<i>CAPO_ANC1_OFFSET</i>		<i>MMReg:0x960</i>		2-126
<i>CAPO_ANC2_OFFSET</i>		<i>MMReg:0x988</i>		2-128
<i>CAPO_ANC3_OFFSET</i>		<i>MMReg:0x98C</i>		2-128
<i>CAPO_ANC_BUF01_BLOCK_CNT</i>		<i>MMReg:0x974</i>		2-291
<i>CAPO_ANC_BUF23_BLOCK_CNT</i>		<i>MMReg:0x97C</i>		2-291
<i>CAPO_ANC_H_WINDOW</i>		<i>MMReg:0x964</i>		2-126

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<i>CAPO_BUF0_OFFSET</i>		<i>MMReg:0x920</i>		2-120
<i>CAPO_BUF1_EVEN_OFFSET</i>		<i>MMReg:0x92C</i>		2-121
<i>CAPO_BUF1_OFFSET</i>		<i>MMReg:0x924</i>		2-121
<i>CAPO_BUF_PITCH</i>		<i>MMReg:0x930</i>		2-121
<i>CAPO_BUF_STATUS</i>		<i>MMReg:0x970</i>		2-127
<i>CAPO_CONFIG</i>		<i>MMReg:0x958</i>		2-124
<i>CAPO_DEBUG</i>		<i>MMReg:0x954</i>		2-124
<i>CAPO_H_WINDOW</i>		<i>MMReg:0x938</i>		2-122
<i>CAPO_ONESHOT_BUF_OFFSET</i>		<i>MMReg:0x96C</i>		2-127
<i>CAPO_PORT_MODE_CNTL</i>		<i>MMReg:0x94C</i>		2-123
<i>CAPO_TRIG_CNTL</i>		<i>MMReg:0x950</i>		2-123
<i>CAPO_V_WINDOW</i>		<i>MMReg:0x934</i>		2-121
<i>CAPO_VBI0_OFFSET</i>		<i>MMReg:0x93C</i>		2-122
<i>CAPO_VBI1_OFFSET</i>		<i>MMReg:0x940</i>		2-122
<i>CAPO_VBI2_OFFSET</i>		<i>MMReg:0x980</i>		2-128
<i>CAPO_VBI3_OFFSET</i>		<i>MMReg:0x984</i>		2-128
<i>CAPO_VBI_H_WINDOW</i>		<i>MMReg:0x948</i>		2-123
<i>CAPO_VBI_V_WINDOW</i>		<i>MMReg:0x944</i>		2-122
<i>CAPO_VIDEO_SYNC_TEST</i>		<i>MMReg:0x968</i>		2-126
<i>CAP_INT_CNTL</i>		<i>MMReg:0x908</i>		2-129
<i>CAP_INT_STATUS</i>		<i>MMReg:0x90C</i>		2-130
<i>CLOCK_CNTL_DATA</i>	<i>IOWReg:0xC</i>	<i>MMReg:0xC</i>		2-266
<i>CLOCK_CNTL_INDEX</i>	<i>IOWReg:0x8</i>	<i>MMReg:0x8</i>		2-266
<i>CLR_CMP_CLR_DST</i>		<i>MMReg:0x15C8</i>		2-179
<i>CLR_CMP_CLR_SRC</i>		<i>MMReg:0x15C4</i>		2-178
<i>CLR_CMP_CNTL</i>		<i>MMReg:0x15C0</i>		2-178
<i>CLR_CMP_MSK</i>		<i>MMReg:0x15CC</i>		2-179
<i>CONFIG_APER_0_BASE</i>		<i>MMReg:0x100</i>		2-240
<i>CONFIG_APER_1_BASE</i>		<i>MMReg:0x104</i>		2-240
<i>CONFIG_APER_SIZE</i>		<i>MMReg:0x108</i>		2-241
<i>CONFIG_CNTL</i>	<i>IOWReg:0xE0</i>	<i>MMReg:0xE0</i>		2-240
<i>CONFIG_MEMSIZE</i>	<i>IOWReg:0xF8</i>	<i>MMReg:0xF8</i>		2-240
<i>CONFIG_REG_1_BASE</i>		<i>MMReg:0x10C</i>		2-241
<i>CONFIG_REG_APER_SIZE</i>		<i>MMReg:0x110</i>		2-241
<i>CP_CSQ_ADDR</i>		<i>MMReg:0x7F0</i>		2-152
<i>CP_CSQ_APER_INDIRECT</i>		<i>MMReg:0x1300-0x13FC</i>		2-144
<i>CP_CSQ_APER_PRIMARY</i>		<i>MMReg:0x1000-0x11FC</i>		2-144
<i>CP_CSQ_CNTL</i>		<i>MMReg:0x740</i>		2-143
<i>CP_CSQ_DATA</i>		<i>MMReg:0x7F4</i>		2-152
<i>CP_CSQ_STAT</i>		<i>MMReg:0x7F8</i>		2-152
<i>CP_IB_BASE</i>		<i>MMReg:0x738</i>		2-143
<i>CP_IB_BUFSZ</i>		<i>MMReg:0x73C</i>		2-143
<i>CP_ME_CNTL</i>		<i>MMReg:0x7D0</i>		2-152
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Table 2-2 MMR Registers Sorted by Name (Continued)

Name	I/OAddress	MM Address	Second Address	Page
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<i>CP_ME_RAM_RADDR</i>		<i>MMReg:0x7D8</i>		2-153
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<i>CP_RB_CNTL</i>		<i>MMReg:0x704</i>		2-141
<i>CP_RB_RPTR</i>		<i>MMReg:0x710</i>		2-142
<i>CP_RB_RPTR_ADDR</i>		<i>MMReg:0x70C</i>		2-142
<i>CP_RB_WPTR</i>		<i>MMReg:0x714</i>		2-142
<i>CP_RB_WPTR_DELAY</i>		<i>MMReg:0x718</i>		2-143
<i>CP_STAT</i>		<i>MMReg:0x7C0</i>		2-272
<i>CRT_CRTC_H_SYNC_STRT_WID</i>		<i>MMReg:0x258</i>		2-258
<i>CRT_CRTC_V_SYNC_STRT_WID</i>		<i>MMReg:0x25C</i>		2-259
<i>CRTC_CRNT_FRAME</i>		<i>MMReg:0x214</i>		2-48
<i>CRTC_DEBUG</i>		<i>MMReg:0x21C</i>		2-49
<i>CRTC_EXT_CNTL</i>	<i>IOWReg:0x54</i>	<i>MMReg:0x54</i>		2-43
<i>CRTC_GEN_CNTL</i>	<i>IOWReg:0x50</i>	<i>MMReg:0x50</i>		2-41
<i>CRTC_GUI_TRIG_VLINE</i>		<i>MMReg:0x218</i>		2-48
<i>CRTC_H_SYNC_STRT_WID</i>		<i>MMReg:0x204</i>		2-47
<i>CRTC_H_TOTAL_DISP</i>		<i>MMReg:0x200</i>		2-47
<i>CRTC_MORE_CNTL</i>		<i>MMReg:0x27C</i>		2-259
<i>CRTC_OFFSET</i>		<i>MMReg:0x224</i>		2-50
<i>CRTC_OFFSET_CNTL</i>		<i>MMReg:0x228</i>		2-51
<i>CRTC_OFFSET_RIGHT</i>		<i>MMReg:0x220</i>		2-50
<i>CRTC_PITCH</i>		<i>MMReg:0x22C</i>		2-53
<i>CRTC_STATUS</i>	<i>IOWReg:0x5C</i>	<i>MMReg:0x5C</i>		2-45
<i>CRTC_V_SYNC_STRT_WID</i>		<i>MMReg:0x20C</i>		2-48
<i>CRTC_V_TOTAL_DISP</i>		<i>MMReg:0x208</i>		2-47
<i>CRTC_VLINE_CRNT_VLINE</i>		<i>MMReg:0x210</i>		2-48
<i>CUR_CLR0</i>		<i>MMReg:0x26C</i>		2-58
<i>CUR_CLR1</i>		<i>MMReg:0x270</i>		2-58
<i>CUR_HORZ_VERT_OFF</i>		<i>MMReg:0x268</i>		2-57
<i>CUR_HORZ_VERT_POSN</i>		<i>MMReg:0x264</i>		2-57
<i>CUR_OFFSET</i>		<i>MMReg:0x260</i>		2-56
<i>DAC_BLANK_LEVEL</i>		<i>MMReg:0xDD8</i>		2-265
<i>DAC_BROAD_PULSE</i>		<i>MMReg:0xDC4</i>		2-264
<i>DAC_CNTL</i>	<i>IOWReg:0x58</i>	<i>MMReg:0x58</i>		2-35
<i>DAC_CRC_SIG1</i>		<i>MMReg:0xD18</i>		2-91
<i>DAC_CRC_SIG2</i>		<i>MMReg:0xD1C</i>		2-91
<i>DAC_EMBEDDED_SYNC_CNTL</i>		<i>MMReg:0xDC0</i>		2-264
<i>DAC_EXT_CNTL</i>		<i>MMReg:0x280</i>		2-59
<i>DAC_INCR</i>		<i>MMReg:0xDCC</i>		2-265
<i>DAC_MACRO_CNTL</i>		<i>MMReg:0xD04</i>		2-88
<i>DAC_NEG_SYNC_LEVEL</i>		<i>MMReg:0xDD0</i>		2-265
<i>DAC_POS_SYNC_LEVEL</i>		<i>MMReg:0xDD4</i>		2-265

Table 2-2 MMR Registers Sorted by Name (Continued)

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<i>DAC_SKEW_CLKS</i>		<i>MMReg:0xDC8</i>		2-264
<i>DEFAULT_PITCH_OFFSET</i>		<i>MMReg:0x16E0</i>		2-188
<i>DEFAULT_SC_BOTTOM_RIGHT</i>		<i>MMReg:0x16E8</i>		2-184
<i>DISP_HW_DEBUG</i>		<i>MMReg:0xD14</i>		2-90
<i>DISP_LIN_TRANS_GRP_H_A</i>		<i>MMReg:0xD80</i>		2-100
<i>DISP_LIN_TRANS_GRP_H_B</i>		<i>MMReg:0xD84</i>		2-100
<i>DISP_LIN_TRANS_GRP_H_C</i>		<i>MMReg:0xD88</i>		2-100
<i>DISP_LIN_TRANS_GRP_H_D</i>		<i>MMReg:0xD8C</i>		2-100
<i>DISP_LIN_TRANS_GRP_H_E</i>		<i>MMReg:0xD90</i>		2-101
<i>DISP_LIN_TRANS_GRP_H_F</i>		<i>MMReg:0xD94</i>		2-101
<i>DISP_LIN_TRANS_VID_A</i>		<i>MMReg:0xD98</i>		2-101
<i>DISP_LIN_TRANS_VID_B</i>		<i>MMReg:0xD9C</i>		2-101
<i>DISP_LIN_TRANS_VID_C</i>		<i>MMReg:0xDA0</i>		2-102
<i>DISP_LIN_TRANS_VID_D</i>		<i>MMReg:0xDA4</i>		2-102
<i>DISP_LIN_TRANS_VID_E</i>		<i>MMReg:0xDA8</i>		2-102
<i>DISP_LIN_TRANS_VID_F</i>		<i>MMReg:0xDAC</i>		2-102
<i>DISP_MERGE_CNTL</i>		<i>MMReg:0xD60</i>		2-95
<i>DISP_MISC_CNTL</i>		<i>MMReg:0xD00</i>		2-88
<i>DISP_OUTPUT_CNTL</i>		<i>MMReg:0xD64</i>		2-97
<i>DISP_PWR_MAN</i>		<i>MMReg:0xD08</i>		2-263
<i>DISP_TEST_DEBUG_CNTL</i>		<i>MMReg:0xD10</i>		2-89
<i>DISPLAY_BASE_ADDR</i>		<i>MMReg:0x23C</i>		2-54
<i>DMA_GUI_ACT_DSCRPTR</i>		<i>MMReg:0x794</i>		2-149
<i>DMA_GUI_COMMAND</i>		<i>MMReg:0x78C</i>		2-147
<i>DMA_GUI_DST_ADDR</i>		<i>MMReg:0x788</i>		2-147
<i>DMA_GUI_SRC_ADDR</i>		<i>MMReg:0x784</i>		2-147
<i>DMA_GUI_STATUS</i>		<i>MMReg:0x790</i>		2-148
<i>DMA_GUI_TABLE_ADDR</i>		<i>MMReg:0x780</i>		2-146
<i>DMA_VID_ACT_DSCRPTR</i>		<i>MMReg:0x7B4</i>		2-151
<i>DMA_VID_COMMAND</i>		<i>MMReg:0x7AC</i>		2-150
<i>DMA_VID_DST_ADDR</i>		<i>MMReg:0x7A8</i>		2-150
<i>DMA_VID_SRC_ADDR</i>		<i>MMReg:0x7A4</i>		2-149
<i>DMA_VID_STATUS</i>		<i>MMReg:0x7B0</i>		2-151
<i>DMA_VID_TABLE_ADDR</i>		<i>MMReg:0x7A0</i>		2-149
<i>DMA_VIP0_TABLE_ADDR</i>		<i>MMReg:0xA20</i>		2-137
<i>DMA_VIP1_TABLE_ADDR</i>		<i>MMReg:0xA30</i>		2-138
<i>DMA_VIP2_TABLE_ADDR</i>		<i>MMReg:0xA40</i>		2-138
<i>DMA_VIP3_TABLE_ADDR</i>		<i>MMReg:0xA50</i>		2-138
<i>DMA_VIPH0_ACTIVE</i>		<i>MMReg:0xA24</i>		2-138
<i>DMA_VIPH0_COMMAND</i>		<i>MMReg:0xA00</i>		2-133
<i>DMA_VIPH1_ACTIVE</i>		<i>MMReg:0xA34</i>		2-138
<i>DMA_VIPH1_COMMAND</i>		<i>MMReg:0xA04</i>		2-133
<i>DMA_VIPH2_ACTIVE</i>		<i>MMReg:0xA44</i>		2-139
<i>DMA_VIPH2_COMMAND</i>		<i>MMReg:0xA08</i>		2-134
<i>DMA_VIPH3_ACTIVE</i>		<i>MMReg:0xA54</i>		2-139

Table 2-2 MMR Registers Sorted by Name (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>DMA_VIPH3_COMMAND</i>		<i>MMReg:0xA0C</i>		2-135
<i>DMA_VIPH_ABORT</i>		<i>MMReg:0xA88</i>		2-139
<i>DMA_VIPH_CHUNK_0</i>		<i>MMReg:0xA18</i>		2-136
<i>DMA_VIPH_CHUNK_1_VAL</i>		<i>MMReg:0xA1C</i>		2-137
<i>DMA_VIPH_STATUS</i>		<i>MMReg:0xA10</i>		2-136
<i>DP_BRUSH_BKGD_CLR</i>		<i>MMReg:0x1478</i>		2-162
<i>DP_BRUSH_FRGD_CLR</i>		<i>MMReg:0x147C</i>		2-162
<i>DP_CNTL</i>		<i>MMReg:0x16C0</i>		2-182
<i>DP_CNTL_XDIR_YDIR_YMAJOR</i>		<i>MMReg:0x16D0</i>		2-288
<i>DP_DATATYPE</i>		<i>MMReg:0x16C4</i>		2-182
<i>DP_DST_ENDIAN</i>		<i>MMReg:0x15D0</i>		2-288
<i>DP_GUI_MASTER_CNTL</i>		<i>MMReg:0x146C</i>		2-159
<i>DP_MIX</i>		<i>MMReg:0x16C8</i>		2-183
<i>DP_SRC_BKGD_CLR</i>		<i>MMReg:0x15DC</i>		2-179
<i>DP_SRC_ENDIAN</i>		<i>MMReg:0x15D4</i>		2-288
<i>DP_SRC_FRGD_CLR</i>		<i>MMReg:0x15D8</i>		2-179
<i>DP_WRITE_MSK</i>		<i>MMReg:0x16CC</i>		2-184
<i>DP_XOP</i>		<i>MMReg:0x17F8</i>		2-188
<i>DST_HEIGHT</i>		<i>MMReg:0x1410</i>		2-157
<i>DST_HEIGHT_WIDTH</i>		<i>MMReg:0x143C</i>		2-159
<i>DST_HEIGHT_WIDTH_8</i>		<i>MMReg:0x158C</i>		2-175
<i>DST_HEIGHT_Y</i>		<i>MMReg:0x15A0</i>		2-177
<i>DST_LINE_END</i>		<i>MMReg:0x1604</i>		2-180
<i>DST_LINE_PATCOUNT</i>		<i>MMReg:0x1608</i>		2-180
<i>DST_LINE_START</i>		<i>MMReg:0x1600</i>		2-179
<i>DST_OFFSET</i>		<i>MMReg:0x1404</i>		2-156
<i>DST_PITCH</i>		<i>MMReg:0x1408</i>		2-156
<i>DST_PITCH_OFFSET</i>		<i>MMReg:0x142C</i>		2-158
<i>DST_TILE</i>		<i>MMReg:0x1700</i>		2-185
<i>DST_WIDTH</i>		<i>MMReg:0x140C</i>		2-156
<i>DST_WIDTH_HEIGHT</i>		<i>MMReg:0x1598</i>		2-176
<i>DST_WIDTH_X</i>		<i>MMReg:0x1588</i>		2-175
<i>DST_WIDTH_X_INCY</i>		<i>MMReg:0x159C</i>		2-176
<i>DST_X</i>		<i>MMReg:0x141C</i>		2-157
<i>DST_X_Y</i>		<i>MMReg:0x1594</i>		2-176
<i>DST_Y</i>		<i>MMReg:0x1420</i>		2-157
<i>DST_Y_X</i>		<i>MMReg:0x1438</i>		2-159
<i>DSTCACHE_CTLSTAT</i>		<i>MMReg:0x1714</i>		2-289
<i>DSTCACHE_MODE</i>		<i>MMReg:0x1710</i>		2-288
<i>EXT_MEM_CNTL</i>		<i>MMReg:0x144</i>		2-19
<i>EXTERN_TRIG_CNTL</i>		<i>MMReg:0x1BC</i>		2-290
<i>FCP_CNTL</i>		<i>MMReg:0x910</i>		2-117
<i>FCP_CNTL</i>		<i>MMReg:0x910</i>		2-118
<i>FP_CRTC_H_TOTAL_DISP</i>		<i>MMReg:0x250</i>		2-55

Table 2-2 MMR Registers Sorted by Name (Continued)

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<i>FP_CRTC_V_TOTAL_DISP</i>		<i>MMReg:0x254</i>		<i>2-56</i>
<i>FP_GEN_CNTL</i>		<i>MMReg:0x284</i>		<i>2-59</i>
<i>FP_H_SYNC_STRT_WID</i>		<i>MMReg:0x2C4</i>		<i>2-65</i>
<i>FP_HORZ_STRETCH</i>		<i>MMReg:0x28C</i>		<i>2-260</i>
<i>FP_HORZ_VERT_ACTIVE</i>		<i>MMReg:0x278</i>		<i>2-259</i>
<i>FP_V_SYNC_STRT_WID</i>		<i>MMReg:0x2C8</i>		<i>2-65</i>
<i>FP_VERT_STRETCH</i>		<i>MMReg:0x290</i>		<i>2-64</i>
<i>GEN_INT_CNTL</i>	<i>IOReg:0x40</i>	<i>MMReg:0x40</i>		<i>2-2</i>
<i>GEN_INT_STATUS</i>	<i>IOReg:0x44</i>	<i>MMReg:0x44</i>		<i>2-3</i>
<i>GEN_INT_STATUS</i>	<i>IOReg:0x44</i>	<i>MMReg:0x44</i>		<i>2-118</i>
<i>GPIO_DVI_DDC</i>	<i>IOReg:0x64</i>	<i>MMReg:0x64</i>		<i>2-258</i>
<i>GPIO_MONID</i>	<i>IOReg:0x68</i>	<i>MMReg:0x68</i>		<i>2-45</i>
<i>GPIO_VGA_DDC</i>	<i>IOReg:0x60</i>	<i>MMReg:0x60</i>		<i>2-257</i>
<i>GRPH_BUFFER_CNTL</i>		<i>MMReg:0x2F0</i>		<i>2-67</i>
<i>HI_STAT</i>	<i>IOReg:0x4C</i>	<i>MMReg:0x4C</i>		<i>2-239</i>
<i>HOST_DATA0</i>		<i>MMReg:0x17C0</i>		<i>2-186</i>
<i>HOST_DATA1</i>		<i>MMReg:0x17C4</i>		<i>2-186</i>
<i>HOST_DATA2</i>		<i>MMReg:0x17C8</i>		<i>2-186</i>
<i>HOST_DATA3</i>		<i>MMReg:0x17CC</i>		<i>2-187</i>
<i>HOST_DATA4</i>		<i>MMReg:0x17D0</i>		<i>2-187</i>
<i>HOST_DATA5</i>		<i>MMReg:0x17D4</i>		<i>2-187</i>
<i>HOST_DATA6</i>		<i>MMReg:0x17D8</i>		<i>2-187</i>
<i>HOST_DATA7</i>		<i>MMReg:0x17DC</i>		<i>2-188</i>
<i>HOST_DATA_LAST</i>		<i>MMReg:0x17E0</i>		<i>2-188</i>
<i>HOST_PATH_CNTL</i>		<i>MMReg:0x130</i>		<i>2-21</i>
<i>I2C_CNTL_0</i>	<i>IOReg:0x90</i>	<i>MMReg:0x90</i>		<i>2-108</i>
<i>I2C_CNTL_1</i>	<i>IOReg:0x94</i>	<i>MMReg:0x94</i>		<i>2-109</i>
<i>I2C_DATA</i>	<i>IOReg:0x98</i>	<i>MMReg:0x98</i>		<i>2-109</i>
<i>ISYNC_CNTL</i>		<i>MMReg:0x1724</i>		<i>2-10</i>
<i>MC_AGP_LOCATION</i>		<i>MMReg:0x14C</i>		<i>2-17</i>
<i>MC_FB_LOCATION</i>		<i>MMReg:0x148</i>		<i>2-16</i>
<i>MEDIA_0_SCRATCH</i>		<i>MMReg:0x1F0</i>		<i>2-290</i>
<i>MEDIA_1_SCRATCH</i>		<i>MMReg:0x1F4</i>		<i>2-291</i>
<i>MEM_CNTL</i>		<i>MMReg:0x140</i>		<i>2-15</i>
<i>MEM_INIT_LATENCY_TIMER</i>		<i>MMReg:0x154</i>		<i>2-17</i>
<i>MEM_SDRAM_MODE_REG</i>		<i>MMReg:0x158</i>		<i>2-18</i>
<i>MEM_VGA_RP_SEL</i>	<i>IOReg:0x3C</i>	<i>MMReg:0x3C</i>		<i>2-201</i>
<i>MEM_VGA_WP_SEL</i>	<i>IOReg:0x38</i>	<i>MMReg:0x38</i>		<i>2-201</i>
<i>MM_DATA</i>	<i>IOReg:0x4</i>	<i>MMReg:0x4</i>		<i>2-237</i>
<i>MM_INDEX</i>	<i>IOReg:0x0</i>	<i>MMReg:0x0</i>		<i>2-237</i>
<i>N_VIF_COUNT</i>		<i>MMReg:0x248</i>		<i>2-55</i>
<i>NQWAIT_UNTIL</i>		<i>MMReg:0xE50</i>		<i>2-10</i>
<i>OV0_AUTO_FLIP_CNTRL</i>		<i>MMReg:0x470</i>		<i>2-77</i>
<i>OV0_BASE_ADDR</i>		<i>MMReg:0x43C</i>		<i>2-74</i>
<i>OV0_DEINTERLACE_PATTERN</i>		<i>MMReg:0x474</i>		<i>2-79</i>

Table 2-2 MMR Registers Sorted by Name (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>OV0_FILTER_CNTL</i>		<i>MMReg:0x4A0</i>		2-83
<i>OV0_FLAG_CNTRL</i>		<i>MMReg:0x4DC</i>		2-85
<i>OV0_FOUR_TAP_COEF_0</i>		<i>MMReg:0x4B0</i>		2-83
<i>OV0_FOUR_TAP_COEF_1</i>		<i>MMReg:0x4B4</i>		2-84
<i>OV0_FOUR_TAP_COEF_2</i>		<i>MMReg:0x4B8</i>		2-84
<i>OV0_FOUR_TAP_COEF_3</i>		<i>MMReg:0x4BC</i>		2-84
<i>OV0_FOUR_TAP_COEF_4</i>		<i>MMReg:0x4C0</i>		2-85
<i>OV0_GAMMA_0_F</i>		<i>MMReg:0xD40</i>		2-93
<i>OV0_GAMMA_10_1F</i>		<i>MMReg:0xD44</i>		2-94
<i>OV0_GAMMA_20_3F</i>		<i>MMReg:0xD48</i>		2-94
<i>OV0_GAMMA_380_3BF</i>		<i>MMReg:0xD50</i>		2-95
<i>OV0_GAMMA_3C0_3FF</i>		<i>MMReg:0xD54</i>		2-95
<i>OV0_GAMMA_40_7F</i>		<i>MMReg:0xD4C</i>		2-94
<i>OV0_GRP_KEY_CLR_HIGH</i>		<i>MMReg:0x4F0</i>		2-86
<i>OV0_GRP_KEY_CLR_LOW</i>		<i>MMReg:0x4EC</i>		2-86
<i>OV0_H_INC</i>		<i>MMReg:0x480</i>		2-80
<i>OV0_KEY_CNTL</i>		<i>MMReg:0x4F4</i>		2-86
<i>OV0_LIN_TRANS_A</i>		<i>MMReg:0xD20</i>		2-92
<i>OV0_LIN_TRANS_B</i>		<i>MMReg:0xD24</i>		2-92
<i>OV0_LIN_TRANS_C</i>		<i>MMReg:0xD28</i>		2-92
<i>OV0_LIN_TRANS_D</i>		<i>MMReg:0xD2C</i>		2-93
<i>OV0_LIN_TRANS_E</i>		<i>MMReg:0xD30</i>		2-93
<i>OV0_LIN_TRANS_F</i>		<i>MMReg:0xD34</i>		2-93
<i>OV0_P1_BLANK_LINES_AT_TOP</i>		<i>MMReg:0x430</i>		2-73
<i>OV0_P1_H_ACCUM_INIT</i>		<i>MMReg:0x488</i>		2-81
<i>OV0_P1_V_ACCUM_INIT</i>		<i>MMReg:0x428</i>		2-72
<i>OV0_P1_X_START_END</i>		<i>MMReg:0x494</i>		2-82
<i>OV0_P23_BLANK_LINES_AT_TOP</i>		<i>MMReg:0x434</i>		2-73
<i>OV0_P23_H_ACCUM_INIT</i>		<i>MMReg:0x48C</i>		2-81
<i>OV0_P23_V_ACCUM_INIT</i>		<i>MMReg:0x42C</i>		2-73
<i>OV0_P2_X_START_END</i>		<i>MMReg:0x498</i>		2-82
<i>OV0_P3_X_START_END</i>		<i>MMReg:0x49C</i>		2-82
<i>OV0_PIPELINE_CNTL</i>		<i>MMReg:0x408</i>		2-262
<i>OV0_REG_LOAD_CNTL</i>		<i>MMReg:0x410</i>		2-69
<i>OV0_SCALE_CNTL</i>		<i>MMReg:0x420</i>		2-70
<i>OV0_SLICE_CNTL</i>		<i>MMReg:0x4E0</i>		2-262
<i>OV0_STEP_BY</i>		<i>MMReg:0x484</i>		2-80
<i>OV0_SUBMIT_HISTORY</i>		<i>MMReg:0x478</i>		2-262
<i>OV0_TEST</i>		<i>MMReg:0x4F8</i>		2-87
<i>OV0_V_INC</i>		<i>MMReg:0x424</i>		2-72
<i>OV0_VID_BUF0_BASE_ADRS</i>		<i>MMReg:0x440</i>		2-74
<i>OV0_VID_BUF1_BASE_ADRS</i>		<i>MMReg:0x444</i>		2-75
<i>OV0_VID_BUF2_BASE_ADRS</i>		<i>MMReg:0x448</i>		2-75
<i>OV0_VID_BUF3_BASE_ADRS</i>		<i>MMReg:0x44C</i>		2-75

Table 2-2 MMR Registers Sorted by Name (Continued)

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<i>OV0_VID_BUF5_BASE_ADRS</i>		<i>MMReg:0x454</i>		2-76
<i>OV0_VID_BUF_PITCH0_VALUE</i>		<i>MMReg:0x460</i>		2-76
<i>OV0_VID_BUF_PITCH1_VALUE</i>		<i>MMReg:0x464</i>		2-77
<i>OV0_VID_KEY_CLR_HIGH</i>		<i>MMReg:0x4E8</i>		2-263
<i>OV0_VID_KEY_CLR_LOW</i>		<i>MMReg:0x4E4</i>		2-85
<i>OV0_Y_X_END</i>		<i>MMReg:0x404</i>		2-68
<i>OV0_Y_X_START</i>		<i>MMReg:0x400</i>		2-68
<i>OVR_CLR</i>		<i>MMReg:0x230</i>		2-53
<i>OVR_WID_LEFT_RIGHT</i>		<i>MMReg:0x234</i>		2-53
<i>OVR_WID_TOP_BOTTOM</i>		<i>MMReg:0x238</i>		2-54
<i>PAD_AGPINPUT_DELAY</i>		<i>MMReg:0x164</i>		2-241
<i>PAD_CTLR_STRENGTH</i>		<i>MMReg:0x168</i>		2-241
<i>PAD_CTLR_UPDATE</i>		<i>MMReg:0x16C</i>		2-242
<i>PALETTE_30_DATA</i>	<i>IOReg:0xB8</i>	<i>MMReg:0xB8</i>		2-46
<i>PALETTE_INDEX</i>	<i>IOReg:0xB0</i>	<i>MMReg:0xB0</i>		2-46
<i>PP_CUBIC_OFFSET_T0_0</i>		<i>MMReg:0x1DD0</i>	<i>MMReg:0x2DD0</i>	2-279
<i>PP_CUBIC_OFFSET_T0_1</i>		<i>MMReg:0x1DD4</i>	<i>MMReg:0x2DD4</i>	2-280
<i>PP_CUBIC_OFFSET_T0_2</i>		<i>MMReg:0x1DD8</i>	<i>MMReg:0x2DD8</i>	2-280
<i>PP_CUBIC_OFFSET_T0_3</i>		<i>MMReg:0x1DDC</i>	<i>MMReg:0x2DDC</i>	2-280
<i>PP_CUBIC_OFFSET_T0_4</i>		<i>MMReg:0x1DE0</i>	<i>MMReg:0x2DE0</i>	2-280
<i>PP_CUBIC_OFFSET_T1_0</i>		<i>MMReg:0x1E00</i>	<i>MMReg:0x2E00</i>	2-280
<i>PP_CUBIC_OFFSET_T1_1</i>		<i>MMReg:0x1E04</i>	<i>MMReg:0x2E04</i>	2-281
<i>PP_CUBIC_OFFSET_T1_2</i>		<i>MMReg:0x1E08</i>	<i>MMReg:0x2E08</i>	2-281
<i>PP_CUBIC_OFFSET_T1_3</i>		<i>MMReg:0x1E0C</i>	<i>MMReg:0x2E0C</i>	2-281
<i>PP_CUBIC_OFFSET_T1_4</i>		<i>MMReg:0x1E10</i>	<i>MMReg:0x2E10</i>	2-281
<i>PP_CUBIC_OFFSET_T2_0</i>		<i>MMReg:0x1E14</i>	<i>MMReg:0x2E14</i>	2-281
<i>PP_CUBIC_OFFSET_T2_1</i>		<i>MMReg:0x1E18</i>	<i>MMReg:0x2E18</i>	2-282
<i>PP_CUBIC_OFFSET_T2_2</i>		<i>MMReg:0x1E1C</i>	<i>MMReg:0x2E1C</i>	2-282
<i>PP_CUBIC_OFFSET_T2_3</i>		<i>MMReg:0x1E20</i>	<i>MMReg:0x2E20</i>	2-282
<i>PP_CUBIC_OFFSET_T2_4</i>		<i>MMReg:0x1E24</i>	<i>MMReg:0x2E24</i>	2-282
<i>PP_CUBIC_OFFSET_T3_0</i>		<i>MMReg:0x2E28</i>		2-282
<i>PP_CUBIC_OFFSET_T3_1</i>		<i>MMReg:0x2E2C</i>		2-283
<i>PP_CUBIC_OFFSET_T3_2</i>		<i>MMReg:0x2E30</i>		2-283
<i>PP_CUBIC_OFFSET_T3_3</i>		<i>MMReg:0x2E34</i>		2-283
<i>PP_CUBIC_OFFSET_T3_4</i>		<i>MMReg:0x2E38</i>		2-283
<i>PP_LUM_MATRIX</i>		<i>MMReg:0x1D00</i>	<i>MMReg:0x2D00</i>	2-284
<i>PP_ROT_MATRIX_0</i>		<i>MMReg:0x1D58</i>	<i>MMReg:0x2D58</i>	2-283
<i>PP_ROT_MATRIX_1</i>		<i>MMReg:0x1D5C</i>	<i>MMReg:0x2D5C</i>	2-284
<i>PP_TRI_JUICE</i>		<i>MMReg:0x2D64</i>		2-284
<i>RB2D_CLRCMP_CNTL</i>		<i>MMReg:0x3414</i>		2-191
<i>RB2D_CLRCMP_DST</i>		<i>MMReg:0x340C</i>		2-190
<i>RB2D_CLRCMP_FLIPE</i>		<i>MMReg:0x3410</i>		2-190
<i>RB2D_CLRCMP_MSK</i>		<i>MMReg:0x3418</i>		2-191
<i>RB2D_CLRCMP_SRC</i>		<i>MMReg:0x3408</i>		2-190

Table 2-2 MMR Registers Sorted by Name (Continued)

Name	I/OAddress	MM Address	Second Address	Page
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<i>RB2D_DST_ENDIAN</i>		<i>MMReg:0x3434</i>		2-286
<i>RB2D_DSTCACHE_CTLSTAT</i>		<i>MMReg:0x342C</i>		2-285
<i>RB2D_DSTCACHE_MODE</i>		<i>MMReg:0x3428</i>		2-284
<i>RB2D_GUI_MASTER_CNTL</i>		<i>MMReg:0x3424</i>		2-192
<i>RB2D_PD1_ADDR</i>		<i>MMReg:0x343C</i>		2-286
<i>RB2D_PD1_DATA</i>		<i>MMReg:0x3438</i>		2-286
<i>RB2D_ROP</i>		<i>MMReg:0x3400</i>		2-190
<i>RB2D_SRC_ENDIAN</i>		<i>MMReg:0x3430</i>		2-286
<i>RB2D_WRITEBACK_ADDR</i>		<i>MMReg:0x3458</i>		2-287
<i>RB2D_WRITEBACK_DATA_HI</i>		<i>MMReg:0x3454</i>		2-287
<i>RB2D_WRITEBACK_DATA_LO</i>		<i>MMReg:0x3450</i>		2-287
<i>RB2D_WRITEMASK</i>		<i>MMReg:0x341C</i>		2-192
<i>RB3D_DEPTHXY_OFFSET</i>		<i>MMReg:0x1D60</i>		2-287
<i>RBBM_CMDFIFO_ADDR</i>		<i>MMReg:0xE70</i>		2-11
<i>RBBM_CMDFIFO_DATAH</i>		<i>MMReg:0xE78</i>		2-12
<i>RBBM_CMDFIFO_DATA_L</i>		<i>MMReg:0xE74</i>		2-12
<i>RBBM_CMDFIFO_STAT</i>		<i>MMReg:0xE7C</i>		2-12
<i>RBBM_CNTL</i>	<i>IOReg:0xEC</i>	<i>MMReg:0xEC</i>	<i>MMReg:0xE44</i>	2-5
<i>RBBM_GUICNTL</i>		<i>MMReg:0x172C</i>		2-11
<i>RBBM_SOFT_RESET</i>	<i>IOReg:0xF0</i>	<i>MMReg:0xF0</i>	<i>MMReg:0xE48</i>	2-7
<i>RBBM_STATUS</i>		<i>MMReg:0xE40</i>	<i>MMReg:0x1740</i>	2-7
<i>RE_AUX_SCISSOR_CNTL</i>		<i>MMReg:0x26F0</i>		2-273
<i>RE_DDA_DS3_0</i>		<i>MMReg:0x2940</i>		2-278
<i>RE_DDA_DS3_1</i>		<i>MMReg:0x2944</i>		2-278
<i>RE_DDA_DS3_2</i>		<i>MMReg:0x2948</i>		2-278
<i>RE_DDA_DS3_3</i>		<i>MMReg:0x294C</i>		2-278
<i>RE_DDA_DT3_0</i>		<i>MMReg:0x2960</i>		2-279
<i>RE_DDA_DT3_1</i>		<i>MMReg:0x2964</i>		2-279
<i>RE_DDA_DT3_2</i>		<i>MMReg:0x2968</i>		2-279
<i>RE_DDA_DT3_3</i>		<i>MMReg:0x296C</i>		2-279
<i>RE_DDA_Q3_0</i>		<i>MMReg:0x28B0</i>		2-277
<i>RE_DDA_Q3_1</i>		<i>MMReg:0x28B4</i>		2-277
<i>RE_DDA_Q3_2</i>		<i>MMReg:0x28B8</i>		2-277
<i>RE_DDA_Q3_3</i>		<i>MMReg:0x28BC</i>		2-278
<i>RE_DDA_RHW_0</i>		<i>MMReg:0x2730</i>		2-274
<i>RE_DDA_RHW_1</i>		<i>MMReg:0x2734</i>		2-275
<i>RE_DDA_RHW_2</i>		<i>MMReg:0x2738</i>		2-275
<i>RE_DDA_RHW_3</i>		<i>MMReg:0x273C</i>		2-275
<i>RE_DDA_S3_0</i>		<i>MMReg:0x2880</i>		2-275
<i>RE_DDA_S3_1</i>		<i>MMReg:0x2884</i>		2-275
<i>RE_DDA_S3_2</i>		<i>MMReg:0x2888</i>		2-276
<i>RE_DDA_S3_3</i>		<i>MMReg:0x288C</i>		2-276
<i>RE_DDA_T3_0</i>		<i>MMReg:0x2890</i>		2-276

Table 2-2 MMR Registers Sorted by Name (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>RE_DDA_T3_1</i>		<i>MMReg:0x2894</i>		2-276
<i>RE_DDA_T3_2</i>		<i>MMReg:0x2898</i>		2-277
<i>RE_DDA_T3_3</i>		<i>MMReg:0x289C</i>		2-277
<i>RE_LINE_PATTERN</i>		<i>MMReg:0x1CD0</i>	<i>MMReg:0x26D0</i>	2-194
<i>RE_LINE_STATE</i>		<i>MMReg:0x1CD4</i>	<i>MMReg:0x26D4</i>	2-194
<i>RE_MISC</i>		<i>MMReg:0x1CC4</i>	<i>MMReg:0x26C4</i>	2-193
<i>RE_NULL_PRIM</i>		<i>MMReg:0x29E0</i>		2-274
<i>RE_SCISSOR_BR_0</i>		<i>MMReg:0x1CDC</i>	<i>MMReg:0x26DC</i>	2-195
<i>RE_SCISSOR_BR_1</i>		<i>MMReg:0x1CE4</i>	<i>MMReg:0x26E4</i>	2-195
<i>RE_SCISSOR_BR_2</i>		<i>MMReg:0x1CEC</i>	<i>MMReg:0x26EC</i>	2-196
<i>RE_SCISSOR_TL_0</i>		<i>MMReg:0x1CD8</i>	<i>MMReg:0x26D8</i>	2-195
<i>RE_SCISSOR_TL_1</i>		<i>MMReg:0x1CE0</i>	<i>MMReg:0x26E0</i>	2-195
<i>RE_SCISSOR_TL_2</i>		<i>MMReg:0x1CE8</i>	<i>MMReg:0x26E8</i>	2-195
<i>RE_SOLID_COLOR</i>		<i>MMReg:0x1C1C</i>	<i>MMReg:0x261C</i>	2-193
<i>RE_STIPPLE_ADDR</i>		<i>MMReg:0x1CC8</i>	<i>MMReg:0x26C8</i>	2-193
<i>RE_STIPPLE_DATA</i>		<i>MMReg:0x1CCC</i>	<i>MMReg:0x26CC</i>	2-194
<i>RE_TOP_LEFT</i>		<i>MMReg:0x26C0</i>		2-273
<i>RE_WIDTH_HEIGHT</i>		<i>MMReg:0x1C44</i>	<i>MMReg:0x2644</i>	2-193
<i>RE_Z_MINMAX_0</i>		<i>MMReg:0x29F0</i>		2-274
<i>RE_Z_MINMAX_1</i>		<i>MMReg:0x29F4</i>		2-274
<i>RE_Z_MINMAX_3</i>		<i>MMReg:0x29FC</i>		2-274
<i>RMX_HORZ_FILTER_0TAP_COEF</i>		<i>MMReg:0xDB0</i>		2-103
<i>RMX_HORZ_FILTER_1TAP_COEF</i>		<i>MMReg:0xDB4</i>		2-103
<i>RMX_HORZ_FILTER_2TAP_COEF</i>		<i>MMReg:0xDB8</i>		2-103
<i>RMX_HORZ_PHASE</i>		<i>MMReg:0xDBC</i>		2-104
<i>SC_BOTTOM</i>		<i>MMReg:0x164C</i>		2-181
<i>SC_BOTTOM_RIGHT</i>		<i>MMReg:0x16F0</i>		2-184
<i>SC_LEFT</i>		<i>MMReg:0x1640</i>		2-180
<i>SC_RIGHT</i>		<i>MMReg:0x1644</i>		2-180
<i>SC_TOP</i>		<i>MMReg:0x1648</i>		2-181
<i>SC_TOP_LEFT</i>		<i>MMReg:0x16EC</i>		2-184
<i>SCRATCH_ADDR</i>		<i>MMReg:0x774</i>		2-146
<i>SCRATCH_REG0</i>		<i>MMReg:0x15E0</i>		2-144
<i>SCRATCH_REG1</i>		<i>MMReg:0x15E4</i>		2-145
<i>SCRATCH_REG2</i>		<i>MMReg:0x15E8</i>		2-145
<i>SCRATCH_REG3</i>		<i>MMReg:0x15EC</i>		2-145
<i>SCRATCH_REG4</i>		<i>MMReg:0x15F0</i>		2-145
<i>SCRATCH_REG5</i>		<i>MMReg:0x15F4</i>		2-145
<i>SCRATCH_UMSK</i>		<i>MMReg:0x770</i>		2-146
<i>SNAPSHOT_F_COUNT</i>		<i>MMReg:0x244</i>		2-54
<i>SNAPSHOT_VH_COUNTS</i>		<i>MMReg:0x240</i>		2-54
<i>SNAPSHOT_VIF_COUNT</i>		<i>MMReg:0x24C</i>		2-55
<i>SRC_CLUT_ADDRESS</i>		<i>MMReg:0x1780</i>		2-185
<i>SRC_CLUT_DATA</i>		<i>MMReg:0x1784</i>		2-186
<i>SRC_CLUT_DATA_RD</i>		<i>MMReg:0x1788</i>		2-186

Table 2-2 MMR Registers Sorted by Name (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>SRC_OFFSET</i>		<i>MMReg:0x15AC</i>		2-177
<i>SRC_PITCH</i>		<i>MMReg:0x15B0</i>		2-177
<i>SRC_PITCH_OFFSET</i>		<i>MMReg:0x1428</i>		2-158
<i>SRC_SC_BOTTOM</i>		<i>MMReg:0x165C</i>		2-181
<i>SRC_SC_BOTTOM_RIGHT</i>		<i>MMReg:0x16F4</i>		2-185
<i>SRC_SC_RIGHT</i>		<i>MMReg:0x1654</i>		2-181
<i>SRC_TILE</i>		<i>MMReg:0x1704</i>		2-185
<i>SRC_X</i>		<i>MMReg:0x1414</i>		2-157
<i>SRC_X_Y</i>		<i>MMReg:0x1590</i>		2-175
<i>SRC_Y</i>		<i>MMReg:0x1418</i>		2-157
<i>SRC_Y_X</i>		<i>MMReg:0x1434</i>		2-158
<i>SURFACE0_INFO</i>		<i>MMReg:0xB0C</i>		2-22
<i>SURFACE0_LOWER_BOUND</i>		<i>MMReg:0xB04</i>		2-23
<i>SURFACE0_UPPER_BOUND</i>		<i>MMReg:0xB08</i>		2-23
<i>SURFACE1_INFO</i>		<i>MMReg:0xB1C</i>		2-24
<i>SURFACE1_LOWER_BOUND</i>		<i>MMReg:0xB14</i>		2-24
<i>SURFACE1_UPPER_BOUND</i>		<i>MMReg:0xB18</i>		2-25
<i>SURFACE2_INFO</i>		<i>MMReg:0xB2C</i>		2-25
<i>SURFACE2_LOWER_BOUND</i>		<i>MMReg:0xB24</i>		2-26
<i>SURFACE2_UPPER_BOUND</i>		<i>MMReg:0xB28</i>		2-26
<i>SURFACE3_INFO</i>		<i>MMReg:0xB3C</i>		2-26
<i>SURFACE3_LOWER_BOUND</i>		<i>MMReg:0xB34</i>		2-27
<i>SURFACE3_UPPER_BOUND</i>		<i>MMReg:0xB38</i>		2-27
<i>SURFACE4_INFO</i>		<i>MMReg:0xB4C</i>		2-27
<i>SURFACE4_LOWER_BOUND</i>		<i>MMReg:0xB44</i>		2-28
<i>SURFACE4_UPPER_BOUND</i>		<i>MMReg:0xB48</i>		2-28
<i>SURFACE5_INFO</i>		<i>MMReg:0xB5C</i>		2-29
<i>SURFACE5_LOWER_BOUND</i>		<i>MMReg:0xB54</i>		2-29
<i>SURFACE5_UPPER_BOUND</i>		<i>MMReg:0xB58</i>		2-30
<i>SURFACE6_INFO</i>		<i>MMReg:0xB6C</i>		2-30
<i>SURFACE6_LOWER_BOUND</i>		<i>MMReg:0xB64</i>		2-31
<i>SURFACE6_UPPER_BOUND</i>		<i>MMReg:0xB68</i>		2-31
<i>SURFACE7_INFO</i>		<i>MMReg:0xB7C</i>		2-31
<i>SURFACE7_LOWER_BOUND</i>		<i>MMReg:0xB74</i>		2-32
<i>SURFACE7_UPPER_BOUND</i>		<i>MMReg:0xB78</i>		2-32
<i>SURFACE_ACCESS_CLR</i>		<i>MMReg:0xBFC</i>		2-255
<i>SURFACE_ACCESS_FLAGS</i>		<i>MMReg:0xBF8</i>		2-254
<i>SURFACE_CNTL</i>		<i>MMReg:0xB00</i>		2-22
<i>SW_SEMAPHORE</i>		<i>MMReg:0x13C</i>		2-22
<i>TMDS_CNTL</i>		<i>MMReg:0x294</i>		2-105
<i>TMDS_CRC</i>		<i>MMReg:0x2A0</i>		2-106
<i>TMDS_PATTERN_GEN_SEED</i>		<i>MMReg:0x2AC</i>		2-291
<i>TMDS_PLL_CNTL</i>		<i>MMReg:0x2A8</i>		2-107
<i>TMDS_SYNC_CHAR_SETA</i>		<i>MMReg:0x298</i>		2-105

Table 2-2 MMR Registers Sorted by Name (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>TMDS_SYNC_CHAR_SETB</i>		<i>MMReg:0x29C</i>		2-106
<i>TMDS_TRANSMITTER_CNTL</i>		<i>MMReg:0x2A4</i>		2-106
<i>TVOUT_0_SCRATCH</i>	<i>IOReg:0x88</i>	<i>MMReg:0x88</i>		2-289
<i>TVOUT_1_SCRATCH</i>	<i>IOReg:0x8C</i>	<i>MMReg:0x8C</i>		2-289
<i>VGA_BUFFER_CNTL</i>		<i>MMReg:0x2F4</i>		2-261
<i>VID_BUFFER_CONTROL</i>		<i>MMReg:0x900</i>		2-128
<i>VIPH_CH0_ABCNT</i>		<i>MMReg:0xC30</i>		2-112
<i>VIPH_CH0_ADDR</i>		<i>MMReg:0xC10</i>		2-110
<i>VIPH_CH0_DATA</i>		<i>MMReg:0xC00</i>		2-110
<i>VIPH_CH0_SBCNT</i>		<i>MMReg:0xC20</i>		2-111
<i>VIPH_CH1_ABCNT</i>		<i>MMReg:0xC34</i>		2-112
<i>VIPH_CH1_ADDR</i>		<i>MMReg:0xC14</i>		2-111
<i>VIPH_CH1_DATA</i>		<i>MMReg:0xC04</i>		2-110
<i>VIPH_CH1_SBCNT</i>		<i>MMReg:0xC24</i>		2-112
<i>VIPH_CH2_ABCNT</i>		<i>MMReg:0xC38</i>		2-113
<i>VIPH_CH2_ADDR</i>		<i>MMReg:0xC18</i>		2-111
<i>VIPH_CH2_DATA</i>		<i>MMReg:0xC08</i>		2-110
<i>VIPH_CH2_SBCNT</i>		<i>MMReg:0xC28</i>		2-112
<i>VIPH_CH3_ABCNT</i>		<i>MMReg:0xC3C</i>		2-113
<i>VIPH_CH3_ADDR</i>		<i>MMReg:0xC1C</i>		2-111
<i>VIPH_CH3_DATA</i>		<i>MMReg:0xC0C</i>		2-110
<i>VIPH_CH3_SBCNT</i>		<i>MMReg:0xC2C</i>		2-112
<i>VIPH_CONTROL</i>		<i>MMReg:0xC40</i>		2-113
<i>VIPH_DMA_CHUNK</i>		<i>MMReg:0xC48</i>		2-114
<i>VIPH_DV_INT</i>		<i>MMReg:0xC4C</i>		2-115
<i>VIPH_DV_LAT</i>		<i>MMReg:0xC44</i>		2-114
<i>VIPH_REG_ADDR</i>	<i>IOReg:0x80</i>	<i>MMReg:0x80</i>		2-116
<i>VIPH_REG_DATA</i>	<i>IOReg:0x84</i>	<i>MMReg:0x84</i>		2-116
<i>VIPH_TIMEOUT_STAT</i>		<i>MMReg:0xC50</i>		2-115
<i>VIPPAD1_MASK</i>		<i>MMReg:0x1A8</i>		2-290
<i>VIPPAD1_Y</i>		<i>MMReg:0x1B4</i>		2-290
<i>VIPPAD_STRENGTH</i>		<i>MMReg:0x194</i>		2-289
<i>WAIT_UNTIL</i>		<i>MMReg:0x1720</i>		2-9

## A.3 MMR Registers Sorted by Address

Table 2-3 MMR Registers Sorted by Address

Name	I/OAddress	MM Address	Second Address	Page
<i>MM_INDEX</i>	<i>IReg:0x0</i>	<i>MMReg:0x0</i>		2-237
<i>BUS_CNTL</i>	<i>IReg:0x30</i>	<i>MMReg:0x30</i>		2-237
<i>BUS_CNTL1</i>	<i>IReg:0x34</i>	<i>MMReg:0x34</i>		2-239
<i>MEM_VGA_WP_SEL</i>	<i>IReg:0x38</i>	<i>MMReg:0x38</i>		2-201
<i>MEM_VGA_RP_SEL</i>	<i>IReg:0x3C</i>	<i>MMReg:0x3C</i>		2-201
<i>MM_DATA</i>	<i>IReg:0x4</i>	<i>MMReg:0x4</i>		2-237
<i>GEN_INT_CNTL</i>	<i>IReg:0x40</i>	<i>MMReg:0x40</i>		2-2
<i>GEN_INT_STATUS</i>	<i>IReg:0x44</i>	<i>MMReg:0x44</i>		2-3
<i>GEN_INT_STATUS</i>	<i>IReg:0x44</i>	<i>MMReg:0x44</i>		2-118
<i>HI_STAT</i>	<i>IReg:0x4C</i>	<i>MMReg:0x4C</i>		2-239
<i>CRTC_GEN_CNTL</i>	<i>IReg:0x50</i>	<i>MMReg:0x50</i>		2-41
<i>CRTC_EXT_CNTL</i>	<i>IReg:0x54</i>	<i>MMReg:0x54</i>		2-43
<i>DAC_CNTL</i>	<i>IReg:0x58</i>	<i>MMReg:0x58</i>		2-35
<i>CRTC_STATUS</i>	<i>IReg:0x5C</i>	<i>MMReg:0x5C</i>		2-45
<i>GPIO_VGA_DDC</i>	<i>IReg:0x60</i>	<i>MMReg:0x60</i>		2-257
<i>GPIO_DVI_DDC</i>	<i>IReg:0x64</i>	<i>MMReg:0x64</i>		2-258
<i>GPIO_MONID</i>	<i>IReg:0x68</i>	<i>MMReg:0x68</i>		2-45
<i>CLOCK_CNTL_INDEX</i>	<i>IReg:0x8</i>	<i>MMReg:0x8</i>		2-266
<i>VIPH_REG_ADDR</i>	<i>IReg:0x80</i>	<i>MMReg:0x80</i>		2-116
<i>VIPH_REG_DATA</i>	<i>IReg:0x84</i>	<i>MMReg:0x84</i>		2-116
<i>TVOUT_0_SCRATCH</i>	<i>IReg:0x88</i>	<i>MMReg:0x88</i>		2-289
<i>TVOUT_1_SCRATCH</i>	<i>IReg:0x8C</i>	<i>MMReg:0x8C</i>		2-289
<i>I2C_CNTL_0</i>	<i>IReg:0x90</i>	<i>MMReg:0x90</i>		2-108
<i>I2C_CNTL_1</i>	<i>IReg:0x94</i>	<i>MMReg:0x94</i>		2-109
<i>I2C_DATA</i>	<i>IReg:0x98</i>	<i>MMReg:0x98</i>		2-109
<i>PALETTE_INDEX</i>	<i>IReg:0xB0</i>	<i>MMReg:0xB0</i>		2-46
<i>PALETTE_30_DATA</i>	<i>IReg:0xB8</i>	<i>MMReg:0xB8</i>		2-46
<i>CLOCK_CNTL_DATA</i>	<i>IReg:0xC</i>	<i>MMReg:0xC</i>		2-266
<i>CONFIG_CNTL</i>	<i>IReg:0xE0</i>	<i>MMReg:0xE0</i>		2-240
<i>RBBM_CNTL</i>	<i>IReg:0xEC</i>	<i>MMReg:0xEC</i>	<i>MMReg:0xE44</i>	2-5
<i>RBBM_SOFT_RESET</i>	<i>IReg:0xF0</i>	<i>MMReg:0xF0</i>	<i>MMReg:0xE48</i>	2-7
<i>CONFIG_MEMSIZE</i>	<i>IReg:0xF8</i>	<i>MMReg:0xF8</i>		2-240
<i>CONFIG_APER_0_BASE</i>		<i>MMReg:0x100</i>		2-240
<i>CP_CSQ_APER_PRIMARY</i>		<i>MMReg:0x1000-0x11FC</i>		2-144
<i>CONFIG_APER_1_BASE</i>		<i>MMReg:0x104</i>		2-240
<i>CONFIG_APER_SIZE</i>		<i>MMReg:0x108</i>		2-241
<i>CONFIG_REG_1_BASE</i>		<i>MMReg:0x10C</i>		2-241
<i>CONFIG_REG_APER_SIZE</i>		<i>MMReg:0x110</i>		2-241
<i>HOST_PATH_CNTL</i>		<i>MMReg:0x130</i>		2-21
<i>CP_CSQ_APER_INDIRECT</i>		<i>MMReg:0x1300-0x13FC</i>		2-144
<i>SW_SEMAPHORE</i>		<i>MMReg:0x13C</i>		2-22

Table 2-3 MMR Registers Sorted by Address (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>MEM_CNTL</i>		<i>MMReg:0x140</i>		<i>2-15</i>
<i>DST_OFFSET</i>		<i>MMReg:0x1404</i>		<i>2-156</i>
<i>DST_PITCH</i>		<i>MMReg:0x1408</i>		<i>2-156</i>
<i>DST_WIDTH</i>		<i>MMReg:0x140C</i>		<i>2-156</i>
<i>DST_HEIGHT</i>		<i>MMReg:0x1410</i>		<i>2-157</i>
<i>SRC_X</i>		<i>MMReg:0x1414</i>		<i>2-157</i>
<i>SRC_Y</i>		<i>MMReg:0x1418</i>		<i>2-157</i>
<i>DST_X</i>		<i>MMReg:0x141C</i>		<i>2-157</i>
<i>DST_Y</i>		<i>MMReg:0x1420</i>		<i>2-157</i>
<i>SRC_PITCH_OFFSET</i>		<i>MMReg:0x1428</i>		<i>2-158</i>
<i>DST_PITCH_OFFSET</i>		<i>MMReg:0x142C</i>		<i>2-158</i>
<i>SRC_Y_X</i>		<i>MMReg:0x1434</i>		<i>2-158</i>
<i>DST_Y_X</i>		<i>MMReg:0x1438</i>		<i>2-159</i>
<i>DST_HEIGHT_WIDTH</i>		<i>MMReg:0x143C</i>		<i>2-159</i>
<i>EXT_MEM_CNTL</i>		<i>MMReg:0x144</i>		<i>2-19</i>
<i>DP_GUI_MASTER_CNTL</i>		<i>MMReg:0x146C</i>		<i>2-159</i>
<i>BRUSH_Y_X</i>		<i>MMReg:0x1474</i>		<i>2-161</i>
<i>DP_BRUSH_BKGD_CLR</i>		<i>MMReg:0x1478</i>		<i>2-162</i>
<i>DP_BRUSH_FRGD_CLR</i>		<i>MMReg:0x147C</i>		<i>2-162</i>
<i>MC_FB_LOCATION</i>		<i>MMReg:0x148</i>		<i>2-16</i>
<i>BRUSH_DATA0</i>		<i>MMReg:0x1480</i>		<i>2-162</i>
<i>BRUSH_DATA1</i>		<i>MMReg:0x1484</i>		<i>2-162</i>
<i>BRUSH_DATA2</i>		<i>MMReg:0x1488</i>		<i>2-162</i>
<i>BRUSH_DATA3</i>		<i>MMReg:0x148C</i>		<i>2-163</i>
<i>BRUSH_DATA4</i>		<i>MMReg:0x1490</i>		<i>2-163</i>
<i>BRUSH_DATA5</i>		<i>MMReg:0x1494</i>		<i>2-163</i>
<i>BRUSH_DATA6</i>		<i>MMReg:0x1498</i>		<i>2-163</i>
<i>BRUSH_DATA7</i>		<i>MMReg:0x149C</i>		<i>2-163</i>
<i>BRUSH_DATA8</i>		<i>MMReg:0x14A0</i>		<i>2-164</i>
<i>BRUSH_DATA9</i>		<i>MMReg:0x14A4</i>		<i>2-164</i>
<i>BRUSH_DATA10</i>		<i>MMReg:0x14A8</i>		<i>2-164</i>
<i>BRUSH_DATA11</i>		<i>MMReg:0x14AC</i>		<i>2-164</i>
<i>BRUSH_DATA12</i>		<i>MMReg:0x14B0</i>		<i>2-164</i>
<i>BRUSH_DATA13</i>		<i>MMReg:0x14B4</i>		<i>2-165</i>
<i>BRUSH_DATA14</i>		<i>MMReg:0x14B8</i>		<i>2-165</i>
<i>BRUSH_DATA15</i>		<i>MMReg:0x14BC</i>		<i>2-165</i>
<i>MC_AGP_LOCATION</i>		<i>MMReg:0x14C</i>		<i>2-17</i>
<i>BRUSH_DATA16</i>		<i>MMReg:0x14C0</i>		<i>2-165</i>
<i>BRUSH_DATA17</i>		<i>MMReg:0x14C4</i>		<i>2-165</i>
<i>BRUSH_DATA18</i>		<i>MMReg:0x14C8</i>		<i>2-166</i>
<i>BRUSH_DATA19</i>		<i>MMReg:0x14CC</i>		<i>2-166</i>
<i>BRUSH_DATA20</i>		<i>MMReg:0x14D0</i>		<i>2-166</i>
<i>BRUSH_DATA21</i>		<i>MMReg:0x14D4</i>		<i>2-166</i>
<i>BRUSH_DATA22</i>		<i>MMReg:0x14D8</i>		<i>2-166</i>
<i>BRUSH_DATA23</i>		<i>MMReg:0x14DC</i>		<i>2-167</i>

Table 2-3 MMR Registers Sorted by Address (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>BRUSH_DATA24</i>		<i>MMReg:0x14E0</i>		2-167
<i>BRUSH_DATA25</i>		<i>MMReg:0x14E4</i>		2-167
<i>BRUSH_DATA26</i>		<i>MMReg:0x14E8</i>		2-167
<i>BRUSH_DATA27</i>		<i>MMReg:0x14EC</i>		2-167
<i>BRUSH_DATA28</i>		<i>MMReg:0x14F0</i>		2-168
<i>BRUSH_DATA29</i>		<i>MMReg:0x14F4</i>		2-168
<i>BRUSH_DATA30</i>		<i>MMReg:0x14F8</i>		2-168
<i>BRUSH_DATA31</i>		<i>MMReg:0x14FC</i>		2-168
<i>BRUSH_DATA32</i>		<i>MMReg:0x1500</i>		2-168
<i>BRUSH_DATA33</i>		<i>MMReg:0x1504</i>		2-169
<i>BRUSH_DATA34</i>		<i>MMReg:0x1508</i>		2-169
<i>BRUSH_DATA35</i>		<i>MMReg:0x150C</i>		2-169
<i>BRUSH_DATA36</i>		<i>MMReg:0x1510</i>		2-169
<i>BRUSH_DATA37</i>		<i>MMReg:0x1514</i>		2-169
<i>BRUSH_DATA38</i>		<i>MMReg:0x1518</i>		2-170
<i>BRUSH_DATA39</i>		<i>MMReg:0x151C</i>		2-170
<i>BRUSH_DATA40</i>		<i>MMReg:0x1520</i>		2-170
<i>BRUSH_DATA41</i>		<i>MMReg:0x1524</i>		2-170
<i>BRUSH_DATA42</i>		<i>MMReg:0x1528</i>		2-170
<i>BRUSH_DATA43</i>		<i>MMReg:0x152C</i>		2-171
<i>BRUSH_DATA44</i>		<i>MMReg:0x1530</i>		2-171
<i>BRUSH_DATA45</i>		<i>MMReg:0x1534</i>		2-171
<i>BRUSH_DATA46</i>		<i>MMReg:0x1538</i>		2-171
<i>BRUSH_DATA47</i>		<i>MMReg:0x153C</i>		2-171
<i>MEM_INIT_LATENCY_TIMER</i>		<i>MMReg:0x154</i>		2-17
<i>BRUSH_DATA48</i>		<i>MMReg:0x1540</i>		2-172
<i>BRUSH_DATA49</i>		<i>MMReg:0x1544</i>		2-172
<i>BRUSH_DATA50</i>		<i>MMReg:0x1548</i>		2-172
<i>BRUSH_DATA51</i>		<i>MMReg:0x154C</i>		2-172
<i>BRUSH_DATA52</i>		<i>MMReg:0x1550</i>		2-172
<i>BRUSH_DATA53</i>		<i>MMReg:0x1554</i>		2-173
<i>BRUSH_DATA54</i>		<i>MMReg:0x1558</i>		2-173
<i>BRUSH_DATA55</i>		<i>MMReg:0x155C</i>		2-173
<i>BRUSH_DATA56</i>		<i>MMReg:0x1560</i>		2-173
<i>BRUSH_DATA57</i>		<i>MMReg:0x1564</i>		2-173
<i>BRUSH_DATA58</i>		<i>MMReg:0x1568</i>		2-174
<i>BRUSH_DATA59</i>		<i>MMReg:0x156C</i>		2-174
<i>BRUSH_DATA60</i>		<i>MMReg:0x1570</i>		2-174
<i>BRUSH_DATA61</i>		<i>MMReg:0x1574</i>		2-174
<i>BRUSH_DATA62</i>		<i>MMReg:0x1578</i>		2-174
<i>BRUSH_DATA63</i>		<i>MMReg:0x157C</i>		2-175
<i>MEM_SDRAM_MODE_REG</i>		<i>MMReg:0x158</i>		2-18
<i>DST_WIDTH_X</i>		<i>MMReg:0x1588</i>		2-175
<i>DST_HEIGHT_WIDTH_8</i>		<i>MMReg:0x158C</i>		2-175

Table 2-3 MMR Registers Sorted by Address (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>SRC_X_Y</i>		<i>MMReg:0x1590</i>		2-175
<i>DST_X_Y</i>		<i>MMReg:0x1594</i>		2-176
<i>DST_WIDTH_HEIGHT</i>		<i>MMReg:0x1598</i>		2-176
<i>DST_WIDTH_X_INCY</i>		<i>MMReg:0x159C</i>		2-176
<i>DST_HEIGHT_Y</i>		<i>MMReg:0x15A0</i>		2-177
<i>SRC_OFFSET</i>		<i>MMReg:0x15AC</i>		2-177
<i>SRC_PITCH</i>		<i>MMReg:0x15B0</i>		2-177
<i>CLR_CMP_CNTL</i>		<i>MMReg:0x15C0</i>		2-178
<i>CLR_CMP_CLR_SRC</i>		<i>MMReg:0x15C4</i>		2-178
<i>CLR_CMP_CLR_DST</i>		<i>MMReg:0x15C8</i>		2-179
<i>CLR_CMP_MSK</i>		<i>MMReg:0x15CC</i>		2-179
<i>DP_DST_ENDIAN</i>		<i>MMReg:0x15D0</i>		2-288
<i>DP_SRC_ENDIAN</i>		<i>MMReg:0x15D4</i>		2-288
<i>DP_SRC_FRGD_CLR</i>		<i>MMReg:0x15D8</i>		2-179
<i>DP_SRC_BKGD_CLR</i>		<i>MMReg:0x15DC</i>		2-179
<i>SCRATCH_REG0</i>		<i>MMReg:0x15E0</i>		2-144
<i>SCRATCH_REG1</i>		<i>MMReg:0x15E4</i>		2-145
<i>SCRATCH_REG2</i>		<i>MMReg:0x15E8</i>		2-145
<i>SCRATCH_REG3</i>		<i>MMReg:0x15EC</i>		2-145
<i>SCRATCH_REG4</i>		<i>MMReg:0x15F0</i>		2-145
<i>SCRATCH_REG5</i>		<i>MMReg:0x15F4</i>		2-145
<i>BM_STATUS</i>		<i>MMReg:0x160</i>		2-243
<i>DST_LINE_START</i>		<i>MMReg:0x1600</i>		2-179
<i>DST_LINE_END</i>		<i>MMReg:0x1604</i>		2-180
<i>DST_LINE_PATCOUNT</i>		<i>MMReg:0x1608</i>		2-180
<i>PAD_AGPINPUT_DELAY</i>		<i>MMReg:0x164</i>		2-241
<i>SC_LEFT</i>		<i>MMReg:0x1640</i>		2-180
<i>SC_RIGHT</i>		<i>MMReg:0x1644</i>		2-180
<i>SC_TOP</i>		<i>MMReg:0x1648</i>		2-181
<i>SC_BOTTOM</i>		<i>MMReg:0x164C</i>		2-181
<i>SRC_SC_RIGHT</i>		<i>MMReg:0x1654</i>		2-181
<i>SRC_SC_BOTTOM</i>		<i>MMReg:0x165C</i>		2-181
<i>PAD_CTLR_STRENGTH</i>		<i>MMReg:0x168</i>		2-241
<i>PAD_CTLR_UPDATE</i>		<i>MMReg:0x16C</i>		2-242
<i>DP_CNTL</i>		<i>MMReg:0x16C0</i>		2-182
<i>DP_DATATYPE</i>		<i>MMReg:0x16C4</i>		2-182
<i>DP_MIX</i>		<i>MMReg:0x16C8</i>		2-183
<i>DP_WRITE_MSK</i>		<i>MMReg:0x16CC</i>		2-184
<i>DP_CNTL_XDIR_YDIR_YMAJOR</i>		<i>MMReg:0x16D0</i>		2-288
<i>DEFAULT_PITCH_OFFSET</i>		<i>MMReg:0x16E0</i>		2-188
<i>DEFAULT_SC_BOTTOM_RIGHT</i>		<i>MMReg:0x16E8</i>		2-184
<i>SC_TOP_LEFT</i>		<i>MMReg:0x16EC</i>		2-184
<i>SC_BOTTOM_RIGHT</i>		<i>MMReg:0x16F0</i>		2-184
<i>SRC_SC_BOTTOM_RIGHT</i>		<i>MMReg:0x16F4</i>		2-185
<i>DST_TILE</i>		<i>MMReg:0x1700</i>		2-185

Table 2-3 MMR Registers Sorted by Address (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>SRC_TILE</i>		<i>MMReg:0x1704</i>		2-185
<i>DSTCACHE_MODE</i>		<i>MMReg:0x1710</i>		2-288
<i>DSTCACHE_CTLSTAT</i>		<i>MMReg:0x1714</i>		2-289
<i>WAIT_UNTIL</i>		<i>MMReg:0x1720</i>		2-9
<i>ISYNC_CNTL</i>		<i>MMReg:0x1724</i>		2-10
<i>RBBM_GUICNTL</i>		<i>MMReg:0x172C</i>		2-11
<i>AGP_CNTL</i>		<i>MMReg:0x174</i>		2-242
<i>SRC_CLUT_ADDRESS</i>		<i>MMReg:0x1780</i>		2-185
<i>SRC_CLUT_DATA</i>		<i>MMReg:0x1784</i>		2-186
<i>SRC_CLUT_DATA_RD</i>		<i>MMReg:0x1788</i>		2-186
<i>HOST_DATA0</i>		<i>MMReg:0x17C0</i>		2-186
<i>HOST_DATA1</i>		<i>MMReg:0x17C4</i>		2-186
<i>HOST_DATA2</i>		<i>MMReg:0x17C8</i>		2-186
<i>HOST_DATA3</i>		<i>MMReg:0x17CC</i>		2-187
<i>HOST_DATA4</i>		<i>MMReg:0x17D0</i>		2-187
<i>HOST_DATA5</i>		<i>MMReg:0x17D4</i>		2-187
<i>HOST_DATA6</i>		<i>MMReg:0x17D8</i>		2-187
<i>HOST_DATA7</i>		<i>MMReg:0x17DC</i>		2-188
<i>HOST_DATA_LAST</i>		<i>MMReg:0x17E0</i>		2-188
<i>DP_XOP</i>		<i>MMReg:0x17F8</i>		2-188
<i>VIPPAD_STRENGTH</i>		<i>MMReg:0x194</i>		2-289
<i>VIPPAD_I_MASK</i>		<i>MMReg:0x1A8</i>		2-290
<i>VIPPAD_I_Y</i>		<i>MMReg:0x1B4</i>		2-290
<i>EXTERN_TRIG_CNTL</i>		<i>MMReg:0x1BC</i>		2-290
<i>RE_SOLID_COLOR</i>		<i>MMReg:0x1C1C</i>	<i>MMReg:0x261C</i>	2-193
<i>RE_WIDTH_HEIGHT</i>		<i>MMReg:0x1C44</i>	<i>MMReg:0x2644</i>	2-193
<i>RE_MISC</i>		<i>MMReg:0x1CC4</i>	<i>MMReg:0x26C4</i>	2-193
<i>RE_STIPPLE_ADDR</i>		<i>MMReg:0x1CC8</i>	<i>MMReg:0x26C8</i>	2-193
<i>RE_STIPPLE_DATA</i>		<i>MMReg:0x1CCC</i>	<i>MMReg:0x26CC</i>	2-194
<i>RE_LINE_PATTERN</i>		<i>MMReg:0x1CD0</i>	<i>MMReg:0x26D0</i>	2-194
<i>RE_LINE_STATE</i>		<i>MMReg:0x1CD4</i>	<i>MMReg:0x26D4</i>	2-194
<i>RE_SCISSOR_TL_0</i>		<i>MMReg:0x1CD8</i>	<i>MMReg:0x26D8</i>	2-195
<i>RE_SCISSOR_BR_0</i>		<i>MMReg:0x1CDC</i>	<i>MMReg:0x26DC</i>	2-195
<i>RE_SCISSOR_TL_1</i>		<i>MMReg:0x1CE0</i>	<i>MMReg:0x26E0</i>	2-195
<i>RE_SCISSOR_BR_1</i>		<i>MMReg:0x1CE4</i>	<i>MMReg:0x26E4</i>	2-195
<i>RE_SCISSOR_TL_2</i>		<i>MMReg:0x1CE8</i>	<i>MMReg:0x26E8</i>	2-195
<i>RE_SCISSOR_BR_2</i>		<i>MMReg:0x1CEC</i>	<i>MMReg:0x26EC</i>	2-196
<i>AIC_CTRL</i>		<i>MMReg:0x1D0</i>		2-251
<i>PP_LUM_MATRIX</i>		<i>MMReg:0x1D00</i>	<i>MMReg:0x2D00</i>	2-284
<i>AIC_STAT</i>		<i>MMReg:0x1D4</i>		2-252
<i>PP_ROT_MATRIX_0</i>		<i>MMReg:0x1D58</i>	<i>MMReg:0x2D58</i>	2-283
<i>PP_ROT_MATRIX_1</i>		<i>MMReg:0x1D5C</i>	<i>MMReg:0x2D5C</i>	2-284
<i>RB3D_DEPTHXY_OFFSET</i>		<i>MMReg:0x1D60</i>		2-287
<i>AIC_PT_BASE</i>		<i>MMReg:0x1D8</i>		2-253

Table 2-3 MMR Registers Sorted by Address (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>AIC_LO_ADDR</i>		<i>MMReg:0x1DC</i>		2-253
<i>PP_CUBIC_OFFSET_T0_0</i>		<i>MMReg:0x1DD0</i>	<i>MMReg:0x2DD0</i>	2-279
<i>PP_CUBIC_OFFSET_T0_1</i>		<i>MMReg:0x1DD4</i>	<i>MMReg:0x2DD4</i>	2-280
<i>PP_CUBIC_OFFSET_T0_2</i>		<i>MMReg:0x1DD8</i>	<i>MMReg:0x2DD8</i>	2-280
<i>PP_CUBIC_OFFSET_T0_3</i>		<i>MMReg:0x1DDC</i>	<i>MMReg:0x2DDC</i>	2-280
<i>PP_CUBIC_OFFSET_T0_4</i>		<i>MMReg:0x1DE0</i>	<i>MMReg:0x2DE0</i>	2-280
<i>AIC_HI_ADDR</i>		<i>MMReg:0x1E0</i>		2-253
<i>PP_CUBIC_OFFSET_T1_0</i>		<i>MMReg:0x1E00</i>	<i>MMReg:0x2E00</i>	2-280
<i>PP_CUBIC_OFFSET_T1_1</i>		<i>MMReg:0x1E04</i>	<i>MMReg:0x2E04</i>	2-281
<i>PP_CUBIC_OFFSET_T1_2</i>		<i>MMReg:0x1E08</i>	<i>MMReg:0x2E08</i>	2-281
<i>PP_CUBIC_OFFSET_T1_3</i>		<i>MMReg:0x1E0C</i>	<i>MMReg:0x2E0C</i>	2-281
<i>PP_CUBIC_OFFSET_T1_4</i>		<i>MMReg:0x1E10</i>	<i>MMReg:0x2E10</i>	2-281
<i>PP_CUBIC_OFFSET_T2_0</i>		<i>MMReg:0x1E14</i>	<i>MMReg:0x2E14</i>	2-281
<i>PP_CUBIC_OFFSET_T2_1</i>		<i>MMReg:0x1E18</i>	<i>MMReg:0x2E18</i>	2-282
<i>PP_CUBIC_OFFSET_T2_2</i>		<i>MMReg:0x1E1C</i>	<i>MMReg:0x2E1C</i>	2-282
<i>PP_CUBIC_OFFSET_T2_3</i>		<i>MMReg:0x1E20</i>	<i>MMReg:0x2E20</i>	2-282
<i>PP_CUBIC_OFFSET_T2_4</i>		<i>MMReg:0x1E24</i>	<i>MMReg:0x2E24</i>	2-282
<i>AIC_TLB_ADDR</i>		<i>MMReg:0x1E4</i>		2-253
<i>AIC_TLB_DATA</i>		<i>MMReg:0x1E8</i>		2-253
<i>MEDIA_0_SCRATCH</i>		<i>MMReg:0x1F0</i>		2-290
<i>MEDIA_1_SCRATCH</i>		<i>MMReg:0x1F4</i>		2-291
<i>CRTC_H_TOTAL_DISP</i>		<i>MMReg:0x200</i>		2-47
<i>CRTC_H_SYNC_STRT_WID</i>		<i>MMReg:0x204</i>		2-47
<i>CRTC_V_TOTAL_DISP</i>		<i>MMReg:0x208</i>		2-47
<i>CRTC_V_SYNC_STRT_WID</i>		<i>MMReg:0x20C</i>		2-48
<i>CRTC_VLINE_CRNT_VLINE</i>		<i>MMReg:0x210</i>		2-48
<i>CRTC_CRNT_FRAME</i>		<i>MMReg:0x214</i>		2-48
<i>CRTC_GUI_TRIG_VLINE</i>		<i>MMReg:0x218</i>		2-48
<i>CRTC_DEBUG</i>		<i>MMReg:0x21C</i>		2-49
<i>CRTC_OFFSET_RIGHT</i>		<i>MMReg:0x220</i>		2-50
<i>CRTC_OFFSET</i>		<i>MMReg:0x224</i>		2-50
<i>CRTC_OFFSET_CNTL</i>		<i>MMReg:0x228</i>		2-51
<i>CRTC_PITCH</i>		<i>MMReg:0x22C</i>		2-53
<i>OVR_CLR</i>		<i>MMReg:0x230</i>		2-53
<i>OVR_WID_LEFT_RIGHT</i>		<i>MMReg:0x234</i>		2-53
<i>OVR_WID_TOP_BOTTOM</i>		<i>MMReg:0x238</i>		2-54
<i>DISPLAY_BASE_ADDR</i>		<i>MMReg:0x23C</i>		2-54
<i>SNAPSHOT_VH_COUNTS</i>		<i>MMReg:0x240</i>		2-54
<i>SNAPSHOT_F_COUNT</i>		<i>MMReg:0x244</i>		2-54
<i>N_VIF_COUNT</i>		<i>MMReg:0x248</i>		2-55
<i>SNAPSHOT_VIF_COUNT</i>		<i>MMReg:0x24C</i>		2-55
<i>FP_CRTC_H_TOTAL_DISP</i>		<i>MMReg:0x250</i>		2-55
<i>FP_CRTC_V_TOTAL_DISP</i>		<i>MMReg:0x254</i>		2-56
<i>CRT_CRTC_H_SYNC_STRT_WID</i>		<i>MMReg:0x258</i>		2-258
<i>CRT_CRTC_V_SYNC_STRT_WID</i>		<i>MMReg:0x25C</i>		2-259

Table 2-3 MMR Registers Sorted by Address (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>CUR_OFFSET</i>		<i>MMReg:0x260</i>		2-56
<i>CUR_HORZ_VERT_POSN</i>		<i>MMReg:0x264</i>		2-57
<i>CUR_HORZ_VERT_OFF</i>		<i>MMReg:0x268</i>		2-57
<i>CUR_CLR0</i>		<i>MMReg:0x26C</i>		2-58
<i>RE_TOP_LEFT</i>		<i>MMReg:0x26C0</i>		2-273
<i>RE_AUX_SCISSOR_CNTL</i>		<i>MMReg:0x26F0</i>		2-273
<i>CUR_CLR1</i>		<i>MMReg:0x270</i>		2-58
<i>RE_DDA_RHW_0</i>		<i>MMReg:0x2730</i>		2-274
<i>RE_DDA_RHW_1</i>		<i>MMReg:0x2734</i>		2-275
<i>RE_DDA_RHW_2</i>		<i>MMReg:0x2738</i>		2-275
<i>RE_DDA_RHW_3</i>		<i>MMReg:0x273C</i>		2-275
<i>FP_HORZ_VERT_ACTIVE</i>		<i>MMReg:0x278</i>		2-259
<i>CRTC_MORE_CNTL</i>		<i>MMReg:0x27C</i>		2-259
<i>DAC_EXT_CNTL</i>		<i>MMReg:0x280</i>		2-59
<i>FP_GEN_CNTL</i>		<i>MMReg:0x284</i>		2-59
<i>RE_DDA_S3_0</i>		<i>MMReg:0x2880</i>		2-275
<i>RE_DDA_S3_1</i>		<i>MMReg:0x2884</i>		2-275
<i>RE_DDA_S3_2</i>		<i>MMReg:0x2888</i>		2-276
<i>RE_DDA_S3_3</i>		<i>MMReg:0x288C</i>		2-276
<i>RE_DDA_T3_0</i>		<i>MMReg:0x2890</i>		2-276
<i>RE_DDA_T3_1</i>		<i>MMReg:0x2894</i>		2-276
<i>RE_DDA_T3_2</i>		<i>MMReg:0x2898</i>		2-277
<i>RE_DDA_T3_3</i>		<i>MMReg:0x289C</i>		2-277
<i>RE_DDA_Q3_0</i>		<i>MMReg:0x28B0</i>		2-277
<i>RE_DDA_Q3_1</i>		<i>MMReg:0x28B4</i>		2-277
<i>RE_DDA_Q3_2</i>		<i>MMReg:0x28B8</i>		2-277
<i>RE_DDA_Q3_3</i>		<i>MMReg:0x28BC</i>		2-278
<i>FP_HORZ_STRETCH</i>		<i>MMReg:0x28C</i>		2-260
<i>FP_VERT_STRETCH</i>		<i>MMReg:0x290</i>		2-64
<i>TMDS_CNTL</i>		<i>MMReg:0x294</i>		2-105
<i>RE_DDA_DS3_0</i>		<i>MMReg:0x2940</i>		2-278
<i>RE_DDA_DS3_1</i>		<i>MMReg:0x2944</i>		2-278
<i>RE_DDA_DS3_2</i>		<i>MMReg:0x2948</i>		2-278
<i>RE_DDA_DS3_3</i>		<i>MMReg:0x294C</i>		2-278
<i>RE_DDA_DT3_0</i>		<i>MMReg:0x2960</i>		2-279
<i>RE_DDA_DT3_1</i>		<i>MMReg:0x2964</i>		2-279
<i>RE_DDA_DT3_2</i>		<i>MMReg:0x2968</i>		2-279
<i>RE_DDA_DT3_3</i>		<i>MMReg:0x296C</i>		2-279
<i>TMDS_SYNC_CHAR_SETA</i>		<i>MMReg:0x298</i>		2-105
<i>TMDS_SYNC_CHAR_SETB</i>		<i>MMReg:0x29C</i>		2-106
<i>RE_NULL_PRIM</i>		<i>MMReg:0x29E0</i>		2-274
<i>RE_Z_MINMAX_0</i>		<i>MMReg:0x29F0</i>		2-274
<i>RE_Z_MINMAX_1</i>		<i>MMReg:0x29F4</i>		2-274
<i>RE_Z_MINMAX_3</i>		<i>MMReg:0x29FC</i>		2-274

Table 2-3 MMR Registers Sorted by Address (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>TMDS_CRC</i>		<i>MMReg:0x2A0</i>		2-106
<i>TMDS_TRANSMITTER_CNTL</i>		<i>MMReg:0x2A4</i>		2-106
<i>TMDS_PLL_CNTL</i>		<i>MMReg:0x2A8</i>		2-107
<i>TMDS_PATTERN_GEN_SEED</i>		<i>MMReg:0x2AC</i>		2-291
<i>FP_H_SYNC_STRT_WID</i>		<i>MMReg:0x2C4</i>		2-65
<i>FP_V_SYNC_STRT_WID</i>		<i>MMReg:0x2C8</i>		2-65
<i>PP_TRI_JUICE</i>		<i>MMReg:0x2D64</i>		2-284
<i>AUX_WINDOW_HORZ_CNTL</i>		<i>MMReg:0x2D8</i>		2-66
<i>AUX_WINDOW_VERT_CNTL</i>		<i>MMReg:0x2DC</i>		2-66
<i>PP_CUBIC_OFFSET_T3_0</i>		<i>MMReg:0x2E28</i>		2-282
<i>PP_CUBIC_OFFSET_T3_1</i>		<i>MMReg:0x2E2C</i>		2-283
<i>PP_CUBIC_OFFSET_T3_2</i>		<i>MMReg:0x2E30</i>		2-283
<i>PP_CUBIC_OFFSET_T3_3</i>		<i>MMReg:0x2E34</i>		2-283
<i>PP_CUBIC_OFFSET_T3_4</i>		<i>MMReg:0x2E38</i>		2-283
<i>GRPH_BUFFER_CNTL</i>		<i>MMReg:0x2F0</i>		2-67
<i>VGA_BUFFER_CNTL</i>		<i>MMReg:0x2F4</i>		2-261
<i>RB2D_ROP</i>		<i>MMReg:0x3400</i>		2-190
<i>RB2D_CLRCMP_SRC</i>		<i>MMReg:0x3408</i>		2-190
<i>RB2D_CLRCMP_DST</i>		<i>MMReg:0x340C</i>		2-190
<i>RB2D_CLRCMP_FLIPE</i>		<i>MMReg:0x3410</i>		2-190
<i>RB2D_CLRCMP_CNTL</i>		<i>MMReg:0x3414</i>		2-191
<i>RB2D_CLRCMP_MSK</i>		<i>MMReg:0x3418</i>		2-191
<i>RB2D_WRITEMASK</i>		<i>MMReg:0x341C</i>		2-192
<i>RB2D_DATATYPE</i>		<i>MMReg:0x3420</i>		2-192
<i>RB2D_GUI_MASTER_CNTL</i>		<i>MMReg:0x3424</i>		2-192
<i>RB2D_DSTCACHE_MODE</i>		<i>MMReg:0x3428</i>		2-284
<i>RB2D_DSTCACHE_CTLSTAT</i>		<i>MMReg:0x342C</i>		2-285
<i>RB2D_SRC_ENDIAN</i>		<i>MMReg:0x3430</i>		2-286
<i>RB2D_DST_ENDIAN</i>		<i>MMReg:0x3434</i>		2-286
<i>RB2D_PD1_DATA</i>		<i>MMReg:0x3438</i>		2-286
<i>RB2D_PD1_ADDR</i>		<i>MMReg:0x343C</i>		2-286
<i>RB2D_WRITEBACK_DATA_LO</i>		<i>MMReg:0x3450</i>		2-287
<i>RB2D_WRITEBACK_DATA_HI</i>		<i>MMReg:0x3454</i>		2-287
<i>RB2D_WRITEBACK_ADDR</i>		<i>MMReg:0x3458</i>		2-287
<i>OV0_Y_X_START</i>		<i>MMReg:0x400</i>		2-68
<i>OV0_Y_X_END</i>		<i>MMReg:0x404</i>		2-68
<i>OV0_PIPELINE_CNTL</i>		<i>MMReg:0x408</i>		2-262
<i>OV0_REG_LOAD_CNTL</i>		<i>MMReg:0x410</i>		2-69
<i>OV0_SCALE_CNTL</i>		<i>MMReg:0x420</i>		2-70
<i>OV0_V_INC</i>		<i>MMReg:0x424</i>		2-72
<i>OV0_P1_V_ACCUM_INIT</i>		<i>MMReg:0x428</i>		2-72
<i>OV0_P23_V_ACCUM_INIT</i>		<i>MMReg:0x42C</i>		2-73
<i>OV0_P1_BLANK_LINES_AT_TO P</i>		<i>MMReg:0x430</i>		2-73

Table 2-3 MMR Registers Sorted by Address (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>OV0_P23_BLANK_LINES_AT_TO P</i>		<i>MMReg:0x434</i>		<i>2-73</i>
<i>OV0_BASE_ADDR</i>		<i>MMReg:0x43C</i>		<i>2-74</i>
<i>OV0_VID_BUF0_BASE_ADRS</i>		<i>MMReg:0x440</i>		<i>2-74</i>
<i>OV0_VID_BUF1_BASE_ADRS</i>		<i>MMReg:0x444</i>		<i>2-75</i>
<i>OV0_VID_BUF2_BASE_ADRS</i>		<i>MMReg:0x448</i>		<i>2-75</i>
<i>OV0_VID_BUF3_BASE_ADRS</i>		<i>MMReg:0x44C</i>		<i>2-75</i>
<i>OV0_VID_BUF4_BASE_ADRS</i>		<i>MMReg:0x450</i>		<i>2-76</i>
<i>OV0_VID_BUF5_BASE_ADRS</i>		<i>MMReg:0x454</i>		<i>2-76</i>
<i>OV0_VID_BUF_PITCH0_VALUE</i>		<i>MMReg:0x460</i>		<i>2-76</i>
<i>OV0_VID_BUF_PITCH1_VALUE</i>		<i>MMReg:0x464</i>		<i>2-77</i>
<i>OV0_AUTO_FLIP_CNTRL</i>		<i>MMReg:0x470</i>		<i>2-77</i>
<i>OV0_DEINTERLACE_PATTERN</i>		<i>MMReg:0x474</i>		<i>2-79</i>
<i>OV0_SUBMIT_HISTORY</i>		<i>MMReg:0x478</i>		<i>2-262</i>
<i>OV0_H_INC</i>		<i>MMReg:0x480</i>		<i>2-80</i>
<i>OV0_STEP_BY</i>		<i>MMReg:0x484</i>		<i>2-80</i>
<i>OV0_P1_H_ACCUM_INIT</i>		<i>MMReg:0x488</i>		<i>2-81</i>
<i>OV0_P23_H_ACCUM_INIT</i>		<i>MMReg:0x48C</i>		<i>2-81</i>
<i>OV0_P1_X_START_END</i>		<i>MMReg:0x494</i>		<i>2-82</i>
<i>OV0_P2_X_START_END</i>		<i>MMReg:0x498</i>		<i>2-82</i>
<i>OV0_P3_X_START_END</i>		<i>MMReg:0x49C</i>		<i>2-82</i>
<i>OV0_FILTER_CNTRL</i>		<i>MMReg:0x4A0</i>		<i>2-83</i>
<i>OV0_FOUR_TAP_COEF_0</i>		<i>MMReg:0x4B0</i>		<i>2-83</i>
<i>OV0_FOUR_TAP_COEF_1</i>		<i>MMReg:0x4B4</i>		<i>2-84</i>
<i>OV0_FOUR_TAP_COEF_2</i>		<i>MMReg:0x4B8</i>		<i>2-84</i>
<i>OV0_FOUR_TAP_COEF_3</i>		<i>MMReg:0x4BC</i>		<i>2-84</i>
<i>OV0_FOUR_TAP_COEF_4</i>		<i>MMReg:0x4C0</i>		<i>2-85</i>
<i>OV0_FLAG_CNTRL</i>		<i>MMReg:0x4DC</i>		<i>2-85</i>
<i>OV0_SLICE_CNTRL</i>		<i>MMReg:0x4E0</i>		<i>2-262</i>
<i>OV0_VID_KEY_CLR_LOW</i>		<i>MMReg:0x4E4</i>		<i>2-85</i>
<i>OV0_VID_KEY_CLR_HIGH</i>		<i>MMReg:0x4E8</i>		<i>2-263</i>
<i>OV0_GRP_KEY_CLR_LOW</i>		<i>MMReg:0x4EC</i>		<i>2-86</i>
<i>OV0_GRP_KEY_CLR_HIGH</i>		<i>MMReg:0x4F0</i>		<i>2-86</i>
<i>OV0_KEY_CNTRL</i>		<i>MMReg:0x4F4</i>		<i>2-86</i>
<i>OV0_TEST</i>		<i>MMReg:0x4F8</i>		<i>2-87</i>
<i>CP_RB_BASE</i>		<i>MMReg:0x700</i>		<i>2-142</i>
<i>CP_RB_CNTRL</i>		<i>MMReg:0x704</i>		<i>2-141</i>
<i>CP_RB_RPTR_ADDR</i>		<i>MMReg:0x70C</i>		<i>2-142</i>
<i>CP_RB_RPTR</i>		<i>MMReg:0x710</i>		<i>2-142</i>
<i>CP_RB_WPTR</i>		<i>MMReg:0x714</i>		<i>2-142</i>
<i>CP_RB_WPTR_DELAY</i>		<i>MMReg:0x718</i>		<i>2-143</i>
<i>CP_IB_BASE</i>		<i>MMReg:0x738</i>		<i>2-143</i>
<i>CP_IB_BUFSZ</i>		<i>MMReg:0x73C</i>		<i>2-143</i>
<i>CP_CSQ_CNTRL</i>		<i>MMReg:0x740</i>		<i>2-143</i>
<i>SCRATCH_UMSK</i>		<i>MMReg:0x770</i>		<i>2-146</i>

Table 2-3 MMR Registers Sorted by Address (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>SCRATCH_ADDR</i>		<i>MMReg:0x774</i>		2-146
<i>DMA_GUI_TABLE_ADDR</i>		<i>MMReg:0x780</i>		2-146
<i>DMA_GUI_SRC_ADDR</i>		<i>MMReg:0x784</i>		2-147
<i>DMA_GUI_DST_ADDR</i>		<i>MMReg:0x788</i>		2-147
<i>DMA_GUI_COMMAND</i>		<i>MMReg:0x78C</i>		2-147
<i>DMA_GUI_STATUS</i>		<i>MMReg:0x790</i>		2-148
<i>DMA_GUI_ACT_DSCRPTR</i>		<i>MMReg:0x794</i>		2-149
<i>DMA_VID_TABLE_ADDR</i>		<i>MMReg:0x7A0</i>		2-149
<i>DMA_VID_SRC_ADDR</i>		<i>MMReg:0x7A4</i>		2-149
<i>DMA_VID_DST_ADDR</i>		<i>MMReg:0x7A8</i>		2-150
<i>DMA_VID_COMMAND</i>		<i>MMReg:0x7AC</i>		2-150
<i>DMA_VID_STATUS</i>		<i>MMReg:0x7B0</i>		2-151
<i>DMA_VID_ACT_DSCRPTR</i>		<i>MMReg:0x7B4</i>		2-151
<i>CP_STAT</i>		<i>MMReg:0x7C0</i>		2-272
<i>CP_ME_CNTL</i>		<i>MMReg:0x7D0</i>		2-152
<i>CP_ME_RAM_ADDR</i>		<i>MMReg:0x7D4</i>		2-153
<i>CP_ME_RAM_RADDR</i>		<i>MMReg:0x7D8</i>		2-153
<i>CP_ME_RAM_DATAH</i>		<i>MMReg:0x7DC</i>		2-153
<i>CP_ME_RAM_DATAH</i>		<i>MMReg:0x7E0</i>		2-154
<i>CP_CSQ_ADDR</i>		<i>MMReg:0x7F0</i>		2-152
<i>CP_CSQ_DATA</i>		<i>MMReg:0x7F4</i>		2-152
<i>CP_CSQ_STAT</i>		<i>MMReg:0x7F8</i>		2-152
<i>VID_BUFFER_CONTROL</i>		<i>MMReg:0x900</i>		2-128
<i>CAP_INT_CNTL</i>		<i>MMReg:0x908</i>		2-129
<i>CAP_INT_STATUS</i>		<i>MMReg:0x90C</i>		2-130
<i>FCP_CNTL</i>		<i>MMReg:0x910</i>		2-117
<i>FCP_CNTL</i>		<i>MMReg:0x910</i>		2-118
<i>CAPO_BUF0_OFFSET</i>		<i>MMReg:0x920</i>		2-120
<i>CAPO_BUF1_OFFSET</i>		<i>MMReg:0x924</i>		2-121
<i>CAPO_BUF0_EVEN_OFFSET</i>		<i>MMReg:0x928</i>		2-121
<i>CAPO_BUF1_EVEN_OFFSET</i>		<i>MMReg:0x92C</i>		2-121
<i>CAPO_BUF_PITCH</i>		<i>MMReg:0x930</i>		2-121
<i>CAPO_V_WINDOW</i>		<i>MMReg:0x934</i>		2-121
<i>CAPO_H_WINDOW</i>		<i>MMReg:0x938</i>		2-122
<i>CAPO_VBI0_OFFSET</i>		<i>MMReg:0x93C</i>		2-122
<i>CAPO_VBI1_OFFSET</i>		<i>MMReg:0x940</i>		2-122
<i>CAPO_VBI_V_WINDOW</i>		<i>MMReg:0x944</i>		2-122
<i>CAPO_VBI_H_WINDOW</i>		<i>MMReg:0x948</i>		2-123
<i>CAPO_PORT_MODE_CNTL</i>		<i>MMReg:0x94C</i>		2-123
<i>CAPO_TRIG_CNTL</i>		<i>MMReg:0x950</i>		2-123
<i>CAPO_DEBUG</i>		<i>MMReg:0x954</i>		2-124
<i>CAPO_CONFIG</i>		<i>MMReg:0x958</i>		2-124
<i>CAPO_ANC0_OFFSET</i>		<i>MMReg:0x95C</i>		2-126
<i>CAPO_ANC1_OFFSET</i>		<i>MMReg:0x960</i>		2-126
<i>CAPO_ANC_H_WINDOW</i>		<i>MMReg:0x964</i>		2-126

Table 2-3 MMR Registers Sorted by Address (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>CAPO_VIDEO_SYNC_TEST</i>		<i>MMReg:0x968</i>		2-126
<i>CAPO_ONESHOT_BUF_OFFSET</i>		<i>MMReg:0x96C</i>		2-127
<i>CAPO_BUF_STATUS</i>		<i>MMReg:0x970</i>		2-127
<i>CAPO_ANC_BUF01_BLOCK_CN T</i>		<i>MMReg:0x974</i>		2-291
<i>CAPO_ANC_BUF23_BLOCK_CN T</i>		<i>MMReg:0x97C</i>		2-291
<i>CAPO_VBI2_OFFSET</i>		<i>MMReg:0x980</i>		2-128
<i>CAPO_VBI3_OFFSET</i>		<i>MMReg:0x984</i>		2-128
<i>CAPO_ANC2_OFFSET</i>		<i>MMReg:0x988</i>		2-128
<i>CAPO_ANC3_OFFSET</i>		<i>MMReg:0x98C</i>		2-128
<i>DMA_VIPH0_COMMAND</i>		<i>MMReg:0xA00</i>		2-133
<i>DMA_VIPH1_COMMAND</i>		<i>MMReg:0xA04</i>		2-133
<i>DMA_VIPH2_COMMAND</i>		<i>MMReg:0xA08</i>		2-134
<i>DMA_VIPH3_COMMAND</i>		<i>MMReg:0xA0C</i>		2-135
<i>DMA_VIPH_STATUS</i>		<i>MMReg:0xA10</i>		2-136
<i>DMA_VIPH_CHUNK_0</i>		<i>MMReg:0xA18</i>		2-136
<i>DMA_VIPH_CHUNK_1_VAL</i>		<i>MMReg:0xA1C</i>		2-137
<i>DMA_VIP0_TABLE_ADDR</i>		<i>MMReg:0xA20</i>		2-137
<i>DMA_VIPH0_ACTIVE</i>		<i>MMReg:0xA24</i>		2-138
<i>DMA_VIP1_TABLE_ADDR</i>		<i>MMReg:0xA30</i>		2-138
<i>DMA_VIPH1_ACTIVE</i>		<i>MMReg:0xA34</i>		2-138
<i>DMA_VIP2_TABLE_ADDR</i>		<i>MMReg:0xA40</i>		2-138
<i>DMA_VIPH2_ACTIVE</i>		<i>MMReg:0xA44</i>		2-139
<i>DMA_VIP3_TABLE_ADDR</i>		<i>MMReg:0xA50</i>		2-138
<i>DMA_VIPH3_ACTIVE</i>		<i>MMReg:0xA54</i>		2-139
<i>DMA_VIPH_ABORT</i>		<i>MMReg:0xA88</i>		2-139
<i>SURFACE_CNTL</i>		<i>MMReg:0xB00</i>		2-22
<i>SURFACE0_LOWER_BOUND</i>		<i>MMReg:0xB04</i>		2-23
<i>SURFACE0_UPPER_BOUND</i>		<i>MMReg:0xB08</i>		2-23
<i>SURFACE0_INFO</i>		<i>MMReg:0xB0C</i>		2-22
<i>SURFACE1_LOWER_BOUND</i>		<i>MMReg:0xB14</i>		2-24
<i>SURFACE1_UPPER_BOUND</i>		<i>MMReg:0xB18</i>		2-25
<i>SURFACE1_INFO</i>		<i>MMReg:0xB1C</i>		2-24
<i>SURFACE2_LOWER_BOUND</i>		<i>MMReg:0xB24</i>		2-26
<i>SURFACE2_UPPER_BOUND</i>		<i>MMReg:0xB28</i>		2-26
<i>SURFACE2_INFO</i>		<i>MMReg:0xB2C</i>		2-25
<i>SURFACE3_LOWER_BOUND</i>		<i>MMReg:0xB34</i>		2-27
<i>SURFACE3_UPPER_BOUND</i>		<i>MMReg:0xB38</i>		2-27
<i>SURFACE3_INFO</i>		<i>MMReg:0xB3C</i>		2-26
<i>SURFACE4_LOWER_BOUND</i>		<i>MMReg:0xB44</i>		2-28
<i>SURFACE4_UPPER_BOUND</i>		<i>MMReg:0xB48</i>		2-28
<i>SURFACE4_INFO</i>		<i>MMReg:0xB4C</i>		2-27
<i>SURFACE5_LOWER_BOUND</i>		<i>MMReg:0xB54</i>		2-29
<i>SURFACE5_UPPER_BOUND</i>		<i>MMReg:0xB58</i>		2-30

Table 2-3 MMR Registers Sorted by Address (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>SURFACE5_INFO</i>		<i>MMReg:0xB5C</i>		2-29
<i>SURFACE6_LOWER_BOUND</i>		<i>MMReg:0xB64</i>		2-31
<i>SURFACE6_UPPER_BOUND</i>		<i>MMReg:0xB68</i>		2-31
<i>SURFACE6_INFO</i>		<i>MMReg:0xB6C</i>		2-30
<i>SURFACE7_LOWER_BOUND</i>		<i>MMReg:0xB74</i>		2-32
<i>SURFACE7_UPPER_BOUND</i>		<i>MMReg:0xB78</i>		2-32
<i>SURFACE7_INFO</i>		<i>MMReg:0xB7C</i>		2-31
<i>SURFACE_ACCESS_FLAGS</i>		<i>MMReg:0xBF8</i>		2-254
<i>SURFACE_ACCESS_CLR</i>		<i>MMReg:0xBFC</i>		2-255
<i>VIPH_CH0_DATA</i>		<i>MMReg:0xC00</i>		2-110
<i>VIPH_CH1_DATA</i>		<i>MMReg:0xC04</i>		2-110
<i>VIPH_CH2_DATA</i>		<i>MMReg:0xC08</i>		2-110
<i>VIPH_CH3_DATA</i>		<i>MMReg:0xC0C</i>		2-110
<i>VIPH_CH0_ADDR</i>		<i>MMReg:0xC10</i>		2-110
<i>VIPH_CH1_ADDR</i>		<i>MMReg:0xC14</i>		2-111
<i>VIPH_CH2_ADDR</i>		<i>MMReg:0xC18</i>		2-111
<i>VIPH_CH3_ADDR</i>		<i>MMReg:0xC1C</i>		2-111
<i>VIPH_CH0_SBCNT</i>		<i>MMReg:0xC20</i>		2-111
<i>VIPH_CH1_SBCNT</i>		<i>MMReg:0xC24</i>		2-112
<i>VIPH_CH2_SBCNT</i>		<i>MMReg:0xC28</i>		2-112
<i>VIPH_CH3_SBCNT</i>		<i>MMReg:0xC2C</i>		2-112
<i>VIPH_CH0_ABCNT</i>		<i>MMReg:0xC30</i>		2-112
<i>VIPH_CH1_ABCNT</i>		<i>MMReg:0xC34</i>		2-112
<i>VIPH_CH2_ABCNT</i>		<i>MMReg:0xC38</i>		2-113
<i>VIPH_CH3_ABCNT</i>		<i>MMReg:0xC3C</i>		2-113
<i>VIPH_CONTROL</i>		<i>MMReg:0xC40</i>		2-113
<i>VIPH_DV_LAT</i>		<i>MMReg:0xC44</i>		2-114
<i>VIPH_DMA_CHUNK</i>		<i>MMReg:0xC48</i>		2-114
<i>VIPH_DV_INT</i>		<i>MMReg:0xC4C</i>		2-115
<i>VIPH_TIMEOUT_STAT</i>		<i>MMReg:0xC50</i>		2-115
<i>DISP_MISC_CNTL</i>		<i>MMReg:0xD00</i>		2-88
<i>DAC_MACRO_CNTL</i>		<i>MMReg:0xD04</i>		2-88
<i>DISP_PWR_MAN</i>		<i>MMReg:0xD08</i>		2-263
<i>DISP_TEST_DEBUG_CNTL</i>		<i>MMReg:0xD10</i>		2-89
<i>DISP_HW_DEBUG</i>		<i>MMReg:0xD14</i>		2-90
<i>DAC_CRC_SIG1</i>		<i>MMReg:0xD18</i>		2-91
<i>DAC_CRC_SIG2</i>		<i>MMReg:0xD1C</i>		2-91
<i>OV0_LIN_TRANS_A</i>		<i>MMReg:0xD20</i>		2-92
<i>OV0_LIN_TRANS_B</i>		<i>MMReg:0xD24</i>		2-92
<i>OV0_LIN_TRANS_C</i>		<i>MMReg:0xD28</i>		2-92
<i>OV0_LIN_TRANS_D</i>		<i>MMReg:0xD2C</i>		2-93
<i>OV0_LIN_TRANS_E</i>		<i>MMReg:0xD30</i>		2-93
<i>OV0_LIN_TRANS_F</i>		<i>MMReg:0xD34</i>		2-93
<i>OV0_GAMMA_0_F</i>		<i>MMReg:0xD40</i>		2-93
<i>OV0_GAMMA_10_1F</i>		<i>MMReg:0xD44</i>		2-94

Table 2-3 MMR Registers Sorted by Address (Continued)

Name	I/OAddress	MM Address	Second Address	Page
<i>OV0_GAMMA_20_3F</i>		<i>MMReg:0xD48</i>		<i>2-94</i>
<i>OV0_GAMMA_40_7F</i>		<i>MMReg:0xD4C</i>		<i>2-94</i>
<i>OV0_GAMMA_380_3BF</i>		<i>MMReg:0xD50</i>		<i>2-95</i>
<i>OV0_GAMMA_3C0_3FF</i>		<i>MMReg:0xD54</i>		<i>2-95</i>
<i>DISP_MERGE_CNTL</i>		<i>MMReg:0xD60</i>		<i>2-95</i>
<i>DISP_OUTPUT_CNTL</i>		<i>MMReg:0xD64</i>		<i>2-97</i>
<i>DISP_LIN_TRANS_GRP_H_A</i>		<i>MMReg:0xD80</i>		<i>2-100</i>
<i>DISP_LIN_TRANS_GRP_H_B</i>		<i>MMReg:0xD84</i>		<i>2-100</i>
<i>DISP_LIN_TRANS_GRP_H_C</i>		<i>MMReg:0xD88</i>		<i>2-100</i>
<i>DISP_LIN_TRANS_GRP_H_D</i>		<i>MMReg:0xD8C</i>		<i>2-100</i>
<i>DISP_LIN_TRANS_GRP_H_E</i>		<i>MMReg:0xD90</i>		<i>2-101</i>
<i>DISP_LIN_TRANS_GRP_H_F</i>		<i>MMReg:0xD94</i>		<i>2-101</i>
<i>DISP_LIN_TRANS_VID_A</i>		<i>MMReg:0xD98</i>		<i>2-101</i>
<i>DISP_LIN_TRANS_VID_B</i>		<i>MMReg:0xD9C</i>		<i>2-101</i>
<i>DISP_LIN_TRANS_VID_C</i>		<i>MMReg:0xDA0</i>		<i>2-102</i>
<i>DISP_LIN_TRANS_VID_D</i>		<i>MMReg:0xDA4</i>		<i>2-102</i>
<i>DISP_LIN_TRANS_VID_E</i>		<i>MMReg:0xDA8</i>		<i>2-102</i>
<i>DISP_LIN_TRANS_VID_F</i>		<i>MMReg:0xDAC</i>		<i>2-102</i>
<i>RMX_HORZ_FILTER_0TAP_COEF</i>		<i>MMReg:0xDB0</i>		<i>2-103</i>
<i>RMX_HORZ_FILTER_1TAP_COEF</i>		<i>MMReg:0xDB4</i>		<i>2-103</i>
<i>RMX_HORZ_FILTER_2TAP_COEF</i>		<i>MMReg:0xDB8</i>		<i>2-103</i>
<i>RMX_HORZ_PHASE</i>		<i>MMReg:0xDBC</i>		<i>2-104</i>
<i>DAC_EMBEDDED_SYNC_CNTL</i>		<i>MMReg:0xDC0</i>		<i>2-264</i>
<i>DAC_BROAD_PULSE</i>		<i>MMReg:0xDC4</i>		<i>2-264</i>
<i>DAC_SKEW_CLKS</i>		<i>MMReg:0xDC8</i>		<i>2-264</i>
<i>DAC_INCR</i>		<i>MMReg:0xDCC</i>		<i>2-265</i>
<i>DAC_NEG_SYNC_LEVEL</i>		<i>MMReg:0xDD0</i>		<i>2-265</i>
<i>DAC_POS_SYNC_LEVEL</i>		<i>MMReg:0xDD4</i>		<i>2-265</i>
<i>DAC_BLANK_LEVEL</i>		<i>MMReg:0xDD8</i>		<i>2-265</i>
<i>RBBM_STATUS</i>		<i>MMReg:0xE40</i>	<i>MMReg:0x1740</i>	<i>2-7</i>
<i>NQWAIT_UNTIL</i>		<i>MMReg:0xE50</i>		<i>2-10</i>
<i>RBBM_CMDFIFO_ADDR</i>		<i>MMReg:0xE70</i>		<i>2-11</i>
<i>RBBM_CMDFIFO_DATA_L</i>		<i>MMReg:0xE74</i>		<i>2-12</i>
<i>RBBM_CMDFIFO_DATA_H</i>		<i>MMReg:0xE78</i>		<i>2-12</i>
<i>RBBM_CMDFIFO_STAT</i>		<i>MMReg:0xE7C</i>		<i>2-12</i>

## A.4 ATTR Registers Sorted by Name

Table A-1 ATTR Registers Sorted by Name

Name	Address	Page
<i>ATTR00</i>	<i>VGAATTRIND:0x0</i>	<i>2-226</i>
<i>ATTR01</i>	<i>VGAATTRIND:0x1</i>	<i>2-226</i>
<i>ATTR02</i>	<i>VGAATTRIND:0x2</i>	<i>2-226</i>
<i>ATTR03</i>	<i>VGAATTRIND:0x3</i>	<i>2-226</i>
<i>ATTR04</i>	<i>VGAATTRIND:0x4</i>	<i>2-227</i>
<i>ATTR05</i>	<i>VGAATTRIND:0x5</i>	<i>2-227</i>
<i>ATTR06</i>	<i>VGAATTRIND:0x6</i>	<i>2-227</i>
<i>ATTR07</i>	<i>VGAATTRIND:0x7</i>	<i>2-227</i>
<i>ATTR08</i>	<i>VGAATTRIND:0x8</i>	<i>2-228</i>
<i>ATTR09</i>	<i>VGAATTRIND:0x9</i>	<i>2-228</i>
<i>ATTR0A</i>	<i>VGAATTRIND:0xA</i>	<i>2-228</i>
<i>ATTR0B</i>	<i>VGAATTRIND:0xB</i>	<i>2-228</i>
<i>ATTR0C</i>	<i>VGAATTRIND:0xC</i>	<i>2-229</i>
<i>ATTR0D</i>	<i>VGAATTRIND:0xD</i>	<i>2-229</i>
<i>ATTR0E</i>	<i>VGAATTRIND:0xE</i>	<i>2-229</i>
<i>ATTR0F</i>	<i>VGAATTRIND:0xF</i>	<i>2-229</i>
<i>ATTR10</i>	<i>VGAATTRIND:0x10</i>	<i>2-230</i>
<i>ATTR11</i>	<i>VGAATTRIND:0x11</i>	<i>2-230</i>
<i>ATTR12</i>	<i>VGAATTRIND:0x12</i>	<i>2-231</i>
<i>ATTR13</i>	<i>VGAATTRIND:0x13</i>	<i>2-231</i>
<i>ATTR14</i>	<i>VGAATTRIND:0x14</i>	<i>2-232</i>

## A.5 CRT Register Address Sorted by Name

Table A-2 CRT Register Address Sorted by Name

Name	Address	Page
<i>CRT00</i>	<i>VGACRTIND:0x0</i>	<i>2-202</i>
<i>CRT01</i>	<i>VGACRTIND:0x1</i>	<i>2-203</i>
<i>CRT02</i>	<i>VGACRTIND:0x2</i>	<i>2-203</i>
<i>CRT03</i>	<i>VGACRTIND:0x3</i>	<i>2-203</i>
<i>CRT04</i>	<i>VGACRTIND:0x4</i>	<i>2-204</i>
<i>CRT05</i>	<i>VGACRTIND:0x5</i>	<i>2-204</i>
<i>CRT06</i>	<i>VGACRTIND:0x6</i>	<i>2-204</i>
<i>CRT07</i>	<i>VGACRTIND:0x7</i>	<i>2-205</i>
<i>CRT08</i>	<i>VGACRTIND:0x8</i>	<i>2-206</i>
<i>CRT09</i>	<i>VGACRTIND:0x9</i>	<i>2-206</i>
<i>CRT0A</i>	<i>VGACRTIND:0xA</i>	<i>2-207</i>
<i>CRT0B</i>	<i>VGACRTIND:0xB</i>	<i>2-207</i>
<i>CRT0C</i>	<i>VGACRTIND:0xC</i>	<i>2-208</i>
<i>CRT0D</i>	<i>VGACRTIND:0xD</i>	<i>2-208</i>
<i>CRT0E</i>	<i>VGACRTIND:0xE</i>	<i>2-208</i>
<i>CRT0F</i>	<i>VGACRTIND:0xF</i>	<i>2-208</i>
<i>CRT10</i>	<i>VGACRTIND:0x10</i>	<i>2-209</i>
<i>CRT11</i>	<i>VGACRTIND:0x11</i>	<i>2-209</i>
<i>CRT12</i>	<i>VGACRTIND:0x12</i>	<i>2-209</i>
<i>CRT13</i>	<i>VGACRTIND:0x13</i>	<i>2-210</i>
<i>CRT14</i>	<i>VGACRTIND:0x14</i>	<i>2-210</i>
<i>CRT15</i>	<i>VGACRTIND:0x15</i>	<i>2-210</i>
<i>CRT16</i>	<i>VGACRTIND:0x16</i>	<i>2-211</i>
<i>CRT17</i>	<i>VGACRTIND:0x17</i>	<i>2-211</i>
<i>CRT18</i>	<i>VGACRTIND:0x18</i>	<i>2-212</i>
<i>CRT1E</i>	<i>VGACRTIND:0x1E</i>	<i>2-212</i>
<i>CRT1F</i>	<i>VGACRTIND:0x1F</i>	<i>2-212</i>
<i>CRT22</i>	<i>VGACRTIND:0x22</i>	<i>2-212</i>
<i>CRT00_S</i>	<i>VGACRTIND:0x40</i>	<i>2-213</i>
<i>CRT01_S</i>	<i>VGACRTIND:0x41</i>	<i>2-213</i>
<i>CRT02_S</i>	<i>VGACRTIND:0x42</i>	<i>2-213</i>
<i>CRT03_S</i>	<i>VGACRTIND:0x43</i>	<i>2-213</i>
<i>CRT04_S</i>	<i>VGACRTIND:0x44</i>	<i>2-214</i>
<i>CRT05_S</i>	<i>VGACRTIND:0x45</i>	<i>2-214</i>
<i>CRT06_S</i>	<i>VGACRTIND:0x46</i>	<i>2-214</i>
<i>CRT07_S</i>	<i>VGACRTIND:0x47</i>	<i>2-215</i>
<i>CRT08_S</i>	<i>VGACRTIND:0x48</i>	<i>2-216</i>
<i>CRT09_S</i>	<i>VGACRTIND:0x49</i>	<i>2-216</i>
<i>CRT0A_S</i>	<i>VGACRTIND:0x4A</i>	<i>2-216</i>
<i>CRT0B_S</i>	<i>VGACRTIND:0x4B</i>	<i>2-217</i>
<i>CRT0C_S</i>	<i>VGACRTIND:0x4C</i>	<i>2-217</i>

**Table A-2 CRT Register Address Sorted by Name (Continued)**

Name	Address	Page
<i>CRT0D_S</i>	<i>VGACRTIND:0x4D</i>	<i>2-217</i>
<i>CRT0E_S</i>	<i>VGACRTIND:0x4E</i>	<i>2-217</i>
<i>CRT0F_S</i>	<i>VGACRTIND:0x4F</i>	<i>2-218</i>
<i>CRT10_S</i>	<i>VGACRTIND:0x50</i>	<i>2-218</i>
<i>CRT11_S</i>	<i>VGACRTIND:0x51</i>	<i>2-218</i>
<i>CRT12_S</i>	<i>VGACRTIND:0x52</i>	<i>2-219</i>
<i>CRT13_S</i>	<i>VGACRTIND:0x53</i>	<i>2-219</i>
<i>CRT14_S</i>	<i>VGACRTIND:0x54</i>	<i>2-219</i>
<i>CRT15_S</i>	<i>VGACRTIND:0x55</i>	<i>2-220</i>
<i>CRT16_S</i>	<i>VGACRTIND:0x56</i>	<i>2-220</i>
<i>CRT17_S</i>	<i>VGACRTIND:0x57</i>	<i>2-220</i>
<i>CRT18_S</i>	<i>VGACRTIND:0x58</i>	<i>2-221</i>
<i>CRT1E_S</i>	<i>VGACRTIND:0x5E</i>	<i>2-221</i>
<i>CRT1F_S</i>	<i>VGACRTIND:0x5F</i>	<i>2-221</i>
<i>CRT22_S</i>	<i>VGACRTIND:0x62</i>	<i>2-222</i>

## A.6 GRPH Registers Sorted by Name

Table A-3 GRPH Registers Sorted by Name

Name	Address	Page
<i>GRA00</i>	<i>VGAGRPHIND:0x0</i>	<i>2-233</i>
<i>GRA01</i>	<i>VGAGRPHIND:0x1</i>	<i>2-233</i>
<i>GRA02</i>	<i>VGAGRPHIND:0x2</i>	<i>2-234</i>
<i>GRA03</i>	<i>VGAGRPHIND:0x3</i>	<i>2-234</i>
<i>GRA04</i>	<i>VGAGRPHIND:0x4</i>	<i>2-235</i>
<i>GRA05</i>	<i>VGAGRPHIND:0x5</i>	<i>2-235</i>
<i>GRA06</i>	<i>VGAGRPHIND:0x6</i>	<i>2-236</i>
<i>GRA07</i>	<i>VGAGRPHIND:0x7</i>	<i>2-236</i>
<i>GRA08</i>	<i>VGAGRPHIND:0x8</i>	<i>2-236</i>

## A.7 SEQ Registers Sorted by Name

Table A-4 SEQ Registers Sorted by Name

Name	Address	Page
<i>SEQ00</i>	<i>VGASEQIND:0x0</i>	<i>2-223</i>
<i>SEQ01</i>	<i>VGASEQIND:0x1</i>	<i>2-224</i>
<i>SEQ02</i>	<i>VGASEQIND:0x2</i>	<i>2-224</i>
<i>SEQ03</i>	<i>VGASEQIND:0x3</i>	<i>2-225</i>
<i>SEQ04</i>	<i>VGASEQIND:0x4</i>	<i>2-225</i>

## A.8 VGA I/O Registers Sorted by Name

Table A-5 VGA I/O Registers Sorted by Name

Name	Address	Secondary Address	Page
<i>ATTRDR</i>	<i>VGA_IO:0x3C1</i>		<i>2-40</i>
<i>ATTRDW</i>	<i>VGA_IO:0x3C0</i>		<i>2-40</i>
<i>ATTRX</i>	<i>VGA_IO:0x3C0</i>		<i>2-40</i>
<i>CRTC8_DATA</i>	<i>VGA_IO:0x3B5</i>	<i>VGA_IO:0x3D5</i>	<i>2-202</i>
<i>CRTC8_IDX</i>	<i>VGA_IO:0x3B4</i>	<i>VGA_IO:0x3D4</i>	<i>2-202</i>
<i>DAC_DATA</i>	<i>VGA_IO:0x3C9</i>		<i>2-39</i>
<i>DAC_MASK</i>	<i>VGA_IO:0x3C6</i>		<i>2-39</i>
<i>DAC_R_INDEX</i>	<i>VGA_IO:0x3C7</i>		<i>2-39</i>
<i>DAC_W_INDEX</i>	<i>VGA_IO:0x3C8</i>		<i>2-39</i>
<i>GENENB</i>	<i>VGA_IO:0x3C3</i>		<i>2-237</i>
<i>GENFC_RD</i>	<i>VGA_IO:0x3CA</i>		<i>2-34</i>
<i>GENFC_RD</i>	<i>VGA_IO:0x3CA</i>		<i>2-200</i>
<i>GENFC_WT</i>	<i>VGA_IO:0x3BA</i>	<i>VGA_IO:0x3DA</i>	<i>2-34</i>
<i>GENFC_WT</i>	<i>VGA_IO:0x3BA</i>	<i>VGA_IO:0x3DA</i>	<i>2-200</i>
<i>GENMO_RD</i>	<i>VGA_IO:0x3CC</i>		<i>2-199</i>
<i>GENMO_WT</i>	<i>VGA_IO:0x3C2</i>		<i>2-198</i>
<i>GENS0</i>	<i>VGA_IO:0x3C2</i>		<i>2-34</i>
<i>GENS0</i>	<i>VGA_IO:0x3C2</i>		<i>2-200</i>
<i>GENS1</i>	<i>VGA_IO:0x3BA</i>	<i>VGA_IO:0x3DA</i>	<i>2-34</i>
<i>GENS1</i>	<i>VGA_IO:0x3BA</i>	<i>VGA_IO:0x3DA</i>	<i>2-200</i>
<i>GRPH8_DATA</i>	<i>VGA_IO:0x3CF</i>		<i>2-233</i>
<i>GRPH8_IDX</i>	<i>VGA_IO:0x3CE</i>		<i>2-233</i>
<i>SEQ8_DATA</i>	<i>VGA_IO:0x3C5</i>		<i>2-223</i>
<i>SEQ8_IDX</i>	<i>VGA_IO:0x3C4</i>		<i>2-223</i>

## A.9 VGA I/O Registers Sorted by Address

Table A-6 VGA I/O Registers Sorted by Address

Name	Address	Secondary Address	Page
<i>CRTC8_IDX</i>	<i>VGA_IO:0x3B4</i>	<i>VGA_IO:0x3D4</i>	2-202
<i>CRTC8_DATA</i>	<i>VGA_IO:0x3B5</i>	<i>VGA_IO:0x3D5</i>	2-202
<i>GENFC_WT</i>	<i>VGA_IO:0x3BA</i>	<i>VGA_IO:0x3DA</i>	2-34
<i>GENSI</i>	<i>VGA_IO:0x3BA</i>	<i>VGA_IO:0x3DA</i>	2-34
<i>GENFC_WT</i>	<i>VGA_IO:0x3BA</i>	<i>VGA_IO:0x3DA</i>	2-200
<i>GENSI</i>	<i>VGA_IO:0x3BA</i>	<i>VGA_IO:0x3DA</i>	2-200
<i>ATTRX</i>	<i>VGA_IO:0x3C0</i>		2-40
<i>ATTRDW</i>	<i>VGA_IO:0x3C0</i>		2-40
<i>ATTRDR</i>	<i>VGA_IO:0x3C1</i>		2-40
<i>GENS0</i>	<i>VGA_IO:0x3C2</i>		2-34
<i>GENMO_WT</i>	<i>VGA_IO:0x3C2</i>		2-198
<i>GENS0</i>	<i>VGA_IO:0x3C2</i>		2-200
<i>GENENB</i>	<i>VGA_IO:0x3C3</i>		2-237
<i>SEQ8_IDX</i>	<i>VGA_IO:0x3C4</i>		2-223
<i>SEQ8_DATA</i>	<i>VGA_IO:0x3C5</i>		2-223
<i>DAC_MASK</i>	<i>VGA_IO:0x3C6</i>		2-39
<i>DAC_R_INDEX</i>	<i>VGA_IO:0x3C7</i>		2-39
<i>DAC_W_INDEX</i>	<i>VGA_IO:0x3C8</i>		2-39
<i>DAC_DATA</i>	<i>VGA_IO:0x3C9</i>		2-39
<i>GENFC_RD</i>	<i>VGA_IO:0x3CA</i>		2-34
<i>GENFC_RD</i>	<i>VGA_IO:0x3CA</i>		2-200
<i>GENMO_RD</i>	<i>VGA_IO:0x3CC</i>		2-199
<i>GRPH8_IDX</i>	<i>VGA_IO:0x3CE</i>		2-233
<i>GRPH8_DATA</i>	<i>VGA_IO:0x3CF</i>		2-233

## A.10 CLK Registers Sorted by Name

Table A-7 CLK Registers Sorted by Name

Name	Address	Page
<i>AGP_PLL_CNTL</i>	<i>CLKIND:0xB</i>	<i>2-297</i>
<i>CLK_PIN_CNTL</i>	<i>CLKIND:0x1</i>	<i>2-291</i>
<i>CLK_PWRMGT_CNTL</i>	<i>CLKIND:0x14</i>	<i>2-13</i>
<i>HTOTAL_CNTL</i>	<i>CLKIND:0x9</i>	<i>2-271</i>
<i>M_SPLL_REF_FB_DIV</i>	<i>CLKIND:0xA</i>	<i>2-294</i>
<i>MCLK_CNTL</i>	<i>CLKIND:0x12</i>	<i>2-303</i>
<i>MDLL_CKO</i>	<i>CLKIND:0xF</i>	<i>2-299</i>
<i>MDLL_RDCKA</i>	<i>CLKIND:0x10</i>	<i>2-300</i>
<i>MDLL_RDCKB</i>	<i>CLKIND:0x11</i>	<i>2-302</i>
<i>MPLL_CNTL</i>	<i>CLKIND:0xE</i>	<i>2-298</i>
<i>PLL_PWRMGT_CNTL</i>	<i>CLKIND:0x15</i>	<i>2-14</i>
<i>PLL_TEST_CNTL</i>	<i>CLKIND:0x13</i>	<i>2-272</i>
<i>PPLL_CNTL</i>	<i>CLKIND:0x2</i>	<i>2-292</i>
<i>PPLL_DIV_0</i>	<i>CLKIND:0x4</i>	<i>2-266</i>
<i>PPLL_DIV_1</i>	<i>CLKIND:0x5</i>	<i>2-267</i>
<i>PPLL_DIV_2</i>	<i>CLKIND:0x6</i>	<i>2-268</i>
<i>PPLL_DIV_3</i>	<i>CLKIND:0x7</i>	<i>2-269</i>
<i>PPLL_REF_DIV</i>	<i>CLKIND:0x3</i>	<i>2-293</i>
<i>SCLK_CNTL</i>	<i>CLKIND:0xD</i>	<i>2-295</i>
<i>SPLL_CNTL</i>	<i>CLKIND:0xC</i>	<i>2-294</i>
<i>VCLK_ECP_CNTL</i>	<i>CLKIND:0x8</i>	<i>2-270</i>

## A.11 CLK Registers Sorted by Address

Table A-8 CLK Registers Sorted by Address

Name	Address	Page
<i>CLK_PIN_CNTL</i>	<i>CLKIND:0x1</i>	2-291
<i>PPLL_CNTL</i>	<i>CLKIND:0x2</i>	2-292
<i>PPLL_REF_DIV</i>	<i>CLKIND:0x3</i>	2-293
<i>PPLL_DIV_0</i>	<i>CLKIND:0x4</i>	2-266
<i>PPLL_DIV_1</i>	<i>CLKIND:0x5</i>	2-267
<i>PPLL_DIV_2</i>	<i>CLKIND:0x6</i>	2-268
<i>PPLL_DIV_3</i>	<i>CLKIND:0x7</i>	2-269
<i>VCLK_ECP_CNTL</i>	<i>CLKIND:0x8</i>	2-270
<i>HTOTAL_CNTL</i>	<i>CLKIND:0x9</i>	2-271
<i>M_SPLL_REF_FB_DIV</i>	<i>CLKIND:0xA</i>	2-294
<i>AGP_PLL_CNTL</i>	<i>CLKIND:0xB</i>	2-297
<i>SPLL_CNTL</i>	<i>CLKIND:0xC</i>	2-294
<i>SCLK_CNTL</i>	<i>CLKIND:0xD</i>	2-295
<i>MPLL_CNTL</i>	<i>CLKIND:0xE</i>	2-298
<i>MDLL_CKO</i>	<i>CLKIND:0xF</i>	2-299
<i>MDLL_RDCKA</i>	<i>CLKIND:0x10</i>	2-300
<i>MDLL_RDCKB</i>	<i>CLKIND:0x11</i>	2-302
<i>MCLK_CNTL</i>	<i>CLKIND:0x12</i>	2-303
<i>PLL_TEST_CNTL</i>	<i>CLKIND:0x13</i>	2-272
<i>CLK_PWRMGT_CNTL</i>	<i>CLKIND:0x14</i>	2-13
<i>PLL_PWRMGT_CNTL</i>	<i>CLKIND:0x15</i>	2-14

## A.12 PCI Configuration Registers Sorted by Name

Table A-9 PCI Configuration Registers Sorted by Name

Name	Address	Secondary Address	Page
<i>ADAPTER_ID</i>	<i>MMReg:0xF2C</i>	<i>pciConfig:0x2C</i>	<i>2-247</i>
<i>ADAPTER_ID_W</i>	<i>MMReg:0xF4C</i>	<i>pciConfig:0x4C</i>	<i>2-249</i>
<i>AGP_CAP_ID</i>	<i>MMReg:0xF58</i>	<i>pciConfig:0x58</i>	<i>2-250</i>
<i>AGP_COMMAND</i>	<i>MMReg:0xF60</i>	<i>pciConfig:0x60</i>	<i>2-251</i>
<i>AGP_STATUS</i>	<i>MMReg:0xF5C</i>	<i>pciConfig:0x5C</i>	<i>2-251</i>
<i>BASE_CODE</i>	<i>MMReg:0xF0B</i>	<i>pciConfig:0xB</i>	<i>2-246</i>
<i>BIOS_ROM</i>	<i>MMReg:0xF30</i>	<i>pciConfig:0x30</i>	<i>2-248</i>
<i>BIST</i>	<i>MMReg:0xF0F</i>	<i>pciConfig:0xF</i>	<i>2-246</i>
<i>CACHE_LINE</i>	<i>MMReg:0xF0C</i>	<i>pciConfig:0xC</i>	<i>2-246</i>
<i>CAPABILITIES_PTR</i>	<i>MMReg:0xF34</i>	<i>pciConfig:0x34</i>	<i>2-248</i>
<i>COMMAND</i>	<i>MMReg:0xF04</i>	<i>pciConfig:0x4</i>	<i>2-244</i>
<i>DEVICE_ID</i>	<i>MMReg:0xF02</i>	<i>pciConfig:0x2</i>	<i>2-244</i>
<i>HEADER</i>	<i>MMReg:0xF0E</i>	<i>pciConfig:0xE</i>	<i>2-246</i>
<i>INTERRUPT_LINE</i>	<i>MMReg:0xF3C</i>	<i>pciConfig:0x3C</i>	<i>2-248</i>
<i>INTERRUPT_PIN</i>	<i>MMReg:0xF3D</i>	<i>pciConfig:0x3D</i>	<i>2-248</i>
<i>IO_BASE</i>	<i>MMReg:0xF14</i>	<i>pciConfig:0x14</i>	<i>2-247</i>
<i>LATENCY</i>	<i>MMReg:0xF0D</i>	<i>pciConfig:0xD</i>	<i>2-246</i>
<i>MAX_LATENCY</i>	<i>MMReg:0xF3F</i>	<i>pciConfig:0x3F</i>	<i>2-249</i>
<i>MEM_BASE</i>	<i>MMReg:0xF10</i>	<i>pciConfig:0x10</i>	<i>2-247</i>
<i>MIN_GRANT</i>	<i>MMReg:0xF3E</i>	<i>pciConfig:0x3E</i>	<i>2-248</i>
<i>PM_STATUS</i>	<i>MMReg:0xF54</i>	<i>pciConfig:0x54</i>	<i>2-250</i>
<i>PMI_CAP_ID</i>	<i>MMReg:0xF50</i>	<i>pciConfig:0x50</i>	<i>2-249</i>
<i>PMI_DATA</i>	<i>MMReg:0xF57</i>	<i>pciConfig:0x57</i>	<i>2-250</i>
<i>PMI_NXT_CAP_PTR</i>	<i>MMReg:0xF51</i>	<i>pciConfig:0x51</i>	<i>2-249</i>
<i>PMI_PMC_REG</i>	<i>MMReg:0xF52</i>	<i>pciConfig:0x52</i>	<i>2-249</i>
<i>REG_BASE</i>	<i>MMReg:0xF18</i>	<i>pciConfig:0x18</i>	<i>2-247</i>
<i>REGPROG_INF</i>	<i>MMReg:0xF09</i>	<i>pciConfig:0x9</i>	<i>2-245</i>
<i>REVISION_ID</i>	<i>MMReg:0xF08</i>	<i>pciConfig:0x8</i>	<i>2-245</i>
<i>STATUS</i>	<i>MMReg:0xF06</i>	<i>pciConfig:0x6</i>	<i>2-244</i>
<i>SUB_CLASS</i>	<i>MMReg:0xF0A</i>	<i>pciConfig:0xA</i>	<i>2-245</i>
<i>VENDOR_ID</i>	<i>MMReg:0xF00</i>	<i>pciConfig:0x0</i>	<i>2-243</i>

## A.13 PCI Configuration Registers Sorted by Address

Table A-10 PCI Configuration Registers Sorted by Address

Name	Address	Secondary Address	Page
<i>VENDOR_ID</i>	<i>MMReg:0xF00</i>	<i>pciConfig:0x0</i>	2-243
<i>DEVICE_ID</i>	<i>MMReg:0xF02</i>	<i>pciConfig:0x2</i>	2-244
<i>COMMAND</i>	<i>MMReg:0xF04</i>	<i>pciConfig:0x4</i>	2-244
<i>STATUS</i>	<i>MMReg:0xF06</i>	<i>pciConfig:0x6</i>	2-244
<i>REVISION_ID</i>	<i>MMReg:0xF08</i>	<i>pciConfig:0x8</i>	2-245
<i>REGPROG_INF</i>	<i>MMReg:0xF09</i>	<i>pciConfig:0x9</i>	2-245
<i>SUB_CLASS</i>	<i>MMReg:0xF0A</i>	<i>pciConfig:0xA</i>	2-245
<i>BASE_CODE</i>	<i>MMReg:0xF0B</i>	<i>pciConfig:0xB</i>	2-246
<i>CACHE_LINE</i>	<i>MMReg:0xF0C</i>	<i>pciConfig:0xC</i>	2-246
<i>LATENCY</i>	<i>MMReg:0xF0D</i>	<i>pciConfig:0xD</i>	2-246
<i>HEADER</i>	<i>MMReg:0xF0E</i>	<i>pciConfig:0xE</i>	2-246
<i>BIST</i>	<i>MMReg:0xF0F</i>	<i>pciConfig:0xF</i>	2-246
<i>MEM_BASE</i>	<i>MMReg:0xF10</i>	<i>pciConfig:0x10</i>	2-247
<i>IO_BASE</i>	<i>MMReg:0xF14</i>	<i>pciConfig:0x14</i>	2-247
<i>REG_BASE</i>	<i>MMReg:0xF18</i>	<i>pciConfig:0x18</i>	2-247
<i>ADAPTER_ID</i>	<i>MMReg:0xF2C</i>	<i>pciConfig:0x2C</i>	2-247
<i>BIOS_ROM</i>	<i>MMReg:0xF30</i>	<i>pciConfig:0x30</i>	2-248
<i>CAPABILITIES_PTR</i>	<i>MMReg:0xF34</i>	<i>pciConfig:0x34</i>	2-248
<i>INTERRUPT_LINE</i>	<i>MMReg:0xF3C</i>	<i>pciConfig:0x3C</i>	2-248
<i>INTERRUPT_PIN</i>	<i>MMReg:0xF3D</i>	<i>pciConfig:0x3D</i>	2-248
<i>MIN_GRANT</i>	<i>MMReg:0xF3E</i>	<i>pciConfig:0x3E</i>	2-248
<i>MAX_LATENCY</i>	<i>MMReg:0xF3F</i>	<i>pciConfig:0x3F</i>	2-249
<i>ADAPTER_ID_W</i>	<i>MMReg:0xF4C</i>	<i>pciConfig:0x4C</i>	2-249
<i>PMI_CAP_ID</i>	<i>MMReg:0xF50</i>	<i>pciConfig:0x50</i>	2-249
<i>PMI_NXT_CAP_PTR</i>	<i>MMReg:0xF51</i>	<i>pciConfig:0x51</i>	2-249
<i>PMI_PMC_REG</i>	<i>MMReg:0xF52</i>	<i>pciConfig:0x52</i>	2-249
<i>PM_STATUS</i>	<i>MMReg:0xF54</i>	<i>pciConfig:0x54</i>	2-250
<i>PMI_DATA</i>	<i>MMReg:0xF57</i>	<i>pciConfig:0x57</i>	2-250
<i>AGP_CAP_ID</i>	<i>MMReg:0xF58</i>	<i>pciConfig:0x58</i>	2-250
<i>AGP_STATUS</i>	<i>MMReg:0xF5C</i>	<i>pciConfig:0x5C</i>	2-251
<i>AGP_COMMAND</i>	<i>MMReg:0xF60</i>	<i>pciConfig:0x60</i>	2-251

Table 2-4 Registers sorted by Address

Name	I/OAddress	MM Address	Sec Address	Page
MM_INDEX	IOReg:0x0	MMReg:0x0		2-237
BUS_CNTL	IOReg:0x30	MMReg:0x30		2-237
BUS_CNTL1	IOReg:0x34	MMReg:0x34		2-239
MEM_VGA_WP_SEL	IOReg:0x38	MMReg:0x38		2-201
MEM_VGA_RP_SEL	IOReg:0x3C	MMReg:0x3C		2-201
MM_DATA	IOReg:0x4	MMReg:0x4		2-237
GEN_INT_CNTL	IOReg:0x40	MMReg:0x40		2-2
GEN_INT_STATUS	IOReg:0x44	MMReg:0x44		2-3
GEN_INT_STATUS	IOReg:0x44	MMReg:0x44		2-118
HI_STAT	IOReg:0x4C	MMReg:0x4C		2-239
CRTC_GEN_CNTL	IOReg:0x50	MMReg:0x50		2-41
CRTC_EXT_CNTL	IOReg:0x54	MMReg:0x54		2-43
DAC_CNTL	IOReg:0x58	MMReg:0x58		2-35
CRTC_STATUS	IOReg:0x5C	MMReg:0x5C		2-45
GPIO_VGA_DDC	IOReg:0x60	MMReg:0x60		2-257
GPIO_DVI_DDC	IOReg:0x64	MMReg:0x64		2-258
GPIO_MONID	IOReg:0x68	MMReg:0x68		2-45
CLOCK_CNTL_INDEX	IOReg:0x8	MMReg:0x8		2-266
VIPH_REG_ADDR	IOReg:0x80	MMReg:0x80		2-116
VIPH_REG_DATA	IOReg:0x84	MMReg:0x84		2-116
TVOUT_0_SCRATCH	IOReg:0x88	MMReg:0x88		2-289
TVOUT_1_SCRATCH	IOReg:0x8C	MMReg:0x8C		2-289
I2C_CNTL_0	IOReg:0x90	MMReg:0x90		2-108
I2C_CNTL_1	IOReg:0x94	MMReg:0x94		2-109
I2C_DATA	IOReg:0x98	MMReg:0x98		2-109
PALETTE_INDEX	IOReg:0xB0	MMReg:0xB0		2-46
PALETTE_30_DATA	IOReg:0xB8	MMReg:0xB8		2-46
CLOCK_CNTL_DATA	IOReg:0xC	MMReg:0xC		2-266
CONFIG_CNTL	IOReg:0xE0	MMReg:0xE0		2-240
RBBM_CNTL	IOReg:0xEC	MMReg:0xEC	MMReg:0xE44	2-5
RBBM_SOFT_RESET	IOReg:0xF0	MMReg:0xF0	MMReg:0xE48	2-7
CONFIG_MEMSIZE	IOReg:0xF8	MMReg:0xF8		2-240
CONFIG_APER_0_BASE		MMReg:0x100		2-240
CP_CSQ_APER_PRIMARY		MMReg:0x1000-0x11FC		2-144
CONFIG_APER_1_BASE		MMReg:0x104		2-240
CONFIG_APER_SIZE		MMReg:0x108		2-241
CONFIG_REG_1_BASE		MMReg:0x10C		2-241
CONFIG_REG_APER_SIZE		MMReg:0x110		2-241
HOST_PATH_CNTL		MMReg:0x130		2-21
CP_CSQ_APER_INDIRECT		MMReg:0x1300-0x13FC		2-144
SW_SEMAPHORE		MMReg:0x13C		2-22
MEM_CNTL		MMReg:0x140		2-15
DST_OFFSET		MMReg:0x1404		2-156

Table 2-4 Registers sorted by Address

<i>Name</i>	<i>I/OAddress</i>	<i>MM Address</i>	<i>Sec Address</i>	<b>Page</b>
<i>DST_PITCH</i>		<i>MMReg:0x1408</i>		2-156
<i>DST_WIDTH</i>		<i>MMReg:0x140C</i>		2-156
<i>DST_HEIGHT</i>		<i>MMReg:0x1410</i>		2-157
<i>SRC_X</i>		<i>MMReg:0x1414</i>		2-157
<i>SRC_Y</i>		<i>MMReg:0x1418</i>		2-157
<i>DST_X</i>		<i>MMReg:0x141C</i>		2-157
<i>DST_Y</i>		<i>MMReg:0x1420</i>		2-157
<i>SRC_PITCH_OFFSET</i>		<i>MMReg:0x1428</i>		2-158
<i>DST_PITCH_OFFSET</i>		<i>MMReg:0x142C</i>		2-158
<i>SRC_Y_X</i>		<i>MMReg:0x1434</i>		2-158
<i>DST_Y_X</i>		<i>MMReg:0x1438</i>		2-159
<i>DST_HEIGHT_WIDTH</i>		<i>MMReg:0x143C</i>		2-159
<i>EXT_MEM_CNTL</i>		<i>MMReg:0x144</i>		2-19
<i>DP_GUI_MASTER_CNTL</i>		<i>MMReg:0x146C</i>		2-159
<i>BRUSH_Y_X</i>		<i>MMReg:0x1474</i>		2-161
<i>DP_BRUSH_BKGD_CLR</i>		<i>MMReg:0x1478</i>		2-162
<i>DP_BRUSH_FRGD_CLR</i>		<i>MMReg:0x147C</i>		2-162
<i>MC_FB_LOCATION</i>		<i>MMReg:0x148</i>		2-16
<i>BRUSH_DATA0</i>		<i>MMReg:0x1480</i>		2-162
<i>BRUSH_DATA1</i>		<i>MMReg:0x1484</i>		2-162
<i>BRUSH_DATA2</i>		<i>MMReg:0x1488</i>		2-162
<i>BRUSH_DATA3</i>		<i>MMReg:0x148C</i>		2-163
<i>BRUSH_DATA4</i>		<i>MMReg:0x1490</i>		2-163
<i>BRUSH_DATA5</i>		<i>MMReg:0x1494</i>		2-163
<i>BRUSH_DATA6</i>		<i>MMReg:0x1498</i>		2-163
<i>BRUSH_DATA7</i>		<i>MMReg:0x149C</i>		2-163
<i>BRUSH_DATA8</i>		<i>MMReg:0x14A0</i>		2-164
<i>BRUSH_DATA9</i>		<i>MMReg:0x14A4</i>		2-164
<i>BRUSH_DATA10</i>		<i>MMReg:0x14A8</i>		2-164
<i>BRUSH_DATA11</i>		<i>MMReg:0x14AC</i>		2-164
<i>BRUSH_DATA12</i>		<i>MMReg:0x14B0</i>		2-164
<i>BRUSH_DATA13</i>		<i>MMReg:0x14B4</i>		2-165
<i>BRUSH_DATA14</i>		<i>MMReg:0x14B8</i>		2-165
<i>BRUSH_DATA15</i>		<i>MMReg:0x14BC</i>		2-165
<i>MC_AGP_LOCATION</i>		<i>MMReg:0x14C</i>		2-17
<i>BRUSH_DATA16</i>		<i>MMReg:0x14C0</i>		2-165
<i>BRUSH_DATA17</i>		<i>MMReg:0x14C4</i>		2-165
<i>BRUSH_DATA18</i>		<i>MMReg:0x14C8</i>		2-166
<i>BRUSH_DATA19</i>		<i>MMReg:0x14CC</i>		2-166
<i>BRUSH_DATA20</i>		<i>MMReg:0x14D0</i>		2-166
<i>BRUSH_DATA21</i>		<i>MMReg:0x14D4</i>		2-166
<i>BRUSH_DATA22</i>		<i>MMReg:0x14D8</i>		2-166
<i>BRUSH_DATA23</i>		<i>MMReg:0x14DC</i>		2-167
<i>BRUSH_DATA24</i>		<i>MMReg:0x14E0</i>		2-167
<i>BRUSH_DATA25</i>		<i>MMReg:0x14E4</i>		2-167

Table 2-4 Registers sorted by Address

<i>Name</i>	<i>I/OAddress</i>	<i>MM Address</i>	<i>Sec Address</i>	<b>Page</b>
<i>BRUSH_DATA26</i>		<i>MMReg:0x14E8</i>		2-167
<i>BRUSH_DATA27</i>		<i>MMReg:0x14EC</i>		2-167
<i>BRUSH_DATA28</i>		<i>MMReg:0x14F0</i>		2-168
<i>BRUSH_DATA29</i>		<i>MMReg:0x14F4</i>		2-168
<i>BRUSH_DATA30</i>		<i>MMReg:0x14F8</i>		2-168
<i>BRUSH_DATA31</i>		<i>MMReg:0x14FC</i>		2-168
<i>BRUSH_DATA32</i>		<i>MMReg:0x1500</i>		2-168
<i>BRUSH_DATA33</i>		<i>MMReg:0x1504</i>		2-169
<i>BRUSH_DATA34</i>		<i>MMReg:0x1508</i>		2-169
<i>BRUSH_DATA35</i>		<i>MMReg:0x150C</i>		2-169
<i>BRUSH_DATA36</i>		<i>MMReg:0x1510</i>		2-169
<i>BRUSH_DATA37</i>		<i>MMReg:0x1514</i>		2-169
<i>BRUSH_DATA38</i>		<i>MMReg:0x1518</i>		2-170
<i>BRUSH_DATA39</i>		<i>MMReg:0x151C</i>		2-170
<i>BRUSH_DATA40</i>		<i>MMReg:0x1520</i>		2-170
<i>BRUSH_DATA41</i>		<i>MMReg:0x1524</i>		2-170
<i>BRUSH_DATA42</i>		<i>MMReg:0x1528</i>		2-170
<i>BRUSH_DATA43</i>		<i>MMReg:0x152C</i>		2-171
<i>BRUSH_DATA44</i>		<i>MMReg:0x1530</i>		2-171
<i>BRUSH_DATA45</i>		<i>MMReg:0x1534</i>		2-171
<i>BRUSH_DATA46</i>		<i>MMReg:0x1538</i>		2-171
<i>BRUSH_DATA47</i>		<i>MMReg:0x153C</i>		2-171
<i>MEM_INIT_LATENCY_TIMER</i>		<i>MMReg:0x154</i>		2-17
<i>BRUSH_DATA48</i>		<i>MMReg:0x1540</i>		2-172
<i>BRUSH_DATA49</i>		<i>MMReg:0x1544</i>		2-172
<i>BRUSH_DATA50</i>		<i>MMReg:0x1548</i>		2-172
<i>BRUSH_DATA51</i>		<i>MMReg:0x154C</i>		2-172
<i>BRUSH_DATA52</i>		<i>MMReg:0x1550</i>		2-172
<i>BRUSH_DATA53</i>		<i>MMReg:0x1554</i>		2-173
<i>BRUSH_DATA54</i>		<i>MMReg:0x1558</i>		2-173
<i>BRUSH_DATA55</i>		<i>MMReg:0x155C</i>		2-173
<i>BRUSH_DATA56</i>		<i>MMReg:0x1560</i>		2-173
<i>BRUSH_DATA57</i>		<i>MMReg:0x1564</i>		2-173
<i>BRUSH_DATA58</i>		<i>MMReg:0x1568</i>		2-174
<i>BRUSH_DATA59</i>		<i>MMReg:0x156C</i>		2-174
<i>BRUSH_DATA60</i>		<i>MMReg:0x1570</i>		2-174
<i>BRUSH_DATA61</i>		<i>MMReg:0x1574</i>		2-174
<i>BRUSH_DATA62</i>		<i>MMReg:0x1578</i>		2-174
<i>BRUSH_DATA63</i>		<i>MMReg:0x157C</i>		2-175
<i>MEM_SDRAM_MODE_REG</i>		<i>MMReg:0x158</i>		2-18
<i>DST_WIDTH_X</i>		<i>MMReg:0x1588</i>		2-175
<i>DST_HEIGHT_WIDTH_8</i>		<i>MMReg:0x158C</i>		2-175
<i>SRC_X_Y</i>		<i>MMReg:0x1590</i>		2-175
<i>DST_X_Y</i>		<i>MMReg:0x1594</i>		2-176

Table 2-4 Registers sorted by Address

<i>Name</i>	<i>I/OAddress</i>	<i>MM Address</i>	<i>Sec Address</i>	<b>Page</b>
<i>DST_WIDTH_HEIGHT</i>		<i>MMReg:0x1598</i>		2-176
<i>DST_WIDTH_X_INCY</i>		<i>MMReg:0x159C</i>		2-176
<i>DST_HEIGHT_Y</i>		<i>MMReg:0x15A0</i>		2-177
<i>SRC_OFFSET</i>		<i>MMReg:0x15AC</i>		2-177
<i>SRC_PITCH</i>		<i>MMReg:0x15B0</i>		2-177
<i>CLR_CMP_CNTL</i>		<i>MMReg:0x15C0</i>		2-178
<i>CLR_CMP_CLR_SRC</i>		<i>MMReg:0x15C4</i>		2-178
<i>CLR_CMP_CLR_DST</i>		<i>MMReg:0x15C8</i>		2-179
<i>CLR_CMP_MSK</i>		<i>MMReg:0x15CC</i>		2-179
<i>DP_DST_ENDIAN</i>		<i>MMReg:0x15D0</i>		2-288
<i>DP_SRC_ENDIAN</i>		<i>MMReg:0x15D4</i>		2-288
<i>DP_SRC_FRGD_CLR</i>		<i>MMReg:0x15D8</i>		2-179
<i>DP_SRC_BKGD_CLR</i>		<i>MMReg:0x15DC</i>		2-179
<i>SCRATCH_REG0</i>		<i>MMReg:0x15E0</i>		2-144
<i>SCRATCH_REG1</i>		<i>MMReg:0x15E4</i>		2-145
<i>SCRATCH_REG2</i>		<i>MMReg:0x15E8</i>		2-145
<i>SCRATCH_REG3</i>		<i>MMReg:0x15EC</i>		2-145
<i>SCRATCH_REG4</i>		<i>MMReg:0x15F0</i>		2-145
<i>SCRATCH_REG5</i>		<i>MMReg:0x15F4</i>		2-145
<i>BM_STATUS</i>		<i>MMReg:0x160</i>		2-243
<i>DST_LINE_START</i>		<i>MMReg:0x1600</i>		2-179
<i>DST_LINE_END</i>		<i>MMReg:0x1604</i>		2-180
<i>DST_LINE_PATCOUNT</i>		<i>MMReg:0x1608</i>		2-180
<i>PAD_AGPINPUT_DELAY</i>		<i>MMReg:0x164</i>		2-241
<i>SC_LEFT</i>		<i>MMReg:0x1640</i>		2-180
<i>SC_RIGHT</i>		<i>MMReg:0x1644</i>		2-180
<i>SC_TOP</i>		<i>MMReg:0x1648</i>		2-181
<i>SC_BOTTOM</i>		<i>MMReg:0x164C</i>		2-181
<i>SRC_SC_RIGHT</i>		<i>MMReg:0x1654</i>		2-181
<i>SRC_SC_BOTTOM</i>		<i>MMReg:0x165C</i>		2-181
<i>PAD_CTLR_STRENGTH</i>		<i>MMReg:0x168</i>		2-241
<i>PAD_CTLR_UPDATE</i>		<i>MMReg:0x16C</i>		2-242
<i>DP_CNTL</i>		<i>MMReg:0x16C0</i>		2-182
<i>DP_DATATYPE</i>		<i>MMReg:0x16C4</i>		2-182
<i>DP_MIX</i>		<i>MMReg:0x16C8</i>		2-183
<i>DP_WRITE_MSK</i>		<i>MMReg:0x16CC</i>		2-184
<i>DP_CNTL_XDIR_YDIR_YMAJOR</i>		<i>MMReg:0x16D0</i>		2-288
<i>DEFAULT_PITCH_OFFSET</i>		<i>MMReg:0x16E0</i>		2-188
<i>DEFAULT_SC_BOTTOM_RIGHT</i>		<i>MMReg:0x16E8</i>		2-184
<i>SC_TOP_LEFT</i>		<i>MMReg:0x16EC</i>		2-184
<i>SC_BOTTOM_RIGHT</i>		<i>MMReg:0x16F0</i>		2-184
<i>SRC_SC_BOTTOM_RIGHT</i>		<i>MMReg:0x16F4</i>		2-185
<i>DST_TILE</i>		<i>MMReg:0x1700</i>		2-185
<i>SRC_TILE</i>		<i>MMReg:0x1704</i>		2-185
<i>DSTCACHE_MODE</i>		<i>MMReg:0x1710</i>		2-288

Table 2-4 Registers sorted by Address

Name	I/OAddress	MM Address	Sec Address	Page
<i>DSTCACHE_CTLSTAT</i>		<i>MMReg:0x1714</i>		2-289
<i>WAIT_UNTIL</i>		<i>MMReg:0x1720</i>		2-9
<i>ISYNC_CNTL</i>		<i>MMReg:0x1724</i>		2-10
<i>RBBM_GUICNTL</i>		<i>MMReg:0x172C</i>		2-11
<i>AGP_CNTL</i>		<i>MMReg:0x174</i>		2-242
<i>SRC_CLUT_ADDRESS</i>		<i>MMReg:0x1780</i>		2-185
<i>SRC_CLUT_DATA</i>		<i>MMReg:0x1784</i>		2-186
<i>SRC_CLUT_DATA_RD</i>		<i>MMReg:0x1788</i>		2-186
<i>HOST_DATA0</i>		<i>MMReg:0x17C0</i>		2-186
<i>HOST_DATA1</i>		<i>MMReg:0x17C4</i>		2-186
<i>HOST_DATA2</i>		<i>MMReg:0x17C8</i>		2-186
<i>HOST_DATA3</i>		<i>MMReg:0x17CC</i>		2-187
<i>HOST_DATA4</i>		<i>MMReg:0x17D0</i>		2-187
<i>HOST_DATA5</i>		<i>MMReg:0x17D4</i>		2-187
<i>HOST_DATA6</i>		<i>MMReg:0x17D8</i>		2-187
<i>HOST_DATA7</i>		<i>MMReg:0x17DC</i>		2-188
<i>HOST_DATA_LAST</i>		<i>MMReg:0x17E0</i>		2-188
<i>DP_XOP</i>		<i>MMReg:0x17F8</i>		2-188
<i>VIPPAD_STRENGTH</i>		<i>MMReg:0x194</i>		2-289
<i>VIPPADI_MASK</i>		<i>MMReg:0x1A8</i>		2-290
<i>VIPPADI_Y</i>		<i>MMReg:0x1B4</i>		2-290
<i>EXTERN_TRIG_CNTL</i>		<i>MMReg:0x1BC</i>		2-290
<i>RE_SOLID_COLOR</i>		<i>MMReg:0x1C1C</i>	<i>MMReg:0x261C</i>	2-193
<i>RE_WIDTH_HEIGHT</i>		<i>MMReg:0x1C44</i>	<i>MMReg:0x2644</i>	2-193
<i>RE_MISC</i>		<i>MMReg:0x1CC4</i>	<i>MMReg:0x26C4</i>	2-193
<i>RE_STIPPLE_ADDR</i>		<i>MMReg:0x1CC8</i>	<i>MMReg:0x26C8</i>	2-193
<i>RE_STIPPLE_DATA</i>		<i>MMReg:0x1CCC</i>	<i>MMReg:0x26CC</i>	2-194
<i>RE_LINE_PATTERN</i>		<i>MMReg:0x1CD0</i>	<i>MMReg:0x26D0</i>	2-194
<i>RE_LINE_STATE</i>		<i>MMReg:0x1CD4</i>	<i>MMReg:0x26D4</i>	2-194
<i>RE_SCISSOR_TL_0</i>		<i>MMReg:0x1CD8</i>	<i>MMReg:0x26D8</i>	2-195
<i>RE_SCISSOR_BR_0</i>		<i>MMReg:0x1CDC</i>	<i>MMReg:0x26DC</i>	2-195
<i>RE_SCISSOR_TL_1</i>		<i>MMReg:0x1CE0</i>	<i>MMReg:0x26E0</i>	2-195
<i>RE_SCISSOR_BR_1</i>		<i>MMReg:0x1CE4</i>	<i>MMReg:0x26E4</i>	2-195
<i>RE_SCISSOR_TL_2</i>		<i>MMReg:0x1CE8</i>	<i>MMReg:0x26E8</i>	2-195
<i>RE_SCISSOR_BR_2</i>		<i>MMReg:0x1CEC</i>	<i>MMReg:0x26EC</i>	2-196
<i>AIC_CTRL</i>		<i>MMReg:0x1D0</i>		2-251
<i>PP_LUM_MATRIX</i>		<i>MMReg:0x1D00</i>	<i>MMReg:0x2D00</i>	2-284
<i>AIC_STAT</i>		<i>MMReg:0x1D4</i>		2-252
<i>PP_ROT_MATRIX_0</i>		<i>MMReg:0x1D58</i>	<i>MMReg:0x2D58</i>	2-283
<i>PP_ROT_MATRIX_1</i>		<i>MMReg:0x1D5C</i>	<i>MMReg:0x2D5C</i>	2-284
<i>RB3D_DEPTHXY_OFFSET</i>		<i>MMReg:0x1D60</i>		2-287
<i>AIC_PT_BASE</i>		<i>MMReg:0x1D8</i>		2-253
<i>AIC_LO_ADDR</i>		<i>MMReg:0x1DC</i>		2-253
<i>PP_CUBIC_OFFSET_T0_0</i>		<i>MMReg:0x1DD0</i>	<i>MMReg:0x2DD0</i>	2-279

Table 2-4 Registers sorted by Address

<i>Name</i>	<i>I/OAddress</i>	<i>MM Address</i>	<i>Sec Address</i>	<b>Page</b>
<i>PP_CUBIC_OFFSET_T0_1</i>		<i>MMReg:0x1DD4</i>	<i>MMReg:0x2DD4</i>	2-280
<i>PP_CUBIC_OFFSET_T0_2</i>		<i>MMReg:0x1DD8</i>	<i>MMReg:0x2DD8</i>	2-280
<i>PP_CUBIC_OFFSET_T0_3</i>		<i>MMReg:0x1DDC</i>	<i>MMReg:0x2DDC</i>	2-280
<i>PP_CUBIC_OFFSET_T0_4</i>		<i>MMReg:0x1DE0</i>	<i>MMReg:0x2DE0</i>	2-280
<i>AIC_HI_ADDR</i>		<i>MMReg:0x1E0</i>		2-253
<i>PP_CUBIC_OFFSET_T1_0</i>		<i>MMReg:0x1E00</i>	<i>MMReg:0x2E00</i>	2-280
<i>PP_CUBIC_OFFSET_T1_1</i>		<i>MMReg:0x1E04</i>	<i>MMReg:0x2E04</i>	2-281
<i>PP_CUBIC_OFFSET_T1_2</i>		<i>MMReg:0x1E08</i>	<i>MMReg:0x2E08</i>	2-281
<i>PP_CUBIC_OFFSET_T1_3</i>		<i>MMReg:0x1E0C</i>	<i>MMReg:0x2E0C</i>	2-281
<i>PP_CUBIC_OFFSET_T1_4</i>		<i>MMReg:0x1E10</i>	<i>MMReg:0x2E10</i>	2-281
<i>PP_CUBIC_OFFSET_T2_0</i>		<i>MMReg:0x1E14</i>	<i>MMReg:0x2E14</i>	2-281
<i>PP_CUBIC_OFFSET_T2_1</i>		<i>MMReg:0x1E18</i>	<i>MMReg:0x2E18</i>	2-282
<i>PP_CUBIC_OFFSET_T2_2</i>		<i>MMReg:0x1E1C</i>	<i>MMReg:0x2E1C</i>	2-282
<i>PP_CUBIC_OFFSET_T2_3</i>		<i>MMReg:0x1E20</i>	<i>MMReg:0x2E20</i>	2-282
<i>PP_CUBIC_OFFSET_T2_4</i>		<i>MMReg:0x1E24</i>	<i>MMReg:0x2E24</i>	2-282
<i>AIC_TLB_ADDR</i>		<i>MMReg:0x1E4</i>		2-253
<i>AIC_TLB_DATA</i>		<i>MMReg:0x1E8</i>		2-253
<i>MEDIA_0_SCRATCH</i>		<i>MMReg:0x1F0</i>		2-290
<i>MEDIA_1_SCRATCH</i>		<i>MMReg:0x1F4</i>		2-291
<i>CRTC_H_TOTAL_DISP</i>		<i>MMReg:0x200</i>		2-47
<i>CRTC_H_SYNC_STRT_WID</i>		<i>MMReg:0x204</i>		2-47
<i>CRTC_V_TOTAL_DISP</i>		<i>MMReg:0x208</i>		2-47
<i>CRTC_V_SYNC_STRT_WID</i>		<i>MMReg:0x20C</i>		2-48
<i>CRTC_VLINE_CRNT_VLINE</i>		<i>MMReg:0x210</i>		2-48
<i>CRTC_CRNT_FRAME</i>		<i>MMReg:0x214</i>		2-48
<i>CRTC_GUI_TRIG_VLINE</i>		<i>MMReg:0x218</i>		2-48
<i>CRTC_DEBUG</i>		<i>MMReg:0x21C</i>		2-49
<i>CRTC_OFFSET_RIGHT</i>		<i>MMReg:0x220</i>		2-50
<i>CRTC_OFFSET</i>		<i>MMReg:0x224</i>		2-50
<i>CRTC_OFFSET_CNTL</i>		<i>MMReg:0x228</i>		2-51
<i>CRTC_PITCH</i>		<i>MMReg:0x22C</i>		2-53
<i>OVR_CLR</i>		<i>MMReg:0x230</i>		2-53
<i>OVR_WID_LEFT_RIGHT</i>		<i>MMReg:0x234</i>		2-53
<i>OVR_WID_TOP_BOTTOM</i>		<i>MMReg:0x238</i>		2-54
<i>DISPLAY_BASE_ADDR</i>		<i>MMReg:0x23C</i>		2-54
<i>SNAPSHOT_VH_COUNTS</i>		<i>MMReg:0x240</i>		2-54
<i>SNAPSHOT_F_COUNT</i>		<i>MMReg:0x244</i>		2-54
<i>N_VIF_COUNT</i>		<i>MMReg:0x248</i>		2-55
<i>SNAPSHOT_VIF_COUNT</i>		<i>MMReg:0x24C</i>		2-55
<i>FP_CRTC_H_TOTAL_DISP</i>		<i>MMReg:0x250</i>		2-55
<i>FP_CRTC_V_TOTAL_DISP</i>		<i>MMReg:0x254</i>		2-56
<i>CRT_CRTC_H_SYNC_STRT_WID</i>		<i>MMReg:0x258</i>		2-258
<i>CRT_CRTC_V_SYNC_STRT_WID</i>		<i>MMReg:0x25C</i>		2-259
<i>CUR_OFFSET</i>		<i>MMReg:0x260</i>		2-56
<i>CUR_HORZ_VERT_POSN</i>		<i>MMReg:0x264</i>		2-57

Table 2-4 Registers sorted by Address

<i>Name</i>	<i>I/OAddress</i>	<i>MM Address</i>	<i>Sec Address</i>	<b>Page</b>
<i>CUR_HORZ_VERT_OFF</i>		<i>MMReg:0x268</i>		2-57
<i>CUR_CLR0</i>		<i>MMReg:0x26C</i>		2-58
<i>RE_TOP_LEFT</i>		<i>MMReg:0x26C0</i>		2-273
<i>RE_AUX_SCISSOR_CNTL</i>		<i>MMReg:0x26F0</i>		2-273
<i>CUR_CLR1</i>		<i>MMReg:0x270</i>		2-58
<i>RE_DDA_RHW_0</i>		<i>MMReg:0x2730</i>		2-274
<i>RE_DDA_RHW_1</i>		<i>MMReg:0x2734</i>		2-275
<i>RE_DDA_RHW_2</i>		<i>MMReg:0x2738</i>		2-275
<i>RE_DDA_RHW_3</i>		<i>MMReg:0x273C</i>		2-275
<i>FP_HORZ_VERT_ACTIVE</i>		<i>MMReg:0x278</i>		2-259
<i>CRTC_MORE_CNTL</i>		<i>MMReg:0x27C</i>		2-259
<i>DAC_EXT_CNTL</i>		<i>MMReg:0x280</i>		2-59
<i>FP_GEN_CNTL</i>		<i>MMReg:0x284</i>		2-59
<i>RE_DDA_S3_0</i>		<i>MMReg:0x2880</i>		2-275
<i>RE_DDA_S3_1</i>		<i>MMReg:0x2884</i>		2-275
<i>RE_DDA_S3_2</i>		<i>MMReg:0x2888</i>		2-276
<i>RE_DDA_S3_3</i>		<i>MMReg:0x288C</i>		2-276
<i>RE_DDA_T3_0</i>		<i>MMReg:0x2890</i>		2-276
<i>RE_DDA_T3_1</i>		<i>MMReg:0x2894</i>		2-276
<i>RE_DDA_T3_2</i>		<i>MMReg:0x2898</i>		2-277
<i>RE_DDA_T3_3</i>		<i>MMReg:0x289C</i>		2-277
<i>RE_DDA_Q3_0</i>		<i>MMReg:0x28B0</i>		2-277
<i>RE_DDA_Q3_1</i>		<i>MMReg:0x28B4</i>		2-277
<i>RE_DDA_Q3_2</i>		<i>MMReg:0x28B8</i>		2-277
<i>RE_DDA_Q3_3</i>		<i>MMReg:0x28BC</i>		2-278
<i>FP_HORZ_STRETCH</i>		<i>MMReg:0x28C</i>		2-260
<i>FP_VERT_STRETCH</i>		<i>MMReg:0x290</i>		2-64
<i>TMDS_CNTL</i>		<i>MMReg:0x294</i>		2-105
<i>RE_DDA_DS3_0</i>		<i>MMReg:0x2940</i>		2-278
<i>RE_DDA_DS3_1</i>		<i>MMReg:0x2944</i>		2-278
<i>RE_DDA_DS3_2</i>		<i>MMReg:0x2948</i>		2-278
<i>RE_DDA_DS3_3</i>		<i>MMReg:0x294C</i>		2-278
<i>RE_DDA_DT3_0</i>		<i>MMReg:0x2960</i>		2-279
<i>RE_DDA_DT3_1</i>		<i>MMReg:0x2964</i>		2-279
<i>RE_DDA_DT3_2</i>		<i>MMReg:0x2968</i>		2-279
<i>RE_DDA_DT3_3</i>		<i>MMReg:0x296C</i>		2-279
<i>TMDS_SYNC_CHAR_SETA</i>		<i>MMReg:0x298</i>		2-105
<i>TMDS_SYNC_CHAR_SETB</i>		<i>MMReg:0x29C</i>		2-106
<i>RE_NULL_PRIM</i>		<i>MMReg:0x29E0</i>		2-274
<i>RE_Z_MINMAX_0</i>		<i>MMReg:0x29F0</i>		2-274
<i>RE_Z_MINMAX_1</i>		<i>MMReg:0x29F4</i>		2-274
<i>RE_Z_MINMAX_3</i>		<i>MMReg:0x29FC</i>		2-274
<i>TMDS_CRC</i>		<i>MMReg:0x2A0</i>		2-106
<i>TMDS_TRANSMITTER_CNTL</i>		<i>MMReg:0x2A4</i>		2-106

**Table 2-4 Registers sorted by Address**

<i>Name</i>	<i>I/OAddress</i>	<i>MM Address</i>	<i>Sec Address</i>	<b>Page</b>
<i>TMDS_PLL_CNTL</i>		<i>MMReg:0x2A8</i>		2-107
<i>TMDS_PATTERN_GEN_SEED</i>		<i>MMReg:0x2AC</i>		2-291
<i>FP_H_SYNC_STRT_WID</i>		<i>MMReg:0x2C4</i>		2-65
<i>FP_V_SYNC_STRT_WID</i>		<i>MMReg:0x2C8</i>		2-65
<i>PP_TRI_JUICE</i>		<i>MMReg:0x2D64</i>		2-284
<i>AUX_WINDOW_HORZ_CNTL</i>		<i>MMReg:0x2D8</i>		2-66
<i>AUX_WINDOW_VERT_CNTL</i>		<i>MMReg:0x2DC</i>		2-66
<i>PP_CUBIC_OFFSET_T3_0</i>		<i>MMReg:0x2E28</i>		2-282
<i>PP_CUBIC_OFFSET_T3_1</i>		<i>MMReg:0x2E2C</i>		2-283
<i>PP_CUBIC_OFFSET_T3_2</i>		<i>MMReg:0x2E30</i>		2-283
<i>PP_CUBIC_OFFSET_T3_3</i>		<i>MMReg:0x2E34</i>		2-283
<i>PP_CUBIC_OFFSET_T3_4</i>		<i>MMReg:0x2E38</i>		2-283
<i>GRPH_BUFFER_CNTL</i>		<i>MMReg:0x2F0</i>		2-67
<i>VGA_BUFFER_CNTL</i>		<i>MMReg:0x2F4</i>		2-261
<i>RB2D_ROP</i>		<i>MMReg:0x3400</i>		2-190
<i>RB2D_CLRCMP_SRC</i>		<i>MMReg:0x3408</i>		2-190
<i>RB2D_CLRCMP_DST</i>		<i>MMReg:0x340C</i>		2-190
<i>RB2D_CLRCMP_FLIPE</i>		<i>MMReg:0x3410</i>		2-190
<i>RB2D_CLRCMP_CNTL</i>		<i>MMReg:0x3414</i>		2-191
<i>RB2D_CLRCMP_MSK</i>		<i>MMReg:0x3418</i>		2-191
<i>RB2D_WRITEMASK</i>		<i>MMReg:0x341C</i>		2-192
<i>RB2D_DATATYPE</i>		<i>MMReg:0x3420</i>		2-192
<i>RB2D_GUI_MASTER_CNTL</i>		<i>MMReg:0x3424</i>		2-192
<i>RB2D_DSTCACHE_MODE</i>		<i>MMReg:0x3428</i>		2-284
<i>RB2D_DSTCACHE_CTLSTAT</i>		<i>MMReg:0x342C</i>		2-285
<i>RB2D_SRC_ENDIAN</i>		<i>MMReg:0x3430</i>		2-286
<i>RB2D_DST_ENDIAN</i>		<i>MMReg:0x3434</i>		2-286
<i>RB2D_PD1_DATA</i>		<i>MMReg:0x3438</i>		2-286
<i>RB2D_PD1_ADDR</i>		<i>MMReg:0x343C</i>		2-286
<i>RB2D_WRITEBACK_DATA_LO</i>		<i>MMReg:0x3450</i>		2-287
<i>RB2D_WRITEBACK_DATA_HI</i>		<i>MMReg:0x3454</i>		2-287
<i>RB2D_WRITEBACK_ADDR</i>		<i>MMReg:0x3458</i>		2-287
<i>OV0_Y_X_START</i>		<i>MMReg:0x400</i>		2-68
<i>OV0_Y_X_END</i>		<i>MMReg:0x404</i>		2-68
<i>OV0_PIPELINE_CNTL</i>		<i>MMReg:0x408</i>		2-262
<i>OV0_REG_LOAD_CNTL</i>		<i>MMReg:0x410</i>		2-69
<i>OV0_SCALE_CNTL</i>		<i>MMReg:0x420</i>		2-70
<i>OV0_V_INC</i>		<i>MMReg:0x424</i>		2-72
<i>OV0_P1_V_ACCUM_INIT</i>		<i>MMReg:0x428</i>		2-72
<i>OV0_P23_V_ACCUM_INIT</i>		<i>MMReg:0x42C</i>		2-73
<i>OV0_P1_BLANK_LINES_AT_TO P</i>		<i>MMReg:0x430</i>		2-73
<i>OV0_P23_BLANK_LINES_AT_TO P</i>		<i>MMReg:0x434</i>		2-73
<i>OV0_BASE_ADDR</i>		<i>MMReg:0x43C</i>		2-74

Table 2-4 Registers sorted by Address

<i>Name</i>	<i>I/OAddress</i>	<i>MM Address</i>	<i>Sec Address</i>	<b>Page</b>
<i>OV0_VID_BUF0_BASE_ADRS</i>		<i>MMReg:0x440</i>		2-74
<i>OV0_VID_BUF1_BASE_ADRS</i>		<i>MMReg:0x444</i>		2-75
<i>OV0_VID_BUF2_BASE_ADRS</i>		<i>MMReg:0x448</i>		2-75
<i>OV0_VID_BUF3_BASE_ADRS</i>		<i>MMReg:0x44C</i>		2-75
<i>OV0_VID_BUF4_BASE_ADRS</i>		<i>MMReg:0x450</i>		2-76
<i>OV0_VID_BUF5_BASE_ADRS</i>		<i>MMReg:0x454</i>		2-76
<i>OV0_VID_BUF_PITCH0_VALUE</i>		<i>MMReg:0x460</i>		2-76
<i>OV0_VID_BUF_PITCH1_VALUE</i>		<i>MMReg:0x464</i>		2-77
<i>OV0_AUTO_FLIP_CNTRL</i>		<i>MMReg:0x470</i>		2-77
<i>OV0_DEINTERLACE_PATTERN</i>		<i>MMReg:0x474</i>		2-79
<i>OV0_SUBMIT_HISTORY</i>		<i>MMReg:0x478</i>		2-262
<i>OV0_H_INC</i>		<i>MMReg:0x480</i>		2-80
<i>OV0_STEP_BY</i>		<i>MMReg:0x484</i>		2-80
<i>OV0_P1_H_ACCUM_INIT</i>		<i>MMReg:0x488</i>		2-81
<i>OV0_P23_H_ACCUM_INIT</i>		<i>MMReg:0x48C</i>		2-81
<i>OV0_P1_X_START_END</i>		<i>MMReg:0x494</i>		2-82
<i>OV0_P2_X_START_END</i>		<i>MMReg:0x498</i>		2-82
<i>OV0_P3_X_START_END</i>		<i>MMReg:0x49C</i>		2-82
<i>OV0_FILTER_CNTRL</i>		<i>MMReg:0x4A0</i>		2-83
<i>OV0_FOUR_TAP_COEF_0</i>		<i>MMReg:0x4B0</i>		2-83
<i>OV0_FOUR_TAP_COEF_1</i>		<i>MMReg:0x4B4</i>		2-84
<i>OV0_FOUR_TAP_COEF_2</i>		<i>MMReg:0x4B8</i>		2-84
<i>OV0_FOUR_TAP_COEF_3</i>		<i>MMReg:0x4BC</i>		2-84
<i>OV0_FOUR_TAP_COEF_4</i>		<i>MMReg:0x4C0</i>		2-85
<i>OV0_FLAG_CNTRL</i>		<i>MMReg:0x4DC</i>		2-85
<i>OV0_SLICE_CNTRL</i>		<i>MMReg:0x4E0</i>		2-262
<i>OV0_VID_KEY_CLR_LOW</i>		<i>MMReg:0x4E4</i>		2-85
<i>OV0_VID_KEY_CLR_HIGH</i>		<i>MMReg:0x4E8</i>		2-263
<i>OV0_GRP_KEY_CLR_LOW</i>		<i>MMReg:0x4EC</i>		2-86
<i>OV0_GRP_KEY_CLR_HIGH</i>		<i>MMReg:0x4F0</i>		2-86
<i>OV0_KEY_CNTRL</i>		<i>MMReg:0x4F4</i>		2-86
<i>OV0_TEST</i>		<i>MMReg:0x4F8</i>		2-87
<i>CP_RB_BASE</i>		<i>MMReg:0x700</i>		2-142
<i>CP_RB_CNTRL</i>		<i>MMReg:0x704</i>		2-141
<i>CP_RB_RPTR_ADDR</i>		<i>MMReg:0x70C</i>		2-142
<i>CP_RB_RPTR</i>		<i>MMReg:0x710</i>		2-142
<i>CP_RB_WPTR</i>		<i>MMReg:0x714</i>		2-142
<i>CP_RB_WPTR_DELAY</i>		<i>MMReg:0x718</i>		2-143
<i>CP_IB_BASE</i>		<i>MMReg:0x738</i>		2-143
<i>CP_IB_BUFSZ</i>		<i>MMReg:0x73C</i>		2-143
<i>CP_CSQ_CNTRL</i>		<i>MMReg:0x740</i>		2-143
<i>SCRATCH_UMSK</i>		<i>MMReg:0x770</i>		2-146
<i>SCRATCH_ADDR</i>		<i>MMReg:0x774</i>		2-146
<i>DMA_GUI_TABLE_ADDR</i>		<i>MMReg:0x780</i>		2-146

Table 2-4 Registers sorted by Address

<i>Name</i>	<i>I/OAddress</i>	<i>MM Address</i>	<i>Sec Address</i>	<b>Page</b>
<a href="#">DMA_GUI_SRC_ADDR</a>		MMReg:0x784		2-147
<a href="#">DMA_GUI_DST_ADDR</a>		MMReg:0x788		2-147
<a href="#">DMA_GUI_COMMAND</a>		MMReg:0x78C		2-147
<a href="#">DMA_GUI_STATUS</a>		MMReg:0x790		2-148
<a href="#">DMA_GUI_ACT_DSCRPTR</a>		MMReg:0x794		2-149
<a href="#">DMA_VID_TABLE_ADDR</a>		MMReg:0x7A0		2-149
<a href="#">DMA_VID_SRC_ADDR</a>		MMReg:0x7A4		2-149
<a href="#">DMA_VID_DST_ADDR</a>		MMReg:0x7A8		2-150
<a href="#">DMA_VID_COMMAND</a>		MMReg:0x7AC		2-150
<a href="#">DMA_VID_STATUS</a>		MMReg:0x7B0		2-151
<a href="#">DMA_VID_ACT_DSCRPTR</a>		MMReg:0x7B4		2-151
<a href="#">CP_STAT</a>		MMReg:0x7C0		2-272
<a href="#">CP_ME_CNTL</a>		MMReg:0x7D0		2-152
<a href="#">CP_ME_RAM_ADDR</a>		MMReg:0x7D4		2-153
<a href="#">CP_ME_RAM_RADDR</a>		MMReg:0x7D8		2-153
<a href="#">CP_ME_RAM_DATAH</a>		MMReg:0x7DC		2-153
<a href="#">CP_ME_RAM_DATAH</a>		MMReg:0x7E0		2-154
<a href="#">CP_CSQ_ADDR</a>		MMReg:0x7F0		2-152
<a href="#">CP_CSQ_DATA</a>		MMReg:0x7F4		2-152
<a href="#">CP_CSQ_STAT</a>		MMReg:0x7F8		2-152
<a href="#">VID_BUFFER_CONTROL</a>		MMReg:0x900		2-128
<a href="#">CAP_INT_CNTL</a>		MMReg:0x908		2-129
<a href="#">CAP_INT_STATUS</a>		MMReg:0x90C		2-130
<a href="#">FCP_CNTL</a>		MMReg:0x910		2-117
<a href="#">FCP_CNTL</a>		MMReg:0x910		2-118
<a href="#">CAPO_BUF0_OFFSET</a>		MMReg:0x920		2-120
<a href="#">CAPO_BUF1_OFFSET</a>		MMReg:0x924		2-121
<a href="#">CAPO_BUF0_EVEN_OFFSET</a>		MMReg:0x928		2-121
<a href="#">CAPO_BUF1_EVEN_OFFSET</a>		MMReg:0x92C		2-121
<a href="#">CAPO_BUF_PITCH</a>		MMReg:0x930		2-121
<a href="#">CAPO_V_WINDOW</a>		MMReg:0x934		2-121
<a href="#">CAPO_H_WINDOW</a>		MMReg:0x938		2-122
<a href="#">CAPO_VBIO_OFFSET</a>		MMReg:0x93C		2-122
<a href="#">CAPO_VBII_OFFSET</a>		MMReg:0x940		2-122
<a href="#">CAPO_VBI_V_WINDOW</a>		MMReg:0x944		2-122
<a href="#">CAPO_VBI_H_WINDOW</a>		MMReg:0x948		2-123
<a href="#">CAPO_PORT_MODE_CNTL</a>		MMReg:0x94C		2-123
<a href="#">CAPO_TRIG_CNTL</a>		MMReg:0x950		2-123
<a href="#">CAPO_DEBUG</a>		MMReg:0x954		2-124
<a href="#">CAPO_CONFIG</a>		MMReg:0x958		2-124
<a href="#">CAPO_ANC0_OFFSET</a>		MMReg:0x95C		2-126
<a href="#">CAPO_ANC1_OFFSET</a>		MMReg:0x960		2-126
<a href="#">CAPO_ANC_H_WINDOW</a>		MMReg:0x964		2-126
<a href="#">CAPO_VIDEO_SYNC_TEST</a>		MMReg:0x968		2-126
<a href="#">CAPO_ONESHOT_BUF_OFFSET</a>		MMReg:0x96C		2-127

Table 2-4 Registers sorted by Address

Name	I/OAddress	MM Address	Sec Address	Page
CAPO_BUF_STATUS		MMReg:0x970		2-127
CAPO_ANC_BUF01_BLOCK_CN T		MMReg:0x974		2-291
CAPO_ANC_BUF23_BLOCK_CN T		MMReg:0x97C		2-291
CAPO_VBI2_OFFSET		MMReg:0x980		2-128
CAPO_VBI3_OFFSET		MMReg:0x984		2-128
CAPO_ANC2_OFFSET		MMReg:0x988		2-128
CAPO_ANC3_OFFSET		MMReg:0x98C		2-128
DMA_VIPH0_COMMAND		MMReg:0xA00		2-133
DMA_VIPH1_COMMAND		MMReg:0xA04		2-133
DMA_VIPH2_COMMAND		MMReg:0xA08		2-134
DMA_VIPH3_COMMAND		MMReg:0xA0C		2-135
DMA_VIPH_STATUS		MMReg:0xA10		2-136
DMA_VIPH_CHUNK_0		MMReg:0xA18		2-136
DMA_VIPH_CHUNK_1_VAL		MMReg:0xA1C		2-137
DMA_VIP0_TABLE_ADDR		MMReg:0xA20		2-137
DMA_VIPH0_ACTIVE		MMReg:0xA24		2-138
DMA_VIP1_TABLE_ADDR		MMReg:0xA30		2-138
DMA_VIPH1_ACTIVE		MMReg:0xA34		2-138
DMA_VIP2_TABLE_ADDR		MMReg:0xA40		2-138
DMA_VIPH2_ACTIVE		MMReg:0xA44		2-139
DMA_VIP3_TABLE_ADDR		MMReg:0xA50		2-138
DMA_VIPH3_ACTIVE		MMReg:0xA54		2-139
DMA_VIPH_ABORT		MMReg:0xA88		2-139
SURFACE_CNTL		MMReg:0xB00		2-22
SURFACE0_LOWER_BOUND		MMReg:0xB04		2-23
SURFACE0_UPPER_BOUND		MMReg:0xB08		2-23
SURFACE0_INFO		MMReg:0xB0C		2-22
SURFACE1_LOWER_BOUND		MMReg:0xB14		2-24
SURFACE1_UPPER_BOUND		MMReg:0xB18		2-25
SURFACE1_INFO		MMReg:0xB1C		2-24
SURFACE2_LOWER_BOUND		MMReg:0xB24		2-26
SURFACE2_UPPER_BOUND		MMReg:0xB28		2-26
SURFACE2_INFO		MMReg:0xB2C		2-25
SURFACE3_LOWER_BOUND		MMReg:0xB34		2-27
SURFACE3_UPPER_BOUND		MMReg:0xB38		2-27
SURFACE3_INFO		MMReg:0xB3C		2-26
SURFACE4_LOWER_BOUND		MMReg:0xB44		2-28
SURFACE4_UPPER_BOUND		MMReg:0xB48		2-28
SURFACE4_INFO		MMReg:0xB4C		2-27
SURFACE5_LOWER_BOUND		MMReg:0xB54		2-29
SURFACE5_UPPER_BOUND		MMReg:0xB58		2-30
SURFACE5_INFO		MMReg:0xB5C		2-29
SURFACE6_LOWER_BOUND		MMReg:0xB64		2-31

Table 2-4 Registers sorted by Address

<i>Name</i>	<i>I/OAddress</i>	<i>MM Address</i>	<i>Sec Address</i>	<b>Page</b>
<i>SURFACE6_UPPER_BOUND</i>		<i>MMReg:0xB68</i>		2-31
<i>SURFACE6_INFO</i>		<i>MMReg:0xB6C</i>		2-30
<i>SURFACE7_LOWER_BOUND</i>		<i>MMReg:0xB74</i>		2-32
<i>SURFACE7_UPPER_BOUND</i>		<i>MMReg:0xB78</i>		2-32
<i>SURFACE7_INFO</i>		<i>MMReg:0xB7C</i>		2-31
<i>SURFACE_ACCESS_FLAGS</i>		<i>MMReg:0xBF8</i>		2-254
<i>SURFACE_ACCESS_CLR</i>		<i>MMReg:0xBFC</i>		2-255
<i>VIPH_CH0_DATA</i>		<i>MMReg:0xC00</i>		2-110
<i>VIPH_CH1_DATA</i>		<i>MMReg:0xC04</i>		2-110
<i>VIPH_CH2_DATA</i>		<i>MMReg:0xC08</i>		2-110
<i>VIPH_CH3_DATA</i>		<i>MMReg:0xC0C</i>		2-110
<i>VIPH_CH0_ADDR</i>		<i>MMReg:0xC10</i>		2-110
<i>VIPH_CH1_ADDR</i>		<i>MMReg:0xC14</i>		2-111
<i>VIPH_CH2_ADDR</i>		<i>MMReg:0xC18</i>		2-111
<i>VIPH_CH3_ADDR</i>		<i>MMReg:0xC1C</i>		2-111
<i>VIPH_CH0_SBCNT</i>		<i>MMReg:0xC20</i>		2-111
<i>VIPH_CH1_SBCNT</i>		<i>MMReg:0xC24</i>		2-112
<i>VIPH_CH2_SBCNT</i>		<i>MMReg:0xC28</i>		2-112
<i>VIPH_CH3_SBCNT</i>		<i>MMReg:0xC2C</i>		2-112
<i>VIPH_CH0_ABCNT</i>		<i>MMReg:0xC30</i>		2-112
<i>VIPH_CH1_ABCNT</i>		<i>MMReg:0xC34</i>		2-112
<i>VIPH_CH2_ABCNT</i>		<i>MMReg:0xC38</i>		2-113
<i>VIPH_CH3_ABCNT</i>		<i>MMReg:0xC3C</i>		2-113
<i>VIPH_CONTROL</i>		<i>MMReg:0xC40</i>		2-113
<i>VIPH_DV_LAT</i>		<i>MMReg:0xC44</i>		2-114
<i>VIPH_DMA_CHUNK</i>		<i>MMReg:0xC48</i>		2-114
<i>VIPH_DV_INT</i>		<i>MMReg:0xC4C</i>		2-115
<i>VIPH_TIMEOUT_STAT</i>		<i>MMReg:0xC50</i>		2-115
<i>DISP_MISC_CNTL</i>		<i>MMReg:0xD00</i>		2-88
<i>DAC_MACRO_CNTL</i>		<i>MMReg:0xD04</i>		2-88
<i>DISP_PWR_MAN</i>		<i>MMReg:0xD08</i>		2-263
<i>DISP_TEST_DEBUG_CNTL</i>		<i>MMReg:0xD10</i>		2-89
<i>DISP_HW_DEBUG</i>		<i>MMReg:0xD14</i>		2-90
<i>DAC_CRC_SIG1</i>		<i>MMReg:0xD18</i>		2-91
<i>DAC_CRC_SIG2</i>		<i>MMReg:0xD1C</i>		2-91
<i>OV0_LIN_TRANS_A</i>		<i>MMReg:0xD20</i>		2-92
<i>OV0_LIN_TRANS_B</i>		<i>MMReg:0xD24</i>		2-92
<i>OV0_LIN_TRANS_C</i>		<i>MMReg:0xD28</i>		2-92
<i>OV0_LIN_TRANS_D</i>		<i>MMReg:0xD2C</i>		2-93
<i>OV0_LIN_TRANS_E</i>		<i>MMReg:0xD30</i>		2-93
<i>OV0_LIN_TRANS_F</i>		<i>MMReg:0xD34</i>		2-93
<i>OV0_GAMMA_0_F</i>		<i>MMReg:0xD40</i>		2-93
<i>OV0_GAMMA_10_1F</i>		<i>MMReg:0xD44</i>		2-94
<i>OV0_GAMMA_20_3F</i>		<i>MMReg:0xD48</i>		2-94
<i>OV0_GAMMA_40_7F</i>		<i>MMReg:0xD4C</i>		2-94

Table 2-4 Registers sorted by Address

<i>Name</i>	<i>I/OAddress</i>	<i>MM Address</i>	<i>Sec Address</i>	<b>Page</b>
<i>OV0_GAMMA_380_3BF</i>		<i>MMReg:0xD50</i>		2-95
<i>OV0_GAMMA_3C0_3FF</i>		<i>MMReg:0xD54</i>		2-95
<i>DISP_MERGE_CNTL</i>		<i>MMReg:0xD60</i>		2-95
<i>DISP_OUTPUT_CNTL</i>		<i>MMReg:0xD64</i>		2-97
<i>DISP_LIN_TRANS_GRP_H_A</i>		<i>MMReg:0xD80</i>		2-100
<i>DISP_LIN_TRANS_GRP_H_B</i>		<i>MMReg:0xD84</i>		2-100
<i>DISP_LIN_TRANS_GRP_H_C</i>		<i>MMReg:0xD88</i>		2-100
<i>DISP_LIN_TRANS_GRP_H_D</i>		<i>MMReg:0xD8C</i>		2-100
<i>DISP_LIN_TRANS_GRP_H_E</i>		<i>MMReg:0xD90</i>		2-101
<i>DISP_LIN_TRANS_GRP_H_F</i>		<i>MMReg:0xD94</i>		2-101
<i>DISP_LIN_TRANS_VID_A</i>		<i>MMReg:0xD98</i>		2-101
<i>DISP_LIN_TRANS_VID_B</i>		<i>MMReg:0xD9C</i>		2-101
<i>DISP_LIN_TRANS_VID_C</i>		<i>MMReg:0xDA0</i>		2-102
<i>DISP_LIN_TRANS_VID_D</i>		<i>MMReg:0xDA4</i>		2-102
<i>DISP_LIN_TRANS_VID_E</i>		<i>MMReg:0xDA8</i>		2-102
<i>DISP_LIN_TRANS_VID_F</i>		<i>MMReg:0xDAC</i>		2-102
<i>RMX_HORZ_FILTER_0TAP_COEF</i>		<i>MMReg:0xDB0</i>		2-103
<i>RMX_HORZ_FILTER_1TAP_COEF</i>		<i>MMReg:0xDB4</i>		2-103
<i>RMX_HORZ_FILTER_2TAP_COEF</i>		<i>MMReg:0xDB8</i>		2-103
<i>RMX_HORZ_PHASE</i>		<i>MMReg:0xDBC</i>		2-104
<i>DAC_EMBEDDED_SYNC_CNTL</i>		<i>MMReg:0xDC0</i>		2-264
<i>DAC_BROAD_PULSE</i>		<i>MMReg:0xDC4</i>		2-264
<i>DAC_SKEW_CLKS</i>		<i>MMReg:0xDC8</i>		2-264
<i>DAC_INCR</i>		<i>MMReg:0xDCC</i>		2-265
<i>DAC_NEG_SYNC_LEVEL</i>		<i>MMReg:0xDD0</i>		2-265
<i>DAC_POS_SYNC_LEVEL</i>		<i>MMReg:0xDD4</i>		2-265
<i>DAC_BLANK_LEVEL</i>		<i>MMReg:0xDD8</i>		2-265
<i>RBBM_STATUS</i>		<i>MMReg:0xE40</i>	<i>MMReg:0x1740</i>	2-7
<i>NQWAIT_UNTIL</i>		<i>MMReg:0xE50</i>		2-10
<i>RBBM_CMDFIFO_ADDR</i>		<i>MMReg:0xE70</i>		2-11
<i>RBBM_CMDFIFO_DATA_L</i>		<i>MMReg:0xE74</i>		2-12
<i>RBBM_CMDFIFO_DATA_H</i>		<i>MMReg:0xE78</i>		2-12
<i>RBBM_CMDFIFO_STAT</i>		<i>MMReg:0xE7C</i>		2-12



# Appendix B

## *Revision History*

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### **B.1 Rev 0.01**

This document is based on the engineering RAGE 6 register specification rev 1.66 (Mar 22, 2000).

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