



# Radeon 7500 Register Reference

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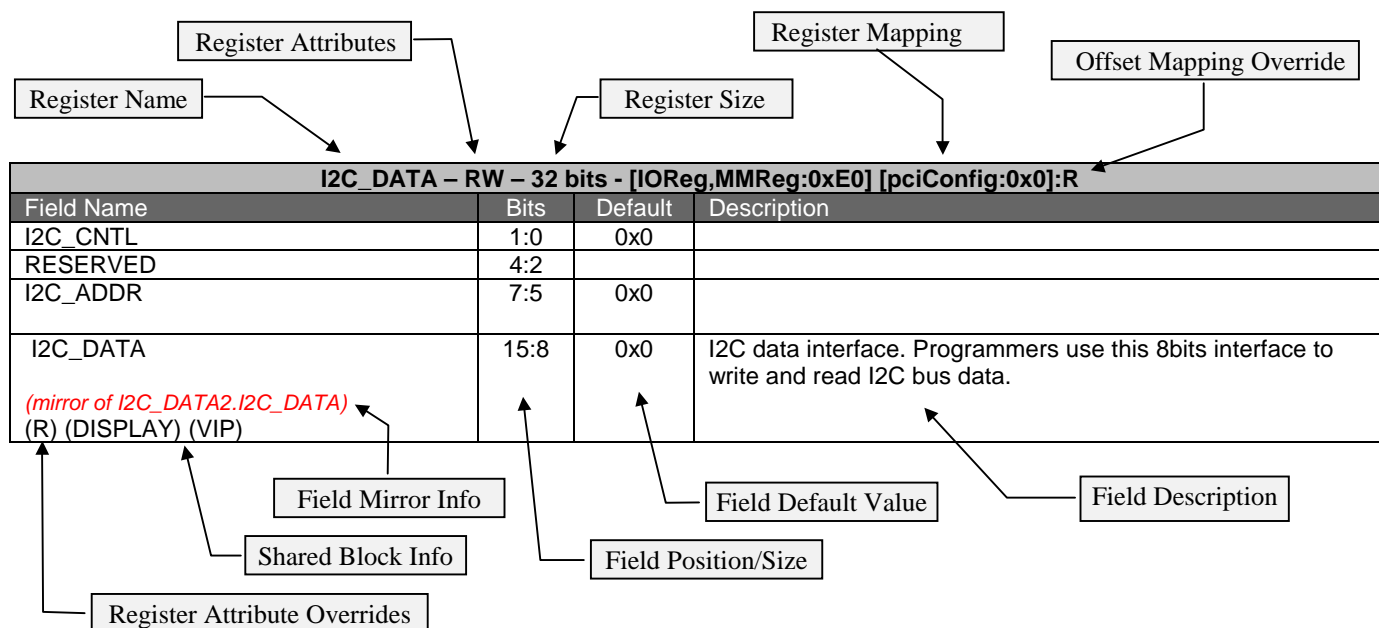
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## 0. Introduction

This document contains register specification for all registers in the morpheus chip. The registers are grouped by functions. Any registers that are not grouped in a function will be listed under 'Miscellaneous'.

### 0.1 Register Table Heading Notations



### Field Explanation:

1. Register Name – Name of the register.
2. Register Attributes – R:Readable; W:Writable
3. Register Mapping – Aperture/Decode the register is mapped to
  - [aperName:offset] – single mapping, to one aperture/decode and one offset
  - [aperName1, aperName2, ..., aperNameN:offset] – multiple mappings to different apertures/decodes but same offset
  - [aperName:startOffset-endOffset] – mapped to an offset range in the same aperture/decode
4. Register Mapping Override – R/W attribute of register is override by the preceding mapping.
5. Register Size – Size of the register in bits.
6. Field Name – Name of fields in the register.
7. Field Position/Size – Field position and size.
8. Field Default Value – The default value of the field when the chip first loads.
9. Field Description –Description of the field.
10. Field Mirror Info – If the field is mirrored, this indicates the register and field the specified field is mirrored to.
11. Share Block Info – If the register is a shared register, this indicates which block the specified field is shared in. (Only in chip level register specification documents)
12. Register Attribute Overrides – If the field R/W attributes have been overridden.

### Note:

1. A 'RESERVED' field indicates the value for that field is undetermined and must not be relied upon.

**1. CFG Detailed Register Reference**

## PCI Configuration Registers

**DEVICE\_ID - R - 16 bits - [MMReg:0xF02] [pciConfig:0x2]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| DEVICE_ID  | 15:0 | 0x5157  |             |

No description available for this register.

**VENDOR\_ID - R - 16 bits - [MMReg:0xF00] [pciConfig:0x0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| VENDOR_ID  | 15:0 | 0x1002  |             |

No description available for this register.

**COMMAND - RW - 16 bits - [MMReg:0xF04]:R [pciConfig:0x4]**

| Field Name                  | Bits | Default | Description           |
|-----------------------------|------|---------|-----------------------|
| IO_ACCESS_EN                | 0    | 0x0     | 0=Disable<br>1=Enable |
| MEM_ACCESS_EN               | 1    | 0x0     | 0=Disable<br>1=Enable |
| BUS_MASTER_EN               | 2    | 0x0     | 0=Disable<br>1=Enable |
| SPECIAL_CYCLE_EN (R)        | 3    | 0x0     | 0=Disable<br>1=Enable |
| MEM_WRITE_INVALIDATE_EN (R) | 4    | 0x0     | 0=Disable<br>1=Enable |
| PAL_SNOOP_EN                | 5    | 0x0     | 0=Disable<br>1=Enable |
| PARITY_ERROR_EN (R)         | 6    | 0x0     | 0=Disable<br>1=Enable |
| AD_STEPPING (R)             | 7    | 0x1     | 0=Disable<br>1=Enable |
| SERR_EN                     | 8    | 0x0     | 0=Disable<br>1=Enable |
| FAST_B2B_EN                 | 9    | 0x0     | 0=Disable<br>1=Enable |

No description available for this register.

**STATUS - RW - 16 bits - [MMReg:0xF06]:R [pciConfig:0x6]**

| Field Name              | Bits | Default | Description           |
|-------------------------|------|---------|-----------------------|
| CAP_LIST (R)            | 4    | 0x1     |                       |
| PCI_66_EN (R)           | 5    | 0x1     |                       |
| UDF_EN (R)              | 6    | 0x0     | 0=Disable<br>1=Enable |
| FAST_BACK_CAPABLE (R)   | 7    | 0x1     |                       |
| DEVSEL_TIMING (R)       | 10:9 | 0x1     |                       |
| SIGNAL_TARGET_ABORT (R) | 11   | 0x0     |                       |

**STATUS - RW - 16 bits - [MMReg:0xF06]:R [pciConfig:0x6]**

| Field Name                | Bits | Default | Description            |
|---------------------------|------|---------|------------------------|
| RECEIVED_TARGET_ABORT     | 12   | 0x0     | 0=Inactive<br>1=Active |
| RECEIVED_MASTER_ABORT     | 13   | 0x0     | 0=Inactive<br>1=Active |
| SIGNALLED_SYSTEM_ERROR    | 14   | 0x0     |                        |
| PARITY_ERROR_DETECTED (R) | 15   | 0x0     |                        |

No description available for this register.

**REVISION\_ID - R - 8 bits - [MMReg:0xF08] [pciConfig:0x8]**

| Field Name   | Bits | Default | Description |
|--------------|------|---------|-------------|
| MINOR_REV_ID | 3:0  | 0x0     |             |
| MAJOR_REV_ID | 7:4  | 0x0     |             |

No description available for this register.

**IO\_BASE - RW - 32 bits - [MMReg:0xF14]:R [pciConfig:0x14]**

| Field Name       | Bits | Default | Description |
|------------------|------|---------|-------------|
| BLOCK_IO_BIT (R) | 7:0  | 0x1     |             |
| IO_BASE          | 31:8 | 0x0     |             |

No description available for this register.

**REG\_BASE - RW - 32 bits - [MMReg:0xF18]:R [pciConfig:0x18]**

| Field Name | Bits  | Default | Description |
|------------|-------|---------|-------------|
| REG_BASE   | 31:16 | 0x0     |             |

No description available for this register.

**MEM\_BASE - RW - 32 bits - [MMReg:0xF10]:R [pciConfig:0x10]**

| Field Name      | Bits  | Default | Description |
|-----------------|-------|---------|-------------|
| PREFETCH_EN (R) | 3     | 0x1     |             |
| MEM_BASE        | 31:25 | 0x0     |             |

No description available for this register.

**ADAPTER\_ID\_W - RW - 32 bits - [MMReg:0xF4C]:R [pciConfig:0x4C]**

| Field Name          | Bits  | Default | Description |
|---------------------|-------|---------|-------------|
| SUBSYSTEM_VENDOR_ID | 15:0  | 0x0     |             |
| SUBSYSTEM_ID        | 31:16 | 0x0     |             |

No description available for this register.

**BASE\_CODE - R - 8 bits - [MMReg:0xF0B] [pciConfig:0xB]**

| Field Name      | Bits | Default | Description |
|-----------------|------|---------|-------------|
| BASE_CLASS_CODE | 7:0  | 0x3     |             |

No description available for this register.

**ADAPTER\_ID - R - 32 bits - [MMReg:0xF2C] [pciConfig:0x2C]**

| Field Name  | Bits | Default | Description |
|---|------|---------|-------------|
| SUBSYSTEM_VENDOR_ID                                     | 15:0 | 0x0     |             |
| <i>(mirror of<br/>ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)</i> |      |         |             |

**ADAPTER\_ID - R - 32 bits - [MMReg:0xF2C] [pciConfig:0x2C]**

| Field Name   | Bits  | Default | Description |
|--------------|-------|---------|-------------|
| SUBSYSTEM_ID | 31:16 | 0x0     |             |

*(mirror of ADAPTER\_ID\_W:SUBSYSTEM\_ID)*

No description available for this register.

**BIOS\_ROM - RW - 32 bits - [MMReg:0xF30]:R [pciConfig:0x30]**

| Field Name     | Bits  | Default | Description           |
|----------------|-------|---------|-----------------------|
| BIOS_ROM_EN    | 0     | 0x0     | 0=Disable<br>1=Enable |
| BIOS_BASE_ADDR | 31:17 | 0x0     |                       |

No description available for this register.

**SUB\_CLASS - R - 8 bits - [MMReg:0xF0A] [pciConfig:0xA]**

| Field Name    | Bits | Default | Description                                   |
|---------------|------|---------|---|
| SUB_CLASS_INF | 7    | 0x0     | 0=00 - VGA device<br>1=80 - extended graphics |

No description available for this register.

**BIST - R - 8 bits - [MMReg:0xF0F] [pciConfig:0xF]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BIST_COMP  | 3:0  | 0x0     |             |
| BIST_STRT  | 6    | 0x0     |             |
| BIST_CAP   | 7    | 0x0     |             |

No description available for this register.

**CAPABILITIES\_PTR - R - 32 bits - [MMReg:0xF34] [pciConfig:0x34]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| CAP_PTR    | 7:0  | 0x50    |             |

No description available for this register.

**CONFIG\_CNTL - RW - 32 bits - [IOReg,MMReg:0xE0]**

| Field Name                             | Bits  | Default | Description           |
|--|-------|---------|-----------------------|
| APER_REG_ENDIAN                        | 5:4   | 0x0     |                       |
| CFG_VGA_RAM_EN                         | 8     | 0x0     | 0=Disable<br>1=Enable |
| <i>(mirror of GENMO_WT:VGA_RAM_EN)</i> |       |         |                       |
| CFG_VGA_IO_DIS                         | 9     | 0x0     |                       |
| CFG_ATI_REV_ID (R)                     | 19:16 | 0x0     |                       |

No description available for this register.

**CONFIG\_MEMSIZE - RW - 32 bits - [IOReg,MMReg:0xF8]**

| Field Name     | Bits  | Default | Description |
|----------------|-------|---------|-------------|
| CONFIG_MEMSIZE | 28:24 | 0x0     |             |

No description available for this register.

**CONFIG\_APER\_0\_BASE - R - 32 bits - [MMReg:0x100]**

| Field Name  | Bits  | Default | Description |
|-------------|-------|---------|-------------|
| APER_0_BASE | 31:25 | 0x0     |             |

No description available for this register.

**CONFIG\_APER\_1\_BASE - R - 32 bits - [MMReg:0x104]**

| Field Name  | Bits  | Default | Description |
|-------------|-------|---------|-------------|
| APER_1_BASE | 31:24 | 0x0     |             |

No description available for this register.

**CONFIG\_APER\_SIZE - R - 32 bits - [MMReg:0x108]**

| Field Name | Bits  | Default | Description |
|------------|-------|---------|-------------|
| APER_SIZE  | 27:24 | 0x0     |             |

No description available for this register.

**CONFIG\_REG\_1\_BASE - R - 32 bits - [MMReg:0x10C]**

| Field Name        | Bits  | Default | Description |
|-------------------|-------|---------|-------------|
| REG_APER_1_SELECT | 15    | 0x1     |             |
| REG_1_BASE        | 31:16 | 0x0     |             |

No description available for this register.

**CONFIG\_REG\_APER\_SIZE - R - 32 bits - [MMReg:0x110]**

| Field Name    | Bits | Default | Description |
|---------------|------|---------|-------------|
| REG_APER_SIZE | 15:0 | 0x8000  |             |

No description available for this register.

**HEADER - R - 8 bits - [MMReg:0xF0E] [pciConfig:0xE]**

| Field Name  | Bits | Default | Description   |
|-------------|------|---------|---|
| HEADER_TYPE | 6:0  | 0x0     |   |
| DEVICE_TYPE | 7    | 0x0     | 0=Single-Function Device<br>1=Multi-Function Device |

No description available for this register.

**INTERRUPT\_LINE - RW - 8 bits - [MMReg:0xF3C]:R [pciConfig:0x3C]**

| Field Name     | Bits | Default | Description |
|----------------|------|---------|-------------|
| INTERRUPT_LINE | 7:0  | 0xff    |             |

No description available for this register.

**INTERRUPT\_PIN - R - 8 bits - [MMReg:0xF3D] [pciConfig:0x3D]**

| Field Name    | Bits | Default | Description |
|---------------|------|---------|-------------|
| INTERRUPT_PIN | 0    | 0x0     |             |

No description available for this register.

**LATENCY - RW - 8 bits - [MMReg:0xF0D]:R [pciConfig:0xD]**

| Field Name    | Bits | Default | Description |
|---------------|------|---------|-------------|
| LATENCY_TIMER | 7:0  | 0x0     |             |

No description available for this register.

**MAX\_LATENCY - R - 8 bits - [MMReg:0xF3F] [pciConfig:0x3F]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| MAX_LAT    | 7:0  | 0x0     |             |

No description available for this register.

**REGPROG\_INF - R - 8 bits - [MMReg:0xF09] [pciConfig:0x9]**



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| Field Name         | Bits | Default | Description |
|--------------------|------|---------|-------------|
| REG_LEVEL_PROG_INF | 7:0  | 0x0     |             |

No description available for this register.

**CACHE\_LINE - RW - 8 bits - [MMReg:0xF0C]:R [pciConfig:0xC]**

| Field Name      | Bits | Default | Description |
|-----------------|------|---------|-------------|
| CACHE_LINE_SIZE | 7:0  | 0x0     |             |

No description available for this register.

**MIN\_GRANT - R - 8 bits - [MMReg:0xF3E] [pciConfig:0x3E]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| MIN_GNT    | 7:0  | 0x8     |             |

Miscellaneous Output Register (Write)

**2. busControl Detailed Register Reference**

## Bus Interface Registers

| <b>BUS_CNTL - RW - 32 bits - [IOReg,MMReg:0x30]</b> |             |                |  |
|---|-------------|----------------|--|
| <b>Field Name</b>                                   | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| BUS_DBL_RESYNC                                      | 0           | 0x1            | 0=Normal<br>1=Add extra resynchronizing clock  |
| BUS_MSTR_RESET (W)                                  | 1           | 0x0            | 0=Normal<br>1=Reset  |
| BUS_FLUSH_BUF (W)                                   | 2           | 0x0            | 0=Normal<br>1=Flush  |
| BUS_STOP_REQ_DIS                                    | 3           | 0x0            | 0=Normal<br>1=Disable  |
| BUS_READ_COMBINE_EN                                 | 4           | 0x0            | 0=Disable<br>1=Enable  |
| BUS_WRT_COMBINE_EN                                  | 5           | 0x0            | 0=Disable<br>1=Enable  |
| BUS_MASTER_DIS                                      | 6           | 0x1            | 0=Enable<br>1=Disable  |
| BIOS_ROM_WRT_EN                                     | 7           | 0x0            | 0=Disable<br>1=Enable  |
| BUS_PREFETCH_MODE                                   | 9:8         | 0x0            | 0=HI prefetching disabled<br>1=HI prefetches during active bus requests only<br>2=HI always prefetches continuously<br>3=HI attempts to hold 1 DW of read data for a delayed read completion |
| BUS_VGA_PREFETCH_EN                                 | 10          | 0x0            | 0=Disable<br>1=Enable  |
| BUS_SGL_READ_DISABLE                                | 11          | 0x0            | 0=Enable<br>1=Disable  |
| BIOS_DIS_ROM  | 12          | 0x0            | 0=Enable<br>1=Disable  |
| BUS_PCI_READ_RETRY_EN                               | 13          | 0x0            | 0=Normal<br>1=Enable   |
| BUS_AGP_AD_STEPPING_EN                              | 14          | 0x1            | 0=No stepping in AGP<br>1=AD Stepping in AGP and PCI   |
| BUS_PCI_WRT_RETRY_EN                                | 15          | 0x0            | 0=Normal<br>1=Enable   |
| BUS_RETRY_WS  | 19:16       | 0xf            |  |
| BUS_MSTR_RD_MULT                                    | 20          | 0x0            | 0=Read line<br>1=Read multiple   |
| BUS_MSTR_RD_LINE                                    | 21          | 0x0            | 0=Read multiple<br>1=Read line   |

**BUS\_CNTL - RW - 32 bits - [IOReg,MMReg:0x30]**

| Field Name             | Bits | Default | Description                                   |
|------------------------|------|---------|---|
| BUS_SUSPEND            | 22   | 0x0     | 0=Resume BM transfer<br>1=Suspend BM transfer |
| LAT_16X                | 23   | 0x0     | 0=1X<br>1=16X                                 |
| BUS_RD_DISCARD_EN      | 24   | 0x0     | 0=Disable<br>1=Enable                         |
| ENFRWCWRDY             | 25   | 0x0     | 0=Disable<br>1=Enable                         |
| BUS_MSTR_WS            | 26   | 0x0     | 0=8 wait states<br>1=32 wait states           |
| BUS_PARKING_DIS        | 27   | 0x1     | 0=Enable<br>1=Disable                         |
| BUS_MSTR_DISCONNECT_EN | 28   | 0x0     | 0=Disable<br>1=Enable                         |
| SERR_EN                | 29   | 0x0     | 0=Disable<br>1=Enable                         |
| BUS_READ_BURST         | 30   | 0x0     | 0=Disable<br>1=Enable                         |
| BUS_RDY_READ_DLY       | 31   | 0x1     | 0=no RDY delay<br>1=RDY delayed 1 mem clk     |

No description available for this register.

**BUS\_CNTL1 - RW - 32 bits - [IOReg,MMReg:0x34]**

| Field Name                           | Bits | Default | Description           |
|--------------------------------------|------|---------|-----------------------|
| PMI_IO_DISABLE                       | 0    | 0x0     | 0=Normal<br>1=Disable |
| PMI_MEM_DISABLE                      | 1    | 0x0     | 0=Normal<br>1=Disable |
| PMI_BM_DISABLE                       | 2    | 0x0     | 0=Normal<br>1=Disable |
| PMI_INT_DISABLE                      | 3    | 0x0     | 0=Normal<br>1=Disable |
| BUS2_IMMEDIATE_PMI_DISABLE           | 5    | 0x0     |                       |
| BUS2_VGA_REG_COHERENCY_DIS           | 8    | 0x0     | 0=Enable<br>1=Disable |
| BUS2_VGA_MEM_COHERENCY_DIS           | 9    | 0x0     | 0=Enable<br>1=Disable |
| BUS2_HDP_REG_COHERENCY_DIS           | 10   | 0x0     | 0=Enable<br>1=Disable |
| BUS2_GUI_INITIATOR_COHERENCY_D<br>IS | 11   | 0x0     | 0=Enable<br>1=Disable |

**BUS\_CNTL1 - RW - 32 bits - [IOReg,MMReg:0x34]**

| Field Name          | Bits  | Default | Description   |
|---------------------|-------|---------|---|
| MOBILE_PLATFORM_SEL | 27:26 | 0x0     | graphic chip selects which mobile platform it is supporting<br>0=Do not choose any mobile platform<br>1=Solano2-M platform<br>2=440BX platform<br>3=Do not choose any mobile platform |
| SEND_SBA_LATENCY    | 30:28 | 0x0     | defines delay to send SBA again after STP_AGP# is de-asserted<br>0=50us<br>1=60us<br>2=70us<br>3=80us<br>4=100us<br>5=200us<br>6=400us<br>7=800us                                     |
| AGPCLK_VALID        | 31    | 0x0     | defines which signal indicates AGP clock is valid<br>0=AGP clock do not stop<br>1=use SUS_STAT# to indicate AGP clock is valid  |

Miscellaneous Output Register (Write)

**HI\_STAT - R - 32 bits - [IOReg,MMReg:0x4C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| AGP_BUSY   | 3    | 0x0     |             |

No description available for this register.

**BM\_STATUS - R - 32 bits - [MMReg:0x160]**

| Field Name        | Bits | Default | Description |
|-------------------|------|---------|-------------|
| BUS_MASTER_STATUS | 31:0 | 0x0     |             |

No description available for this register.

**AGP\_COMMAND - RW - 32 bits - [MMReg:0xF60]:R [pciConfig:0x60]**

| Field Name | Bits  | Default | Description           |
|------------|-------|---------|-----------------------|
| DATA_RATE  | 2:0   | 0x0     |                       |
| AGP_EN     | 8     | 0x0     | 0=disable<br>1=enable |
| SBA_EN (R) | 9     | 0x1     | 0=Disable<br>1=Enable |
| RQ_DEPTH   | 31:24 | 0x0     |                       |

No description available for this register.

**AGP\_CNTL - RW - 32 bits - [MMReg:0x174]**

| Field Name          | Bits | Default | Description |
|---------------------|------|---------|-------------|
| MAX_IDLE_CLK        | 7:0  | 0x0     |             |
| HOLD_RD_FIFO        | 8    | 0x0     |             |
| HOLD_RQ_FIFO        | 9    | 0x0     |             |
| EN_2X_STBB          | 10   | 0x0     |             |
| FORCE_FULL_SBA      | 11   | 0x0     |             |
| SBA_DIS             | 12   | 0x0     |             |
| AGP_REV_ID          | 13   | 0x0     |             |
| REG_CRIPPLE_AGP4X   | 14   | 0x0     |             |
| REG_CRIPPLE_AGP2X4X | 15   | 0x0     |             |
| FORCE_INT_VREF      | 16   | 0x0     |             |

**AGP\_CNTL - RW - 32 bits - [MMReg:0x174]**

| Field Name              | Bits  | Default | Description  |
|-------------------------|-------|---------|--|
| PENDING_SLOTS_VAL       | 18:17 | 0x0     |  |
| PENDING_SLOTS_SEL       | 19    | 0x0     |  |
| EN_EXTENDED_AD_STB_2X   | 20    | 0x0     |  |
| DIS_QUEUED_GNT_FIX      | 21    | 0x0     | 0=Enable<br>1=Disable                                    |
| EN_RDATA2X4X_MULTIRESET | 22    | 0x0     |  |
| EN_RBFCALM              | 23    | 0x0     |  |
| FORCE_EXT_VREF          | 24    | 0x0     |  |
| DIS_RBF                 | 25    | 0x0     | 0=Allow normal RBF operation<br>1=Disable RBF generation |
| DELAY_FIRST_SBA_EN      | 26    | 0x0     |  |
| DELAY_FIRST_SBA_VAL     | 29:27 | 0x0     |  |
| AGP_MISC                | 31:30 | 0x0     |  |

No description available for this register.

**AGP\_CAP\_ID - R - 32 bits - [MMReg:0xF58] [pciConfig:0x58]**

| Field Name | Bits  | Default | Description |
|------------|-------|---------|-------------|
| CAP_ID     | 7:0   | 0x2     |             |
| NEXT_PTR   | 15:8  | 0x50    |             |
| AGP_MINOR  | 19:16 | 0x0     |             |
| AGP_MAJOR  | 23:20 | 0x2     |             |

No description available for this register.

**AGP\_STATUS - R - 32 bits - [MMReg:0xF5C] [pciConfig:0x5C]**

| Field Name | Bits  | Default | Description |
|------------|-------|---------|-------------|
| RATE1X     | 0     | 0x1     |             |
| RATE2X     | 1     | 0x1     |             |
| RATE4X     | 2     | 0x1     |             |
| SBA        | 9     | 0x1     |             |
| RQ         | 31:24 | 0x2f    |             |

No description available for this register.

**MM\_INDEX - RW - 32 bits - [IOReg,MMReg:0x0]**

| Field Name | Bits | Default | Description                                |
|------------|------|---------|--|
| MM_ADDR    | 30:0 | 0x0     |  |
| MM_APER    | 31   | 0x0     | 0=Register Aperture<br>1=Linear Aperture 0 |

No description available for this register.

**MM\_DATA - RW - 32 bits - [IOReg,MMReg:0x4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| MM_DATA    | 31:0 | 0x0     |             |

No description available for this register.

**PAD\_CTLR\_STRENGTH - RW - 32 bits - [MMReg:0x168]**

| Field Name                   | Bits  | Default | Description |
|------------------------------|-------|---------|-------------|
| PAD_N_STRENGTH_READ_BACK (R) | 3:0   | 0x0     |             |
| PAD_P_STRENGTH_READ_BACK (R) | 7:4   | 0x0     |             |
| PAD_N_MANUAL_STRENGTH        | 11:8  | 0x0     |             |
| PAD_P_MANUAL_STRENGTH        | 15:12 | 0x0     |             |

**PAD\_CTLR\_STRENGTH - RW - 32 bits - [MMReg:0x168]**

| Field Name                | Bits | Default | Description   |
|---------------------------|------|---------|---|
| PAD_MANUAL_OVERRIDE       | 16   | 0x1     | 0=Allow normal impedance compensation operation<br>1=Default to manual settings |
| PAD_TEST_OUT (R)          | 17   | 0x0     |   |
| PAD_DUMMY_OUT (R)         | 18   | 0x0     |   |
| PAD_HI_IO_DFR             | 19   | 0x0     |   |
| PAD_HI_IO_SCHMEN          | 20   | 0x0     |   |
| PAD_HI_IO_DREN            | 21   | 0x0     |   |
| PAD_HI_IO_VDIFF           | 23   | 0x0     |   |
| PAD_HI_IO_DFR_OVERRIDE    | 24   | 0x0     |   |
| PAD_HI_IO_SCHMEN_OVERRIDE | 25   | 0x0     |   |
| PAD_HI_IO_DREN_OVERRIDE   | 26   | 0x0     |   |
| PAD_HI_IO_VDIFF_OVERRIDE  | 28   | 0x0     |   |
| PAD_HI_IO_SLEWN           | 29   | 0x1     |   |
| PAD_HI_IO_SLEWP           | 30   | 0x1     |   |
| PAD_HI_IO_SLEW_OVERRIDE   | 31   | 0x0     |   |

No description available for this register.

**PAD\_CTLR\_UPDATE - RW - 32 bits - [MMReg:0x16C]**

| Field Name        | Bits  | Default | Description |
|-------------------|-------|---------|-------------|
| PAD_UPDATE_RATE   | 4:0   | 0x16    |             |
| PAD_SAMPLE_DELAY  | 12:8  | 0x6     |             |
| PAD_INC_THRESHOLD | 20:16 | 0x18    |             |
| PAD_DEC_THRESHOLD | 28:24 | 0x8     |             |

No description available for this register.

**PAD\_AGPINPUT\_DELAY - RW - 32 bits - [MMReg:0x164]**

| Field Name         | Bits | Default | Description |
|--------------------|------|---------|-------------|
| PAD_AGPINPUT_DELAY | 31:0 | 0x0     |             |

No description available for this register.

**GENENB - R - 8 bits - VGA\_IO:0x3C3**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| BLK_IO_BASE | 7:0  | 0x0     |             |

No description available for this register.

**GENMO\_WT - W - 8 bits - VGA\_IO:0x3C2**

| Field Name                    | Bits | Default | Description  |
|-------------------------------|------|---------|--|
| GENMO_MONO_ADDRESS_B<br>(BIF) | 0    | 0x0     | VGA addressing mode.<br>0=Monochrome emulation, regs at 0x3Bx<br>1=Color/Graphic emulation, regs at 0x3Dx  |
| VGA_RAM_EN<br>(BIF)           | 1    | 0x0     | Enables/Disables CPU access to video RAM at VGA aperture.<br>0=Disable<br>1=Enable   |
| VGA_CKSEL<br>(DISPLAY)        | 3:2  | 0x0     | Selects pixel clock frequency to use in VGA modes. Used when CRTC_GEN_CNTL.CRTC_EXT_DISP_EN=0. See CLOCK_CNTL_INDEX.PPLL_DIV_SEL for non-VGA mode pixel clock selection.<br>0=25.1744MHz (640 Pels)<br>1=28.3212MHz (720 Pels)<br>2=Reserved<br>3=Reserved |

**GENMO\_WT - W - 8 bits - VGA\_IO:0x3C2**

| Field Name                 | Bits | Default | Description  |
|----------------------------|------|---------|--|
| ODD_EVEN_MD_PGSEL<br>(HDP) | 5    | 0x0     | This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled.<br>Used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory.<br>0=Selects odd (high) memory locations<br>1=Selects even (low) memory locations |
| VGA_HSYNC_POL<br>(DISPLAY) | 6    | 0x0     | Determines polarity of horizontal sync (HSYNC) for VGA modes.<br>0 = HSYNC pulse active high<br>1 = HSYNC pulse active low<br>The covention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes.   |
| VGA_VSYNC_POL<br>(DISPLAY) | 7    | 0x0     | Determines polarity of vertical sync (VSYNC) for VGA modes.<br>0 = VSYNC pulse active high<br>1 = VSYNC pulse active low<br>The covention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes.   |

Miscellaneous Output Register (Write)

**GENMO\_RD - R - 8 bits - VGA\_IO:0x3CC**

| Field Name  | Bits | Default | Description  |
|---|------|---------|--|
| GENMO_MONO_ADDRESS_B<br><i>(mirror of GENMO_WT:GENMO_MONO_ADDRESS_B)</i><br>(BIF) | 0    | 0x0     | VGA addressing mode.   |
| VGA_RAM_EN<br><i>(mirror of GENMO_WT:VGA_RAM_EN)</i><br>(BIF)                     | 1    | 0x0     | Enables/Disables CPU access to video RAM at VGA aperture.  |
| VGA_CKSEL<br><i>(mirror of GENMO_WT:VGA_CKSEL)</i><br>(DISPLAY)                   | 3:2  | 0x0     | Selects pixel clock frequency to use.  |
| ODD_EVEN_MD_PGSEL<br><i>(mirror of GENMO_WT:ODD_EVEN_MD_PGSEL)</i><br>(HDP)       | 5    | 0x0     | This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled.<br>Used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory.                   |
| VGA_HSYNC_POL<br><i>(mirror of GENMO_WT:VGA_HSYNC_POL)</i><br>(DISPLAY)           | 6    | 0x0     | Determines polarity of horizontal sync (HSYNC) for VGA modes.<br>0 = HSYNC pulse active high<br>1 = HSYNC pulse active low<br>The covention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes. |

**GENMO\_RD - R - 8 bits - VGA\_IO:0x3CC**

| Field Name  | Bits | Default | Description   |
|---|------|---------|---|
| VGA_VSYNC_POL<br><i>(mirror of GENMO_WT:VGA_VSYNC_POL)</i><br><br>(DISPLAY) | 7    | 0x0     | Determines polarity of vertical sync (VSYNC) for VGA modes.<br>0 = VSYNC pulse active high<br>1 = VSYNC pulse active low<br>The convention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes. |

Miscellaneous Output Register (Read)

**DAC\_CNTL - RW - 32 bits - [IOReg,MMReg:0x58]**

| Field Name                          | Bits | Default | Description  |
|-------------------------------------|------|---------|--|
| DAC_RANGE_CNTL<br><br>(DISPLAY)     | 1:0  | 0x2     | DAC control bits. Default = 2.<br>0=Reserved<br>1=Reserved<br>2=PS2 Output Level<br>3=YPbPr output level   |
| DAC_BLANKING<br><br>(DISPLAY)       | 2    | 0x0     | Controls use of DAC blanking pedestal during horizontal and vertical blanks.<br>VGA PS2 compatible monitors expect a 0 IRE blanking pedestal.  |
| DAC_CMP_EN<br><br>(DISPLAY)         | 3    | 0x0     | Control DAC comparators for analog termination checking. When enabled, the results of the three comparators are read back in the DAC_CMP_OUT_R/G/B fields. Use for the DAC_FORCE fields of DAC_EXT_CNTL is recommended for testing analog monitor connection. DAC_FORCE allows the correct 10 bit data values to be forced on the DAC channels without corrupting the TMDS or TV out images.<br>When using the DAC comparators, be sure the comparator settling times are met by waiting at least 1 us between changing the DAC_FORCE parameters and reading the comparator status bits.<br>The comparator reference voltage is 0.440V. The recommended 10 bit DAC value for testing 75 or 37.5 ohm termination for PS2 current levels is 0x1AC.<br>For each channel, if the comparator output is 0, it indicates the termination is 75 ohms, and therefore no monitor is attached. When the comparator output is 1, the termination is 37.5 ohms and a monitor is attached. |
| DAC_CMP_OUT_R (R)<br><br>(DISPLAY)  | 4    | 0x0     | Red channel comparator output.   |
| DAC_CMP_OUT_G (R)<br><br>(DISPLAY)  | 5    | 0x0     | Green channel comparator output.   |
| DAC_CMP_OUT_B (R)<br><br>(DISPLAY)  | 6    | 0x0     | Blue channel comparator output.  |
| DAC_CMP_OUTPUT (R)<br><br>(DISPLAY) | 7    | 0x0     | Logical AND of R, G & B comparator outputs.  |

**DAC\_CNTL - RW - 32 bits - [IOReg,MMReg:0x58]**

| Field Name                      | Bits | Default | Description  |
|---------------------------------|------|---------|--|
| DAC_8BIT_EN<br>(DISPLAY)        | 8    | 0x0     | Enables 8 bit DAC operation. 8 bit is normal, 6 bit used for VGA emulation.<br>When in 6 bit writes and reads to DAC_DATA and PALETTE_DATA are affected. Writes shift 6 bits left by 2 to make 8 bits in the palette memory. Reads shift 8 bit palette data right by 2 to give 6 MSBs to the host.<br>0=DAC_DATA and PALETTE_DATA read/writes emulate 6 bit palette<br>1=DAC_DATA and PALETTE_DATA read/writes emulate 8 bit palette   |
| DAC_4BPP_PIX_ORDER<br>(DISPLAY) | 9    | 0x0     | Selects the order of pixel nibbles within bytes for 4 bpp extended (non-VGA) display modes.  |
| DAC_VGA_ADR_EN<br>(BIF)         | 13   | 0x0     | Enables access of the palette (DAC) at the VGA I/O DAC addresses when in extended display modes (non-VGA, or CRTC_EXT_DISP_EN=1).  |
| DAC_EXPAND_MODE<br>(DISPLAY)    | 14   | 0x0     | Method to expand 4,5 or 6 bit Red/Green/Blue color codes to 8 bit addresses.<br>0 = Zero Extension<br>1 = Dynamic Expansion<br>0=Convert 4, 5 & 6 bit colors to 8 bits by zero extension<br>1=Convert 4, 5 & 6 bit colors to 8 bits by dynamic expansion   |
| DAC_PDWN<br>(DISPLAY)           | 15   | 0x0     | Power down internal DAC macro bandgap unit. Should also set the R, G & B powerdowns in the DAC_MACRO_CNTL register at the same time.<br>Powering down the DAC does not affect the digital outputs (TV or flat panel).<br>The DAC is automatically powered down when the PML_POWER_STATE register is not in the D0 state.<br>Setting all DAC_PDWN fields should save about 56 mA when PS2 output levels.  |
| CRT_SENSE (R)<br>(DISPLAY)      | 16   | 0x0     | 0=CRT Monitor Detection result - not connected<br>1=CRT Monitor Detection result - connected   |
| CRT_DETECTION_ON<br>(DISPLAY)   | 17   | 0x0     | 0=CRT Monitor Detection disabled<br>1=CRT Monitor Detection enabled  |
| DAC_CRC_CONT_EN<br>(DISPLAY)    | 18   | 0x0     | When CRC is in one shot mode, one-and-only-one frame or field is CRCed after DAC_CRC_EN is set high. In continuous mode every frame/field is CRCed and the results are valid for one field/frame until the next set of results are ready. If a field/frames results are not read within one frame in continuous mode they are over written. In one-shot mode the results remain and can be read until DAC_CRC_EN is cleared.<br>0=DAC CRC runs in one shot mode.<br>1=DAC CRC runs in continuous mode. |



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**DAC\_CNTL - RW - 32 bits - [IOReg,MMReg:0x58]**

| Field Name                         | Bits  | Default | Description   |
|------------------------------------|-------|---------|---|
| DAC_CRC_EN<br>(DISPLAY)            | 19    | 0x0     | Enables the CRC signature check on the data going to the DAC macro. This is what appears on the screen, and includes graphics, HW cursor, video overlay, sub-picture, and overscan. CRC will start in next vertical blank on the first pixel of the line where VSYNC goes active, and run for one field/frame. For interlaced modes the CRC block will not start working until the beginning of a field with odd/even polarity matching the DAC_CRC_FIELD setting.<br>0=Reset DAC CRC.<br>1=Enable DAC CRC for next frame/field in one shot, or all frames/fields in continuous mode. |
| DAC_CRC_FIELD<br>(DISPLAY)         | 20    | 0x0     | Used only for interlaced mode CRCs. Controls which field polarity starts the CRC block after DAC_CRC_EN is set high.<br>0=If interlace display and one shot mode, then CRC even field only<br>1=If interlace display and one shot mode, then CRC odd field only   |
| DAC_LUT_COUNTER_LIMIT<br>(DISPLAY) | 22:21 | 0x0     | Anti-sparkle timeout. The palette circuit will search for a place in the display image to hide palette reads or writes. If no hiding location is found within this many pixels, a dot-stretch is forced to hide the cycle as best as possible. Setting this register too high in low resolution modes may cause long delays on the PCI/AGP bus. The recommended settings are best.<br>0=anti-sparkle timeout 3 clocks<br>1=anti-sparkle timeout 7 clocks<br>2=anti-sparkle timeout 15 clocks<br>3=anti-sparkle timeout 31 clocks  |
| DAC_LUT_READ_SEL<br>(DISPLAY)      | 23    | 0x0     | Used for diagnostics only. Selects palette for HOST reads.<br>0=Palette reads come from main palette<br>1=Palette reads come from secondary palette   |
| DAC_MASK<br>(DISPLAY)              | 31:24 | 0xff    | Mirror VGA DAC_MASK. No affect in non-VGA modes. Masks off usage of individual palette index bits before pixel index is looked-up in the palette.<br>0 = do not use this bit of the index<br>1 = use this bit of the index<br>This is a mirror of the VGA DAC_MASK register. It only has an effect in VGA emulation modes (CRTC_EXT_DISP_EN=0), not for VESA modes or extended display modes.   |

General control for the RGB DAC and palette.

**CRTC\_GEN\_CNTL - RW - 32 bits - [IOReg,MMReg:0x50]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



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**CRTC\_GEN\_CNTL - RW - 32 bits - [IOReg,MMReg:0x50]**

| Field Name                     | Bits | Default | Description  |
|--------------------------------|------|---------|--|
| CRTC_DBL_SCAN_EN<br>(DISPLAY)  | 0    | 0x0     | Double scan enable.<br>Double scan only affects the calculation of display addresses by adding the CRTC_PITCH every second line (also applies to the hardware cursor pitch). Enabling double scan does not change the CRTC vertical programming or VSYNC timing. The overscan top & bottom are not affected and remain the number of lines programmed (i.e. not double). The hardware cursor programming remains in terms of physical lines (not logical lines). The cursor vertical position must begin on an even line number when in double scan. The cursor itself is limited to 64 physical lines in height, which means only 32 logical lines. This is because the cursor pitch is only added at the end of odd scan lines, but the CRTC vertical logic stops the cursor after 64 physical lines.<br>0=disable<br>1=enable |
| CRTC_INTERLACE_EN<br>(DISPLAY) | 1    | 0x0     | Interlace display mode enable.<br>0=Non-Interlace<br>1=Interlace   |
| CRTC_C_SYNC_EN<br>(DISPLAY)    | 4    | 0x0     | Enables composite sync on horizontal sync output. When this is set, the VSYNC pin should be disabled by setting CRTC_EXT_CNTL.CRTC_VSYNC_TRISTATE=1.<br>0=Disable<br>1=Enable  |
| CRTC_PIX_WIDTH<br>(DISPLAY)    | 11:8 | 0x0     | Display pixel width (actually depth).<br>For 4bpp mode DAC_CNTL.DAC_4BPP_PIX_ORDER selects the order of nibbles within bytes.<br>When R, G, or B components are only 4, 5 or 6 bits, DAC_CNTL.DAC_EXPAND_MODE selects how these components are expanded to 8 bits each for keying and palette lookup.<br>When alpha values are 1 or 4 bits, they are expanded to 8 bits by dynamic expansion of the high order bits to the missing lower order bits.<br>0=Disable pixel clock for primary CRTC<br>1=4bpp Indexed<br>2=8bpp Indexed<br>3=15bpp aRGB 1555<br>4=16bpp RGB 565<br>5=24bpp RGB 888<br>6=32bpp aRGB 8888<br>7=16bpp aRGB 4444<br>8=16bpp aIndex 88   |
| CRTC_ICON_EN<br>(DISPLAY)      | 15   | 0x0     | 0=Disable Hardware Icon<br>1=Enable Hardware Icon  |
| CRTC_CUR_EN<br>(DISPLAY)       | 16   | 0x0     | Hardware cursor enable.<br>This field is double buffered and locked with the CUR_LOCK register field.<br>0=Disable<br>1=Enable   |

**CRTC\_GEN\_CNTL - RW - 32 bits - [IOReg,MMReg:0x50]**

| Field Name                          | Bits  | Default | Description  |
|-------------------------------------|-------|---------|--|
| CRTC_VSTAT_MODE<br>(DISPLAY)        | 18:17 | 0x0     | Selects the location of the display updating of CRTC_OFFSET and CUR_OFFSET and related fields during the vertical retrace. Also determines where the VGA_VSTATUS update will occur within the vertical retrace for VGA modes.<br>For non-VGA modes only the upper bit of this field is used. When 00 or 01 in non-VGA the updating of the CRTC_OFFSET and the CUR_OFFSET is delayed as long as possible within the vertical retrace until the start of the last line of the retrace. When 10 or 11 in non-VGA the CRTC_OFFSET and CUR_OFFSET are updated at the leading edge of VSYNC, which is normally relatively early in the vertical retrace. No matter how this is set, the update of status bits like WAIT_UNTIL_PFLIP will reflect the actual location of the update. Any writes to CRTC_OFFSET or CUR_OFFSET after the selected point has passed in the vertical retrace will have no affect until the display frame after the next vertical retrace.<br>For VGA modes this field affects the behaviour of page flipping in some applications/games that poll the VGA_VSTATUS flag. This field should be tuned by the BIOS for compatibility with the most games.<br>0=VGA_VSTATUS until vcount= vt total<br>1=VGA_VSTATUS until vblank end, DISP_ADDR loads when vcount=vt otal<br>2=VGA_VSTATUS until vblank end, DISP_ADDR loads when vcount=vtotal<br>3=VGA_VSTATUS until vsync start<br>DISP_ADDR loads in vsync start |
| CRTC_CUR_MODE<br>(DISPLAY)          | 22:20 | 0x0     | Hardware cursor mode.<br>For 2bpp mode, each line of cursor data is stored in memory as 64 bits of AND data followed by 64 bits of XOR data.<br>For color AND/XOR mode, each pixel is stored sequentially in memory as 32bits each in aRGB8888 format with bit 31 of each DWord being the AND bit.<br>For the color alpha modes the format is also 32bpp aRGB8888 with all 8 bits of the alpha being used.<br>All HW cursor lines must be 64 pixels wide and all lines must be stored sequentially in memory.<br>0=Mono + 1 bit AND (2bpp), 64x64<br>1=Color 24bpp + 1 bit AND, 32hx64v<br>2=Color 24bpp + 8 bit alpha, premultiplied alpha, 32hx64v<br>3=Color 24bpp + 8 bit alpha, unmultiplied alpha, 32hx64v   |
| CRTC_EXT_DISP_EN<br>(BIF) (DISPLAY) | 24    | 0x0     | Extended display mode enable. No affect if strapped<br>VGA_DISABLE=1.<br>0=VGA<br>1=Extended   |
| CRTC_EN<br>(DISPLAY)                | 25    | 0x0     | Enables CRT controller.<br>When reset, the CRTC horizontal counter is set to zero, and the vertical counter is set to the current value of CRTC_V_TOTAL_DISP.CRTC_V_DISP.<br>0=Reset<br>1=Enable   |



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**CRTC\_GEN\_CNTL - RW - 32 bits - [IOReg,MMReg:0x50]**

| Field Name                          | Bits | Default | Description  |
|-------------------------------------|------|---------|--|
| CRTC_DISP_REQ_EN_B<br><br>(DISPLAY) | 26   | 0x1     | Enables display graphics requests to the memory controller.<br>Affects only graphics and VGA text requests. Does not affect HW cursor, overlay or subpic.<br>When setting this bit, CRTC_EXT_CNTL.CRTC_DISPLAY_DIS is also normally set to blank the screen.<br>Active low.<br>0=Enable<br>1=Disable |

CRTC general controls



### 3. GART Detailed Register Reference

Registers related to graphics address remapping table

| <b>AIC_CTRL - RW - 32 bits - [MMReg:0x1D0]</b> |             |                |   |
|--|-------------|----------------|---|
| <b>Field Name</b>                              | <b>Bits</b> | <b>Default</b> | <b>Description</b>                      |
| TRANSLATE_EN                                   | 0           | 0x0            | 0=disable pci gart<br>1=enable pci gart |

PCI GART page table base address in system memory

| <b>AIC_STAT - R - 32 bits - [MMReg:0x1D4]</b> |             |                |                    |
|---|-------------|----------------|--------------------|
| <b>Field Name</b>                             | <b>Bits</b> | <b>Default</b> | <b>Description</b> |
| AIC_TLB_VLD                                   | 0           | 0x0            |                    |
| AIC_STAT1                                     | 1           | 0x0            |                    |
| AIC_STAT0                                     | 2           | 0x0            |                    |

PCI GART page table base address in system memory

| <b>AIC_PT_BASE - RW - 32 bits - [MMReg:0x1D8]</b> |             |                |                    |
|---|-------------|----------------|--------------------|
| <b>Field Name</b>                                 | <b>Bits</b> | <b>Default</b> | <b>Description</b> |
| AIC_PT_BASE                                       | 31:12       | 0x0            |                    |

PCI GART page table base address in system memory

| <b>AIC_LO_ADDR - RW - 32 bits - [MMReg:0x1DC]</b> |             |                |                    |
|---|-------------|----------------|--------------------|
| <b>Field Name</b>                                 | <b>Bits</b> | <b>Default</b> | <b>Description</b> |
| AIC_LO_ADDR                                       | 31:12       | 0x0            |                    |

PCI GART page table base address in system memory

| <b>AIC_HI_ADDR - RW - 32 bits - [MMReg:0x1E0]</b> |             |                |                    |
|---|-------------|----------------|--------------------|
| <b>Field Name</b>                                 | <b>Bits</b> | <b>Default</b> | <b>Description</b> |
| AIC_HI_ADDR                                       | 31:12       | 0x0            |                    |

Upper boundary of PCI addresses responded to by the PCI GART; addresses higher than this are not translated

| <b>AIC_TLB_ADDR - R - 32 bits - [MMReg:0x1E4]</b> |             |                |                    |
|---|-------------|----------------|--------------------|
| <b>Field Name</b>                                 | <b>Bits</b> | <b>Default</b> | <b>Description</b> |
| AIC_TLB_ADDR                                      | 31:12       | 0x0            |                    |

Current page address before translation by the PCI GART

| <b>AIC_TLB_DATA - R - 32 bits - [MMReg:0x1E8]</b> |             |                |                    |
|---|-------------|----------------|--------------------|
| <b>Field Name</b>                                 | <b>Bits</b> | <b>Default</b> | <b>Description</b> |
| AIC_TLB_DATA                                      | 31:12       | 0x0            |                    |

Current page address after translation by the PCI GART



#### 4. PMI Detailed Register Reference

Power management registers

##### PMI\_CAP\_ID - R - 8 bits - [MMReg:0xF50] [pciConfig:0x50]

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| PMI_CAP_ID | 7:0  | 0x1     | 1=PCI Bus Power Management Interface (PMI) register section |

No description available for this register.

##### PMI\_NXT\_CAP\_PTR - R - 8 bits - [MMReg:0xF51] [pciConfig:0x51]

| Field Name      | Bits | Default | Description |
|-----------------|------|---------|-------------|
| PMI_NXT_CAP_PTR | 7:0  | 0x0     |             |

No description available for this register.

##### PM\_STATUS - RW - 16 bits - [MMReg:0xF54]:R [pciConfig:0x54]

| Field Name          | Bits  | Default | Description |
|---------------------|-------|---------|-------------|
| PMI_POWER_STATE     | 1:0   | 0x0     |             |
| PMI_PME_EN (R)      | 8     | 0x0     |             |
| PMI_DATA_SELECT (R) | 12:9  | 0x0     |             |
| PMI_DATA_SCALE (R)  | 14:13 | 0x0     |             |
| PMI_PME_STATUS (R)  | 15    | 0x0     |             |

No description available for this register.

##### PMI\_PMC\_REG - R - 16 bits - [MMReg:0xF52] [pciConfig:0x52]

| Field Name            | Bits  | Default | Description                                    |
|-----------------------|-------|---------|--|
| PMI_VERSION           | 2:0   | 0x2     | 2=Compliant with PMI Specification version 1.1 |
| PMI_PME_CLOCK         | 3     | 0x0     |  |
| PMI_DEV_SPECIFIC_INIT | 5     | 0x0     |  |
| PMI_D1_SUPPORT        | 9     | 0x1     |  |
| PMI_D2_SUPPORT        | 10    | 0x1     |  |
| PMI_PME_SUPPORT       | 15:11 | 0x0     |  |

No description available for this register.

##### PMI\_DATA - R - 8 bits - [MMReg:0xF57] [pciConfig:0x57]

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| PMI_DATA   | 7:0  | 0x0     |             |

No description available for this register.

**5. ClockGenerator Detailed Register Reference**

## Clock Generator Control Registers

| CLK_PWRMGT_CNTL - RW - 32 bits - CLKIND:0x14 |       |         |   |
|--|-------|---------|---|
| Field Name                                   | Bits  | Default | Description   |
| MPLL_PWRMGT_OFF<br>(CGM)                     | 0     | 0x0     | M domain clock power management off   |
| SPLL_PWRMGT_OFF<br>(CG)                      | 1     | 0x0     | S domain clock power management off   |
| PPLL_PWRMGT_OFF<br>(CG)                      | 2     | 0x0     | Pixel clock power management off  |
| P2PLL_PWRMGT_OFF<br>(CG)                     | 3     | 0x0     |   |
| MCLK_TURNOFF<br>(CGM)                        | 4     | 0x0     | Turn off M domain clocks  |
| SCLK_TURNOFF<br>(CG)                         | 5     | 0x0     | Turn off S domain clocks  |
| PCLK_TURNOFF<br>(CG)                         | 6     | 0x0     | Turn off pixel clocks   |
| P2CLK_TURNOFF<br>(CG)                        | 7     | 0x0     |   |
| MC_CH_MODE<br>(CGM)                          | 8     | 0x1     | 0=single channel<br>1=dual channel  |
| TEST_MODE<br>(CG) (CGM)                      | 9     | 0x0     | Disable long internal timing to speed up regression tests                           |
| GLOBAL_PMAN_EN<br>(CG)                       | 10    | 0x0     | 0=Power managment off<br>1=Power managment on                                       |
| ENGINE_DYNCLK_MODE<br>(CG)                   | 12    | 0x1     | 0=Provide Clock for each Eng block separately<br>1=Treat Engine as one single block |
| ACTIVE_HILO_LAT<br>(CG)                      | 14:13 | 0x3     | 0=5 clocks<br>1=12 clocks<br>2=20 clocks<br>3=32 clocks                             |
| DISP_DYN_STOP_LAT<br>(CG)                    | 15    | 0x0     | 0=10 clocks<br>1=20 clocks  |
| MC_BUSY (R)<br>(CGM)                         | 16    | 0x0     | 0=MC is idle<br>1=MC is busy  |
| MC_INT_CNTL<br>(CGM)                         | 17    | 0x0     | 0=HW control<br>1=SW over-ride  |
| MC_SWITCH<br>(CGM)                           | 18    | 0x0     | 0=source of memory clock is not changed<br>1=source of memory clock is changed      |
| DLL_READY<br>(CGM)                           | 19    | 0x0     | 0=DLL is not ready<br>1=DLL is ready  |

**CLK\_PWRMGT\_CNTL - RW - 32 bits - CLKIND:0x14**

| Field Name                 | Bits  | Default | Description  |
|----------------------------|-------|---------|--|
| DISP_PM<br>(CG)            | 20    | 0x0     | 0=display clocks running in PM modes<br>1=clocks OFF |
| DYN_STOP_MODE<br>(CG)      | 23:21 | 0x7     | 0=10 clocks<br>7=111 = 140 clocks                    |
| CG_NO1_DEBUG<br>(CG) (CGM) | 29:24 | 0x0     | 1st 16-bit hardware debug register                   |
| TVPLL_PWRMGT_OFF<br>(CG)   | 30    | 0x0     |  |
| TVCLK_TURNOFF<br>(CG)      | 31    | 0x0     |  |

Clock power management control

**PLL\_PWRMGT\_CNTL - RW - 32 bits - CLKIND:0x15**

| Field Name                  | Bits  | Default | Description   |
|-----------------------------|-------|---------|---|
| MPLL_TURNOFF<br>(CGM)       | 0     | 0x0     | Enable M domain PLL to be turned off at power state D3                          |
| SPLL_TURNOFF<br>(CG)        | 1     | 0x0     | Enable S domain PLL to be turned off at power state D3                          |
| PPLL_TURNOFF<br>(CG)        | 2     | 0x0     | Enable pixel clock PLL to be turned off at power state D3                       |
| P2PLL_TURNOFF<br>(CG)       | 3     | 0x0     |   |
| TVPLL_TURNOFF<br>(CG)       | 4     | 0x0     |   |
| AGPCLK_DYN_STOP_LAT<br>(CG) | 8:5   | 0x0     |   |
| APM_POWER_STATE<br>(CG)     | 10:9  | 0x0     |   |
| APM_PWRSTATE_RD (R)<br>(CG) | 12:11 | 0x0     |   |
| PM_MODE_SEL<br>(CG)         | 13    | 0x0     | 0=ACPI<br>1=APM   |
| EN_PWRSEQ_DONE_COND<br>(CG) | 14    | 0x1     | 0=Switch states without PWRSEQ_DONE rising edge condition<br>1=Enable condition |
| EN_DISP_PARKED_COND<br>(CG) | 15    | 0x1     | 0=Switch states without DISP_PARKED condition<br>1=Enable condition             |
| MOBILE_SU<br>(CG)           | 16    | 0x1     | 0=Regular<br>1=Optimize power consumption in Suspend mode                       |
| SU_SCLK_USE_BCLK<br>(CG)    | 17    | 0x1     | 1=During Suspend, SCLK is sourced from BCLK                                     |
| SU_MCLK_USE_BCLK<br>(CG)    | 18    | 0x1     | 1=During Suspend, MCLK is sourced from BCLK                                     |



**PLL\_PWRMGT\_CNTL - RW - 32 bits - CLKIND:0x15**

| Field Name                      | Bits  | Default | Description                                     |
|---------------------------------|-------|---------|---|
| SU_SUSTAIN_DISABLE<br>(CG)      | 19    | 0x0     | 0=Sustain Suspend until PLL lockup<br>1=Disable |
| TCL_BYPASS_DISABLE<br>(CG)      | 20    | 0x0     | 0=Enable TCL_SCLK power management<br>1=Disable |
| TCL_CLOCK_ACTIVE_RD (R)<br>(CG) | 21    | 0x0     | 0=TCL_SCLK stopped<br>1=TCL_SCLK running        |
| CG_NO2_DEBUG<br>(CG) (CGM)      | 31:24 | 0x0     | 2nd 16-bit hardware debug register              |

PLL power management control

**CLK\_PIN\_CNTL - RW - 32 bits - CLKIND:0x1**

| Field Name             | Bits  | Default | Description  |
|------------------------|-------|---------|--|
| OSC_EN                 | 0     | 0x1     | Oscillation enable<br>0=Disable<br>1=Enable  |
| XTL_LOW_GAIN           | 2     | 0x1     | Oscillator high gain or low gain control<br>0=High Gain<br>1=Low Gain  |
| DONT_USE_XTALIN        | 4     | 0x0     | 0=Use XTALIN pin to generate internal timing (for simulation only)<br>1=Use divided version of PLL reference clock   |
| SLOW_CLOCK_SOURCE      | 5     | 0x0     | 0=XTALIN is used for power sequencing block<br>1=PCICLKBY2   |
| CG_CLK_TO_OUTPIN       | 11    | 0x0     | 0=disabled<br>1=send out selected clock for jitter test  |
| CG_COUNT_UP_TO_OUTPIN  | 12    | 0x0     | 0=disabled<br>1=send out COUNT_UP signal for test tuning   |
| ACCESS_REGS_IN_SUSPEND | 13    | 0x0     | 0=disabled<br>1=force all SCLK branches, to allow accessing any registers in APM Suspend mode  |
| CG_SPARE               | 14    | 0x0     |  |
| SCLK_DYN_START_CNTL    | 15    | 0x1     | 0=SCLK starts 4 clocks after BUSY active<br>1=SCLK starts 1 clock after BUSY active  |
| CP_CLK_RUNNING (R)     | 16    | 0x0     | 0=CP SCLK STOPPED<br>1=CP SCLK RUNNING   |
| CG_SPARE_RD (R)        | 18:17 | 0x0     |  |
| XTALIN_ALWAYS_ONb      | 19    | 0x0     | 0=force XTALIN to run in Suspend mode<br>1=PM control over XTALIN pad  |
| PWRSEQ_DELAY           | 31:24 | 0x0     | Programmable value of panel power sequencing block. This value can be programmed up to 225 ms in increments of 1 ms (generated from F32KHz clock). If 0 is programmed, SLOW_CLOCK is stopped<br>0=Programmable value of panel power sequencing block.<br>1=This value can be programmed up to 225 ms in increments of 1 ms (generated from F32KHz clock).<br>2=If 0 is programmed, SLOW_CLOCK is stopped |



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**CLK\_PIN\_CNTL - RW - 32 bits - CLKIND:0x1**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

Clock pin control

**PPLL\_CNTL - RW - 32 bits - CLKIND:0x2**

| Field Name                | Bits  | Default | Description   |
|---------------------------|-------|---------|---|
| PPLL_RESET                | 0     | 0x1     | Power down pixel clock PLL<br>0=Not Reset<br>1=Reset  |
| PPLL_SLEEP                | 1     | 0x1     | Reset pixel clock PLL<br>1=Powerdown  |
| PPLL_TST_EN               | 2     | 0x0     | Enable pixel clock PLL test mode  |
| PPLL_REFCLK_SEL           | 4     | 0x0     | 0=not flopped<br>1=flopped  |
| PPLL_FBCLK_SEL            | 5     | 0x0     | 0=not flopped<br>1=flopped  |
| PPLL_TCPOFF               | 6     | 0x0     | 0=normal<br>1=test mode: Hi-Z   |
| PPLL_TVCOMAX              | 7     | 0x0     | 0=normal<br>1=test mode: runaway  |
| PPLL_PCP                  | 10:8  | 0x4     | Pixel clock PLL charge pump gain. Programmed by BIOS. Do not change.  |
| PPLL_PVG                  | 13:11 | 0x4     | Pixel clock PLL VCO gain. Programmed by BIOS. Do not change.  |
| PPLL_PDC                  | 15:14 | 0x2     | Pixel clock PLL duty cycle. Programmed by BIOS. Do not change.  |
| PPLL_ATOMIC_UPDATE_EN     | 16    | 0x0     | Pixel clock PLL atomic update enable for non-VGA modes. Reference and feedback dividers are double buffered and updated concurrently when a PPLL_ATOMIC_UPDATE_W field is set.<br>0=Atomic Update Disabled<br>1=Atomic Update Enabled |
| PPLL_VGA_ATOMIC_UPDATE_EN | 17    | 0x0     | Same as PPLL_ATOMIC_UPDATE_EN, but for VGA modes.<br>0=VGA Atomic Update Disabled<br>1=VGA Atomic Update Enabled  |
| PPLL_ATOMIC_UPDATE_SYNC   | 18    | 0x0     | Selects pixel clock PLL atomic update trigger position. Using VSYNC delays update, but allows clock frequency change to be hidden in the vertical retrace.<br>0=Update ASAP<br>1=Update in VSYNC                                      |
| PPLL_DISABLE_AUTO_RESET   | 19    | 0x0     | 0=When Atomic Update Disabled, PPLL resets upon REF_DIV or FB_DIV changes<br>1=PPLL automatic reset Disabled  |

Pixel clock PLL control

**PPLL\_REF\_DIV - RW - 32 bits - CLKIND:0x3**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**PPLL\_REF\_DIV - RW - 32 bits - CLKIND:0x3**

| Field Name               | Bits  | Default | Description   |
|--------------------------|-------|---------|---|
| PPLL_REF_DIV             | 9:0   | 0x3f    | Pixel clock PLL reference divider.<br>Must be set so reference frequency is between 1MHz and 400kHz. i.e. $1\text{MHz} \geq (\text{PPLL\_REF}) / \text{PPLL\_REF\_DIV} \geq 400\text{kHz}$ . Also 0 and 1 are not legal settings for this register field. |
| PPLL_ATOMIC_UPDATE_W (W) | 15    | 0x0     | If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.<br>0=No Update<br>1=Update  |
| PPLL_ATOMIC_UPDATE_R (R) | 15    | 0x0     | Readback of atomic update status.<br>0=Update done<br>1=Update Pending  |
| PPLL_REF_DIV_SRC         | 17:16 | 0x0     | Pixel clock PLL reference divider input source selection.<br>0=PPLL_REF = XTALIN<br>1=PPLL_REF = PLLSCLK/2<br>2=PPLL_REF = PLLSCLK/4<br>3=PPLL_REF = Secondary Reference Clock  |

Pixel clock PLL reference division configuration

**SPLL\_CNTL - RW - 32 bits - CLKIND:0xC**

| Field Name                  | Bits  | Default | Description  |
|-----------------------------|-------|---------|--|
| SPLL_SLEEP                  | 0     | 0x1     | Power down S domain PLL<br>1=Powerdown             |
| SPLL_RESET                  | 1     | 0x1     | Reset S domain PLL<br>0=Not Reset<br>1=Reset       |
| SPLL_TST_EN                 | 2     | 0x0     | Enable S domain PLL test mode                      |
| SPLL_REFCLK_SEL             | 4     | 0x0     | 0=not flopped<br>1=flopped                         |
| SPLL_FBCLK_SEL              | 5     | 0x0     | 0=not flopped<br>1=flopped                         |
| SPLL_TCPOFF                 | 6     | 0x0     | 0=normal<br>1=test mode: Hi-Z                      |
| SPLL_TVCOMAX                | 7     | 0x0     | 0=normal<br>1=test mode: runaway                   |
| SPLL_PCP                    | 10:8  | 0x4     | Program S domain PLL charge pump                   |
| SPLL_PVG                    | 13:11 | 0x4     | Program S domain PLL VCO gain                      |
| SPLL_PDC                    | 15:14 | 0x1     | Program S domain clock duty cycle                  |
| SPLL_X1_CLK_SKEW            | 18:16 | 0x0     |  |
| SPLL_X2_CLK_SKEW            | 22:20 | 0x0     |  |
| SPLL_MODE                   | 27:24 | 0x4     |  |
| MYCLK_SOURCED_FROM_SPLL_SEL | 29:28 | 0x0     | 0=SPLLBY1<br>1=SPLLBY1b<br>2=SPLLBY2<br>3=SPLLBY2b |

**SPLL\_CNTL - RW - 32 bits - CLKIND:0xC**

| Field Name             | Bits | Default | Description                 |
|------------------------|------|---------|-----------------------------|
| ENABLE_MYCLK_FROM_SPLL | 30   | 0x0     | 0=clock stop<br>1=clock run |

S domain PLL control

**SCLK\_CNTL - RW - 32 bits - CLKIND:0xD**

| Field Name            | Bits | Default | Description   |
|-----------------------|------|---------|---|
| SCLK_SRC_SEL          | 2:0  | 0x0     | S domain clock source selection<br>0=not PCICLK<br>1=SCLK/1<br>2=SCLK/2<br>3=SCLK/4<br>4=SCLK/8<br>5=External Source/Scan Clock (AUXWIN pin)<br>6=Test Clock from Test Controller<br>7=MPLL |
| CP_MAX_DYN_STOP_LAT   | 3    | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency   |
| HDP_MAX_DYN_STOP_LAT  | 4    | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency   |
| TV_MAX_DYN_STOP_LAT   | 5    | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency   |
| E2_MAX_DYN_STOP_LAT   | 6    | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency   |
| SE_MAX_DYN_STOP_LAT   | 7    | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency   |
| IDCT_MAX_DYN_STOP_LAT | 8    | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency   |
| VIP_MAX_DYN_STOP_LAT  | 9    | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency   |
| RE_MAX_DYN_STOP_LAT   | 10   | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency   |
| PB_MAX_DYN_STOP_LAT   | 11   | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency   |
| TAM_MAX_DYN_STOP_LAT  | 12   | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency   |
| TDM_MAX_DYN_STOP_LAT  | 13   | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency   |
| RB_MAX_DYN_STOP_LAT   | 14   | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency   |
| FORCE_DISP2           | 15   | 0x1     | 0=Dynamic<br>1=ForceOn  |
| FORCE_CP              | 16   | 0x1     | CP block dynamic power management off<br>0=Dynamic<br>1=ForceOn   |



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**SCLK\_CNTL - RW - 32 bits - CLKIND:0xD**

| Field Name    | Bits | Default | Description   |
|---------------|------|---------|---|
| FORCE_HDP     | 17   | 0x1     | HDP block dynamic power management off<br>0=Dynamic<br>1=ForceOn  |
| FORCE_DISP1   | 18   | 0x1     | 0=Dynamic<br>1=ForceOn  |
| FORCE_TOP     | 19   | 0x1     | 0=Dynamic<br>1=ForceOn  |
| FORCE_E2      | 20   | 0x1     | E2 block dynamic power management off<br>0=Dynamic<br>1=ForceOn   |
| FORCE_SE      | 21   | 0x1     | SE block dynamic power management off<br>0=Dynamic<br>1=ForceOn   |
| FORCE_IDCT    | 22   | 0x1     | IDCT block dynamic power management off<br>0=Dynamic<br>1=ForceOn |
| FORCE_VIP     | 23   | 0x1     | VIP block dynamic power management off<br>0=Dynamic<br>1=ForceOn  |
| FORCE_RE      | 24   | 0x1     | RE block dynamic power management off<br>0=Dynamic<br>1=ForceOn   |
| FORCE_PB      | 25   | 0x1     | PB block dynamic power management off<br>0=Dynamic<br>1=ForceOn   |
| FORCE_TAM     | 26   | 0x1     | TAM block dynamic power management off<br>0=Dynamic<br>1=ForceOn  |
| FORCE_TDM     | 27   | 0x1     | TDM block dynamic power management off<br>0=Dynamic<br>1=ForceOn  |
| FORCE_RB      | 28   | 0x1     | RB block dynamic power management off<br>0=Dynamic<br>1=ForceOn   |
| FORCE_TV_SCLK | 29   | 0x1     | 0=Dynamic<br>1=ForceOn  |
| FORCE_SUBPIC  | 30   | 0x1     | 0=Dynamic<br>1=ForceOn  |
| FORCE_OV0     | 31   | 0x1     | 0=Dynamic<br>1=ForceOn  |

Clock source selection and dynamic power management control

**AGP\_PLL\_CNTL - RW - 32 bits - CLKIND:0xB**

| Field Name | Bits | Default | Description        |
|------------|------|---------|--------------------|
| APLL_SLEEP | 0    | 0x0     | Power down AGP PLL |

**AGP\_PLL\_CNTL - RW - 32 bits - CLKIND:0xB**

| Field Name             | Bits  | Default | Description  |
|------------------------|-------|---------|--|
| APLL_RESET             | 1     | 0x0     | Reset AGP PLL  |
| APLL_XSEL              | 3:2   | 0x0     | Select different AGP mode for testing<br>0=TESTMODE REFCLK<br>1=TESTMODE AGP1X<br>2=TESTMODE AGP2X<br>3=TESTMODE AGP4X |
| APLL_TST_EN            | 4     | 0x0     | Enable AGP PLL test mode<br>0=normal<br>1=test mode  |
| APLL_TCPOFF            | 5     | 0x0     | 0=normal<br>1=test mode: Hi-Z  |
| APLL_TVCOMAX           | 6     | 0x0     | 0=normal<br>1=test mode: runaway   |
| APLL_REF_SKEW          | 9:7   | 0x4     |  |
| APLL_FB_SKEW           | 12:10 | 0x0     |  |
| APLL_X0_CLK_SKEW       | 15:13 | 0x0     |  |
| APLL_X1_CLK_SKEW       | 18:16 | 0x0     | Program AGP1X mode clock skew  |
| APLL_PUMP_GAIN         | 27:25 | 0x4     | Program AGP PLL charge pump  |
| APLL_VCO_GAIN          | 30:28 | 0x5     |  |
| APLL_SEL_SKWADJ_PCICLK | 31    | 0x0     |  |

AGP PLL control

**P2PLL\_CNTL - RW - 32 bits - CLKIND:0x2A**

| Field Name               | Bits  | Default | Description  |
|--------------------------|-------|---------|--|
| P2PLL_RESET              | 0     | 0x1     | 0=Not Reset P2PLL<br>1=Reset P2PLL   |
| P2PLL_SLEEP              | 1     | 0x1     | 1=Powerdown P2PLL  |
| P2PLL_TST_EN             | 2     | 0x0     |  |
| P2PLL_REFCLK_SEL         | 4     | 0x0     | 0=not flopped<br>1=flopped   |
| P2PLL_FBCLK_SEL          | 5     | 0x0     | 0=not flopped<br>1=flopped   |
| P2PLL_TCPOFF             | 6     | 0x0     | 0=normal<br>1=test mode: Hi-Z  |
| P2PLL_TVCOMAX            | 7     | 0x0     | 0=normal<br>1=test mode: runaway   |
| P2PLL_PCP                | 10:8  | 0x4     |  |
| P2PLL_PVG                | 13:11 | 0x4     |  |
| P2PLL_PDC                | 15:14 | 0x2     |  |
| P2PLL_ATOMIC_UPDATE_EN   | 16    | 0x0     | 0=Atomic Update Disabled<br>1=Atomic Update Enabled  |
| P2PLL_ATOMIC_UPDATE_SYNC | 18    | 0x0     | 0=Update ASAP<br>1=Update in VSYNC   |
| P2PLL_DISABLE_AUTO_RESET | 19    | 0x0     | 0=When Atomic Update Disabled, P2PLL resets upon REF_DIV or FB_DIV changes<br>1=P2PLL automatic reset Disabled |

**P2PLL\_CNTL - RW - 32 bits - CLKIND:0x2A**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

No description available for this register.

**P2PLL\_REF\_DIV - RW - 32 bits - CLKIND:0x2B**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                           |       |     |   |
|---------------------------|-------|-----|---|
| P2PLL_REF_DIV             | 9:0   | 0x0 |   |
| P2PLL_ATOMIC_UPDATE_W (W) | 15    | 0x0 | 0=No Update<br>1=Update   |
| P2PLL_ATOMIC_UPDATE_R (R) | 15    | 0x0 | 0=Update done<br>1=Update Pending   |
| P2PLL_REF_DIV_SRC         | 17:16 | 0x0 | 0=P2PLL_REF = XTALIN<br>1=P2PLL_REF = PLLSCLK/2<br>2=P2PLL_REF = PLLSCLK/4<br>3=P2PLL_REF = Secondary Reference Clock |

No description available for this register.

**CLOCK\_CNTL\_INDEX - RW - 32 bits - [IOReg,MMReg:0x8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                                      |     |     |   |
|--------------------------------------|-----|-----|---|
| PLL_ADDR<br>(DISPLAY) (CG) (CGM)     | 5:0 | 0x0 | Indirect CG and PLL register index  |
| PLL_WR_EN<br>(DISPLAY) (CG) (CGM)    | 7   | 0x0 | Indirect CG and PLL register write enable<br>0=Disable writes to CLOCK_CNTL_DATA<br>1=Enable writing to CLOCK_CNTL_DATA   |
| PPLL_DIV_SEL<br>(DISPLAY) (CG) (CGM) | 9:8 | 0x0 | Pixel clock PLL feedback division selection for non-VGA modes. Used when CRTC_GEN_CNTL.CRTC_EXT_DISP_EN=1. See GENMO_WT.VGA_CKSEL for pixel clock selection when VGA mode active.<br>0=PPLL_DIV0<br>1=PPLL_DIV1<br>2=PPLL_DIV2<br>3=PPLL_DIV3 |

CG and PLL indirect register control

**CLOCK\_CNTL\_DATA - RW - 32 bits - [IOReg,MMReg:0xC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                                  |      |     |   |
|----------------------------------|------|-----|---|
| PLL_DATA<br>(DISPLAY) (CG) (CGM) | 31:0 | 0x0 | Data for write to CG and PLL indirect registers |
|----------------------------------|------|-----|---|

Data for write to CG and PLL indirect registers

**PPLL\_DIV\_0 - RW - 32 bits - CLKIND:0x4**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                      |      |       |  |
|----------------------|------|-------|--|
| PPLL_FB0_DIV<br>(CG) | 10:0 | 0x1bb | Feedback divider for pixel clock PLL.<br>PLL output to post divider is PPIIClk = PPLL_REF * PPLL_FBx_DIV / PPLL_REF_DIV.<br>PPIIClk required to always run in the 350 MHz >= PPIIClk >= 125 MHz range. For slower pixel clocks use the PPLL_POSTx_DIV field.<br>The PPLL_FBx_DIV setting must be >= 4. |
|----------------------|------|-------|--|

**PPLL\_DIV\_0 - RW - 32 bits - CLKIND:0x4**

| Field Name  | Bits  | Default | Description   |
|---|-------|---------|---|
| PPLL_ATOMIC_UPDATE_W<br><i>(mirror of<br/>PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i><br>(W)<br><br>(CG) | 15    | 0x0     | If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers. |
| PPLL_ATOMIC_UPDATE_R<br><i>(mirror of<br/>PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i><br>(R)<br><br>(CG) | 15    | 0x0     | Readback of atomic update status.   |
| PPLL_POST0_DIV<br><br>(DISPLAY)   | 18:16 | 0x0     | Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided.                                 |

Pixel clock PLL feedback and post division selection 0

**PPLL\_DIV\_1 - RW - 32 bits - CLKIND:0x5**

| Field Name  | Bits  | Default | Description   |
|---|-------|---------|---|
| PPLL_FB1_DIV<br><br>(CG)  | 10:0  | 0x1f2   | Feedback divider for pixel clock PLL.<br>PLL output to post divider is $PPIIClk = PPLL\_REF * PPLL\_FBx\_DIV / PPLL\_REF\_DIV$ .<br>PPIIClk required to always run in the 350 MHz $\geq$ PPIIClk $\geq$ 125 MHz range. For slower pixel clocks us the PPLL_POSTx_DIV field.<br>The PPLL_FBx_DIV setting must be $\geq$ 4. |
| PPLL_ATOMIC_UPDATE_W<br><i>(mirror of<br/>PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i><br>(W)<br><br>(CG) | 15    | 0x0     | If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.   |
| PPLL_ATOMIC_UPDATE_R<br><i>(mirror of<br/>PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i><br>(R)<br><br>(CG) | 15    | 0x0     | Readback of atomic update status.   |
| PPLL_POST1_DIV<br><br>(DISPLAY)   | 18:16 | 0x0     | Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided.   |

Pixel clock PLL feedback and post division selection 1

**PPLL\_DIV\_2 - RW - 32 bits - CLKIND:0x6**

| Field Name               | Bits | Default | Description   |
|--------------------------|------|---------|---|
| PPLL_FB2_DIV<br><br>(CG) | 10:0 | 0x1bb   | Feedback divider for pixel clock PLL.<br>PLL output to post divider is $PPIIClk = PPLL\_REF * PPLL\_FBx\_DIV / PPLL\_REF\_DIV$ .<br>PPIIClk required to always run in the 350 MHz $\geq$ PPIIClk $\geq$ 125 MHz range. For slower pixel clocks us the PPLL_POSTx_DIV field.<br>The PPLL_FBx_DIV setting must be $\geq$ 4. |

**PPLL\_DIV\_2 - RW - 32 bits - CLKIND:0x6**

| Field Name  | Bits  | Default | Description   |
|---|-------|---------|---|
| PPLL_ATOMIC_UPDATE_W<br><i>(mirror of<br/>PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i><br>(W)<br><br>(CG) | 15    | 0x0     | If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers. |
| PPLL_ATOMIC_UPDATE_R<br><i>(mirror of<br/>PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i><br>(R)<br><br>(CG) | 15    | 0x0     | Readback of atomic update status.   |
| PPLL_POST2_DIV<br><br>(DISPLAY)   | 18:16 | 0x0     | Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided.                                 |

Pixel clock PLL feedback and post division selection 2

**PPLL\_DIV\_3 - RW - 32 bits - CLKIND:0x7**

| Field Name  | Bits  | Default | Description  |
|---|-------|---------|--|
| PPLL_FB3_DIV<br><br>(CG)  | 10:0  | 0x1bb   | Feedback divider for pixel clock PLL.<br>PLL output to post divider is $PPIIClk = PPLL\_REF * PPLL\_FBx\_DIV / PPLL\_REF\_DIV$ .<br>PPIIClk required to always run in the 350 MHz $\geq$ PPIIClk $\geq$ 125 MHz range. For slower pixel clocks use the PPLL_POSTx_DIV field.<br>The PPLL_FBx_DIV setting must be $\geq$ 4. |
| PPLL_ATOMIC_UPDATE_W<br><i>(mirror of<br/>PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i><br>(W)<br><br>(CG) | 15    | 0x0     | If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.  |
| PPLL_ATOMIC_UPDATE_R<br><i>(mirror of<br/>PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i><br>(R)<br><br>(CG) | 15    | 0x0     | Readback of atomic update status.  |
| PPLL_POST3_DIV<br><br>(DISPLAY)   | 18:16 | 0x0     | Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided.  |

Pixel clock PLL feedback and post division selection 3

**HTOTAL\_CNTL - RW - 32 bits - CLKIND:0x9**

| Field Name                     | Bits | Default | Description  |
|--------------------------------|------|---------|--|
| HTOT_PIX_SLIP<br><br>(DISPLAY) | 3:0  | 0x0     | Pixel accurate control of horizontal total. Selects the extra number of pixels to add to each display line. Valid range is 0 to 15.<br>For VGA modes with SEQ_PCLKBY2 = 1 each increment adds one physical pixel or 1/2 a logical pixel to the line total.<br>For 9-dot 40 column VGA text modes, it is not possible to add 16/18ths or 17/18ths of a character extra to the display line times. |

**HTOTAL\_CNTL - RW - 32 bits - CLKIND:0x9**

| Field Name                         | Bits  | Default | Description   |
|------------------------------------|-------|---------|---|
| HTOT_VCLK_SLIP<br>(DISPLAY)        | 11:8  | 0x0     | Reserved for future use. No affect in this ASIC.  |
| HTOT_PPLL_SLIP<br>(CG)             | 18:16 | 0x0     | Select the number of 1/5 PPIIClk phase slips to do in the PLL at every HSYNC. This is used as a sub-pixel accurate adjustment of the frame rate for TV out or video gen-locking.                    |
| HTOT_CNTL_EDGE<br>(DISPLAY) (CG)   | 24    | 0x0     | Select which HSYNC edge the slip correction based on HTOT_PPLL_SLIP is done.  |
| HTOT_CNTL_VGA_EN<br>(DISPLAY) (CG) | 28    | 0x0     | Select if the slip controls based on HTOT_PIX_SLIP, HTOT_VCLK_SLIP and HTOT_PPLL_SLIP are enabled for VGA mode. These are always enabled for non-VGA modes when the respective fields are non-zero. |

Horizontal total control. Used to fine-tune the horizontal total. This lengthens the time of each display line by sub-character and/or sub-pixel amounts. The purpose is fine adjustment of the overall frame refresh rate for applications that require it (e.g. TV output, GEN-lock to video input).

**M\_SPLL\_REF\_FB\_DIV - RW - 32 bits - CLKIND:0xA**

| Field Name                   | Bits  | Default | Description                           |
|------------------------------|-------|---------|---------------------------------------|
| M_SPLL_REF_DIV<br>(CG) (CGM) | 7:0   | 0x0     | Memory/System PLL reference division  |
| MPLL_FB_DIV<br>(CGM)         | 15:8  | 0x0     | Memory PLL feedback division          |
| SPLL_FB_DIV<br>(CG)          | 23:16 | 0x0     | System PLL feedback division          |
| MPLL_REF_SRC_SEL<br>(CGM)    | 24    | 0x0     | 0=Normal<br>1=Cleaner one through I/O |

Memory/System PLL reference/feedback division configuration

**PLL\_TEST\_CNTL - RW - 32 bits - CLKIND:0x13**

| Field Name                    | Bits  | Default | Description  |
|-------------------------------|-------|---------|--|
| TST_SRC_SEL<br>(CG) (CGM)     | 6:0   | 0x0     | Select different clock source to readable counter and as test clock output |
| TST_SRC_INV<br>(CG) (CGM)     | 7     | 0x0     | Invert test clock output   |
| TST_DIVIDERS<br>(CG) (CGM)    | 8     | 0x0     | Enable driver test   |
| PLL_MASK_READ_B<br>(CG) (CGM) | 9     | 0x1     | Mask test clock output and 3 LSBs of readable counter                      |
| TESTCLK_MUX_SEL<br>(CG)       | 12    | 0x0     | 0=cg<br>1=cgm  |
| ANALOG_MON<br>(DISPLAY)       | 23:15 | 0x0     |  |
| TEST_COUNT (R)<br>(CG) (CGM)  | 31:24 | 0x0     | Readable counter read back   |

CG and PLL test control

**P2PLL\_DIV\_0 - RW - 32 bits - CLKIND:0x2C**

| Field Name  | Bits  | Default | Description  |
|---|-------|---------|--|
| P2PLL_FB_DIV<br>(CG)  | 10:0  | 0x0     |  |
| P2PLL_ATOMIC_UPDATE_W<br><i>(mirror of P2PLL_REF_DIV:P2PLL_ATOMIC_UPDATE_W)</i> (W)<br>(CG) | 15    | 0x0     |  |
| P2PLL_ATOMIC_UPDATE_R<br><i>(mirror of P2PLL_REF_DIV:P2PLL_ATOMIC_UPDATE_R)</i> (R)<br>(CG) | 15    | 0x0     |  |
| P2PLL_POST_DIV<br>(DISPLAY)   | 18:16 | 0x0     | 0=V2CLK = V2CLK_SRC<br>1=V2CLK = V2CLK_SRC/2<br>2=V2CLK = V2CLK_SRC/4<br>3=V2CLK = V2CLK_SRC/8<br>4=V2CLK = V2CLK_SRC/3<br>5=reserved<br>6=V2CLK = V2CLK_SRC/6<br>7=V2CLK = V2CLK_SRC/12 |

No description available for this register.

**HTOTAL2\_CNTL - RW - 32 bits - CLKIND:0x2E**

| Field Name                        | Bits  | Default | Description |
|-----------------------------------|-------|---------|-------------|
| HTOT2_PIX_SLIP<br>(DISPLAY)       | 3:0   | 0x0     |             |
| HTOT2_PIX2CLK_SLIP<br>(DISPLAY)   | 11:8  | 0x0     |             |
| HTOT2_P2PLL_SLIP<br>(CG)          | 18:16 | 0x0     |             |
| HTOT2_CNTL_EDGE<br>(DISPLAY) (CG) | 24    | 0x0     |             |
| HTOT2_CNTL_UPDATE<br>(CG)         | 28    | 0x0     |             |

No description available for this register.

**6. MemClockGenerator Detailed Register Reference**

## Memory Clock Generator Control Registers

| CLK_PWRMGT_CNTL - RW - 32 bits - CLKIND:0x14 |       |         |   |
|--|-------|---------|---|
| Field Name                                   | Bits  | Default | Description   |
| MPLL_PWRMGT_OFF<br>(CGM)                     | 0     | 0x0     | M domain clock power management off   |
| SPLL_PWRMGT_OFF<br>(CG)                      | 1     | 0x0     | S domain clock power management off   |
| PPLL_PWRMGT_OFF<br>(CG)                      | 2     | 0x0     | Pixel clock power management off  |
| P2PLL_PWRMGT_OFF<br>(CG)                     | 3     | 0x0     |   |
| MCLK_TURNOFF<br>(CGM)                        | 4     | 0x0     | Turn off M domain clocks  |
| SCLK_TURNOFF<br>(CG)                         | 5     | 0x0     | Turn off S domain clocks  |
| PCLK_TURNOFF<br>(CG)                         | 6     | 0x0     | Turn off pixel clocks   |
| P2CLK_TURNOFF<br>(CG)                        | 7     | 0x0     |   |
| MC_CH_MODE<br>(CGM)                          | 8     | 0x1     | 0=single channel<br>1=dual channel  |
| TEST_MODE<br>(CG) (CGM)                      | 9     | 0x0     | Disable long internal timing to speed up regression tests                           |
| GLOBAL_PMAN_EN<br>(CG)                       | 10    | 0x0     | 0=Power managment off<br>1=Power managment on                                       |
| ENGINE_DYNCLK_MODE<br>(CG)                   | 12    | 0x1     | 0=Provide Clock for each Eng block separately<br>1=Treat Engine as one single block |
| ACTIVE_HILO_LAT<br>(CG)                      | 14:13 | 0x3     | 0=5 clocks<br>1=12 clocks<br>2=20 clocks<br>3=32 clocks                             |
| DISP_DYN_STOP_LAT<br>(CG)                    | 15    | 0x0     | 0=10 clocks<br>1=20 clocks  |
| MC_BUSY (R)<br>(CGM)                         | 16    | 0x0     | 0=MC is idle<br>1=MC is busy  |
| MC_INT_CNTL<br>(CGM)                         | 17    | 0x0     | 0=HW control<br>1=SW over-ride  |
| MC_SWITCH<br>(CGM)                           | 18    | 0x0     | 0=source of memory clock is not changed<br>1=source of memory clock is changed      |
| DLL_READY<br>(CGM)                           | 19    | 0x0     | 0=DLL is not ready<br>1=DLL is ready  |

**CLK\_PWRMGT\_CNTL - RW - 32 bits - CLKIND:0x14**

| Field Name                 | Bits  | Default | Description  |
|----------------------------|-------|---------|--|
| DISP_PM<br>(CG)            | 20    | 0x0     | 0=display clocks running in PM modes<br>1=clocks OFF |
| DYN_STOP_MODE<br>(CG)      | 23:21 | 0x7     | 0=10 clocks<br>7=111 = 140 clocks                    |
| CG_NO1_DEBUG<br>(CG) (CGM) | 29:24 | 0x0     | 1st 16-bit hardware debug register                   |
| TVPLL_PWRMGT_OFF<br>(CG)   | 30    | 0x0     |  |
| TVCLK_TURNOFF<br>(CG)      | 31    | 0x0     |  |

Clock power management control

**PLL\_PWRMGT\_CNTL - RW - 32 bits - CLKIND:0x15**

| Field Name                  | Bits  | Default | Description   |
|-----------------------------|-------|---------|---|
| MPLL_TURNOFF<br>(CGM)       | 0     | 0x0     | Enable M domain PLL to be turned off at power state D3                          |
| SPLL_TURNOFF<br>(CG)        | 1     | 0x0     | Enable S domain PLL to be turned off at power state D3                          |
| PPLL_TURNOFF<br>(CG)        | 2     | 0x0     | Enable pixel clock PLL to be turned off at power state D3                       |
| P2PLL_TURNOFF<br>(CG)       | 3     | 0x0     |   |
| TVPLL_TURNOFF<br>(CG)       | 4     | 0x0     |   |
| AGPCLK_DYN_STOP_LAT<br>(CG) | 8:5   | 0x0     |   |
| APM_POWER_STATE<br>(CG)     | 10:9  | 0x0     |   |
| APM_PWRSTATE_RD (R)<br>(CG) | 12:11 | 0x0     |   |
| PM_MODE_SEL<br>(CG)         | 13    | 0x0     | 0=ACPI<br>1=APM   |
| EN_PWRSEQ_DONE_COND<br>(CG) | 14    | 0x1     | 0=Switch states without PWRSEQ_DONE rising edge condition<br>1=Enable condition |
| EN_DISP_PARKED_COND<br>(CG) | 15    | 0x1     | 0=Switch states without DISP_PARKED condition<br>1=Enable condition             |
| MOBILE_SU<br>(CG)           | 16    | 0x1     | 0=Regular<br>1=Optimize power consumption in Suspend mode                       |
| SU_SCLK_USE_BCLK<br>(CG)    | 17    | 0x1     | 1=During Suspend, SCLK is sourced from BCLK                                     |
| SU_MCLK_USE_BCLK<br>(CG)    | 18    | 0x1     | 1=During Suspend, MCLK is sourced from BCLK                                     |

**PLL\_PWRMGT\_CNTL - RW - 32 bits - CLKIND:0x15**

| Field Name                      | Bits  | Default | Description                                     |
|---------------------------------|-------|---------|---|
| SU_SUSTAIN_DISABLE<br>(CG)      | 19    | 0x0     | 0=Sustain Suspend until PLL lockup<br>1=Disable |
| TCL_BYPASS_DISABLE<br>(CG)      | 20    | 0x0     | 0=Enable TCL_SCLK power management<br>1=Disable |
| TCL_CLOCK_ACTIVE_RD (R)<br>(CG) | 21    | 0x0     | 0=TCL_SCLK stopped<br>1=TCL_SCLK running        |
| CG_NO2_DEBUG<br>(CG) (CGM)      | 31:24 | 0x0     | 2nd 16-bit hardware debug register              |

PLL power management control

**MPLL\_CNTL - RW - 32 bits - CLKIND:0xE**

| Field Name       | Bits  | Default | Description                                  |
|------------------|-------|---------|--|
| MPLL_RESET       | 0     | 0x1     | Reset M domain PLL<br>0=Not Reset<br>1=Reset |
| MPLL_SLEEP       | 1     | 0x1     | Power down M domain PLL<br>1=Powerdown       |
| MPLL_TST_EN      | 2     | 0x0     | Enable M domain PLL test mode                |
| MPLL_REFCLK_SEL  | 4     | 0x0     | 0=not flopped<br>1=flopped                   |
| MPLL_FBCLK_SEL   | 5     | 0x0     | 0=not flopped<br>1=flopped                   |
| MPLL_TCPOFF      | 6     | 0x0     | 0=normal<br>1=test mode: Hi-Z                |
| MPLL_TVCOMAX     | 7     | 0x0     | 0=normal<br>1=test mode: runaway             |
| MPLL_PCP         | 10:8  | 0x4     | Program M domain PLL charge pump             |
| MPLL_PVG         | 13:11 | 0x4     | Program M domain PLL VCO gain                |
| MPLL_PDC         | 15:14 | 0x1     | Program M domain clock duty cycle            |
| MPLL_X1_CLK_SKEW | 18:16 | 0x0     |  |
| MPLL_X2_CLK_SKEW | 22:20 | 0x0     |  |
| MPLL_MODE        | 27:24 | 0x4     |  |

M domain PLL control

**MDLL\_CKO - RW - 32 bits - CLKIND:0xF**

| Field Name  | Bits | Default | Description              |
|-------------|------|---------|--------------------------|
| MCKOA_SLEEP | 0    | 0x1     | 0=Enabled<br>1=PowerDown |
| MCKOA_RESET | 1    | 0x1     | 0=Enabled<br>1=Reset     |
| MCKOA_RANGE | 3:2  | 0x2     |                          |

**MDLL\_CKO - RW - 32 bits - CLKIND:0xF**

| Field Name     | Bits  | Default | Description   |
|----------------|-------|---------|---|
| ERSTA_SOUTSEL  | 5:4   | 0x1     | 1=no delay<br>2=2 elements<br>3=4 elements                  |
| MCKOA_FB_SEL   | 7:6   | 0x1     | 0=raw feedback<br>1=delayed feedback<br>2=internal feedback |
| MCKOA_REF_SKEW | 10:8  | 0x0     |   |
| MCKOA_FB_SKEW  | 14:12 | 0x0     |   |
| MCKOA_BP_SEL   | 15    | 0x1     | 0=DLL clock<br>1=MCLK                                       |
| MCKOB_SLEEP    | 16    | 0x1     | 0=Enabled<br>1=PowerDown                                    |
| MCKOB_RESET    | 17    | 0x1     | 0=Enabled<br>1=Reset  |
| MCKOB_RANGE    | 19:18 | 0x2     |   |
| ERSTB_SOUTSEL  | 21:20 | 0x1     | 1=no delay<br>2=2 elements<br>3=4 elements                  |
| MCKOB_FB_SEL   | 23:22 | 0x1     | 0=raw feedback<br>1=delayed feedback<br>2=internal feedback |
| MCKOB_REF_SKEW | 26:24 | 0x0     |   |
| MCKOB_FB_SKEW  | 30:28 | 0x0     |   |
| MCKOB_BP_SEL   | 31    | 0x1     | 0=DLL clock<br>1=MCLK                                       |

No description available for this register.

**MDLL\_RDCKA - RW - 32 bits - CLKIND:0x10**

| Field Name       | Bits  | Default | Description   |
|------------------|-------|---------|---|
| MRDCKA0_SLEEP    | 0     | 0x1     | 0=Enabled<br>1=PowerDown                                  |
| MRDCKA0_RESET    | 1     | 0x1     | 0=Enabled<br>1=Reset                                      |
| MRDCKA0_RANGE    | 3:2   | 0x2     |   |
| MRDCKA0_REF_SEL  | 5:4   | 0x0     | 0=MCLK<br>1=QSA0 pad<br>2=delayed HCLK1 feedback          |
| MRDCKA0_FB_SEL   | 7:6   | 0x0     | 0=strobe leaf node<br>1=logic zero<br>2=internal feedback |
| MRDCKA0_REF_SKEW | 10:8  | 0x0     |   |
| MRDCKA0_SINSEL   | 11    | 0x0     | 0=read strobe per 32 bits<br>1=read strobe per 8 bits     |
| MRDCKA0_FB_SKEW  | 14:12 | 0x0     |   |
| MRDCKA0_BP_SEL   | 15    | 0x1     | 0=DLL clock<br>1=MCLK                                     |

**MDLL\_RDCKA - RW - 32 bits - CLKIND:0x10**

| Field Name       | Bits  | Default | Description   |
|------------------|-------|---------|---|
| MRDCKA1_SLEEP    | 16    | 0x1     | 0=Enabled<br>1=PowerDown                                  |
| MRDCKA1_RESET    | 17    | 0x1     | 0=Enabled<br>1=Reset                                      |
| MRDCKA1_RANGE    | 19:18 | 0x2     |   |
| MRDCKA1_REF_SEL  | 21:20 | 0x0     | 0=MCLK<br>1=QSA4 pad<br>2=delayed HCLK1 feedback          |
| MRDCKA1_FB_SEL   | 23:22 | 0x0     | 0=strobe leaf node<br>1=logic zero<br>2=internal feedback |
| MRDCKA1_REF_SKEW | 26:24 | 0x0     |   |
| MRDCKA1_SINSEL   | 27    | 0x0     | 0=read strobe per 32 bits<br>1=read strobe per 8 bits     |
| MRDCKA1_FB_SKEW  | 30:28 | 0x0     |   |
| MRDCKA1_BP_SEL   | 31    | 0x1     | 0=DLL clock<br>1=MCLK                                     |

No description available for this register.

**MCLK\_CNTL - RW - 32 bits - CLKIND:0x12**

| Field Name    | Bits | Default | Description   |
|---------------|------|---------|---|
| MCLKA_SRC_SEL | 2:0  | 0x0     | 0=PCICLK<br>1=MPLLCLK/1<br>2=MPLLCLK/2<br>3=MPLLCLK/4<br>4=MPLLCLK/8<br>5=External Source/Scan Clock (GPIO13 pin)<br>6=Test clock from test controller<br>7=SPLL    |
| YCLKA_SRC_SEL | 6:4  | 0x0     | 0=PCICLK<br>1=MPLLCLK/1<br>2=MPLLCLK/2<br>3=MPLLCLK/4<br>4=MPLLCLK/8<br>5=External Source/Scan Clock (GPIO12 pin)<br>6=Test clock from test controller<br>7=SPLL    |
| MCLKB_SRC_SEL | 10:8 | 0x0     | 0=PCICLK<br>1=MPLLCLK/1<br>2=MPLLCLK/2<br>3=MPLLCLK/4<br>4=MPLLCLK/8<br>5=External Source/Scan Clock (CLKAFB pin)<br>6=Test clock from test controller<br>7=Stopped |

**MCLK\_CNTL - RW - 32 bits - CLKIND:0x12**

| Field Name      | Bits  | Default | Description   |
|-----------------|-------|---------|---|
| YCLKB_SRC_SEL   | 14:12 | 0x0     | 0=PCICLK<br>1=MPLLCLK/1<br>2=MPLLCLK/2<br>3=MPLLCLK/4<br>4=MPLLCLK/8<br>5=External Source/Scan Clock (CLKBFB pin)<br>6=Test clock from test controller<br>7=Stopped |
| FORCE_MCLKA     | 16    | 0x1     | 0=Dynamic<br>1=ForceOn  |
| FORCE_MCLKB     | 17    | 0x1     | 0=Dynamic<br>1=ForceOn  |
| FORCE_YCLKA     | 18    | 0x1     | 0=Dynamic<br>1=ForceOn  |
| FORCE_YCLKB     | 19    | 0x1     | 0=Dynamic<br>1=ForceOn  |
| FORCE_MC        | 20    | 0x1     | 0=Dynamic<br>1=ForceOn  |
| FORCE_AIC       | 21    | 0x1     | 0=Dynamic<br>1=ForceOn  |
| MRDCKA0_SOUTSEL | 25:24 | 0x0     | 0=DLL output clock<br>1=QS pin<br>2=QS delayed 2 elements<br>3=QS delayed 4 elements  |
| MRDCKA1_SOUTSEL | 27:26 | 0x0     | 0=DLL output clock<br>1=QS pin<br>2=QS delayed 2 elements<br>3=QS delayed 4 elements  |
| MRDCKB0_SOUTSEL | 29:28 | 0x0     | 0=DLL output clock<br>1=QS pin<br>2=QS delayed 2 elements<br>3=QS delayed 4 elements  |
| MRDCKB1_SOUTSEL | 31:30 | 0x0     | 0=DLL output clock<br>1=QS pin<br>2=QS delayed 2 elements<br>3=QS delayed 4 elements  |

No description available for this register.

**MCLK\_MISC - RW - 32 bits - CLKIND:0x1F**

| Field Name                 | Bits | Default | Description   |
|----------------------------|------|---------|---|
| SCLK_SOURCED_FROM_MPLL_SEL | 1:0  | 0x0     | 0=MPLLBY1<br>1=MPLLBY1b<br>2=MPLLBY2<br>3=MPLLBY2b                                      |
| MCLK_FROM_SPLL_DIV_SEL     | 2    | 0x0     | 0=selection of MYCLK_SOURCED_FROM_SPLL_SEL<br>1=MYCLK_SOURCED_FROM_SPLL_SEL divided BY2 |
| ENABLE_SCLK_FROM_MPLL      | 3    | 0x0     | 0=clock stop<br>1=clock run   |

**MCLK\_MISC - RW - 32 bits - CLKIND:0x1F**

| Field Name                  | Bits  | Default | Description   |
|-----------------------------|-------|---------|---|
| MPLL_MODEA_MODEC_HW_SEL_EN  | 4     | 0x0     | 0=Hardware selects output source select for CLK1 and CLK3<br>1=Software override for MPLL CLK1 and CLK3 |
| DLL_READY_LAT               | 8     | 0x0     | 0=min latency<br>1=max latency  |
| MC_MCLK_MAX_DYN_STOP_LAT    | 12    | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency                               |
| IO_MCLK_MAX_DYN_STOP_LAT    | 13    | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency                               |
| MC_MCLK_DYN_ENABLE          | 14    | 0x0     | 0=MC_MCLK is the same as MCLKA/MCLKB<br>1=Dynamic stopping enabled                                      |
| IO_MCLK_DYN_ENABLE          | 15    | 0x0     | 0=IO_MCLK is the same as MCLKA/MCLKB<br>1=Dynamic stopping enabled                                      |
| CGM_CLK_TO_OUTPIN           | 16    | 0x0     | 0=disabled<br>1=send out selected clock for jitter test   |
| CLK_OR_COUNT_SEL            | 17    | 0x0     | 0=select TST_MUX_CLK<br>1=select COUNT_UP   |
| EN_MCLK_TRISTATE_IN_SUSPEND | 18    | 0x0     | 0=disable<br>1=tristate MCLK in ACPI/APM Suspend  |
| CGM_SPARE_RD (R)            | 21:20 | 0x0     |   |
| CGM_SPARE_A_RD (R)          | 23:22 | 0x0     |   |
| TCLK_TO_YCLKB_EN            | 24    | 0x0     | 0=Disable TCLK to YCLKB in normal mode<br>1=Enable TCLK to YCLKB in normal mode                         |
| CGM_SPARE_A                 | 27:25 | 0x0     |   |

No description available for this register.

**CLOCK\_CNTL\_INDEX - RW - 32 bits - [IOReg,MMReg:0x8]**

| Field Name                           | Bits | Default | Description   |
|--------------------------------------|------|---------|---|
| PLL_ADDR<br>(DISPLAY) (CG) (CGM)     | 5:0  | 0x0     | Indirect CG and PLL register index  |
| PLL_WR_EN<br>(DISPLAY) (CG) (CGM)    | 7    | 0x0     | Indirect CG and PLL register write enable<br>0=Disable writes to CLOCK_CNTL_DATA<br>1=Enable writing to CLOCK_CNTL_DATA   |
| PPLL_DIV_SEL<br>(DISPLAY) (CG) (CGM) | 9:8  | 0x0     | Pixel clock PLL feedback division selection for non-VGA modes. Used when CRTC_GEN_CNTL.CRTC_EXT_DISP_EN=1. See GENMO_WT.VGA_CKSEL for pixel clock selection when VGA mode active.<br>0=PPLL_DIV0<br>1=PPLL_DIV1<br>2=PPLL_DIV2<br>3=PPLL_DIV3 |

CG and PLL indirect register control

**CLOCK\_CNTL\_DATA - RW - 32 bits - [IOReg,MMReg:0xC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



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**CLOCK\_CNTL\_DATA - RW - 32 bits - [IOReg,MMReg:0xC]**

| Field Name                       | Bits | Default | Description                                     |
|----------------------------------|------|---------|---|
| PLL_DATA<br>(DISPLAY) (CG) (CGM) | 31:0 | 0x0     | Data for write to CG and PLL indirect registers |

Data for write to CG and PLL indirect registers

**M\_SPLL\_REF\_FB\_DIV - RW - 32 bits - CLKIND:0xA**

| Field Name                   | Bits  | Default | Description                           |
|------------------------------|-------|---------|---------------------------------------|
| M_SPLL_REF_DIV<br>(CG) (CGM) | 7:0   | 0x0     | Memory/System PLL reference division  |
| MPLL_FB_DIV<br>(CGM)         | 15:8  | 0x0     | Memory PLL feedback division          |
| SPLL_FB_DIV<br>(CG)          | 23:16 | 0x0     | System PLL feedback division          |
| MPLL_REF_SRC_SEL<br>(CGM)    | 24    | 0x0     | 0=Normal<br>1=Cleaner one through I/O |

Memory/System PLL reference/feedback division configuration



## 7. ClkCntl Detailed Register Reference

Clock control registers

| CLOCK_CNTL_INDEX - RW - 32 bits - [IOReg,MMReg:0x8] |      |         |   |
|---|------|---------|---|
| Field Name  | Bits | Default | Description   |
| PLL_ADDR<br>(DISPLAY) (CG) (CGM)                    | 5:0  | 0x0     | Indirect CG and PLL register index  |
| PLL_WR_EN<br>(DISPLAY) (CG) (CGM)                   | 7    | 0x0     | Indirect CG and PLL register write enable<br>0=Disable writes to CLOCK_CNTL_DATA<br>1=Enable writing to CLOCK_CNTL_DATA   |
| PPLL_DIV_SEL<br>(DISPLAY) (CG) (CGM)                | 9:8  | 0x0     | Pixel clock PLL feedback division selection for non-VGA modes. Used when CRTC_GEN_CNTL.CRTC_EXT_DISP_EN=1. See GENMO_WT.VGA_CKSEL for pixel clock selection when VGA mode active.<br>0=PPLL_DIV0<br>1=PPLL_DIV1<br>2=PPLL_DIV2<br>3=PPLL_DIV3 |

CG and PLL indirect register control

| CLOCK_CNTL_DATA - RW - 32 bits - [IOReg,MMReg:0xC] |      |         |   |
|--|------|---------|---|
| Field Name   | Bits | Default | Description                                     |
| PLL_DATA<br>(DISPLAY) (CG) (CGM)                   | 31:0 | 0x0     | Data for write to CG and PLL indirect registers |

Data for write to CG and PLL indirect registers

| PPLL_DIV_0 - RW - 32 bits - CLKIND:0x4  |       |         |  |
|---|-------|---------|--|
| Field Name  | Bits  | Default | Description  |
| PPLL_FB0_DIV<br>(CG)  | 10:0  | 0x1bb   | Feedback divider for pixel clock PLL.<br>PLL output to post divider is PPIIClk = PPLL_REF * PPLL_FBx_DIV / PPLL_REF_DIV.<br>PPIIClk required to always run in the 350 MHz >= PPIIClk >= 125 MHz range. For slower pixel clocks use the PPLL_POSTx_DIV field.<br>The PPLL_FBx_DIV setting must be >= 4. |
| PPLL_ATOMIC_UPDATE_W<br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i><br>(W)<br>(CG) | 15    | 0x0     | If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.  |
| PPLL_ATOMIC_UPDATE_R<br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i><br>(R)<br>(CG) | 15    | 0x0     | Readback of atomic update status.  |
| PPLL_POST0_DIV<br>(DISPLAY)   | 18:16 | 0x0     | Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided.  |

Pixel clock PLL feedback and post division selection 0

**PPLL\_DIV\_1 - RW - 32 bits - CLKIND:0x5**

| Field Name  | Bits  | Default | Description   |
|---|-------|---------|---|
| PPLL_FB1_DIV<br><br>(CG)  | 10:0  | 0x1f2   | Feedback divider for pixel clock PLL.<br>PLL output to post divider is $PPllClk = PPLL\_REF * PPLL\_FBx\_DIV / PPLL\_REF\_DIV$ .<br>PPllClk required to always run in the 350 MHz $\geq$ PPllClk $\geq$ 125 MHz range. For slower pixel clocks us the PPLL_POSTx_DIV field.<br>The PPLL_FBx_DIV setting must be $\geq$ 4. |
| PPLL_ATOMIC_UPDATE_W<br><br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i><br>(W)<br><br>(CG) | 15    | 0x0     | If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.   |
| PPLL_ATOMIC_UPDATE_R<br><br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i><br>(R)<br><br>(CG) | 15    | 0x0     | Readback of atomic update status.   |
| PPLL_POST1_DIV<br><br>(DISPLAY)   | 18:16 | 0x0     | Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided.   |

Pixel clock PLL feedback and post division selection 1

**PPLL\_DIV\_2 - RW - 32 bits - CLKIND:0x6**

| Field Name  | Bits  | Default | Description   |
|---|-------|---------|---|
| PPLL_FB2_DIV<br><br>(CG)  | 10:0  | 0x1bb   | Feedback divider for pixel clock PLL.<br>PLL output to post divider is $PPllClk = PPLL\_REF * PPLL\_FBx\_DIV / PPLL\_REF\_DIV$ .<br>PPllClk required to always run in the 350 MHz $\geq$ PPllClk $\geq$ 125 MHz range. For slower pixel clocks us the PPLL_POSTx_DIV field.<br>The PPLL_FBx_DIV setting must be $\geq$ 4. |
| PPLL_ATOMIC_UPDATE_W<br><br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i><br>(W)<br><br>(CG) | 15    | 0x0     | If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.   |
| PPLL_ATOMIC_UPDATE_R<br><br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i><br>(R)<br><br>(CG) | 15    | 0x0     | Readback of atomic update status.   |
| PPLL_POST2_DIV<br><br>(DISPLAY)   | 18:16 | 0x0     | Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided.   |

Pixel clock PLL feedback and post division selection 2

**PPLL\_DIV\_3 - RW - 32 bits - CLKIND:0x7**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**PPLL\_DIV\_3 - RW - 32 bits - CLKIND:0x7**

| Field Name  | Bits  | Default | Description   |
|---|-------|---------|---|
| PPLL_FB3_DIV<br>(CG)  | 10:0  | 0x1bb   | Feedback divider for pixel clock PLL.<br>PLL output to post divider is PPIIClk = PPLL_REF * PPLL_FBx_DIV / PPLL_REF_DIV.<br>PPIIClk required to always run in the 350 MHz >= PPIIClk >= 125 MHz range. For slower pixel clocks us the PPLL_POSTx_DIV field.<br>The PPLL_FBx_DIV setting must be >= 4. |
| PPLL_ATOMIC_UPDATE_W<br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i><br>(W)<br>(CG) | 15    | 0x0     | If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.   |
| PPLL_ATOMIC_UPDATE_R<br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i><br>(R)<br>(CG) | 15    | 0x0     | Readback of atomic update status.   |
| PPLL_POST3_DIV<br>(DISPLAY)   | 18:16 | 0x0     | Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided.   |

Pixel clock PLL feedback and post division selection 3

**VCLK\_ECP\_CNTL - RW - 32 bits - CLKIND:0x8**

| Field Name            | Bits | Default | Description  |
|-----------------------|------|---------|--|
| VCLK_SRC_SEL          | 1:0  | 0x0     | Selects source of PIXCLK. The output of this mux selection is post divided by PPLL_POSTx_DIV to create the final PIXCLK.<br>If set to BYTE_CLK, then see BYTE_CLK_POST_DIV below to select the PIXCLK source.<br>Both the clock source you are switching to and from must be running, or the switch will not occur.<br>0=CPUCLK<br>1=PSCANCLK<br>2=BYTE_CLK<br>3=PPIIClk |
| VCLK_INVERT           | 4    | 0x0     | Used to invert PPIIClk to get opposite duty cycle. Only takes effect when VCLK_SRC_SEL is using PPIIClk, and PPLL_POSTx_DIV is divide-by-1. Don't care in other cases.<br>0=Not Invert<br>1=Invert   |
| PIXCLK_SRC_INVERT     | 5    | 0x0     | Used to invert PIXCLK_SRC to get opposite duty cycle.<br>0=Not Invert<br>1=Invert  |
| PIXCLK_ALWAYS_ONb     | 6    | 0x0     | 0=PIXCLK is on regardless of CRTC_PIX_WIDTH field (should be set to zero in VGA mode)<br>1=PIXCLK is off if CRTC_PIX_WIDTH is 0 otherwise PIXCLK is on   |
| PIXCLK_DAC_ALWAYS_ONb | 7    | 0x0     | 0=PIXCLK is always on<br>1=PIXCLK is off during blank time   |

**VCLK\_ECP\_CNTL - RW - 32 bits - CLKIND:0x8**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| ECP_DIV         | 9:8  | 0x0     | OV0CLK clock speed select.<br>Should always be set to 00 for PIXCLK <= 175 MHz and to 01 for PIXCLK > 175 MHz. When set to 01, the overlay and subpic horizontal scale parameters must be adjusted for the extra horizontal replication this causes. Settings 10 and 11 are reserved.<br>0=VCLK<br>1=VCLK/2 |
| ECP_FORCE_ON    | 18   | 0x0     | Controls the dynamic clock control for the back-end overlay/scaler. Set to low for power reduction.<br>0=SCALER ACTIVITY<br>1=CONTINUOUS  |
| SUBCLK_FORCE_ON | 19   | 0x0     | 0=SUBPIC ACTIVITY<br>1=CONTINUOUS   |

General controls for the display clocks.

VCLK is the pixel, or dot, clock.

ECP is the overlay/scaler clock.

**PIXCLKS\_CNTL - RW - 32 bits - CLKIND:0x2D**

| Field Name                 | Bits | Default | Description   |
|----------------------------|------|---------|---|
| PIX2CLK_SRC_SEL            | 1:0  | 0x0     | 0=PIX2CLK_SRC = CPUCLK (input pin)<br>1=PIX2CLK_SRC = PSCANCLK (input pin)<br>2=Reserved<br>3=PIX2CLK_SRC = P2PIIClk    |
| PIX2CLK_INVERT             | 4    | 0x0     | 0=Not Invert<br>1=Invert  |
| PIX2CLK_SRC_INVERT         | 5    | 0x0     | 0=Not Invert<br>1=Invert  |
| PIX2CLK_ALWAYS_ONb         | 6    | 0x0     | 0=PIX2CLK is on regardless of CRTC2_PIX_WIDTH field<br>1=PIX2CLK is off if CRTC2_PIX_WIDTH is 0 otherwise PIX2CLK is on |
| PIX2CLK_DAC_ALWAYS_ONb     | 7    | 0x0     | 0=PIX2CLK is always on<br>1=PIX2CLK is off during blank time  |
| PIXCLK_TV_SRC_SEL          | 8    | 0x0     | 0=PIXCLK_TV = PIXCLK<br>1=PIXCLK_TV = PIX2CLK   |
| PIXCLK_BLEND_ALWAYS_ONb    | 11   | 0x0     | 0=1 = Enable dynamic stopping for PIXCLK_BLEND  |
| PIXCLK_GV_ALWAYS_ONb       | 12   | 0x0     | 0=1 = Enable dynamic stopping for PIXCLK_GV   |
| PIXCLK_DIG_TMDS_ALWAYS_ONb | 13   | 0x0     |   |
| PIXCLK_LVDS_ALWAYS_ONb     | 14   | 0x0     |   |
| PIXCLK_TMDS_ALWAYS_ONb     | 15   | 0x0     |   |

No description available for this register.

**P2PLL\_DIV\_0 - RW - 32 bits - CLKIND:0x2C**

| Field Name           | Bits | Default | Description |
|----------------------|------|---------|-------------|
| P2PLL_FB_DIV<br>(CG) | 10:0 | 0x0     |             |



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**P2PLL\_DIV\_0 - RW - 32 bits - CLKIND:0x2C**

| Field Name   | Bits  | Default | Description  |
|--|-------|---------|--|
| P2PLL_ATOMIC_UPDATE_W<br><i>(mirror of<br/>P2PLL_REF_DIV:P2PLL_ATOMIC_UPDATE_</i><br><i>W) (W)</i><br><br>(CG) | 15    | 0x0     |  |
| P2PLL_ATOMIC_UPDATE_R<br><i>(mirror of<br/>P2PLL_REF_DIV:P2PLL_ATOMIC_UPDATE_</i><br><i>R) (R)</i><br><br>(CG) | 15    | 0x0     |  |
| P2PLL_POST_DIV<br><br>(DISPLAY)  | 18:16 | 0x0     | 0=V2CLK = V2CLK_SRC<br>1=V2CLK = V2CLK_SRC/2<br>2=V2CLK = V2CLK_SRC/4<br>3=V2CLK = V2CLK_SRC/8<br>4=V2CLK = V2CLK_SRC/3<br>5=reserved<br>6=V2CLK = V2CLK_SRC/6<br>7=V2CLK = V2CLK_SRC/12 |

No description available for this register.

**8. MemoryController Detailed Register Reference**

## Memory Controller Registers

| MEM_CNTL - RW - 32 bits - [MMReg:0x140] |       |         |  |
|---|-------|---------|--|
| Field Name                              | Bits  | Default | Description  |
| MEM_NUM_CHANNELS                        | 0     | 0x0     | 0=One channel<br>1=Two channels  |
| MC_USE_B_CH_ONLY                        | 1     | 0x0     | 0=Use A channel in 1 channel system<br>1=Use B channel in 1 channel system |
| DISABLE_AP                              | 2     | 0x0     | 0=Auto-Precharge Enabled<br>1=Auto-Precharge Disabled                      |
| MEM_CHANNEL_MAPPING                     | 3     | 0x0     | 0=Interleave on 128 bytes<br>1=Interleave on 256 bytes                     |
| MEM_BANK_MAPPING_A                      | 7:4   | 0x0     | 0=Reserved   |
| MEM_ADDR_MAPPING_A                      | 15:8  | 0x0     |  |
| MEM_BANK_MAPPING_B                      | 23:20 | 0x0     | 0=Reserved   |
| MEM_ADDR_MAPPING_B                      | 31:24 | 0x0     |  |

No description available for this register.

| MC_FB_LOCATION - RW - 32 bits - [MMReg:0x148] |       |         |  |
|---|-------|---------|--|
| Field Name                                    | Bits  | Default | Description  |
| MC_FB_START<br>(MC) (HDP)                     | 15:0  | 0x0     | Start of local frame buffer section of 32 bit internal address space. Recommend setting this register to same as CONFIG_APER_0_BASE.APER_0_BASE shr 16.<br><br>NOTE: Bits 0:5 of this field are hardwired to ZERO.                         |
| MC_FB_TOP<br>(MC)                             | 31:16 | 0x3f    | End of local frame buffer section of 32 bit internal address space. Recommend setting this register to (CONFIG_APER_0_BASE.APER_0_BASE + CONFIG_APER_SIZE.APER_SIZE - 1) shr 16.<br><br>NOTE: Bits 0:5 of this field are hardwired to ONE. |

This register defines the location of the frame buffer in the internal address space. The internal address space has 32 address bits. Minimum Frame buffer size for Rage 5 is 2 MB, and the start location is required to be on a 4 MB boundry. Therefore START(21:0) must be 0x000000 and TOP(21:0) must be 0x3FFFFFF. Only the 16 MSBs of each are loaded in the register.

| MC_AGP_LOCATION - RW - 32 bits - [MMReg:0x14C] |       |         |   |
|--|-------|---------|---|
| Field Name                                     | Bits  | Default | Description   |
| MC_AGP_START                                   | 15:0  | 0x0     | NOTE: Bits 0:5 of this field are hardwired to ZERO. |
| MC_AGP_TOP                                     | 31:16 | 0x3f    | NOTE: Bits 0:5 of this field are hardwired to ONE.  |

No description available for this register.

| MEM_INIT_LATENCY_TIMER - RW - 32 bits - [MMReg:0x154] |       |         |             |
|---|-------|---------|-------------|
| Field Name  | Bits  | Default | Description |
| MEM_RB0R_INIT_LAT                                     | 3:0   | 0x0     |             |
| MEM_RB1R_INIT_LAT                                     | 7:4   | 0x0     |             |
| MEM_PPR_INIT_LAT                                      | 11:8  | 0x0     |             |
| MEM_DISPR_INIT_LAT                                    | 15:12 | 0x0     |             |

**MEM\_INIT\_LATENCY\_TIMER - RW - 32 bits - [MMReg:0x154]**

| Field Name         | Bits  | Default | Description |
|--------------------|-------|---------|-------------|
| MEM_RB0W_INIT_LAT  | 19:16 | 0x0     |             |
| MEM_RB1W_INIT_LAT  | 23:20 | 0x0     |             |
| MEM_FIXED_INIT_LAT | 27:24 | 0x0     |             |
| SAME_PAGE_Prio     | 30:28 | 0x0     |             |

No description available for this register.

**MEM\_SDRAM\_MODE\_REG - RW - 32 bits - [MMReg:0x158]**

| Field Name        | Bits  | Default | Description  |
|-------------------|-------|---------|--|
| MEM_MODE_REG      | 14:0  | 0x0     |  |
| MEM_WR_LATENCY    | 19:16 | 0x0     | 0=0 clocks<br>1=0.5 clock<br>2=1.0 clock<br>3=1.5 clocks<br>4=2.0 clocks<br>5=2.5 clocks<br>6=3.0 clocks<br>7=3.5 clocks<br>8=4.0 clocks<br>9=4.5 clocks<br>10=5.0 clocks<br>11=5.5 clocks<br>12=6.0 clocks<br>13=6.5 clocks<br>14=7.0 clocks<br>15=7.5 clocks |
| MEM_CAS_LATENCY   | 22:20 | 0x0     | 1=1 clock<br>2=2 clocks<br>3=3 clocks<br>4=4 clocks<br>5=5 clocks<br>6=6 clocks<br>7=7 clocks  |
| MEM_CMD_LATENCY   | 23    | 0x0     | 0=Command latency 0 clocks<br>1=Command latency 1/2 clock  |
| MEM_STR_LATENCY   | 24    | 0x0     | 0=Strobe latency the same as MEM_WR_LATENCY<br>1=Strobe latency equal MEM_WR_LATENCY plus 1/2 clock  |
| MEM_FALL_OUT_CMD  | 25    | 0x0     | 0=Command/Address out on YCLK rise<br>1=Command/Address out on YCLK fall, 1/4 clock delay  |
| MEM_FALL_OUT_DATA | 26    | 0x0     | 0=Data/Mask out on YCLK rise<br>1=Data/Mask out on YCLK fall, 1/4 clock delay  |
| MEM_FALL_OUT_STR  | 27    | 0x0     | 0=Strobe out on YCLK rise<br>1=Strobe out on YCLK fall, 1/4 clock delay  |
| MC_INIT_COMPLETE  | 28    | 0x0     | 0=Register Initialization Not Complete<br>1=Register Initialization Complete   |
| MEM_DDR_DLL       | 29    | 0x0     | 0=PM do NOT reset DDR DLL<br>1=PM reset DDR DLL  |
| MEM_CFG_TYPE      | 30    | 0x0     | 0=SDR<br>1=DDR   |
| MEM_SDRAM_RESET   | 31    | 0x0     | 0=Normal<br>1=Reset  |



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**MEM\_SDRAM\_MODE\_REG - RW - 32 bits - [MMReg:0x158]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

No description available for this register.

**9. RegisterBackboneManager Detailed Register Reference**

Register Backbone Manager (RBBM) Control Registers.

| <b>RBBM_CNTL - RW - 32 bits - [IOReg,MMReg:0xEC] [MMReg:0xE44]</b> |             |                |   |
|--|-------------|----------------|---|
| <b>Field Name</b>  | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| RB_SETTLE  | 3:0         | 0xf            | Read Daisy Chain Bus Settling Time. (in clocks + 2; minimum time is 2 clocks)<br>Default = 15   |
| ABORTCLKS_HI   | 6:4         | 0x0            | The number of clocks that we will allow a non-queued write from the Host Interface to stall before it is aborted.<br>A value of 0 means never abort.<br>Default = 0.    |
| ABORTCLKS_CP   | 10:8        | 0x0            | The number of clocks that we will allow a non-queued write from the Command Processor to stall before it is aborted.<br>A value of 0 means never abort.<br>Default = 0. |
| ABORTCLKS_CFIFO  | 14:12       | 0x0            | The number of clocks that we will allow a write from the Command FIFO to stall before it is aborted.<br>A value of 0 means never abort.<br>Default = 0.                 |
| CPQ_DATA_SWAP  | 17          | 0x0            | Endian Swap Control for writes to the Command Stream Queue.<br>0 = No swap<br>1 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA<br>Default = 0                             |
| NO_ABORT_IDCT  | 21          | 0x0            | Any write transaction to the IDCT block cannot be aborted.<br>Default = 0.  |
| NO_ABORT_BIOS  | 22          | 0x0            | Any write transaction to the BIOS block cannot be aborted.<br>Default = 0.  |
| NO_ABORT_CP  | 24          | 0x0            | Any write transaction to the Command Processor block cannot be aborted.<br>Default = 0.   |
| NO_ABORT_HI  | 25          | 0x0            | Any write transaction to the Host Interface block cannot be aborted.<br>Default = 0.  |
| NO_ABORT_HDP   | 26          | 0x0            | Any write transaction to the Host Data Processor block cannot be aborted.<br>Default = 0.   |
| NO_ABORT_MC  | 27          | 0x0            | Any write transaction to the Memory Controller block cannot be aborted.<br>Default = 0.   |
| NO_ABORT_AIC   | 28          | 0x0            | Any write transaction to the AGP Interface block cannot be aborted.<br>Default = 0.   |
| NO_ABORT_VIP   | 29          | 0x0            | Any write transaction to the VIP block cannot be aborted.<br>Default = 0.   |
| NO_ABORT_DISP  | 30          | 0x0            | Any write transaction to the Display block cannot be aborted.<br>Default = 0.   |

**RBBM\_CNTL - RW - 32 bits - [IOReg,MMReg:0xEC] [MMReg:0xE44]**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| NO_ABORT_CG | 31   | 0x0     | Any write transaction to the CG or CGM blocks cannot be aborted.<br>Default = 0. |

Control Register

**RBBM\_SOFT\_RESET - RW - 32 bits - [IOReg,MMReg:0xF0] [MMReg:0xE48]**

| Field Name      | Bits | Default | Description  |
|-----------------|------|---------|--|
| SOFT_RESET_CP   | 0    | 0x0     | Soft Reset to the Command Processor block.<br>Default = 0    |
| SOFT_RESET_HI   | 1    | 0x0     | Soft Reset to the Host Interface block.<br>Default = 0       |
| SOFT_RESET_SE   | 2    | 0x0     | Soft Reset to the 3D Setup Engine block.<br>Default = 0      |
| SOFT_RESET_RE   | 3    | 0x0     | Soft Reset to the 3D Raster Engine block.<br>Default = 0     |
| SOFT_RESET_PP   | 4    | 0x0     | Soft Reset to the 3D Pixel Pipe block.<br>Default = 0        |
| SOFT_RESET_E2   | 5    | 0x0     | Soft Reset to the 2D Engine block.<br>Default = 0            |
| SOFT_RESET_RB   | 6    | 0x0     | Soft Reset to the 2D/3D Render Backend block.<br>Default = 0 |
| SOFT_RESET_HDP  | 7    | 0x0     | Soft Reset to the Host Data Processor block.<br>Default = 0  |
| SOFT_RESET_MC   | 8    | 0x0     | Soft Reset to the Memory Controller block.<br>Default = 0    |
| SOFT_RESET_AIC  | 9    | 0x0     | Soft Reset to the AGP Interface block.<br>Default = 0        |
| SOFT_RESET_VIP  | 10   | 0x0     | Soft Reset to the VIP block.<br>Default = 0                  |
| SOFT_RESET_DISP | 11   | 0x0     | Soft Reset to the Display block.<br>Default = 0              |
| SOFT_RESET_CG   | 12   | 0x0     | Soft Reset to Clock Generator blocks.<br>Default = 0         |

Soft Reset Generation

**RBBM\_STATUS - R - 32 bits - [MMReg:0xE40] [MMReg:0x1740]**

| Field Name    | Bits | Default | Description  |
|---------------|------|---------|--|
| CMDFIFO_AVAIL | 6:0  | 0x40    | Number of available entries (doublewords) in the Command FIFO.<br>Default = 64 |
| HIRQ_ON_RBB   | 8    | none    | There is a request from the Host Interface on the backbone.                    |
| CPRQ_ON_RBB   | 9    | none    | There is a request from the Command Processor on the backbone.                 |

**RBBM\_STATUS - R - 32 bits - [MMReg:0xE40] [MMReg:0x1740]**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| CFRQ_ON_RBB     | 10   | none    | There is a request from the Command FIFO on the backbone.   |
| HIRQ_IN_RTBUF   | 11   | none    | There is a request from the Host Interface present in the Retry Buffer.   |
| CPRQ_IN_RTBUF   | 12   | none    | There is a request from the Command Processor present in the Retry Buffer.  |
| CFRQ_IN_RTBUF   | 13   | none    | There is a request from the Command FIFO present in the Retry Buffer.   |
| CF_PIPE_BUSY    | 14   | none    | The Command FIFO pipeline is busy. This indicates that there is something in the command FIFO, or a command fifo request is present further down in the RBBM pipe, eg, on the backbone. |
| ENG_EV_BUSY     | 15   | none    | The RBBM's Event Engine is Busy. That is, we are waiting for a WAIT_UNTIL synchronization event.  |
| CP_CMDSTRM_BUSY | 16   | none    | The Command Processor's Command Stream is Busy. This covers from the Ring Buffer (in memory) through the CP's internal processing pipeline.   |
| E2_BUSY         | 17   | none    | 2D Engine is Busy   |
| RB2D_BUSY       | 18   | none    | 2D portion of Render Backend is Busy  |
| RB3D_BUSY       | 19   | none    | 3D portion of Render Backend is Busy  |
| SE_BUSY         | 20   | none    | 3D Setup Engine is Busy   |
| RE_BUSY         | 21   | none    | 3D Raster Engine is Busy  |
| TAM_BUSY        | 22   | none    | 3D Texture Address Module (sub-block of Pixel Pipe) is Busy   |
| TDM_BUSY        | 23   | none    | 3D Texture Data Module (sub-block of Pixel Pipe) is Busy  |
| PB_BUSY         | 24   | none    | 3D Pixel Blender (sub-block of Pixel Pipe) is Busy  |
| GUI_ACTIVE      | 31   | none    | 2D engine busy OR<br>3D engine busy OR<br>Command FIFO not empty OR<br>CP Microengine busy OR<br>Command Stream Queue not empty OR<br>Ring Buffer not empty                             |

Status Register

**ISYNC\_CNTL - RW - 32 bits - [MMReg:0x1724]**

| Field Name         | Bits | Default | Description   |
|--------------------|------|---------|---|
| ISYNC_ANY2D_IDLE3D | 0    | 0x0     | A write to any 2D Engine register stalls if the 3D Engine is busy OR<br>the Render Backend is not clean of 3D destination data OR<br>the Memory Controller is not clean of 3D destination data.<br>Default = 0. |



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**ISYNC\_CNTL - RW - 32 bits - [MMReg:0x1724]**

| Field Name              | Bits | Default | Description   |
|-------------------------|------|---------|---|
| ISYNC_ANY3D_IDLE2D      | 1    | 0x0     | A write to any 3D Engine register stalls if the 2D Engine is busy OR<br>the Render Backend is not clean of 3D destination data OR<br>the Memory Controller is not clean of 3D destination data.<br>Default = 0.   |
| ISYNC_TRIG2D_IDLE3D     | 2    | 0x0     | A write to any 2D trigger register stalls if the 3D Engine is busy OR<br>the Render Backend is not clean of 3D destination data OR<br>the Memory Controller is not clean of 3D destination data.<br>The 2D trigger registers are:<br>DST_WIDTH_HEIGHT<br>DST_HEIGHT_WIDTH<br>DST_HEIGHT_WIDTH_8<br>DST_WIDTH_X<br>DST_WIDTH_X_INCY<br>DP_GUI_MASTER_CNTL<br>DP_DATATYPE<br>DP_WRITE_MSK<br>DP_MIX<br>CLR_CMP_CNTL<br>RB2D_WRITEBACK_DATA_LO<br>RB2D_WRITEBACK_DATA_HI<br>RB2D_WRITEBACK_ADDR<br>RB2D_DSTCACHE_CTLSTAT<br>Default = 0. |
| ISYNC_TRIG3D_IDLE2D     | 3    | 0x0     | A write to any 3D trigger register stalls if the 2D Engine is busy OR<br>the Render Backend is not clean of 2D destination data OR<br>the Memory Controller is not clean of 2D destination data.<br>The 3D trigger registers are:<br>SE_VF_CNTL<br>RE_E2_3<br>PP_CNTL<br>PP_MC_CONTEXT<br>RB3D_WRITEBACK_DATA_LO<br>RB3D_WRITEBACK_DATA_HI<br>RB3D_WRITEBACK_ADDR<br>RB3D_CNTL<br>RB3D_PLANEMASK<br>RB3D_BLEND_CNTL<br>RB3D_ROPCNTL<br>RB3D_DSTCACHE_CTLSTAT<br>Default = 0.  |
| ISYNC_WAIT_IDLEGUI      | 4    | 0x0     | A write to the WAIT_UNTIL register stalls if the 2D or 3D Engine is busy.<br>Default = 0.   |
| ISYNC_CPSCRATCH_IDLEGUI | 5    | 0x0     | A write to any of the CP's GUI ScratchPad Registers stalls if the 2D or 3D Engine is busy. (For Rage128 compatibility)<br>Default = 0.  |

Implicit Synchronization Control

**RBBM\_GUICNTL - RW - 32 bits - [MMReg:0x172C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**RBBM\_GUICNTL - RW - 32 bits - [MMReg:0x172C]**

| Field Name     | Bits | Default | Description  |
|----------------|------|---------|--|
| HOST_DATA_SWAP | 1:0  | 0x0     | Endian Swap Control for 'Host Data' writes to 2D engine.<br>0 = No swap<br>1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC<br>2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA<br>3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB<br>Default = 0 |

GUI Control

**RBBM\_CMDFIFO\_ADDR - W - 32 bits - [MMReg:0xE70]**

| Field Name   | Bits | Default | Description   |
|--------------|------|---------|---|
| CMDFIFO_ADDR | 5:0  | none    | Address into the Command FIFO which is to be read from. Used for debug, to read the contents of the Command FIFO. |

Command FIFO Address

**RBBM\_CMDFIFO\_DATAH - R - 32 bits - [MMReg:0xE74]**

| Field Name    | Bits | Default | Description   |
|---------------|------|---------|---|
| CMDFIFO_DATAH | 31:0 | none    | Data from the Command FIFO, from location pointed to by the RBBM_CMDFIFO_ADDR register. Used for debug, to read the contents of the Command FIFO. |

Command FIFO Data Low

**RBBM\_CMDFIFO\_DATAH - R - 32 bits - [MMReg:0xE78]**

| Field Name    | Bits | Default | Description   |
|---------------|------|---------|---|
| CMDFIFO_DATAH | 11:0 | none    | Upper Data from the Command FIFO, from location pointed to by the RBBM_CMDFIFO_ADDR register. Used for debug, to read the contents of the Command FIFO. These bits contain the register-space Address and the Byte Enables. |

Command FIFO Data High

**RBBM\_CMDFIFO\_STAT - R - 32 bits - [MMReg:0xE7C]**

| Field Name   | Bits | Default | Description   |
|--------------|------|---------|---|
| CMDFIFO_RPTR | 5:0  | none    | Current Read Pointer into the Command FIFO. Default = 0.  |
| CMDFIFO_WPTR | 13:8 | none    | Current Write Pointer into the Command FIFO. Default = 0. |

Command FIFO Status

**WAIT\_UNTIL - RW - 32 bits - [MMReg:0x1720]**

| Field Name         | Bits | Default | Description                                  |
|--------------------|------|---------|--|
| WAIT_CRTC_PFLIP    | 0    | 0x0     | Wait for the 'Pending Flip' signal to be OFF |
| WAIT_RE_CRTC_VLINE | 1    | 0x0     | Wait for Rising Edge of CRTC_VLINE signal    |
| WAIT_FE_CRTC_VLINE | 2    | 0x0     | Wait for Falling Edge of CRTC_VLINE signal   |

**WAIT\_UNTIL - RW - 32 bits - [MMReg:0x1720]**

| Field Name           | Bits  | Default | Description  |
|----------------------|-------|---------|--|
| WAIT_CRTC_VLINE      | 3     | 0x0     | Wait for CRTC_VLINE signal to be ON  |
| WAIT_DMA_VIPH0_IDLE  | 4     | 0x0     | Wait for VIP Host DMA Channel 0 to be idle   |
| WAIT_DMA_VIPH1_IDLE  | 5     | 0x0     | Wait for VIP Host DMA Channel 1 to be idle   |
| WAIT_DMA_VIPH2_IDLE  | 6     | 0x0     | Wait for VIP Host DMA Channel 2 to be idle   |
| WAIT_DMA_VIPH3_IDLE  | 7     | 0x0     | Wait for VIP Host DMA Channel 3 to be idle   |
| WAIT_DMA_VID_IDLE    | 8     | 0x0     | Wait for VID DMA Channel to be idle  |
| WAIT_DMA_GUI_IDLE    | 9     | 0x0     | Wait for GUI DMA Channel to be idle  |
| WAIT_CMDFIFO         | 10    | 0x0     | Wait until there are at least CMDFIFO_ENTRIES number of occupied entries in the Command FIFO. Used to 'batch-up' a group of writes, to ensure they get written within a short time period of each other. |
| WAIT_OV0_FLIP        | 11    | 0x0     | Wait for Overlay Flip signal to be ON  |
| WAIT_OV0_SLICEDONE   | 12    | 0x0     | Wait for Overlay Slice Done signal to be ON  |
| WAIT_2D_IDLE         | 14    | 0x0     | Wait for 2D engine (including 2D render backend) to be idle  |
| WAIT_3D_IDLE         | 15    | 0x0     | Wait for 3D engine (including 3D render backend) to be idle  |
| WAIT_2D_IDLECLEAN    | 16    | 0x0     | Wait for 2D engine to be idle and 2D render backend to be clean and Memory Controller to be clean of 2D destination data   |
| WAIT_3D_IDLECLEAN    | 17    | 0x0     | Wait for 3D engine to be idle and 3D render backend to be clean and Memory Controller to be clean of 3D destination data   |
| WAIT_HOST_IDLECLEAN  | 18    | 0x0     | Wait for Host Interface/Host Data Path to be idle and clean  |
| WAIT_EXTERN_SIG      | 19    | 0x0     | Wait for External Signal (from VIP block) to be ON   |
| CMDFIFO_ENTRIES      | 26:20 | 0x0     | Number of entries to wait for if the WAIT_CMDFIFO bit is ON  |
| WAIT_BOTH_CRTC_PFLIP | 30    | 0x0     | Wait for both CRTC1_PFLIP and CRTC2_PFLIP  |
| ENG_DISPLAY_SELECT   | 31    | 0x0     | Selects VLINE and PFLIP to be used in 0-3 wait conditions  |

This register is for Explicit Synchronization.

A write to this register will travel through the Command FIFO, and when it gets to the bottom of the FIFO, the write will stall until its condition(s) is/are met. If multiple conditions are being tested, they \*all\* must be true in order to un-stall the write. While it is stalled, other writes can continue to fill-up the Command FIFO behind it.

**NQWAIT\_UNTIL - W - 32 bits - [MMReg:0xE50]**

| Field Name    | Bits | Default | Description  |
|---------------|------|---------|--|
| WAIT_GUI_IDLE | 0    | 0x0     | Wait for 2D and 3D engines to be idle, and for Command FIFO to be empty. |

**NQWAIT\_UNTIL - W - 32 bits - [MMReg:0xE50]****Field Name****Bits****Default****Description**

This register is for Explicit Synchronization.

A write to this register will stall \*at the top of the Command FIFO\*, so that the entire FIFO has to flush before this write can become un-stalled. This technique helps you control ordering of a write to a non-queued register, to make sure it happens after a certain group of writes to the queued registers.

\*\*This register is not implemented in the host's address space; only the CP's\*\*

**GEN\_INT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x40]****Field Name****Bits****Default****Description**

CRTC\_VBLANK\_MASK

0

0x0

Vertical blank interrupt mask.

0=Disable  
1=Enable

(DISPLAY)

CRTC\_VLINE\_MASK

1

0x0

Vertical line interrupt mask.

0=Disable  
1=Enable

(DISPLAY)

CRTC\_VSYNC\_MASK

2

0x0

Vertical sync interrupt mask.

0=Disable  
1=Enable

(DISPLAY)

SNAPSHOT\_MASK

3

0x0

Snapshot interrupt mask.

0=Disable  
1=Enable

(DISPLAY)

FP\_DETECT\_MASK

4

0x0

Hot plug detect (HPD) interrupt mask.

0=Disable  
1=Enable

(DISPLAY)

CRTC2\_VLINE\_MASK

5

0x0

0=Disable  
1=Enable

(DISPLAY)

CRTC2\_VSYNC\_MASK

6

0x0

0=Disable  
1=Enable

(DISPLAY)

SNAPSHOT2\_MASK

7

0x0

0=Disable  
1=Enable

(DISPLAY)

CRTC2\_VBLANK\_MASK

9

0x0

0=Disable  
1=Enable

(DISPLAY)

FP2\_DETECT\_MASK

10

0x0

0=Disable  
1=Enable

(DISPLAY)

VSYNC\_DIFF\_OVER\_LIMIT\_MASK

11

0x0

0=Disable  
1=Enable

(TVOUT)

DMA\_VIPH0\_INT\_EN

12

0x0

0=Disable  
1=Enable

(VIP)

DMA\_VIPH1\_INT\_EN

13

0x0

0=Disable  
1=Enable

(VIP)

DMA\_VIPH2\_INT\_EN

14

0x0

0=Disable  
1=Enable

(VIP)

DMA\_VIPH3\_INT\_EN

15

0x0

0=Disable  
1=Enable

(VIP)

I2C\_INT\_EN

17

0x0

0=Disable  
1=Enable

(VIP)

**GEN\_INT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x40]**

| Field Name                            | Bits | Default | Description  |
|---------------------------------------|------|---------|--|
| GUI_IDLE_MASK<br>(RBBM)               | 19   | 0x0     | GUI idle interrupt mask.<br>0=Disable<br>1=Enable                  |
| VIPH_INT_EN<br>(VIP)                  | 24   | 0x0     | 0=Disable<br>1=Enable  |
| SW_INT_EN<br>(HDP)                    | 25   | 0x0     | Software interrupt mask.<br>0=Disable<br>1=Enable                  |
| GEYSERVILLE_MASK<br>(VIP)             | 27   | 0x0     | 0=Disable<br>1=Enable  |
| HDCP_AUTHORIZED_INT_MASK<br>(DISPLAY) | 28   | 0x0     | 0=Disable<br>1=Enable  |
| DVI_I2C_INT_MASK<br>(DISPLAY)         | 29   | 0x0     | 0=Disable<br>1=Enable  |
| GUIDMA_MASK<br>(CP)                   | 30   | 0x0     | GUI DMA channel interrupt mask.<br>0=Disable<br>1=Enable           |
| VIDDMA_MASK<br>(CP)                   | 31   | 0x0     | Video capture DMA channel interrupt mask.<br>0=Disable<br>1=Enable |

General Interrupt Control register.

The MASK/EN fields control whether the respective status bits are enabled to drive the system interrupt pin. Even if enabled here, the interrupt line is not driven unless enabled in the PCI configuration space.

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                           | Bits | Default | Description   |
|--------------------------------------|------|---------|---|
| CRTC_VBLANK_STAT (R)<br>(DISPLAY)    | 0    | 0x0     | Vertical blank interrupt. Set when display in vertical retrace.<br>0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC_VBLANK_STAT_AK (W)<br>(DISPLAY) | 0    | 0x0     | Vertical blank interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| CRTC_VLINE_STAT (R)<br>(DISPLAY)     | 1    | 0x0     | Vertical line interrupt. Set on display line on programmed by the CRTC_VLINE_CRNT_VLINE.CRTC_VLINE register.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| CRTC_VLINE_STAT_AK (W)<br>(DISPLAY)  | 1    | 0x0     | Vertical line interrupt acknowledge.<br>0=No effect<br>1=Clear status   |
| CRTC_VSYNC_STAT (R)<br>(DISPLAY)     | 2    | 0x0     | Vertical sync interrupt. Set on start of VSYNC at the DAC.<br>0=No event<br>1=Event has occurred, interrupting if enabled   |
| CRTC_VSYNC_STAT_AK (W)<br>(DISPLAY)  | 2    | 0x0     | Vertical sync interrupt acknowledge.<br>0=No effect<br>1=Clear status   |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                                   | Bits | Default | Description  |
|--|------|---------|--|
| SNAPSHOT_STAT (R)<br>(DISPLAY)               | 3    | 0x0     | Snapshot interrupt. Set as controlled by SNAPSHOT_VIF_COUNT register.<br>0=No event<br>1=Event has occurred, interrupting if enabled   |
| SNAPSHOT_STAT_AK (W)<br>(DISPLAY)            | 3    | 0x0     | Snapshot interrupt acknowledge.<br>0=No effect<br>1=Clear status   |
| FP_DETECT_STAT (R)<br>(DISPLAY)              | 4    | 0x0     | Hot plug detect (HPD) interrupt. Set on HPD connect or disconnect as controlled by FP_GEN_CNTL.FP_DETECT_INT_POL.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| FP_DETECT_STAT_AK (W)<br>(DISPLAY)           | 4    | 0x0     | Hot plug detect (HPD) interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| CRTC2_VLINE_STAT (R)<br>(DISPLAY)            | 5    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC2_VLINE_STAT_AK (W)<br>(DISPLAY)         | 5    | 0x0     | 0=No effect<br>1=Clear status  |
| CRTC2_VSYNC_STAT (R)<br>(DISPLAY)            | 6    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC2_VSYNC_STAT_AK (W)<br>(DISPLAY)         | 6    | 0x0     | 0=No effect<br>1=Clear status  |
| SNAPSHOT2_STAT (R)<br>(DISPLAY)              | 7    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| SNAPSHOT2_STAT_AK (W)<br>(DISPLAY)           | 7    | 0x0     | 0=No effect<br>1=Clear status  |
| CAPO_INT_ACTIVE (R)<br>(VIP)                 | 8    | 0x0     | Capture port 0 has active interrupt(s).<br>0=Capture port 0 not source of any active interrupt<br>1=Capture port 0 has active interrupt(s)                                       |
| CRTC2_VBLANK_STAT (R)<br>(DISPLAY)           | 9    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC2_VBLANK_STAT_AK (W)<br>(DISPLAY)        | 9    | 0x0     | 0=No effect<br>1=Clear status  |
| FP2_DETECT_STAT (R)<br>(DISPLAY)             | 10   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| FP2_DETECT_STAT_AK (W)<br>(DISPLAY)          | 10   | 0x0     | 0=No effect<br>1=Clear status  |
| VSYNC_DIFF_OVER_LIMIT_STAT (R)<br>(TVOUT)    | 11   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| VSYNC_DIFF_OVER_LIMIT_STAT_AK (W)<br>(TVOUT) | 11   | 0x0     | 0=No effect<br>1=Clear status  |
| DMA_VIPH0_INT (R)<br>(VIP)                   | 12   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                                | Bits | Default | Description   |
|---|------|---------|---|
| DMA_VIPH0_INT_AK (W)<br>(VIP)             | 12   | 0x0     | 0=No effect<br>1=Clear status   |
| DMA_VIPH1_INT (R)<br>(VIP)                | 13   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DMA_VIPH1_INT_AK (W)<br>(VIP)             | 13   | 0x0     | 0=No effect<br>1=Clear status   |
| DMA_VIPH2_INT (R)<br>(VIP)                | 14   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DMA_VIPH2_INT_AK (W)<br>(VIP)             | 14   | 0x0     | 0=No effect<br>1=Clear status   |
| DMA_VIPH3_INT (R)<br>(VIP)                | 15   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DMA_VIPH3_INT_AK (W)<br>(VIP)             | 15   | 0x0     | 0=No effect<br>1=Clear status   |
| I2C_INT (R)<br>(VIP)                      | 17   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| I2C_INT_AK (W)<br>(VIP)                   | 17   | 0x0     | 0=No effect<br>1=Clear status   |
| GUI_IDLE_STAT (R)<br>(RBBM)               | 19   | 0x1     | GUI idle interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled  |
| GUI_IDLE_STAT_AK (W)<br>(RBBM)            | 19   | 0x0     | GUI idle interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| VIPH_INT (R)<br>(VIP)                     | 24   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| SW_INT (R)<br>(HDP)                       | 25   | 0x0     | Software interrupt. General purpose interrupt that can only be set by software event by writing to SW_INT_SET.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| SW_INT_AK (W)<br>(HDP)                    | 25   | 0x0     | Software interrupt acknowledge.<br>0=No effect<br>1=Clear SW_INT (set low)  |
| SW_INT_SET (W)<br>(HDP)                   | 26   | 0x0     | Software interrupt trigger.<br>0=No effect<br>1=Set SW_INT active (high)  |
| GEYSERVILLE_STAT (R)<br>(VIP)             | 27   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| GEYSERVILLE_STAT_AK (W)<br>(VIP)          | 27   | 0x0     | 0=No effect<br>1=Clear status   |
| HDCP_AUTHORIZED_INT_STAT (R)<br>(DISPLAY) | 28   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| HDCP_AUTHORIZED_INT_AK (W)<br>(DISPLAY)   | 28   | 0x0     | 0=No effect<br>1=Clear status   |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                        | Bits | Default | Description   |
|-----------------------------------|------|---------|---|
| DVI_I2C_INT_STAT (R)<br>(DISPLAY) | 29   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DVI_I2C_INT_AK (W)<br>(DISPLAY)   | 29   | 0x0     | 0=No effect<br>1=Clear status   |
| GUIDMA_STAT (R)<br>(CP)           | 30   | 0x0     | GUI DMA channel interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled           |
| GUIDMA_AK (W)<br>(CP)             | 30   | 0x0     | GUI DMA channel interrupt acknowledge.<br>0=No effect<br>1=Clear status                             |
| VIDDMA_STAT (R)<br>(CP)           | 31   | 0x0     | Video capture DMA channel interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| VIDDMA_AK (W)<br>(CP)             | 31   | 0x0     | Video capture DMA channel interrupt acknowledge.<br>0=No effect<br>1=Clear status                   |

General Interrupt Status register.

These fields can be polled and acknowledged even if interrupts are disabled, or the respective fields are masked in the GEN\_INT\_CNTL register.

**10. CommandProcessor Detailed Register Reference**

Command Processor Control Registers.

| <b>CP_RB_CNTL - RW - 32 bits - [MMReg:0x704]</b> |             |                |  |
|--|-------------|----------------|--|
| <b>Field Name</b>                                | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| RB_BUFSZ   | 5:0         | 0x0            | Ring Buffer Size. This size is expressed in log2 of the actual size (in 64-bit 'quadwords' ). For example, for a buffer of 1024 quadwords, you would program this field to 10(decimal).<br>Default = 0   |
| RB_BLKSZ   | 13:8        | 0x0            | Ring Buffer Block Size. This defines the number of quadwords that the Command Processor will read between updates to the host's copy of the Read Pointer. This size is expressed in log2 of the actual size (in 64-bit 'quadwords' ). For example, for a block of 1024 quadwords, you would program this field to 10(decimal).<br>Default = 0  |
| BUF_SWAP   | 17:16       | 0x0            | Endian Swap Control for Ring Buffer and Indirect Buffer. Only affects the chip behavior if the buffer resides in system memory.<br>0 = No swap<br>1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC<br>2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA<br>3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB<br>Default = 0  |
| MAX_FETCH  | 19:18       | 0x0            | Maximum Fetch Size for any read request that the CP makes to memory.<br>0 = 1 octword. (16 bytes)<br>1 = 2 octwords. (32 bytes)<br>2 = 4 octwords. (64 bytes)<br>3 = reserved<br>Default = 0   |
| RB_NO_UPDATE                                     | 27          | 0x0            | Ring Buffer No Write to Read Pointer<br>0= Write to Host's copy of Read Pointer in system memory.<br>1= Do not write to Host's copy of Read pointer.<br>The purpose of this control bit is to have a fall-back position if the bus-mastered write to system memory doesn't work, in which case the driver will have to read the Graphics Controller's copy of the Read Pointer directly, with some performance penalty.<br>Default = 0 |
| RB_RPTR_WR_ENA                                   | 31          | 0x0            | Ring Buffer Read Pointer Write Transfer Enable. When set the contents of the CP_RB_RPTR_WR register is transferred to the active read pointer (CP_RB_RPTR) whenever the CP_RB_WPTR register is written. Default=0 (Not Enabled).   |

Ring Buffer Control

| <b>CP_RB_BASE - RW - 32 bits - [MMReg:0x700]</b> |             |                |  |
|--|-------------|----------------|--|
| <b>Field Name</b>                                | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| RB_BASE  | 31:2        | none           | Ring Buffer Base. Address of the beginning of the ring buffer. |

**CP\_RB\_BASE - RW - 32 bits - [MMReg:0x700]**

| Field Name       | Bits | Default | Description |
|------------------|------|---------|-------------|
| Ring Buffer Base |      |         |             |

**CP\_RB\_RPTR\_ADDR - RW - 32 bits - [MMReg:0x70C]**

| Field Name   | Bits | Default | Description   |
|--------------|------|---------|---|
| RB_RPTR_SWAP | 1:0  | 0x0     | Swap Control to MC when writing the read pointer.<br>Default = 0  |
| RB_RPTR_ADDR | 31:2 | 0x0     | Ring Buffer Read Pointer Address. Address of the Host's copy of the Read Pointer. CP_RB_RPTR (RO) Ring Buffer Read Pointer<br>Default = 0 |

Ring Buffer Read Pointer Address

**CP\_RB\_RPTR - R - 32 bits - [MMReg:0x710]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| RB_RPTR    | 22:0 | none    | Ring Buffer Read Pointer. This is an index (in dwords) of the current element being read from the ring buffer.<br>Read Only. |

Ring Buffer Read Pointer Address

**CP\_RB\_RPTR\_WR - RW - 32 bits - [MMReg:0x71C]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| RB_RPTR_WR | 22:0 | 0x0     | Writable Ring Buffer Read Pointer. Used to set the read pointer following an ACPI event.<br>Default = 0 |

Writable Ring Buffer Read Pointer Address

**CP\_RB\_WPTR - RW - 32 bits - [MMReg:0x714]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| RB_WPTR    | 22:0 | 0x0     | Ring Buffer Write Pointer. This is an index (in dwords) of the last known element to be written to the ring buffer (by the host).<br>Default = 0 |

Ring Buffer Write Pointer

**CP\_RB\_WPTR\_DELAY - RW - 32 bits - [MMReg:0x718]**

| Field Name      | Bits  | Default | Description  |
|-----------------|-------|---------|--|
| PRE_WRITE_TIMER | 27:0  | 0x0     | Pre-Write Timer. The number of clocks that a write to the CP_RB_WPTR register will be delayed until actually taking effect.<br>Default = 0   |
| PRE_WRITE_LIMIT | 31:28 | 0x0     | Pre-Write Limit. The number of times that the CP_RB_WPTR register can be written (while the PRE_WRITE_TIMER has not expired) before the CP_RB_WPTR register is forced to be updated with the most recently written value.<br>Default = 0 |

Ring Buffer Write Pointer Delay



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**CP\_IB\_BASE - RW - 32 bits - [MMReg:0x738]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| IB_BASE    | 31:2 | none    | Indirect Buffer Base. Address of the beginning of the indirect buffer. |

Indirect Buffer Base

**CP\_IB\_BUFSZ - RW - 32 bits - [MMReg:0x73C]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| IB_BUFSZ   | 22:0 | 0x0     | Indirect Buffer Size. This size is expressed in dwords. This field is an initiator to begin fetching commands from the Indirect Buffer.<br>Default = 0 |

Indirect Buffer Size

**CP\_CSQ\_CNTL - RW - 32 bits - [MMReg:0x740]**

| Field Name           | Bits  | Default | Description   |
|----------------------|-------|---------|---|
| CSQ_CNT_PRIMARY (R)  | 7:0   | none    | Count of available dwords in the queue for the Primary Stream.<br>Read Only.  |
| CSQ_CNT_INDIRECT (R) | 15:8  | none    | Count of available dwords in the queue for the Indirect Stream.<br>Read Only.   |
| CSQ_MODE             | 31:28 | 0x0     | Command Stream Queue Mode. Controls whether each command stream is enabled, and whether it is in push mode (Programmed I/O), or pull mode (Bus-Master). Encodings are chosen to be compatible with Rage128.<br>0= Primary Disabled, Indirect Disabled.<br>1= Primary PIO, Indirect Disabled.<br>2= Primary BM, Indirect Disabled.<br>3,5,7= Primary PIO, Indirect BM.<br>4,6,8= Primary BM, Indirect BM.<br>9-14= Reserved.<br>15= Primary PIO, Indirect PIO<br>Default = 0 |

Command Stream Queue Control

**SCRATCH\_UMSK - RW - 32 bits - [MMReg:0x770]**

| Field Name   | Bits  | Default | Description   |
|--------------|-------|---------|---|
| SCRATCH_UMSK | 5:0   | 0x0     | Update Mask for ScratchPad Registers. One bit for each of the scratchpad registers.<br>1 = Write the contents of the respective ScratchPad register to Memory (using the SCRATCH_ADDR register as a base) whenever that ScratchPad register is written.<br>0 = No write to memory.<br>Default = 0 |
| SCRATCH_SWAP | 17:16 | 0x0     | Update Mask for ScratchPad Registers. One bit for each of the scratchpad registers.<br>1 = Write the contents of the respective ScratchPad register to Memory (using the SCRATCH_ADDR register as a base) whenever that ScratchPad register is written.<br>0 = No write to memory.<br>Default = 0 |

Micro Engine Control

**SCRATCH\_ADDR - RW - 32 bits - [MMReg:0x774]**

| Field Name   | Bits | Default | Description  |
|--------------|------|---------|--|
| SCRATCH_ADDR | 31:5 | none    | Memory Address to which the contents of scratchpad registers should be written.<br>Reg 0 is written to address: SCRATCH_ADDR + 0<br>Reg 1 is written to address: SCRATCH_ADDR + 4<br>Reg 2 is written to address: SCRATCH_ADDR + 8<br>... etc... |

ScratchPad Register Address

**CP\_ME\_CNTL - RW - 32 bits - [MMReg:0x7D0]**

| Field Name  | Bits  | Default | Description   |
|-------------|-------|---------|---|
| ME_STAT (R) | 15:0  | none    | Status of MicroEngine internal registers. This value depends on the current value of the ME_STATMUX field.<br>Read Only.  |
| ME_STATMUX  | 20:16 | 0x0     | Selects which status is to be returned on the ME_STAT field.  |
| ME_BUSY (R) | 29    | none    | Busy indicator for the MicroEngine.<br>0 = MicroEngine not busy.<br>1 = MicroEngine is active.<br>Read Only.  |
| ME_MODE     | 30    | 0x1     | Run-Mode of MicroEngine.<br>0 = Single-Step Mode.<br>1 = Free-running Mode.<br>Default = 1  |
| ME_STEP (W) | 31    | 0x0     | Step the MicroEngine by one instruction. Writing a '1' to this field causes the MicroEngine to step by one instruction, if and only if the ME_MODE bit is a '0'.<br>Write Only. |

Micro Engine Control

**CP\_ME\_RAM\_ADDR - RW - 32 bits - [MMReg:0x7D4]**

| Field Name  | Bits | Default | Description   |
|-------------|------|---------|---|
| ME_RAM_ADDR | 7:0  | none    | MicroEngine RAM Address (Write Mode) Writing this register puts the RAM access circuitry into 'Write Mode', which allows the address to auto-increment as data is written into the RAM. |

MicroEngine RAM Address

**CP\_ME\_RAM\_RADDR - W - 32 bits - [MMReg:0x7D8]**

| Field Name  | Bits | Default | Description   |
|---|------|---------|---|
| ME_RAM_RADDR<br><i>(mirror of CP_ME_RAM_ADDR:ME_RAM_ADDR)</i> | 7:0  | none    | MicroEngine RAM Address (Read Mode) Writing this register puts the RAM access circuitry into 'Read Mode', which allows the address to auto-increment as data is read from the RAM.<br>Write Only. |

MicroEngine RAM Read Address

**CP\_ME\_RAM\_DATAH - RW - 32 bits - [MMReg:0x7DC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**CP\_ME\_RAM\_DATAH - RW - 32 bits - [MMReg:0x7DC]**

| Field Name   | Bits | Default | Description   |
|--------------|------|---------|---|
| ME_RAM_DATAH | 5:0  | none    | MicroEngine RAM Data High Used to load the MicroEngine RAM. |

MicroEngine RAM Data High

**CP\_ME\_RAM\_DATA\_L - RW - 32 bits - [MMReg:0x7E0]**

| Field Name    | Bits | Default | Description  |
|---------------|------|---------|--|
| ME_RAM_DATA_L | 31:0 | none    | MicroEngine RAM Data Low Used to load the MicroEngine RAM. |

MicroEngine RAM Data Low

**CP\_CSQ\_ADDR - W - 32 bits - [MMReg:0x7F0]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| CSQ_ADDR   | 9:2  | none    | Address into the Command Stream Queue which is to be read from. Used for debug, to read the contents of the Command Stream Queue. |

(WO) Command Stream Queue Address

**CP\_CSQ\_DATA - R - 32 bits - [MMReg:0x7F4]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| CSQ_DATA   | 31:0 | none    | Data from the Command Stream Queue, from location pointed to by the CP_CSQ_ADDR register. Used for debug, to read the contents of the Command Stream Queue. |

(RO) Command Stream Queue Data

**CP\_CSQ\_STAT - R - 32 bits - [MMReg:0x7F8]**

| Field Name        | Bits  | Default | Description                                    |
|-------------------|-------|---------|--|
| CSQ_RPTR_PRIMARY  | 7:0   | none    | Current Read Pointer into the Primary Queue.   |
| CSQ_WPTR_PRIMARY  | 15:8  | none    | Current Write Pointer into the Primary Queue.  |
| CSQ_RPTR_INDIRECT | 23:16 | none    | Current Read Pointer into the Indirect Queue.  |
| CSQ_WPTR_INDIRECT | 31:24 | none    | Current Write Pointer into the Indirect Queue. |

(RO) Command Stream Queue Status

**SCRATCH\_REG0 - RW - 32 bits - [MMReg:0x15E0]**

| Field Name   | Bits | Default | Description          |
|--------------|------|---------|----------------------|
| SCRATCH_REG0 | 31:0 | none    | ScratchPad Register. |

ScratchPad Register.

**SCRATCH\_REG1 - RW - 32 bits - [MMReg:0x15E4]**

| Field Name   | Bits | Default | Description          |
|--------------|------|---------|----------------------|
| SCRATCH_REG1 | 31:0 | none    | ScratchPad Register. |

ScratchPad Register.

**SCRATCH\_REG2 - RW - 32 bits - [MMReg:0x15E8]**

| Field Name   | Bits | Default | Description          |
|--------------|------|---------|----------------------|
| SCRATCH_REG2 | 31:0 | none    | ScratchPad Register. |

ScratchPad Register.

**SCRATCH\_REG3 - RW - 32 bits - [MMReg:0x15EC]**

| Field Name   | Bits | Default | Description          |
|--------------|------|---------|----------------------|
| SCRATCH_REG3 | 31:0 | none    | ScratchPad Register. |

ScratchPad Register.

**SCRATCH\_REG4 - RW - 32 bits - [MMReg:0x15F0]**

| Field Name   | Bits | Default | Description          |
|--------------|------|---------|----------------------|
| SCRATCH_REG4 | 31:0 | none    | ScratchPad Register. |

ScratchPad Register.

**SCRATCH\_REG5 - RW - 32 bits - [MMReg:0x15F4]**

| Field Name   | Bits | Default | Description          |
|--------------|------|---------|----------------------|
| SCRATCH_REG5 | 31:0 | none    | ScratchPad Register. |

ScratchPad Register.

**CP\_CSQ\_APER\_PRIMARY - RW - 32 bits - [MMReg:0x1000-0x11FC]**

| Field Name          | Bits | Default | Description |
|---------------------|------|---------|-------------|
| CP_CSQ_APER_PRIMARY | 31:0 | none    |             |

No description available for this register.

**CP\_CSQ\_APER\_INDIRECT - RW - 32 bits - [MMReg:0x1300-0x13FC]**

| Field Name           | Bits | Default | Description |
|----------------------|------|---------|-------------|
| CP_CSQ_APER_INDIRECT | 31:0 | none    |             |

No description available for this register.

**CP\_STAT - R - 32 bits - [MMReg:0x7C0]**

| Field Name        | Bits | Default | Description   |
|-------------------|------|---------|---|
| MRU_BUSY          | 0    | none    | Memory Read Unit is Busy  |
| MWU_BUSY          | 1    | none    | Memory Write Unit is Busy                                       |
| RSIU_BUSY         | 2    | none    | Register Server Interface is Busy                               |
| RCIU_BUSY         | 3    | none    | Register Client Interface is Busy                               |
| CSF_PRIMARY_BUSY  | 9    | none    | Command Stream Fetcher is Busy operating on the Primary Stream  |
| CSF_INDIRECT_BUSY | 10   | none    | Command Stream Fetcher is Busy operating on the Indirect Stream |
| CSQ_PRIMARY_BUSY  | 11   | none    | Command Stream Queue is Busy operating on the Primary Stream    |
| CSQ_INDIRECT_BUSY | 12   | none    | Command Stream Queue is Busy operating on the Indirect Stream   |



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**CP\_STAT - R - 32 bits - [MMReg:0x7C0]**

| Field Name   | Bits | Default | Description                                |
|--------------|------|---------|--|
| CSI_BUSY     | 13   | none    | Command Stream Interpreter is Busy         |
| GUIDMA_BUSY  | 28   | none    | GUI DMA Engine is Busy                     |
| VIDDMA_BUSY  | 29   | none    | VID DMA Engine is Busy                     |
| CMDSTRM_BUSY | 30   | none    | Command Processor's Command Stream is Busy |
| CP_BUSY      | 31   | none    | Any Block in the CP is Busy                |

Command Processor Status Register

**11. dma Detailed Register Reference**

Direct memory access (busmastering) registers

| <b>DMA_GUI_TABLE_ADDR - W - 32 bits - [MMReg:0x780]</b> |             |                |   |
|---|-------------|----------------|---|
| <b>Field Name</b>                                       | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| CP_SYNC   | 0           | none           | Synchronize with the Command Processor. Indicates that the MicroEngine cannot proceed to write anything to the register backbone while this DMA is running. |
| TABLE_ADDR  | 31:4        | none           | Memory Address of the most recently active descriptor.  |

(WO) GUI DMA Engine Descriptor Table Address

| <b>DMA_GUI_SRC_ADDR - R - 32 bits - [MMReg:0x784]</b> |             |                |  |
|---|-------------|----------------|--|
| <b>Field Name</b>                                     | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| SRC_ADDR  | 31:0        | none           | Memory Address or Register-space Address where Source data begins, for the currently active descriptor that is being processed by the DMA engine. Read Only. |

GUI DMA Engine Source Address

| <b>DMA_GUI_DST_ADDR - R - 32 bits - [MMReg:0x788]</b> |             |                |  |
|---|-------------|----------------|--|
| <b>Field Name</b>                                     | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| DST_ADDR  | 31:0        | none           | Memory Address or Register-space Address where Source data is being written, for the currently active descriptor that is being processed by the DMA engine. Read Only. |

GUI DMA Engine Destination Address

| <b>DMA_GUI_COMMAND - R - 32 bits - [MMReg:0x78C]</b> |             |                |   |
|--|-------------|----------------|---|
| <b>Field Name</b>                                    | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| BYTE_COUNT   | 20:0        | none           | Number of Bytes remaining to be transferred from Source to Destination.   |
| SRC_SWAP   | 23:22       | none           | Source Endian Swap Control.<br>0 = No swap<br>1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC<br>2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA<br>3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB      |
| DST_SWAP   | 25:24       | none           | Destination Endian Swap Control.<br>0 = No swap<br>1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC<br>2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA<br>3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB |
| SAS  | 26          | none           | Source Address Space.<br>0 = Source Address is a memory-space address<br>1 = Source Address is a register-space address   |
| DAS  | 27          | none           | Destination Address Space.<br>0 = Destination Address is a memory-space address<br>1 = Destination Address is a register-space address  |



**DMA\_GUI\_COMMAND - R - 32 bits - [MMReg:0x78C]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| SAIC       | 28   | none    | Source Address Increment Control.<br>0 = Increment the internal Source Address with each data transfer.<br>1 = No increment.               |
| DAIC       | 29   | none    | Destination Address Increment Control.<br>0 = Increment the internal Destination Address with each data transfer.<br>1 = No increment.     |
| INTDIS     | 30   | none    | Interrupt Disable. This value is a don't care if the EOL bit is '0'.<br>1= Disable the EndOfList interrupt.<br>0= Don't disable interrupt. |
| EOL        | 31   | none    | End Of List. Indicates that the currently active descriptor is the last one in the Descriptor Table.                                       |

(RO)

**DMA\_GUI\_STATUS - RW - 32 bits - [MMReg:0x790]**

| Field Name            | Bits  | Default | Description  |
|-----------------------|-------|---------|--|
| DTAQ_AVAIL (R)        | 4:0   | none    | The number of available entries in the Descriptor Table Address Queue. Read Only.  |
| LAST_TABLE_NUM (R)    | 11:8  | none    | This is a pointer into the Descriptor Table Address Queue, indicating which queue entry was the last one to be written. Read Only.   |
| CURRENT_TABLE_NUM (R) | 15:12 | none    | This is a pointer into the Descriptor Table Address Queue, indicating which queue entry the DMA engine is currently processing. Read Only.   |
| ABORT_EN              | 20    | none    | 1 = Abort the Descriptor Table Address Queue entry pointed to by the ABORT_TABLE_NUM field. If (ABORT_TABLE_NUM= = CURRENT_TABLE_NUM) the DMA engine freezes, to allow the host the opportunity to read the status. Otherwise, the DMA engine proceeds with normal operation on current descriptor. 0 = No Abort. If (ABORT_TABLE_NUM= = CURRENT_TABLE_NUM) the DMA engine starts processing the next entry in the Descriptor Table Address Queue. Otherwise, the DMA engine continues with the current operation. |
| ACTIVE (R)            | 21    | none    | Indicates that the DMA engine is currently working on a descriptor. It indicates whether the CURRENT_TABLE_NUM field is a valid entry in the Descriptor Table Address Queue. Read Only.  |
| SWAP                  | 23:22 | 0x0     | Endian Swap Control for fetching the Descriptor Table. 0 = No swap 1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC 2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA 3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB<br>Default = 0   |

GUI DMA Engine Status

**DMA\_GUI\_ACT\_DSCRPTR - R - 32 bits - [MMReg:0x794]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**DMA\_GUI\_ACT\_DSCRPTR - R - 32 bits - [MMReg:0x794]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| TABLE_ADDR | 31:4 | none    | Memory Address of the most recently active descriptor. |

(RO)

**DMA\_VID\_TABLE\_ADDR - W - 32 bits - [MMReg:0x7A0]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| CP_SYNC    | 0    | none    | Synchronize with the Command Processor. Indicates that the MicroEngine cannot proceed to write anything to the register backbone while this DMA is running. |
| TABLE_ADDR | 31:4 | none    | Memory Address of the most recently active descriptor.  |

(WO) VID DMA Engine Descriptor Table Address

**DMA\_VID\_SRC\_ADDR - R - 32 bits - [MMReg:0x7A4]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| SRC_ADDR   | 31:0 | none    | Memory Address or Register-space Address where Source data begins, for the currently active descriptor that is being processed by the DMA engine. Read Only. |

VID DMA Engine Source Address

**DMA\_VID\_DST\_ADDR - R - 32 bits - [MMReg:0x7A8]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| DST_ADDR   | 31:0 | none    | Memory Address or Register-space Address where Source data is being written, for the currently active descriptor that is being processed by the DMA engine. Read Only. |

(WO) GUI DMA Engine Descriptor Table Address

**DMA\_VID\_COMMAND - R - 32 bits - [MMReg:0x7AC]**

| Field Name | Bits  | Default | Description   |
|------------|-------|---------|---|
| BYTE_COUNT | 20:0  | none    | Number of Bytes remaining to be transferred from Source to Destination.   |
| SRC_SWAP   | 23:22 | none    | Source Endian Swap Control.<br>0 = No swap<br>1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC<br>2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA<br>3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB      |
| DST_SWAP   | 25:24 | none    | Destination Endian Swap Control.<br>0 = No swap<br>1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAADDCC<br>2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA<br>3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB |
| SAS        | 26    | none    | Source Address Space.<br>0 = Source Address is a memory-space address<br>1 = Source Address is a register-space address   |

**DMA\_VID\_COMMAND - R - 32 bits - [MMReg:0x7AC]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| DAS        | 27   | none    | Destination Address Space.<br>0 = Destination Address is a memory-space address<br>1 = Destination Address is a register-space address     |
| SAIC       | 28   | none    | Source Address Increment Control.<br>0 = Increment the internal Source Address with each data transfer.<br>1 = No increment.               |
| DAIC       | 29   | none    | Destination Address Increment Control.<br>0 = Increment the internal Destination Address with each data transfer.<br>1 = No increment.     |
| INTDIS     | 30   | none    | Interrupt Disable. This value is a don't care if the EOL bit is '0'.<br>1= Disable the EndOfList interrupt.<br>0= Don't disable interrupt. |
| EOL        | 31   | none    | End Of List. Indicates that the currently active descriptor is the last one in the Descriptor Table.                                       |

(RO)

**DMA\_VID\_STATUS - RW - 32 bits - [MMReg:0x7B0]**

| Field Name            | Bits  | Default | Description  |
|-----------------------|-------|---------|--|
| DTAQ_AVAIL (R)        | 4:0   | none    | The number of available entries in the Descriptor Table Address Queue. Read Only.  |
| LAST_TABLE_NUM (R)    | 11:8  | none    | This is a pointer into the Descriptor Table Address Queue, indicating which queue entry was the last one to be written. Read Only.   |
| CURRENT_TABLE_NUM (R) | 15:12 | none    | This is a pointer into the Descriptor Table Address Queue, indicating which queue entry the DMA engine is currently processing. Read Only.   |
| ABORT_EN              | 20    | none    | 1 = Abort the Descriptor Table Address Queue entry pointed to by the ABORT_TABLE_NUM field. If (ABORT_TABLE_NUM = CURRENT_TABLE_NUM) the DMA engine freezes, to allow the host the opportunity to read the status. Otherwise, the DMA engine proceeds with normal operation on current descriptor. 0 = No Abort. If (ABORT_TABLE_NUM = CURRENT_TABLE_NUM) the DMA engine starts processing the next entry in the Descriptor Table Address Queue. Otherwise, the DMA engine continues with the current operation. |
| ACTIVE (R)            | 21    | none    | Indicates that the DMA engine is currently working on a descriptor. It indicates whether the CURRENT_TABLE_NUM field is a valid entry in the Descriptor Table Address Queue. Read Only.  |
| SWAP                  | 23:22 | 0x0     | Endian Swap Control for fetching the Descriptor Table. 0 = No swap 1 = 16-bit swap: 0xAABBCCDD becomes 0xBBAAADDCC 2 = 32-bit swap: 0xAABBCCDD becomes 0xDDCCBBAA 3 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB<br>Default = 0  |

VID DMA Engine Status

**DMA\_VID\_ACT\_DSCRPTR - R - 32 bits - [MMReg:0x7B4]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| TABLE_ADDR | 31:4 | none    | Memory Address of the most recently active descriptor. |

(RO)

**GEN\_INT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x40]**

| Field Name                            | Bits | Default | Description  |
|---------------------------------------|------|---------|--|
| CRTC_VBLANK_MASK<br>(DISPLAY)         | 0    | 0x0     | Vertical blank interrupt mask.<br>0=Disable<br>1=Enable        |
| CRTC_VLINE_MASK<br>(DISPLAY)          | 1    | 0x0     | Vertical line interrupt mask.<br>0=Disable<br>1=Enable         |
| CRTC_VSYNC_MASK<br>(DISPLAY)          | 2    | 0x0     | Vertical sync interrupt mask.<br>0=Disable<br>1=Enable         |
| SNAPSHOT_MASK<br>(DISPLAY)            | 3    | 0x0     | Snapshot interrupt mask.<br>0=Disable<br>1=Enable              |
| FP_DETECT_MASK<br>(DISPLAY)           | 4    | 0x0     | Hot plug detect (HPD) interrupt mask.<br>0=Disable<br>1=Enable |
| CRTC2_VLINE_MASK<br>(DISPLAY)         | 5    | 0x0     | 0=Disable<br>1=Enable  |
| CRTC2_VSYNC_MASK<br>(DISPLAY)         | 6    | 0x0     | 0=Disable<br>1=Enable  |
| SNAPSHOT2_MASK<br>(DISPLAY)           | 7    | 0x0     | 0=Disable<br>1=Enable  |
| CRTC2_VBLANK_MASK<br>(DISPLAY)        | 9    | 0x0     | 0=Disable<br>1=Enable  |
| FP2_DETECT_MASK<br>(DISPLAY)          | 10   | 0x0     | 0=Disable<br>1=Enable  |
| VSYNC_DIFF_OVER_LIMIT_MASK<br>(TVOUT) | 11   | 0x0     | 0=Disable<br>1=Enable  |
| DMA_VIPH0_INT_EN<br>(VIP)             | 12   | 0x0     | 0=Disable<br>1=Enable  |
| DMA_VIPH1_INT_EN<br>(VIP)             | 13   | 0x0     | 0=Disable<br>1=Enable  |
| DMA_VIPH2_INT_EN<br>(VIP)             | 14   | 0x0     | 0=Disable<br>1=Enable  |
| DMA_VIPH3_INT_EN<br>(VIP)             | 15   | 0x0     | 0=Disable<br>1=Enable  |
| I2C_INT_EN<br>(VIP)                   | 17   | 0x0     | 0=Disable<br>1=Enable  |

**GEN\_INT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x40]**

| Field Name                            | Bits | Default | Description  |
|---------------------------------------|------|---------|--|
| GUI_IDLE_MASK<br>(RBBM)               | 19   | 0x0     | GUI idle interrupt mask.<br>0=Disable<br>1=Enable                  |
| VIPH_INT_EN<br>(VIP)                  | 24   | 0x0     | 0=Disable<br>1=Enable  |
| SW_INT_EN<br>(HDP)                    | 25   | 0x0     | Software interrupt mask.<br>0=Disable<br>1=Enable                  |
| GEYSERVILLE_MASK<br>(VIP)             | 27   | 0x0     | 0=Disable<br>1=Enable  |
| HDCP_AUTHORIZED_INT_MASK<br>(DISPLAY) | 28   | 0x0     | 0=Disable<br>1=Enable  |
| DVI_I2C_INT_MASK<br>(DISPLAY)         | 29   | 0x0     | 0=Disable<br>1=Enable  |
| GUIDMA_MASK<br>(CP)                   | 30   | 0x0     | GUI DMA channel interrupt mask.<br>0=Disable<br>1=Enable           |
| VIDDMA_MASK<br>(CP)                   | 31   | 0x0     | Video capture DMA channel interrupt mask.<br>0=Disable<br>1=Enable |

General Interrupt Control register.

The MASK/EN fields control whether the respective status bits are enabled to drive the system interrupt pin. Even if enabled here, the interrupt line is not driven unless enabled in the PCI configuration space.

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                           | Bits | Default | Description   |
|--------------------------------------|------|---------|---|
| CRTC_VBLANK_STAT (R)<br>(DISPLAY)    | 0    | 0x0     | Vertical blank interrupt. Set when display in vertical retrace.<br>0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC_VBLANK_STAT_AK (W)<br>(DISPLAY) | 0    | 0x0     | Vertical blank interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| CRTC_VLINE_STAT (R)<br>(DISPLAY)     | 1    | 0x0     | Vertical line interrupt. Set on display line on programmed by the CRTC_VLINE_CRNT_VLINE.CRTC_VLINE register.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| CRTC_VLINE_STAT_AK (W)<br>(DISPLAY)  | 1    | 0x0     | Vertical line interrupt acknowledge.<br>0=No effect<br>1=Clear status   |
| CRTC_VSYNC_STAT (R)<br>(DISPLAY)     | 2    | 0x0     | Vertical sync interrupt. Set on start of VSYNC at the DAC.<br>0=No event<br>1=Event has occurred, interrupting if enabled   |
| CRTC_VSYNC_STAT_AK (W)<br>(DISPLAY)  | 2    | 0x0     | Vertical sync interrupt acknowledge.<br>0=No effect<br>1=Clear status   |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                                   | Bits | Default | Description  |
|--|------|---------|--|
| SNAPSHOT_STAT (R)<br>(DISPLAY)               | 3    | 0x0     | Snapshot interrupt. Set as controlled by SNAPSHOT_VIF_COUNT register.<br>0=No event<br>1=Event has occurred, interrupting if enabled   |
| SNAPSHOT_STAT_AK (W)<br>(DISPLAY)            | 3    | 0x0     | Snapshot interrupt acknowledge.<br>0=No effect<br>1=Clear status   |
| FP_DETECT_STAT (R)<br>(DISPLAY)              | 4    | 0x0     | Hot plug detect (HPD) interrupt. Set on HPD connect or disconnect as controlled by FP_GEN_CNTL.FP_DETECT_INT_POL.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| FP_DETECT_STAT_AK (W)<br>(DISPLAY)           | 4    | 0x0     | Hot plug detect (HPD) interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| CRTC2_VLINE_STAT (R)<br>(DISPLAY)            | 5    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC2_VLINE_STAT_AK (W)<br>(DISPLAY)         | 5    | 0x0     | 0=No effect<br>1=Clear status  |
| CRTC2_VSYNC_STAT (R)<br>(DISPLAY)            | 6    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC2_VSYNC_STAT_AK (W)<br>(DISPLAY)         | 6    | 0x0     | 0=No effect<br>1=Clear status  |
| SNAPSHOT2_STAT (R)<br>(DISPLAY)              | 7    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| SNAPSHOT2_STAT_AK (W)<br>(DISPLAY)           | 7    | 0x0     | 0=No effect<br>1=Clear status  |
| CAPO_INT_ACTIVE (R)<br>(VIP)                 | 8    | 0x0     | Capture port 0 has active interrupt(s).<br>0=Capture port 0 not source of any active interrupt<br>1=Capture port 0 has active interrupt(s)                                       |
| CRTC2_VBLANK_STAT (R)<br>(DISPLAY)           | 9    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC2_VBLANK_STAT_AK (W)<br>(DISPLAY)        | 9    | 0x0     | 0=No effect<br>1=Clear status  |
| FP2_DETECT_STAT (R)<br>(DISPLAY)             | 10   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| FP2_DETECT_STAT_AK (W)<br>(DISPLAY)          | 10   | 0x0     | 0=No effect<br>1=Clear status  |
| VSYNC_DIFF_OVER_LIMIT_STAT (R)<br>(TVOUT)    | 11   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| VSYNC_DIFF_OVER_LIMIT_STAT_AK (W)<br>(TVOUT) | 11   | 0x0     | 0=No effect<br>1=Clear status  |
| DMA_VIPH0_INT (R)<br>(VIP)                   | 12   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                                | Bits | Default | Description   |
|---|------|---------|---|
| DMA_VIPH0_INT_AK (W)<br>(VIP)             | 12   | 0x0     | 0=No effect<br>1=Clear status   |
| DMA_VIPH1_INT (R)<br>(VIP)                | 13   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DMA_VIPH1_INT_AK (W)<br>(VIP)             | 13   | 0x0     | 0=No effect<br>1=Clear status   |
| DMA_VIPH2_INT (R)<br>(VIP)                | 14   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DMA_VIPH2_INT_AK (W)<br>(VIP)             | 14   | 0x0     | 0=No effect<br>1=Clear status   |
| DMA_VIPH3_INT (R)<br>(VIP)                | 15   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DMA_VIPH3_INT_AK (W)<br>(VIP)             | 15   | 0x0     | 0=No effect<br>1=Clear status   |
| I2C_INT (R)<br>(VIP)                      | 17   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| I2C_INT_AK (W)<br>(VIP)                   | 17   | 0x0     | 0=No effect<br>1=Clear status   |
| GUI_IDLE_STAT (R)<br>(RBBM)               | 19   | 0x1     | GUI idle interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled  |
| GUI_IDLE_STAT_AK (W)<br>(RBBM)            | 19   | 0x0     | GUI idle interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| VIPH_INT (R)<br>(VIP)                     | 24   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| SW_INT (R)<br>(HDP)                       | 25   | 0x0     | Software interrupt. General purpose interrupt that can only be set by software event by writing to SW_INT_SET.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| SW_INT_AK (W)<br>(HDP)                    | 25   | 0x0     | Software interrupt acknowledge.<br>0=No effect<br>1=Clear SW_INT (set low)  |
| SW_INT_SET (W)<br>(HDP)                   | 26   | 0x0     | Software interrupt trigger.<br>0=No effect<br>1=Set SW_INT active (high)  |
| GEYSERVILLE_STAT (R)<br>(VIP)             | 27   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| GEYSERVILLE_STAT_AK (W)<br>(VIP)          | 27   | 0x0     | 0=No effect<br>1=Clear status   |
| HDCP_AUTHORIZED_INT_STAT (R)<br>(DISPLAY) | 28   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| HDCP_AUTHORIZED_INT_AK (W)<br>(DISPLAY)   | 28   | 0x0     | 0=No effect<br>1=Clear status   |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                        | Bits | Default | Description   |
|-----------------------------------|------|---------|---|
| DVI_I2C_INT_STAT (R)<br>(DISPLAY) | 29   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DVI_I2C_INT_AK (W)<br>(DISPLAY)   | 29   | 0x0     | 0=No effect<br>1=Clear status   |
| GUIDMA_STAT (R)<br>(CP)           | 30   | 0x0     | GUI DMA channel interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled           |
| GUIDMA_AK (W)<br>(CP)             | 30   | 0x0     | GUI DMA channel interrupt acknowledge.<br>0=No effect<br>1=Clear status                             |
| VIDDMA_STAT (R)<br>(CP)           | 31   | 0x0     | Video capture DMA channel interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| VIDDMA_AK (W)<br>(CP)             | 31   | 0x0     | Video capture DMA channel interrupt acknowledge.<br>0=No effect<br>1=Clear status                   |

General Interrupt Status register.

These fields can be polled and acknowledged even if interrupts are disabled, or the respective fields are masked in the GEN\_INT\_CNTL register.

**12. control Detailed Register Reference**

General control/status registers for the display engine

| DISPLAY_BASE_ADDR - RW - 32 bits - [MMReg:0x23C] |      |         |  |
|--|------|---------|--|
| Field Name                                       | Bits | Default | Description  |
| DISPLAY_BASE_ADDR                                | 31:0 | 0x0     | Base address added to all graphics, cursor and icon requests to the internal memory controller. This should normally be set equal to MC_FB_LOCATION.MC_FB_START. It could be set to other places to allow display out of system (e.g. AGP) memory, but this is not recommended. This is a 4 Megabyte aligned base address.<br><br>NOTE: Bits 0:21 of this field are hardwired to ZERO. |

Primary display graphics, cursor and icon base address

| DISP_OUTPUT_CNTL - RW - 32 bits - [MMReg:0xD64] |       |         |  |
|---|-------|---------|--|
| Field Name                                      | Bits  | Default | Description  |
| DISP_DAC_SOURCE                                 | 1:0   | 0x0     | DAC data source select. When doing ratiometric expansion, this should always be set to 10. When pixel clock is above 165 MHz, this MUST be set to 00.<br>0=DAC output data comes directly from display merger.<br>1=Reserved - DAC output data comes from output linear transform unit.<br>2=DAC output data comes from ratiometric expansion unit.<br>3=Reserved - DAC output data comes from display transform unit, and DAC is in YPbPr mode. |
| DISP_RMX_SOURCE                                 | 8     | 0x0     | Ratiometric expansion source select. This bit has no use in M6.<br>0=Ratiometric expansion data comes directly from display merger.<br>1=Ratiometric expansion data comes from output linear transform unit.   |
| DISP_RMX_DITH_EN                                | 10    | 0x1     | Selects how 30 bit data is converted to 24 bits at input to ratiometric expansion unit.<br>0=Convert 30 bit color data to 24 bits by truncation of lower bits.<br>1=Convert 30 bit color data to 24 bits by 1-D dithering.   |
| DISP_TV_EVEN_FLAG_CNTL                          | 28:27 | 0x0     | 0=TV out even flag inverse of video field polarity. i.e. 1 for even.<br>1=TV out even flag equal to video field polarity. i.e. 1 for odd.<br>2=TV out even flag forced to 0.<br>3=TV out even flag forced to 1.  |

Display outout control register

| DISP_MERGE_CNTL - RW - 32 bits - [MMReg:0xD60] |      |         |             |
|--|------|---------|-------------|
| Field Name                                     | Bits | Default | Description |

**DISP\_MERGE\_CNTL - RW - 32 bits - [MMReg:0xD60]**

| Field Name         | Bits  | Default | Description   |
|--------------------|-------|---------|---|
| DISP_ALPHA_MODE    | 1:0   | 0x0     | Graphics and overlay blend mode select. There are three choices of blend mode as described below. Per pixel alpha is really only for graphics modes that have alpha values embedded (32bpp aRGB8888, 16bpp aRGB1555, 16bpp aRGB4444, 16bpp alphaIndex88. When the global alphas are set to 1 (i.e. 0xFF), the key mode works like key mixing in past chips.<br>0=Key mode: For GRPH_VID_KEY = 0, then Pixel = DISP_GRP_ALPHA * Primary Graphics. For KEY = 1, then Pixel = DISP_OV0_ALPHA * Overlay pixel<br>1=Per pixel alpha mode: See DISP_ALPHA_PREMULT and DISP_ALPHA_INV for result<br>2=Global alpha mode: Outside overlay window Pixel = DISP_GRP_ALPHA * Primary Graphics. Inside overlay window Pixel = (1-DISP_OV0_ALPHA * Primary Graphics + DISP_OV0_ALPHA * Overlay pixel |
| DISP_ALPHA_INV     | 2     | 0x0     | For use with per pixel alpha blend mode. Applies optional inversion to the alpha value extracted from the graphics surface data.<br>0=When DISP_ALPHA_MODE = 01, then use per pixel alpha as primary graphics opacity (PIX_ALPHA <= alpha from pixel)<br>1=When DISP_ALPHA_MODE = 01, then use per pixel alpha as primary graphics transparency (PIX_ALPHA <= 1 - (alpha from pixel))   |
| DISP_ALPHA_PREMULT | 3     | 0x0     | For use with per pixel alpha blend mode. Selects whether pre-multiplied alpha or non-pre-multiplied alpha mix equation is used.<br>0=When DISP_ALPHA_MODE = 01, then Pixel = PIX_ALPHA * graphics pixel + (1-PIX_ALPHA) * overlay pixel<br>1=When DISP_ALPHA_MODE = 01, then Pixel = graphics pixel + (1-PIX_ALPHA) * overlay pixel   |
| DISP_RGB_OFFSET_EN | 8     | 0x0     | Enable for no clamping for YUV input to YUV tvout output. Should always be enabled, unless it doesn't work. When enabled, DISP_LIN_TRANS must not be in bypass mode.<br>0=RGB mixing pipe operates in 0 to 1 (i.e. 0..1023) limited RGB space. Overlay pixel values outside this range are clamped to be in range.<br>1=RGB mixing pipe operates in -1.5 to +1.5 range. No clamping occurs for YCbCr or YPbPr mode outputs. Clamping is applied for RGB mode outputs.   |
| DISP_GRP_ALPHA     | 23:16 | 0xff    | Global graphics alpha for use in key mode and global alpha modes of DISP_ALPHA_MODE.  |
| DISP_OV0_ALPHA     | 31:24 | 0xff    | Global video alpha for use in key mode and global alpha modes of DISP_ALPHA_MODE.   |

Controls for mixing of graphics and video layers

**DISP2\_MERGE\_CNTL - RW - 32 bits - [MMReg:0xD68]**

| Field Name          | Bits | Default | Description  |
|---------------------|------|---------|--|
| DISP2_RGB_OFFSET_EN | 8    | 0x0     | Enable for no clamping for YUV input to YUV tvout output. Should always be enabled, unless it doesn't work. When enabled, DISP_LIN_TRANS must not be in bypass mode.<br>0=Compositing unit operates in normal RGB space<br>1=Compositing unit operates in +1536 offset RGB space |

No description available for this register.

**DISP\_MISC\_CNTL - RW - 32 bits - [MMReg:0xD00]**

| Field Name             | Bits  | Default | Description  |
|------------------------|-------|---------|--|
| SOFT_RESET_GRP_H_PP    | 0     | 0x0     | 0=Not reset<br>1=Reset graphics and cursor pixel pipe in pixel clock domain  |
| SOFT_RESET_SUBPIC_PP   | 1     | 0x0     | 0=Not reset<br>1=Reset sub-picture pixel pipe in pixel clock domain  |
| SOFT_RESET_OV0_PP      | 2     | 0x0     | 0=Not reset<br>1=Reset ov0scale pixel pipe in pixel clock domain   |
| SOFT_RESET_GRP_H_SCLK  | 4     | 0x0     | 0=Not reset<br>1=Reset graphics and cursor logic in system clock domain  |
| SOFT_RESET_SUBPIC_SCLK | 5     | 0x0     | 0=Not reset<br>1=Reset sub-picture logic in system clock domain  |
| SOFT_RESET_OV0_SCLK    | 6     | 0x0     | 0=Not reset<br>1=Reset ov0scale logic in system clock domain   |
| SYNC_STRENGTH          | 9:8   | 0x2     | 0=Minimum drive. ~74 ohms.<br>1=Matched impedance drive. ~63 ohms.<br>2=Optimal drive. ~47 ohms.<br>3=Maximum drive. ~42 ohms. |
| SYNC_PAD_FLOP_EN       | 10    | 0x0     | 0=do not flop SYNC signals on the pad<br>1=flop SYNC signals on the pad  |
| SOFT_RESET_GRP_H2_PP   | 12    | 0x0     | 0=Not reset<br>1=Reset graphics and cursor pixel pipe in pixel clock domain  |
| SOFT_RESET_GRP_H2_SCLK | 15    | 0x0     | 0=Not reset<br>1=Reset graphics and cursor logic in system clock domain  |
| SOFT_RESET_LVDS        | 16    | 0x0     | 0=Not reset<br>1=Reset   |
| SOFT_RESET_TMDS        | 17    | 0x0     | 0=Not reset<br>1=Reset   |
| SOFT_RESET_DIG_TMDS    | 18    | 0x0     | 0=Not reset<br>1=Reset   |
| SOFT_RESET_TV          | 19    | 0x0     | 0=Not reset<br>1=Reset   |
| PALETTE2_MEM_RD_MARGIN | 23:20 | 0x3     |  |
| PALETTE_MEM_RD_MARGIN  | 27:24 | 0x3     |  |
| RMX_BUF_MEM_RD_MARGIN  | 31:28 | 0x3     |  |

No description available for this register.

**HTOTAL\_CNTL - RW - 32 bits - CLKIND:0x9**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**HTOTAL\_CNTL - RW - 32 bits - CLKIND:0x9**

| Field Name                         | Bits  | Default | Description  |
|------------------------------------|-------|---------|--|
| HTOT_PIX_SLIP<br>(DISPLAY)         | 3:0   | 0x0     | Pixel accurate control of horizontal total. Selects the extra number of pixels to add to each display line. Valid range is 0 to 15.<br>For VGA modes with SEQ_PCLKBY2 = 1 each increment adds one physical pixel or 1/2 a logical pixel to the line total.<br>For 9-dot 40 column VGA text modes, it is not possible to add 16/18ths or 17/18ths of a character extra to the display line times. |
| HTOT_VCLK_SLIP<br>(DISPLAY)        | 11:8  | 0x0     | Reserved for future use. No affect in this ASIC.   |
| HTOT_PPLL_SLIP<br>(CG)             | 18:16 | 0x0     | Select the number of 1/5 PPIIClk phase slips to do in the PLL at every HSYNC. This is used as a sub-pixel accurate adjustment of the frame rate for TV out or video gen-locking.   |
| HTOT_CNTL_EDGE<br>(DISPLAY) (CG)   | 24    | 0x0     | Select which HSYNC edge the slip correction based on HTOT_PPLL_SLIP is done.   |
| HTOT_CNTL_VGA_EN<br>(DISPLAY) (CG) | 28    | 0x0     | Select if the slip controls based on HTOT_PIX_SLIP, HTOT_VCLK_SLIP and HTOT_PPLL_SLIP are enabled for VGA mode. These are always enabled for non-VGA modes when the respective fields are non-zero.  |

Horizontal total control. Used to fine-tune the horizontal total. This lengthens the time of each display line by sub-character and/or sub-pixel amounts. The purpose is fine adjustment of the overall frame refresh rate for applications that require it (e.g. TV output, GEN-lock to video input).

**HTOTAL2\_CNTL - RW - 32 bits - CLKIND:0x2E**

| Field Name                        | Bits  | Default | Description |
|-----------------------------------|-------|---------|-------------|
| HTOT2_PIX_SLIP<br>(DISPLAY)       | 3:0   | 0x0     |             |
| HTOT2_PIX2CLK_SLIP<br>(DISPLAY)   | 11:8  | 0x0     |             |
| HTOT2_P2PLL_SLIP<br>(CG)          | 18:16 | 0x0     |             |
| HTOT2_CNTL_EDGE<br>(DISPLAY) (CG) | 24    | 0x0     |             |
| HTOT2_CNTL_UPDATE<br>(CG)         | 28    | 0x0     |             |

No description available for this register.

**DISP\_PWR\_MAN - RW - 32 bits - [MMReg:0xD08]**

| Field Name                | Bits | Default | Description   |
|---------------------------|------|---------|---|
| DISP_PWR_MAN_D3_CRTC_EN   | 0    | 0x1     | 0=Resume display at previous CRTC settings on D3hot to D0 power state transistion.<br>1=Leave CRTC idle on D3hot to D0 power transition until BIOS/driver re-initializes.                     |
| DISP2_PWR_MAN_D3_CRTC2_EN | 4    | 0x1     | 0=Resume secondary display at previous CRTC settings on D3hot to D0 power state transistion.<br>1=Leave secondary CRTC idle on D3hot to D0 power transition until BIOS/driver re-initializes. |

**DISP\_PWR\_MAN - RW - 32 bits - [MMReg:0xD08]**

| Field Name           | Bits | Default | Description   |
|----------------------|------|---------|---|
| DISP_PWR_MAN_DPMS    | 9:8  | 0x0     | 0=DPMS On. HSYNC and VSYNC not blocked.<br>1=DPMS Standby. HSYNC blocked, VSYNC not blocked.<br>2=DPMS Suspend. VSYNC blocked, HSYNC not blocked.<br>3=DPMS Off. HSYNC and VSYNC blocked. |
| DISP_D3_RST          | 16   | 0x1     | 0=D3hot to D0 does not reset display.<br>1=D3hot to D0 resets all display blocks.   |
| DISP_D3_REG_RST      | 17   | 0x1     | 0=D3hot to D0 does not reset display registers.<br>1=D3hot to D0 resets all display registers.  |
| DISP_D3_GRP_H_RST    | 18   | 0x1     | 0=D3hot to D0 does not reset graphics logic.<br>1=D3hot to D0 resets graphics logic, but not registers.   |
| DISP_D3_SUBPIC_RST   | 19   | 0x1     | 0=D3hot to D0 does not reset sub-picture logic.<br>1=D3hot to D0 resets sub-picture logic, but not registers.   |
| DISP_D3_OV0_RST      | 20   | 0x1     | 0=D3hot to D0 does not reset ov0scale logic.<br>1=D3hot to D0 resets ov0scale logic, but not registers.   |
| DISP_D1D2_GRP_H_RST  | 21   | 0x1     | 0=D1 or D2 to D0 does not reset graphics logic.<br>1=D1 or D2 to D0 resets graphics logic, but not registers.   |
| DISP_D1D2_SUBPIC_RST | 22   | 0x1     | 0=D1 or D2 to D0 does not reset sub-picture logic.<br>1=D1 or D2 to D0 resets sub-picture logic, but not registers.   |
| DISP_D1D2_OV0_RST    | 23   | 0x1     | 0=D1 or D2 to D0 does not reset ov0scale logic.<br>1=D1 or D2 to D0 resets ov0scale logic, but not registers.   |
| DIG_TMDS_ENABLE_RST  | 24   | 0x1     | 0=Disable RST when DIG_TMDS is enabled<br>1=Enable RST when FP2_ON is enabled   |
| TV_ENABLE_RST        | 25   | 0x1     | 0=Disable RST when TV is enabled<br>1=Enable RST when TV_ON is enabled  |
| AUTO_PWRUP_EN        | 26   | 0x0     | 0=Disable<br>1=Enable   |

No description available for this register.

**13. DAC Detailed Register Reference**

## VGA DAC Registers

| DAC_CNTL - RW - 32 bits - [IOReg,MMReg:0x58] |      |         |   |
|--|------|---------|---|
| Field Name                                   | Bits | Default | Description   |
| DAC_RANGE_CNTL<br>(DISPLAY)                  | 1:0  | 0x2     | DAC control bits. Default = 2.<br>0=Reserved<br>1=Reserved<br>2=PS2 Output Level<br>3=YPbPr output level  |
| DAC_BLANKING<br>(DISPLAY)                    | 2    | 0x0     | Controls use of DAC blanking pedestal during horizontal and vertical blanks.<br>VGA PS2 compatible monitors expect a 0 IRE blanking pedestal.   |
| DAC_CMP_EN<br>(DISPLAY)                      | 3    | 0x0     | Control DAC comparators for analog termination checking. When enabled, the results of the three comparators are read back in the DAC_CMP_OUT_R/G/B fields. Use for the DAC_FORCE fields of DAC_EXT_CNTL is recommended for testing analog monitor connection. DAC_FORCE allows the correct 10 bit data values to be forced on the DAC channels without corrupting the TMDS or TV out images.<br>When using the DAC comparators, be sure the comparator settling times are met by waiting at least 1us between changing the DAC_FORCE parameters and reading the comparator status bits.<br>The comparator reference voltage is 0.440V. The recommended 10 bit DAC value for testing 75 or 37.5 ohm termination for PS2 current levels is 0x1AC.<br>For each channel, if the comparator output is 0, it indicates the termination is 75 ohms, and therefore no monitor is attached. When the comparator output is 1, the termination is 37.5 ohms and a monitor is attached. |
| DAC_CMP_OUT_R (R)<br>(DISPLAY)               | 4    | 0x0     | Red channel comparator output.  |
| DAC_CMP_OUT_G (R)<br>(DISPLAY)               | 5    | 0x0     | Green channel comparator output.  |
| DAC_CMP_OUT_B (R)<br>(DISPLAY)               | 6    | 0x0     | Blue channel comparator output.   |
| DAC_CMP_OUTPUT (R)<br>(DISPLAY)              | 7    | 0x0     | Logical AND of R, G & B comparator outputs.   |
| DAC_8BIT_EN<br>(DISPLAY)                     | 8    | 0x0     | Enables 8 bit DAC operation. 8 bit is normal, 6 bit used for VGA emulation.<br>When in 6 bit writes and reads to DAC_DATA and PALETTE_DATA are affected. Writes shift 6 bits left by 2 to make 8 bits in the palette memory. Reads shift 8 bit palette data right by 2 to give 6 MSBs to the host.<br>0=DAC_DATA and PALETTE_DATA read/writes emulate 6 bit palette<br>1=DAC_DATA and PALETTE_DATA read/writes emulate 8 bit palette  |
| DAC_4BPP_PIX_ORDER<br>(DISPLAY)              | 9    | 0x0     | Selects the order of pixel nibbles within bytes for 4 bpp extended (non-VGA) display modes.   |



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**DAC\_CNTL - RW - 32 bits - [IOReg,MMReg:0x58]**

| Field Name                    | Bits | Default | Description   |
|-------------------------------|------|---------|---|
| DAC_VGA_ADR_EN<br>(BIF)       | 13   | 0x0     | Enables access of the palette (DAC) at the VGA I/O DAC addresses when in extended display modes (non-VGA, or CRT_EXT_DISP_EN=1).  |
| DAC_EXPAND_MODE<br>(DISPLAY)  | 14   | 0x0     | Method to expand 4,5 or 6 bit Red/Green/Blue color codes to 8 bit addresses.<br>0 = Zero Extension<br>1 = Dynamic Expansion<br>0=Convert 4, 5 & 6 bit colors to 8 bits by zero extension<br>1=Convert 4, 5 & 6 bit colors to 8 bits by dynamic expansion  |
| DAC_PDWN<br>(DISPLAY)         | 15   | 0x0     | Power down internal DAC macro bandgap unit. Should also set the R, G & B powerdowns in the DAC_MACRO_CNTL register at the same time. Powering down the DAC does not affect the digital outputs (TV or flat panel). The DAC is automatically powered down when the PMI_POWER_STATE register is not in the D0 state. Setting all DAC_PDWN fields should save about 56 mA when PS2 output levels.  |
| CRT_SENSE (R)<br>(DISPLAY)    | 16   | 0x0     | 0=CRT Monitor Detection result - not connected<br>1=CRT Monitor Detection result - connected  |
| CRT_DETECTION_ON<br>(DISPLAY) | 17   | 0x0     | 0=CRT Monitor Detection disabled<br>1=CRT Monitor Detection enabled   |
| DAC_CRC_CONT_EN<br>(DISPLAY)  | 18   | 0x0     | When CRC is in one shot mode, one-and-only-one frame or field is CRCed after DAC_CRC_EN is set high. In continuous mode every frame/field is CRCed and the results are valid for one field/frame until the next set of results are ready. If a field/frames results are not read within one frame in continuous mode they are over written. In one-shot mode the results remain and can be read until DAC_CRC_EN is cleared.<br>0=DAC CRC runs in one shot mode.<br>1=DAC CRC runs in continuous mode.  |
| DAC_CRC_EN<br>(DISPLAY)       | 19   | 0x0     | Enables the CRC signature check on the data going to the DAC macro. This is what appears on the screen, and includes graphics, HW cursor, video overlay, sub-picture, and overscan. CRC will start in next vertical blank on the first pixel of the line where VSYNC goes active, and run for one field/frame. For interlaced modes the CRC block will not start working until the beginning of a field with odd/even polarity matching the DAC_CRC_FIELD setting.<br>0=Reset DAC CRC.<br>1=Enable DAC CRC for next frame/field in one shot, or all frames/fields in continuous mode. |
| DAC_CRC_FIELD<br>(DISPLAY)    | 20   | 0x0     | Used only for interlaced mode CRCs. Controls which field polarity starts the CRC block after DAC_CRC_EN is set high.<br>0=If interlace display and one shot mode, then CRC even field only<br>1=If interlace display and one shot mode, then CRC odd field only   |

**DAC\_CNTL - RW - 32 bits - [IOReg,MMReg:0x58]**

| Field Name                         | Bits  | Default | Description  |
|------------------------------------|-------|---------|--|
| DAC_LUT_COUNTER_LIMIT<br>(DISPLAY) | 22:21 | 0x0     | Anti-sparkle timeout. The palette circuit will search for a place in the display image to hide palette reads or writes. If no hiding location is found within this many pixels, a dot-stretch is forced to hide the cycle as best as possible. Setting this register too high in low resolution modes may cause long delays on the PCI/AGP bus. The recommended settings are best.<br>0=anti-sparkle timeout 3 clocks<br>1=anti-sparkle timeout 7 clocks<br>2=anti-sparkle timeout 15 clocks<br>3=anti-sparkle timeout 31 clocks |
| DAC_LUT_READ_SEL<br>(DISPLAY)      | 23    | 0x0     | Used for diagnostics only. Selects palette for HOST reads.<br>0=Palette reads come from main palette<br>1=Palette reads come from secondary palette  |
| DAC_MASK<br>(DISPLAY)              | 31:24 | 0xff    | Mirror VGA DAC_MASK. No affect in non-VGA modes. Masks off usage of individual palette index bits before pixel index is looked-up in the palette.<br>0 = do not use this bit of the index<br>1 = use this bit of the index<br>This is a mirror of the VGA DAC_MASK register. It only has an effect in VGA emulation modes (CRTC_EXT_DISP_EN=0), not for VESA modes or extended display modes.  |

General control for the RGB DAC and palette.

**DAC\_DATA - RW - 8 bits - VGA\_IO:0x3C9**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| DAC_DATA   | 7:0  | 0x0     | VGA Palette (DAC) Data. Use DAC_R_INDEX and DAC_W_INDEX to set read or write mode, and entry to access.<br>Access order is Red, Green, Blue, and then auto-increment occurs to next entry.<br>DAC_8BIT_EN controls whether 6 or 8 bit access. |

VGA Palette (DAC) Data

**DAC\_MASK - RW - 8 bits - VGA\_IO:0x3C6**

| Field Name                                       | Bits | Default | Description  |
|--|------|---------|--|
| DAC_MASK<br><i>(mirror of DAC_CNTL:DAC_MASK)</i> | 7:0  | 0x0     | Masks off usage of individual palette index bits before pixel index is looked-up in the palette.<br>0 = do not use this bit of the index<br>1 = use this bit of the index<br>Only has an effect in VGA emulation modes (CRTC_EXT_DISP_EN=0), not for VESA modes or extended display modes. |

Palette index mask for VGA emulation modes.

**DAC\_R\_INDEX - RW - 8 bits - VGA\_IO:0x3C7**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**DAC\_R\_INDEX - RW - 8 bits - VGA\_IO:0x3C7**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| DAC_R_INDEX | 7:0  | 0x0     | Write: Sets the index for a palette (DAC) read operation. Index auto-increments after every third read of DAC_DATA.<br>Read: Indicates if palette in read or write mode.<br>0 = Palette in write mode (DAC_W_INDEX last written).<br>3 = Palette in read mode (DAC_R_INDEX last written).<br>Also see DAC_W_INDEX. |

Palette (DAC) Read Index

**DAC\_W\_INDEX - RW - 8 bits - VGA\_IO:0x3C8**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| DAC_W_INDEX | 7:0  | 0x0     | Sets the index for a palette (DAC) write operation. Index auto-increments after every third write of DAC_DATA. Also see DAC_R_INDEX. |

Palette (DAC) Write Index

**DAC\_EXT\_CNTL - RW - 32 bits - [MMReg:0x280]**

| Field Name              | Bits | Default | Description  |
|-------------------------|------|---------|--|
| DAC2_FORCE_BLANK_OFF_EN | 0    | 0x0     | 0=Normal DAC2 BLANK functionality.<br>1=DAC2 BLANK forced off. Use this setting with DAC FORCE logic to detect CRT connection.   |
| DAC2_FORCE_DATA_EN      | 1    | 0x0     | 0=DAC2 FORCE logic disabled<br>1=DAC2 input data forced as per DAC_FORCE_DATA_SEL and DAC_FORCE_DATA fields  |
| DAC_FORCE_BLANK_OFF_EN  | 4    | 0x0     | When doing DAC comparator test this is best set to 1 so horizontal and vertical retraces do not interrupt the testing.<br>0=Normal DAC BLANK functionality.<br>1=DAC BLANK forced off. Use this setting with DAC FORCE logic to detect CRT connection. |
| DAC_FORCE_DATA_EN       | 5    | 0x0     | Enables DAC force logic.<br>0=DAC FORCE logic disabled<br>1=DAC input data forced as per DAC_FORCE_DATA_SEL and DAC_FORCE_DATA fields  |
| DAC_FORCE_DATA_SEL      | 7:6  | 0x0     | Selects combination of black (0x00) and DAC_FORCE_DATA value forced on red, green and blue DAC channels.<br>0=R=DAC_FORCE_DATA,G=B=0x00<br>1=G=DAC_FORCE_DATA,R=B=0x00<br>2=B=DAC_FORCE_DATA,R=G=0x00<br>3=R=G=B=DAC_FORCE_DATA                        |
| DAC_FORCE_DATA          | 17:8 | 0x0     | Data forced on DAC channels as per DAC_FORCE_DATA_SEL and DAC_FORCE_DATA_EN.   |

DAC force control for analog monitor connection detection. This is used in combination with the DAC\_CNTL register comparator fields.

**DAC\_CRC\_SIG1 - R - 32 bits - [MMReg:0xD18]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**DAC\_CRC\_SIG1 - R - 32 bits - [MMReg:0xD18]**

| Field Name    | Bits  | Default | Description  |
|---------------|-------|---------|--|
| DAC_CRC_SIG_B | 9:0   | 0x0     | CRC signature value for blue data.<br>When reset,<br>CRCB(9:0) <= 0x3FF;<br>When CRC is running,<br>CRCB(9:1) <= CRCB(8:0) xor blue(9:1),<br>CRCB(0) <= CRCB(9) xor CRCB(2) xor blue(0)    |
| DAC_CRC_SIG_G | 25:16 | 0x0     | CRC signature value for green data.<br>When reset,<br>CRCG(9:0) <= 0x3FF;<br>When CRC is running,<br>CRCG(9:1) <= CRCG(8:0) xor green(9:1),<br>CRCG(0) <= CRCG(9) xor CRCG(2) xor green(0) |

CRC signature value for blue and green components. Use DAC\_CRC\_EN to initiate a field or frame analysis. See DAC\_CRC\_EN for details.

**DAC\_CRC\_SIG2 - R - 32 bits - [MMReg:0xD1C]**

| Field Name    | Bits  | Default | Description  |
|---------------|-------|---------|--|
| DAC_CRC_SIG_R | 9:0   | 0x0     | CRC signature value for red data.<br>When reset,<br>CRCR(9:0) <= 0x3FF;<br>When CRC is running,<br>CRCR(9:1) <= CRCR(8:0) xor red(9:1),<br>CRCR(0) <= CRCR(9) xor CRCR(2) xor red(0)   |
| DAC_CRC_SIG_C | 21:16 | 0x0     | CRC signature value for control signals.<br>The control signal input vector is made up as follows:<br>control(0) <= not blank (0 in retrace, 1 in active or overscan)<br>control(1) <= Display Enable (0 in retrace or overscan, 1 in active)<br>control(2) <= HSYNC<br>control(3) <= VSYNC<br>control(4) <= AUXWIN<br>control(5) <= STEREO SYNC<br>When reset,<br>CRCC(5:0) <= 0x3F;<br>When CRC is running,<br>CRCC(5:1) <= CRCC(4:0) xor control(5:1),<br>CRCC(0) <= CRCC(5) xor CRCC(0) xor control(0) |

CRC signature value for red component and control signals. Use DAC\_CRC\_EN to initiate a field or frame analysis. See DAC\_CRC\_EN for details.

**DAC\_CRC2\_SIG1 - R - 32 bits - [MMReg:0xD70]**

| Field Name     | Bits  | Default | Description  |
|----------------|-------|---------|--|
| DAC_CRC2_SIG_B | 9:0   | 0x0     | CRC signature value for blue data.<br>When reset,<br>CRCB(9:0) <= 0x3FF;<br>When CRC is running,<br>CRCB(9:1) <= CRCB(8:0) xor blue(9:1),<br>CRCB(0) <= CRCB(9) xor CRCB(2) xor blue(0)    |
| DAC_CRC2_SIG_G | 25:16 | 0x0     | CRC signature value for green data.<br>When reset,<br>CRCG(9:0) <= 0x3FF;<br>When CRC is running,<br>CRCG(9:1) <= CRCG(8:0) xor green(9:1),<br>CRCG(0) <= CRCG(9) xor CRCG(2) xor green(0) |

**DAC\_CRC2\_SIG1 - R - 32 bits - [MMReg:0xD70]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

Secondary display path CRC signature vales for the blue and green components

**DAC\_CRC2\_SIG2 - R - 32 bits - [MMReg:0xD74]**

| Field Name     | Bits  | Default | Description  |
|----------------|-------|---------|--|
| DAC_CRC2_SIG_R | 9:0   | 0x0     | CRC signature value for red data.<br>When reset,<br>CRCR(9:0) <= 0x3FF;<br>When CRC is running,<br>CRCR(9:1) <= CRCR(8:0) xor red(9:1),<br>CRCR(0) <= CRCR(9) xor CRCR(2) xor red(0)   |
| DAC_CRC2_SIG_C | 21:16 | 0x0     | CRC signature value for control signals.<br>The control signal input vector is made up as follows:<br>control(0) <= not blank (0 in retrace, 1 in active or<br>overscan)<br>control(1) <= Display Enable (0 in retrace or overscan, 1 in<br>active)<br>control(2) <= HSYNC<br>control(3) <= VSYNC<br>control(4) <= AUXWIN<br>control(5) <= STEREO SYNC<br>When reset,<br>CRCC(5:0) <= 0x3F;<br>When CRC is running,<br>CRCC(5:1) <= CRCC(4:0) xor control(5:1),<br>CRCC(0) <= CRCC(5) xor CRCC(0) xor control(0) |

Secondary display path CRC signature value for red component and control signals. Use DAC\_CRC\_EN to initiate a field or frame analysis. See DAC\_CRC\_EN for details.

**DAC\_CNTL2 - RW - 32 bits - [IOReg,MMReg:0x7C]**

| Field Name                       | Bits | Default | Description  |
|----------------------------------|------|---------|--|
| DAC_CLK_SEL<br>(DISPLAY)         | 0    | 0x0     | 0=Selects Primary Display (CRTC1) as source for CRT<br>DAC<br>1=Selects Secondary Display (CRTC2) as source for<br>CRT DAC                                     |
| DAC2_CLK_SEL<br>(DISPLAY)        | 1    | 0x0     | 0=Selects TV OUT as source for TV DAC<br>1=Use TV DAC as secondary CRT. For source of display<br>check CRT2_DISP1_SEL@DISP_HW_DEBUG                            |
| PALETTE_ACCESS_CNTL<br>(DISPLAY) | 5    | 0x0     | 0=Access Primary Palette through PALETTE_INDEX<br>and PALETTE_DATA registers<br>1=Access Secondary Palette through PALETTE_INDEX<br>and PALETTE_DATA registers |
| DAC2_CMP_EN<br>(DISPLAY)         | 7    | 0x0     |  |
| DAC2_CMP_OUT_R (R)<br>(DISPLAY)  | 8    | 0x0     |  |
| DAC2_CMP_OUT_G (R)<br>(DISPLAY)  | 9    | 0x0     |  |
| DAC2_CMP_OUT_B (R)<br>(DISPLAY)  | 10   | 0x0     |  |
| DAC2_CMP_OUTPUT (R)<br>(DISPLAY) | 11   | 0x0     |  |

**DAC\_CNTL2 - RW - 32 bits - [IOReg,MMReg:0x7C]**

| Field Name                          | Bits  | Default | Description  |
|-------------------------------------|-------|---------|--|
| DAC2_EXPAND_MODE<br>(DISPLAY)       | 14    | 0x0     | 0=Convert 4, 5 & 6 bit colors to 8 bits by zero extension<br>1=Convert 4, 5 & 6 bit colors to 8 bits by dynamic expansion                  |
| CRT2_SENSE (R)<br>(DISPLAY)         | 16    | 0x0     | 0=Secondary CRT Monitor Detection result - not connected<br>1=Secondary CRT Monitor Detection result - connected                           |
| CRT2_DETECTION_ON<br>(DISPLAY)      | 17    | 0x0     | 0=Secondary CRT Monitor Detection disabled<br>1=Secondary CRT Monitor Detection enabled  |
| DAC_CRC2_CONT_EN<br>(DISPLAY)       | 18    | 0x0     | 0=DAC CRC2 runs in one shot mode.<br>1=DAC CRC2 runs in continuous mode.   |
| DAC_CRC2_EN<br>(DISPLAY)            | 19    | 0x0     | 0=Reset DAC CRC2.<br>1=Enable DAC CRC2 for next frame/field in one shot, or all frames/fields in continuous mode.                          |
| DAC_CRC2_FIELD<br>(DISPLAY)         | 20    | 0x0     | 0=If interlace display and one shot mode, then CRC even field only<br>1=If interlace display and one shot mode, then CRC odd field only    |
| DAC2_LUT_COUNTER_LIMIT<br>(DISPLAY) | 22:21 | 0x0     | 0=anti-sparkle timeout 3 clocks<br>1=anti-sparkle timeout 7 clocks<br>2=anti-sparkle timeout 15 clocks<br>3=anti-sparkle timeout 31 clocks |

No description available for this register.

**DAC\_MACRO\_CNTL - RW - 32 bits - [MMReg:0xD04]**

| Field Name     | Bits | Default | Description |
|----------------|------|---------|-------------|
| DAC_WHITE_CNTL | 3:0  | 0x8     |             |
| DAC_BG_ADJ     | 11:8 | 0x8     |             |
| DAC_PDWN_R     | 16   | 0x0     |             |
| DAC_PDWN_G     | 17   | 0x0     |             |
| DAC_PDWN_B     | 18   | 0x0     |             |

Graphics & cursor base address

**14. vgaStat Detailed Register Reference**

General purpose status VGA

**GENFC\_RD - R - 8 bits - VGA\_IO:0x3CA**

| Field Name   | Bits | Default | Description   |
|--|------|---------|---|
| VSYNC_SEL_R<br><i>(mirror of GENFC_WT:VSYNC_SEL_W)</i> | 3    | 0x0     | Vertical sync select (read).<br>0=Normal vertical sync<br>1=Sync is 'vertical sync' ORed with 'vertical display enable' |

Feature Control Register (Read)

**GENFC\_WT - W - 8 bits - [VGA\_IO:0x3BA] [VGA\_IO:0x3DA]**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| VSYNC_SEL_W | 3    | 0x0     | Vertical sync select (write).<br>0=Normal vertical sync<br>1=Sync is 'vertical sync' ORed with 'vertical display enable' |

Feature Control Register (Read)

**GENMO\_WT - W - 8 bits - VGA\_IO:0x3C2**

| Field Name                    | Bits | Default | Description  |
|-------------------------------|------|---------|--|
| GENMO_MONO_ADDRESS_B<br>(BIF) | 0    | 0x0     | VGA addressing mode.<br>0=Monochrome emulation, regs at 0x3Bx<br>1=Color/Graphic emulation, regs at 0x3Dx  |
| VGA_RAM_EN<br>(BIF)           | 1    | 0x0     | Enables/Disables CPU access to video RAM at VGA aperture.<br>0=Disable<br>1=Enable   |
| VGA_CKSEL<br>(DISPLAY)        | 3:2  | 0x0     | Selects pixel clock frequency to use in VGA modes. Used when CRTC_GEN_CNTL.CRTC_EXT_DISP_EN=0. See CLOCK_CNTL_INDEX.PPLL_DIV_SEL for non-VGA mode pixel clock selection.<br>0=25.1744MHz (640 Pels)<br>1=28.3212MHz (720 Pels)<br>2=Reserved<br>3=Reserved   |
| ODD_EVEN_MD_PGSEL<br>(HDP)    | 5    | 0x0     | This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled.<br>Used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory.<br>0=Selects odd (high) memory locations<br>1=Selects even (low) memory locations |
| VGA_HSYNC_POL<br>(DISPLAY)    | 6    | 0x0     | Determines polarity of horizontal sync (HSYNC) for VGA modes.<br>0 = HSYNC pulse active high<br>1 = HSYNC pulse active low<br>The convention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes.  |

**GENMO\_WT - W - 8 bits - VGA\_IO:0x3C2**

| Field Name                     | Bits | Default | Description  |
|--------------------------------|------|---------|--|
| VGA_VSYNC_POL<br><br>(DISPLAY) | 7    | 0x0     | Determines polarity of vertical sync (VSYNC) for VGA modes.<br>0 = VSYNC pulse active high<br>1 = VSYNC pulse active low<br>The covention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes. |

Miscellaneous Output Register (Write)

**GENMO\_RD - R - 8 bits - VGA\_IO:0x3CC**

| Field Name  | Bits | Default | Description  |
|---|------|---------|--|
| GENMO_MONO_ADDRESS_B<br><br><i>(mirror of<br/>GENMO_WT:GENMO_MONO_ADDRESS_B)</i><br><br>(BIF) | 0    | 0x0     | VGA addressing mode.   |
| VGA_RAM_EN<br><br><i>(mirror of GENMO_WT:VGA_RAM_EN)</i><br><br>(BIF)                         | 1    | 0x0     | Enables/Disables CPU access to video RAM at VGA aperture.  |
| VGA_CKSEL<br><br><i>(mirror of GENMO_WT:VGA_CKSEL)</i><br><br>(DISPLAY)                       | 3:2  | 0x0     | Selects pixel clock frequency to use.  |
| ODD_EVEN_MD_PGSEL<br><br><i>(mirror of<br/>GENMO_WT:ODD_EVEN_MD_PGSEL)</i><br><br>(HDP)       | 5    | 0x0     | This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled.<br>Used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory.                   |
| VGA_HSYNC_POL<br><br><i>(mirror of GENMO_WT:VGA_HSYNC_POL)</i><br><br>(DISPLAY)               | 6    | 0x0     | Determines polarity of horizontal sync (HSYNC) for VGA modes.<br>0 = HSYNC pulse active high<br>1 = HSYNC pulse active low<br>The covention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes. |
| VGA_VSYNC_POL<br><br><i>(mirror of GENMO_WT:VGA_VSYNC_POL)</i><br><br>(DISPLAY)               | 7    | 0x0     | Determines polarity of vertical sync (VSYNC) for VGA modes.<br>0 = VSYNC pulse active high<br>1 = VSYNC pulse active low<br>The covention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes.   |

Miscellaneous Output Register (Read)

**GENS0 - R - 8 bits - VGA\_IO:0x3C2**

| Field Name   | Bits | Default | Description  |
|--------------|------|---------|--|
| SENSE_SWITCH | 4    | 0x0     | DAC comparator read back. Used for monitor detection.<br>Mirror of DAC_CMP_OUTPUT@DAC_CNTL. See description there. |

**GENS0 - R - 8 bits - VGA\_IO:0x3C2**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| CRT_INTR   | 7    | 0x0     | CRT Interrupt:<br>0=Vertical retrace interrupt is cleared<br>1=Vertical retrace interrupt is pending |

Input Status 0 Register

**GENS1 - R - 8 bits - [VGA\_IO:0x3BA] [VGA\_IO:0x3DA]**

| Field Name      | Bits | Default | Description  |
|-----------------|------|---------|--|
| NO_DIPLAY       | 0    | 0x0     | Display enable.<br>0=Enable<br>1=Disable   |
| VGA_VSTATUS     | 3    | 0x0     | Vertical Retrace Status.<br>0=Vertical retrace not active<br>1=Vertical retrace active   |
| PIXEL_READ_BACK | 5:4  | 0x0     | Diagnostic bits 0, 1 respectively.<br>These two bits are connected to two of the eight colour outputs (P7:P0) of the attribute controller. Connections are controlled by ATTR12(5,4) as follows:<br>0=P2,P0<br>1=P5,P4<br>2=P3,P1<br>3=P7,P6 |

Input Status 1 Register

**GRPH\_BUFFER\_CNTL - RW - 32 bits - [MMReg:0x2F0]**

| Field Name           | Bits  | Default | Description   |
|----------------------|-------|---------|---|
| GRPH_START_REQ       | 6:0   | 0x5c    | Request watermark where display requests to memory controller will start. Normally set to the upper limit.<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO.   |
| GRPH_STOP_REQ        | 14:8  | 0x5c    | Request watermark where display requests to memory controller will stop. Normally set to the upper limit.<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO.  |
| GRPH_CRITICAL_POINT  | 22:16 | 0x20    | Read data watermark where pending display requests to the memory controller go to high priority. This forces the memory controller to service the pending display requests ASAP. Setting 0x00 forces all display requests to remain high priority at all times. |
| GRPH_CRITICAL_CNTL   | 28    | 0x0     | For debug. Should always be set low.<br>0=Critical point based on current lowest write point.<br>1=Critical point based on last write point.  |
| GRPH_BUFFER_SIZE     | 29    | 0x1     | For debug. Should always be set high.<br>0=Extended mode graphics buffer is 64 entries maximum.<br>1=Extended mode graphics buffer is 96 entries maximum.   |
| GRPH_CRITICAL_AT_SOF | 30    | 0x0     | For debug. Should always be set low.<br>0=Wait 1/2 line before going critical at start of each frame.<br>1=Go critical immediately at the start of each frame.  |

**GRPH\_BUFFER\_CNTL - RW - 32 bits - [MMReg:0x2F0]**

| Field Name     | Bits | Default | Description   |
|----------------|------|---------|---|
| GRPH_STOP_CNTL | 31   | 0x0     | For debug. Should always be set low.<br>0=GRPH_STOP_REQ and VGA_STOP_REQ are -4 from actual stop point.<br>1=GRPH_STOP_REQ and VGA_STOP_REQ are exact stop point. |

Control of display buffer fill requests for non-VGA modes. This register is programmed by the BIOS or DAL on display mode switches.

**VGA\_BUFFER\_CNTL - RW - 32 bits - [MMReg:0x2F4]**

| Field Name         | Bits  | Default | Description   |
|--------------------|-------|---------|---|
| VGA_START_REQ      | 5:0   | 0x3c    | Request watermark where display requests to memory controller will start.<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO.  |
| VGA_STOP_REQ       | 13:8  | 0x3c    | Request watermark where display requests to memory controller will stop.<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO.   |
| VGA_CRITICAL_POINT | 21:16 | 0x20    | Read data watermark where pending display requests to the memory controller go to high priority. Setting 0x00 forces all display requests to remain high priority at all times. |

Control of display buffer fill requests for VGA modes. This register is programmed by the BIOS on VGA mode switches.

**GRPH2\_BUFFER\_CNTL - RW - 32 bits - [MMReg:0x3F0]**

| Field Name            | Bits  | Default | Description   |
|-----------------------|-------|---------|---|
| GRPH2_START_REQ       | 6:0   | 0x5c    | Request watermark where display requests to memory controller will start. Normally set to the upper limit.<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO.   |
| GRPH2_STOP_REQ        | 14:8  | 0x5c    | Request watermark where display requests to memory controller will stop. Normally set to the upper limit.<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO.  |
| GRPH2_CRITICAL_POINT  | 22:16 | 0x20    | Read data watermark where pending display requests to the memory controller go to high priority. This forces the memory controller to service the pending display requests ASAP. Setting 0x00 forces all display requests to remain high priority at all times. |
| GRPH2_CRITICAL_CNTL   | 28    | 0x0     | For debug. Should always be set low.<br>0=Critical point based on current lowest write point.<br>1=Critical point based on last write point.  |
| GRPH2_BUFFER_SIZE     | 29    | 0x1     | For debug. Should always be set high.<br>0=Extended mode graphics buffer is 64 entries maximum.<br>1=Extended mode graphics buffer is 96 entries maximum.   |
| GRPH2_CRITICAL_AT_SOF | 30    | 0x0     | For debug. Should always be set low.<br>0=Wait 1/2 line before going critical at start of each frame.<br>1=Go critical immediately at the start of each frame.  |
| GRPH2_STOP_CNTL       | 31    | 0x0     | For debug. Should always be set low.<br>0=GRPH_STOP_REQ is -4 from actual stop point.<br>1=GRPH_STOP_REQ is exact stop point.   |

**GRPH2\_BUFFER\_CNTL - RW - 32 bits - [MMReg:0x3F0]****Field Name****Bits****Default****Description**

Control of secondary display buffer fill requests. This register is programmed by the BIOS or DAL on display mode switches.

**GEN\_INT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x40]****Field Name****Bits****Default****Description**

CRTC\_VBLANK\_MASK

0

0x0

Vertical blank interrupt mask.

0=Disable

1=Enable

(DISPLAY)

CRTC\_VLINE\_MASK

1

0x0

Vertical line interrupt mask.

0=Disable

1=Enable

(DISPLAY)

CRTC\_VSYNC\_MASK

2

0x0

Vertical sync interrupt mask.

0=Disable

1=Enable

(DISPLAY)

SNAPSHOT\_MASK

3

0x0

Snapshot interrupt mask.

0=Disable

1=Enable

(DISPLAY)

FP\_DETECT\_MASK

4

0x0

Hot plug detect (HPD) interrupt mask.

0=Disable

1=Enable

(DISPLAY)

CRTC2\_VLINE\_MASK

5

0x0

0=Disable

1=Enable

(DISPLAY)

CRTC2\_VSYNC\_MASK

6

0x0

0=Disable

1=Enable

(DISPLAY)

SNAPSHOT2\_MASK

7

0x0

0=Disable

1=Enable

(DISPLAY)

CRTC2\_VBLANK\_MASK

9

0x0

0=Disable

1=Enable

(DISPLAY)

FP2\_DETECT\_MASK

10

0x0

0=Disable

1=Enable

(DISPLAY)

VSYNC\_DIFF\_OVER\_LIMIT\_MASK

11

0x0

0=Disable

1=Enable

(TVOUT)

DMA\_VIPH0\_INT\_EN

12

0x0

0=Disable

1=Enable

(VIP)

DMA\_VIPH1\_INT\_EN

13

0x0

0=Disable

1=Enable

(VIP)

DMA\_VIPH2\_INT\_EN

14

0x0

0=Disable

1=Enable

(VIP)

DMA\_VIPH3\_INT\_EN

15

0x0

0=Disable

1=Enable

(VIP)

I2C\_INT\_EN

17

0x0

0=Disable

1=Enable

(VIP)

GUI\_IDLE\_MASK

19

0x0

GUI idle interrupt mask.

0=Disable

1=Enable

(RBBM)

**GEN\_INT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x40]**

| Field Name                            | Bits | Default | Description  |
|---------------------------------------|------|---------|--|
| VIPH_INT_EN<br>(VIP)                  | 24   | 0x0     | 0=Disable<br>1=Enable  |
| SW_INT_EN<br>(HDP)                    | 25   | 0x0     | Software interrupt mask.<br>0=Disable<br>1=Enable                  |
| GEYSERVILLE_MASK<br>(VIP)             | 27   | 0x0     | 0=Disable<br>1=Enable  |
| HDCP_AUTHORIZED_INT_MASK<br>(DISPLAY) | 28   | 0x0     | 0=Disable<br>1=Enable  |
| DVI_I2C_INT_MASK<br>(DISPLAY)         | 29   | 0x0     | 0=Disable<br>1=Enable  |
| GUIDMA_MASK<br>(CP)                   | 30   | 0x0     | GUI DMA channel interrupt mask.<br>0=Disable<br>1=Enable           |
| VIDDMA_MASK<br>(CP)                   | 31   | 0x0     | Video capture DMA channel interrupt mask.<br>0=Disable<br>1=Enable |

General Interrupt Control register.

The MASK/EN fields control whether the respective status bits are enabled to drive the system interrupt pin. Even if enabled here, the interrupt line is not driven unless enabled in the PCI configuration space.

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                           | Bits | Default | Description   |
|--------------------------------------|------|---------|---|
| CRTC_VBLANK_STAT (R)<br>(DISPLAY)    | 0    | 0x0     | Vertical blank interrupt. Set when display in vertical retrace.<br>0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC_VBLANK_STAT_AK (W)<br>(DISPLAY) | 0    | 0x0     | Vertical blank interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| CRTC_VLINE_STAT (R)<br>(DISPLAY)     | 1    | 0x0     | Vertical line interrupt. Set on display line on programmed by the CRTC_VLINE_CRNT_VLINE.CRTC_VLINE register.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| CRTC_VLINE_STAT_AK (W)<br>(DISPLAY)  | 1    | 0x0     | Vertical line interrupt acknowledge.<br>0=No effect<br>1=Clear status   |
| CRTC_VSYNC_STAT (R)<br>(DISPLAY)     | 2    | 0x0     | Vertical sync interrupt. Set on start of VSYNC at the DAC.<br>0=No event<br>1=Event has occurred, interrupting if enabled   |
| CRTC_VSYNC_STAT_AK (W)<br>(DISPLAY)  | 2    | 0x0     | Vertical sync interrupt acknowledge.<br>0=No effect<br>1=Clear status   |
| SNAPSHOT_STAT (R)<br>(DISPLAY)       | 3    | 0x0     | Snapshot interrupt. Set as controlled by SNAPSHOT_VIF_COUNT register.<br>0=No event<br>1=Event has occurred, interrupting if enabled  |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                                   | Bits | Default | Description  |
|--|------|---------|--|
| SNAPSHOT_STAT_AK (W)<br>(DISPLAY)            | 3    | 0x0     | Snapshot interrupt acknowledge.<br>0=No effect<br>1=Clear status   |
| FP_DETECT_STAT (R)<br>(DISPLAY)              | 4    | 0x0     | Hot plug detect (HPD) interrupt. Set on HPD connect or disconnect as controlled by FP_GEN_CNTL.FP_DETECT_INT_POL.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| FP_DETECT_STAT_AK (W)<br>(DISPLAY)           | 4    | 0x0     | Hot plug detect (HPD) interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| CRTC2_VLINE_STAT (R)<br>(DISPLAY)            | 5    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC2_VLINE_STAT_AK (W)<br>(DISPLAY)         | 5    | 0x0     | 0=No effect<br>1=Clear status  |
| CRTC2_VSYNC_STAT (R)<br>(DISPLAY)            | 6    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC2_VSYNC_STAT_AK (W)<br>(DISPLAY)         | 6    | 0x0     | 0=No effect<br>1=Clear status  |
| SNAPSHOT2_STAT (R)<br>(DISPLAY)              | 7    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| SNAPSHOT2_STAT_AK (W)<br>(DISPLAY)           | 7    | 0x0     | 0=No effect<br>1=Clear status  |
| CAP0_INT_ACTIVE (R)<br>(VIP)                 | 8    | 0x0     | Capture port 0 has active interrupt(s).<br>0=Capture port 0 not source of any active interrupt<br>1=Capture port 0 has active interrupt(s)                                       |
| CRTC2_VBLANK_STAT (R)<br>(DISPLAY)           | 9    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC2_VBLANK_STAT_AK (W)<br>(DISPLAY)        | 9    | 0x0     | 0=No effect<br>1=Clear status  |
| FP2_DETECT_STAT (R)<br>(DISPLAY)             | 10   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| FP2_DETECT_STAT_AK (W)<br>(DISPLAY)          | 10   | 0x0     | 0=No effect<br>1=Clear status  |
| VSYNC_DIFF_OVER_LIMIT_STAT (R)<br>(TVOUT)    | 11   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| VSYNC_DIFF_OVER_LIMIT_STAT_AK (W)<br>(TVOUT) | 11   | 0x0     | 0=No effect<br>1=Clear status  |
| DMA_VIPH0_INT (R)<br>(VIP)                   | 12   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| DMA_VIPH0_INT_AK (W)<br>(VIP)                | 12   | 0x0     | 0=No effect<br>1=Clear status  |
| DMA_VIPH1_INT (R)<br>(VIP)                   | 13   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                                | Bits | Default | Description   |
|---|------|---------|---|
| DMA_VIPH1_INT_AK (W)<br>(VIP)             | 13   | 0x0     | 0=No effect<br>1=Clear status   |
| DMA_VIPH2_INT (R)<br>(VIP)                | 14   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DMA_VIPH2_INT_AK (W)<br>(VIP)             | 14   | 0x0     | 0=No effect<br>1=Clear status   |
| DMA_VIPH3_INT (R)<br>(VIP)                | 15   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DMA_VIPH3_INT_AK (W)<br>(VIP)             | 15   | 0x0     | 0=No effect<br>1=Clear status   |
| I2C_INT (R)<br>(VIP)                      | 17   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| I2C_INT_AK (W)<br>(VIP)                   | 17   | 0x0     | 0=No effect<br>1=Clear status   |
| GUI_IDLE_STAT (R)<br>(RBBM)               | 19   | 0x1     | GUI idle interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled  |
| GUI_IDLE_STAT_AK (W)<br>(RBBM)            | 19   | 0x0     | GUI idle interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| VIPH_INT (R)<br>(VIP)                     | 24   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| SW_INT (R)<br>(HDP)                       | 25   | 0x0     | Software interrupt. General purpose interrupt that can only be set by software event by writing to SW_INT_SET.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| SW_INT_AK (W)<br>(HDP)                    | 25   | 0x0     | Software interrupt acknowledge.<br>0=No effect<br>1=Clear SW_INT (set low)  |
| SW_INT_SET (W)<br>(HDP)                   | 26   | 0x0     | Software interrupt trigger.<br>0=No effect<br>1=Set SW_INT active (high)  |
| GEYSERVILLE_STAT (R)<br>(VIP)             | 27   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| GEYSERVILLE_STAT_AK (W)<br>(VIP)          | 27   | 0x0     | 0=No effect<br>1=Clear status   |
| HDCP_AUTHORIZED_INT_STAT (R)<br>(DISPLAY) | 28   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| HDCP_AUTHORIZED_INT_AK (W)<br>(DISPLAY)   | 28   | 0x0     | 0=No effect<br>1=Clear status   |
| DVI_I2C_INT_STAT (R)<br>(DISPLAY)         | 29   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DVI_I2C_INT_AK (W)<br>(DISPLAY)           | 29   | 0x0     | 0=No effect<br>1=Clear status   |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name              | Bits | Default | Description   |
|-------------------------|------|---------|---|
| GUIDMA_STAT (R)<br>(CP) | 30   | 0x0     | GUI DMA channel interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled           |
| GUIDMA_AK (W)<br>(CP)   | 30   | 0x0     | GUI DMA channel interrupt acknowledge.<br>0=No effect<br>1=Clear status                             |
| VIDDMA_STAT (R)<br>(CP) | 31   | 0x0     | Video capture DMA channel interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| VIDDMA_AK (W)<br>(CP)   | 31   | 0x0     | Video capture DMA channel interrupt acknowledge.<br>0=No effect<br>1=Clear status                   |

General Interrupt Status register.

These fields can be polled and acknowledged even if interrupts are disabled, or the respective fields are masked in the GEN\_INT\_CNTL register.

**15. vgaSeq Detailed Register Reference**

## VGA Sequencer Registers

| <b>SEQ00 - RW - 8 bits - VGASEQIND:0x0</b> |             |                |   |
|--|-------------|----------------|---|
| <b>Field Name</b>                          | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| SEQ_RST0B                                  | 0           | 0x1            | Synchronous reset bit 0:<br>0=Follows SEQ_RST1B<br>1=Sequencer runs unless SEQ_RST1B=0  |
| SEQ_RST1B                                  | 1           | 0x1            | Synchronous reset bit 1:<br>0=Disable character clock, display requests, and H/V syncs<br>1=Sequencer runs unless SEQ_RST0B=0 |

Reset Register

| <b>SEQ01 - RW - 8 bits - VGASEQIND:0x1</b> |             |                |   |
|--|-------------|----------------|---|
| <b>Field Name</b>                          | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| SEQ_DOT8                                   | 0           | 0x1            | 8/9 Dot Clocks (Modes 1, 2, 3, and 7 use 9-dot characters. To change bit 0, GENVS(0) must be logical 0).<br>0=9 dot char clock. Modes 0, 1, 2, 3 & 7<br>1=8 dot char clock.   |
| SEQ_SHIFT2                                 | 2           | 0x0            | Shift load bits.<br>0=Load video serializer every clock, if SEQ_SHIFT4=0<br>1=Load video serializer every other clock, if SEQ_SHIFT4=0  |
| SEQ_PCLKBY2                                | 3           | 0x0            | Dot Clock (typically, 320 and 360 horizontal modes use divide-by-2 to provide 40 column displays. To change this bit SEQ00[0:0] must be first set to zero.)).<br>0=Dot clock is normal<br>1=Dot clock is divided by 2 |
| SEQ_SHIFT4                                 | 4           | 0x0            | Shift load bits.<br>0=SEQ_SHIFT2 determines serializer loading<br>1=Load video serializer every fourth clock. Ignore SEQ_SHIFT2   |
| SEQ_MAXBW                                  | 5           | 0x1            | Screen off:<br>0=Normal. Screen on<br>1=Screen off and blanked. CPU has uninterrupted access to frame buffer  |

Clock Mode Register

| <b>SEQ03 - RW - 8 bits - VGASEQIND:0x3</b> |             |                |                              |
|--|-------------|----------------|------------------------------|
| <b>Field Name</b>                          | <b>Bits</b> | <b>Default</b> | <b>Description</b>           |
| SEQ_FONT_B1                                | 0           | 0x0            | Character Map Select B Bit 1 |
| SEQ_FONT_B2                                | 1           | 0x0            | Character Map Select B Bit 2 |
| SEQ_FONT_A1                                | 2           | 0x0            | Character Map Select A Bit 1 |
| SEQ_FONT_A2                                | 3           | 0x0            | Character Map Select A Bit 2 |
| SEQ_FONT_B0                                | 4           | 0x0            | Character Map Select B Bit 0 |



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**SEQ03 - RW - 8 bits - VGASEQIND:0x3**

| Field Name  | Bits | Default | Description                  |
|-------------|------|---------|------------------------------|
| SEQ_FONT_A0 | 5    | 0x0     | Character Map Select A Bit 0 |

Character Map Select Register

**SEQ8\_IDX - RW - 8 bits - VGA\_IO:0x3C4**

| Field Name                 | Bits | Default | Description  |
|----------------------------|------|---------|--|
| SEQ_IDX<br>(HDP) (DISPLAY) | 2:0  | 0x0     | This index points to one of the sequencer registers (SEQ_) at I/O port address 0x3C5, for the next SEQ read/write operation. |

SEQ Index Register

**SEQ8\_DATA - RW - 8 bits - VGA\_IO:0x3C5**

| Field Name                  | Bits | Default | Description              |
|-----------------------------|------|---------|--------------------------|
| SEQ_DATA<br>(HDP) (DISPLAY) | 7:0  | 0x0     | SEQ data indirect access |

SEQ Data Register

**16. vgaCrt Detailed Register Reference**

## VGA CRT Registers

**CRTC8\_IDX - RW - 8 bits - [VGA\_IO:0x3B4] [VGA\_IO:0x3D4]**

| Field Name  | Bits | Default | Description   |
|---|------|---------|---|
| VCRTC_IDX<br><i>(mirror bits 0:5 of<br/>CRTC_EXT_CNTL:VCRTC_IDX_MASTER)</i> | 5:0  | 0x0     | This index points to one of the internal registers of the CRT controller (CRTC) at address 0x3?5, for the next CRTC read/write operation. |

(HDP) (DISPLAY)

CRT Index Register

**CRTC8\_DATA - RW - 8 bits - [VGA\_IO:0x3B5] [VGA\_IO:0x3D5]**

| Field Name | Bits | Default | Description               |
|------------|------|---------|---------------------------|
| VCRTC_DATA | 7:0  | 0x0     | CRTC data indirect access |

(HDP) (DISPLAY)

CRTC Data Register

**CRT00 - RW - 8 bits - VGACRTIND:0x0**

| Field Name  | Bits | Default | Description  |
|---|------|---------|--|
| H_TOTAL<br><i>(mirror bits 0:7 of<br/>CRTC_H_TOTAL_DISP:CRTC_H_TOTAL)</i> | 7:0  | 0x0     | These bits define the active horizontal display in a scan line, including the retrace period. The value is five less than the total number of displayed characters in a scan line. |

Horizontal Total Register

**CRT01 - RW - 8 bits - VGACRTIND:0x1**

| Field Name  | Bits | Default | Description   |
|---|------|---------|---|
| H_DISP_END<br><i>(mirror bits 0:7 of<br/>CRTC_H_TOTAL_DISP:CRTC_H_DISP)</i> | 7:0  | 0x0     | These bits define the active horizontal display in a scan line. The value is one less than the total number of displayed characters in a scan line. |

Horizontal Display Enable End Register

**CRT02 - RW - 8 bits - VGACRTIND:0x2**

| Field Name    | Bits | Default | Description  |
|---------------|------|---------|--|
| H_BLANK_START | 7:0  | 0x0     | These bits define the horizontal character count that represents the character count in the active display area plus the right border. In other words, the count is from the start of active display to the start of triggering of the H blanking pulse. |

Start Horizontal Blanking Register

**CRT03 - RW - 8 bits - VGACRTIND:0x3**

| Field Name  | Bits | Default | Description   |
|-------------|------|---------|---|
| H_BLANK_END | 4:0  | 0x0     | H blanking bits 4-0 respectively. These are the five low-order bits (of six bits in total) of horizontal character count for triggering the end of the horizontal blanking pulse. |

**CRT03 - RW - 8 bits - VGACRTIND:0x3**

| Field Name       | Bits | Default | Description  |
|------------------|------|---------|--|
| H_DE_SKEW        | 6:5  | 0x0     | Display-enable skew:<br>0=0Skew<br>1=1Skew<br>2=2Skew<br>3=3Skew |
| CR10CR11_R_DIS_B | 7    | 0x0     | Comptibility Read:<br>0=WrtOnlyToCRT10-11<br>1=WrtRdToCRT10-11   |

End Horizontal Blanking Register

**CRT04 - RW - 8 bits - VGACRTIND:0x4**

| Field Name  | Bits | Default | Description  |
|---|------|---------|--|
| H_SYNC_START<br><br><i>(mirror bits 0:7 of<br/>CRTC_H_SYNC_STRT_WID:CRTC_H_SYNC<br/>_STRT_CHAR)</i> | 7:0  | 0x0     | These bits define the horizontal character count at which the horizontal retrace pulse becomes active. |

Start Horizontal Retrace Register

**CRT05 - RW - 8 bits - VGACRTIND:0x5**

| Field Name  | Bits | Default | Description   |
|---|------|---------|---|
| H_SYNC_END<br><br><i>(mirror bits 0:4 of<br/>CRTC_H_SYNC_STRT_WID:CRTC_H_SYNC<br/>_WID)</i> | 4:0  | 0x0     | H Retrace Bits (these are the 5-bit result from the sum of CRT0 plus the width of the horizontal retrace pulse, in character clock units).      |
| H_SYNC_SKEW   | 6:5  | 0x0     | H Retrace Delay bits (these two bits skew the horizontal retrace pulse).  |
| H_BLANK_END_B5  | 7    | 0x0     | H blocking end bit 5 (this is the bit of the 6-bit character count for the H blanking end pulse). The other five low-order bits are CRT03[4:0]. |

End Horizontal Retrace Register

**CRT06 - RW - 8 bits - VGACRTIND:0x6**

| Field Name  | Bits | Default | Description  |
|---|------|---------|--|
| V_TOTAL<br><br><i>(mirror bits 0:7 of<br/>CRTC_V_TOTAL_DISP:CRTC_V_TOTAL)</i> | 7:0  | 0x0     | These are the eight low-order bits of the 10-bit vertical total register. The 2 high-order bits are CRT07[5:0] in the CRTC overflow register. The value of this register represents the total number of H raster scans plus vertical retrace (active display, blanking), minus two scan lines. |

Vertical Total Register

**CRT07 - RW - 8 bits - VGACRTIND:0x7**

| Field Name   | Bits | Default | Description   |
|--|------|---------|---|
| V_TOTAL_B8<br><br><i>(mirror bits 8:8 of<br/>CRTC_V_TOTAL_DISP:CRTC_V_TOTAL)</i>   | 0    | 0x0     | V Total Bit 8 (CRT06). Bit 8 of 10 bit vertical count for V Total. For functional description see CRT06 register.               |
| V_DISP_END_B8<br><br><i>(mirror bits 8:8 of<br/>CRTC_V_TOTAL_DISP:CRTC_V_DISP)</i> | 1    | 0x0     | End V Display Bit 8 (CRT12). Bit 8 of 10-bit vertical count for V Display enable. For functional desription see CRT12 register. |

**CRT07 - RW - 8 bits - VGACRTIND:0x7**

| Field Name   | Bits | Default | Description   |
|--|------|---------|---|
| V_SYNC_START_B8<br><i>(mirror bits 8:8 of<br/>CRTC_V_SYNC_STRT_WID:CRTC_V_SYNC_STRT)</i> | 2    | 0x0     | Start V Retrace Bit 8 (CRT10). Bit 8 of 10-bit vertical count for V Retrace start. For functional description see CRT10 register.       |
| V_BLANK_START_B8   | 3    | 0x0     | Start V Blanking Bit 8 (CRT15). Bit 8 of the 10-bit vertical count for V Blanking start. For functional description see CRT15 register. |
| LINE_CMP_B8<br><i>(mirror bits 8:8 of<br/>CRTC_VLINE_CRNT_VLINE:CRTC_VLINE)</i>          | 4    | 0x0     | Line compare bit 8 (CRT18). Bit 8 of the 10-bit vertical count for line compare. For functional description see CRT18 register.         |
| V_TOTAL_B9<br><i>(mirror bits 9:9 of<br/>CRTC_V_TOTAL_DISP:CRTC_V_TOTAL)</i>             | 5    | 0x0     | V Total Bit 9 (CRT06). Bit 9 of 10-bit vertical count for V Total. For functional description see CRT06 register.                       |
| V_DISP_END_B9<br><i>(mirror bits 9:9 of<br/>CRTC_V_TOTAL_DISP:CRTC_V_DISP)</i>           | 6    | 0x0     | End V Display Bit 9 (CRT12). Bit 9 of 10-bit vertical count for V Display enable end (for functional description see CRT12 register).   |
| V_SYNC_START_B9<br><i>(mirror bits 9:9 of<br/>CRTC_V_SYNC_STRT_WID:CRTC_V_SYNC_STRT)</i> | 7    | 0x0     | Start V Retrace Bit (CRT10). Bit 9 of 10-bit vertical count for V Retrace start. For functional description see CRT10 register.         |

CRTC Overflow Register

**CRT08 - RW - 8 bits - VGACRTIND:0x8**

| Field Name     | Bits | Default | Description  |
|----------------|------|---------|--|
| ROW_SCAN_START | 4:0  | 0x0     | Preset row scan bit 4:0. This register is used for software-controlled vertical scrolling in text or graphics modes. The value specifies the first line to be scanned after a V retrace (in the next frame). Each H Retrace pulse increments the counter by 1, up to the maximum scan line value programmed by CRT09, then the counter is cleared. |
| BYTE_PAN       | 6:5  | 0x0     | Byte panning control bits 1 and 0 (respectively). Bits 6 and 5 extend the capability of byte panning (shifting) by up to three characters (for description H_PEL Panning register ATTR13).   |

Preset Row Scan Register

**CRT09 - RW - 8 bits - VGACRTIND:0x9**

| Field Name  | Bits | Default | Description   |
|---|------|---------|---|
| MAX_ROW_SCAN  | 4:0  | 0x0     | Maximum scan line bits. These bits define a value that is the actual number of scan line per character minus 1.                 |
| V_BLANK_START_B9  | 5    | 0x0     | Start V Blanking bit 9 (CRT15). Bit 9 of 10-bit vertical count for line compare. For functional description see CRT18 register. |
| LINE_CMP_B9<br><i>(mirror bits 9:9 of<br/>CRTC_VLINE_CRNT_VLINE:CRTC_VLINE)</i> | 6    | 0x0     | Line Compare Bit 9 (CRT18). Bit 9 of 10-bit vertical count for line compare. For functional description see CRT18 register.     |

**CRT09 - RW - 8 bits - VGACRTIND:0x9**

| Field Name         | Bits | Default | Description  |
|--------------------|------|---------|--|
| DOUBLE_CHAR_HEIGHT | 7    | 0x0     | 200/400 line scan. NOTE H/V display and blanking timings etc. (in CRT00-CRT06 registers) are not affected.<br>0=200LineScan<br>1=400LineScan |

Maximum Scan Line Register

**CRT0A - RW - 8 bits - VGACRTIND:0xA**

| Field Name     | Bits | Default | Description  |
|----------------|------|---------|--|
| CURSOR_START   | 4:0  | 0x0     | Cursor start bits 4:0 (respectively). These bits define a value that is the starting scan line (on a character row) for the line cursor. The 5-bit value is equal to the actual number minus one. This value is used together with the Cursor End Bits CRT0B[4:0] to determine the height of the cursor. The cursor height in VGA does not wrap around (as in EGA) and is actually absent when the 'end' value is less than the 'start' value. In EGA when the 'end' value is less, the cursor is a full block cursor the same height as the character cell. |
| CURSOR_DISABLE | 5    | 0x0     | Cursor on/off.<br>0=on<br>1=off  |

Cursor Start Register

**CRT0B - RW - 8 bits - VGACRTIND:0xB**

| Field Name  | Bits | Default | Description   |
|-------------|------|---------|---|
| CURSOR_END  | 4:0  | 0x0     | Cursor End Bits 4-0, respectively.- These bits define the ending scan row (on a character line) for the line cursor. In EGA, this 5-bit value is equal to the actual number of lines plus one.- The cursor height in VGA does not wrap around (as in EGA) and is actually absent when the 'end' value is less than the 'start' value. In EGA when the 'end' value is less, the cursor is a full block cursor the same height as the character cell. |
| CURSOR_SKEW | 6:5  | 0x0     | Cursor Skew Bits 1 and 0, respectively.- These bits define the number of characters the cursor is to be shifted to the right (skewed) from the character pointed at by the cursor location (registers CRT0E and CRT0F), in VGA mode. Skew values when in EGA mode are enclosed in brackets.   |

Cursor End Register

**CRT0C - RW - 8 bits - VGACRTIND:0xC**

| Field Name  | Bits | Default | Description   |
|---|------|---------|---|
| DISP_START<br><i>(mirror bits 11:18 of<br/>CRTC_OFFSET:CRTC_OFFSET)</i> | 7:0  | 0x0     | SA bits 15:8-These are the eight high-order bits of the 16-bit display buffer start location. The low order bits are contained in CRT0D.-In split screen mode, CRT0C = CRT0D point to the starting location of screen A (top half.) The starting address for screen B is always zero. |

Start Address (High Byte) Register

**CRT0D - RW - 8 bits - VGACRTIND:0xD**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**CRT0D - RW - 8 bits - VGACRTIND:0xD**

| Field Name   | Bits | Default | Description  |
|--|------|---------|--|
| DISP_START<br><br><i>(mirror bits 3:10 of<br/>CRTC_OFFSET:CRTC_OFFSET)</i> | 7:0  | 0x0     | SA bits 7:0- These are the eight low-order bits of the 16-bit display buffer start location. The high-order bits are contained in CRT0C. - In split screen mode, CRT0C + CRT0D points to the starting location of screen A (top half.) The starting address for screen B is always zero. |

Start Address (Low Byte) Register

**CRT0E - RW - 8 bits - VGACRTIND:0xE**

| Field Name    | Bits | Default | Description  |
|---------------|------|---------|--|
| CURSOR_LOC_HI | 7:0  | 0x0     | CA bits 15:8- These are the eight high-order bits of the 16 bit cursor start address. The low-order CA bits are contained in CRT0F. This address is relative to the start of physical display memory address pointed to by CRT0C + CRT0D. In other words, if CRT0C + CRT0D is changed, the cursor still pints to the same character as before. |

Cursor Location (High Byte) Register

**CRT0F - RW - 8 bits - VGACRTIND:0xF**

| Field Name    | Bits | Default | Description   |
|---------------|------|---------|---|
| CURSOR_LOC_LO | 7:0  | 0x0     | CA bits 7:0- These are the eight low-order bits of the 16 bit cursor start address. The high-order CA bits are contained in CRT0E. This address is relative to the start of physical display memory address pointed to by CRT0C + CRT0D. In other words, if CRT0C + TOD is changed, the cursor still points to the same character as before |

Cursor Location (Low Byte) Register

**CRT10 - RW - 8 bits - VGACRTIND:0x10**

| Field Name  | Bits | Default | Description   |
|---|------|---------|---|
| V_SYNC_START<br><br><i>(mirror bits 0:7 of<br/>CRTC_V_SYNC_STRT_WID:CRTC_V_SYNC_STRT)</i> | 7:0  | 0x0     | Bits CRT10[7:0] are the eight low-order bits of the 10-bit vertical retrace start count. The two high-order bits are CRT07[2:7], located in the CRTC overflow register.- These bits define the horizontal scan count that triggers the V retrace pulse. |

Start Vertical Retrace Register

**CRT11 - RW - 8 bits - VGACRTIND:0x11**

| Field Name   | Bits | Default | Description  |
|--|------|---------|--|
| V_SYNC_END<br><br><i>(mirror bits 0:3 of<br/>CRTC_V_SYNC_STRT_WID:CRTC_V_SYNC_WID)</i> | 3:0  | 0x0     | V Retrace End Bits 3-0- Bits CRT11[0:3] define the horizontal scan count that triggers the end of the V Retrace pulse. |
| V_INTR_CLR   | 4    | 0x0     | V Retrace Interrupt Set:<br>0=VRetraceIntCleared<br>1=Not Cleared  |
| V_INTR_EN  | 5    | 0x0     | V Retrace Interrupt Disabled:<br>0=VRetraceIntEna<br>1=Disable   |

**CRT11 - RW - 8 bits - VGACRTIND:0x11**

| Field Name       | Bits | Default | Description  |
|------------------|------|---------|--|
| SEL5_REFRESH_CYC | 6    | 0x0     | 0=3 DRAM Refresh/Horz Line<br>1=5 DRAM Refresh/Horz Line   |
| C0T7_WR_ONLY     | 7    | 0x0     | Write Protect (CRT00-CRT06). All register bits except CRT07[4] are write protected.<br>0=EnaWrtToCRT00-07<br>1=C0T7B4WrtOnly |

End Vertical Retrace Register

**CRT12 - RW - 8 bits - VGACRTIND:0x12**

| Field Name  | Bits | Default | Description  |
|---|------|---------|--|
| V_DISP_END<br><br><i>(mirror bits 0:7 of<br/>CRTC_V_TOTAL_DISP:CRTC_V_DISP)</i> | 7:0  | 0x0     | These are the eight low-order bits of the 10-bit register containing the horizontal scan count indicating where the active display on the screen should end. The high-order bits are CRT07 [1:6] in the CRT overflow register. |

Vertical Display Enable End Register

**CRT13 - RW - 8 bits - VGACRTIND:0x13**

| Field Name  | Bits | Default | Description   |
|---|------|---------|---|
| DISP_PITCH<br><br><i>(mirror bits 0:7 of<br/>CRTC_PITCH:CRTC_PITCH)</i> | 7:0  | 0x0     | - These bits define an offset value, equal to the logical line width of the screen (from the first character of the current line to the first character of the next line).- Memory organization is dependent on the video mode. Bit CRT17[6] selects byte or word mode. Bit CRT14[6], which overrides the byte/word mode setting, selects Double-Word mode when it is logical one.- The first character of the next line is specified by the start address (CRT0C + CRT0D) plus the offset. The offset for byte mode is 2x CRT13; for word mode, 4x; for double word mode 8x. |

Offset Register

**CRT14 - RW - 8 bits - VGACRTIND:0x14**

| Field Name                         | Bits | Default | Description   |
|------------------------------------|------|---------|---|
| UNDRLN_LOC<br><br>(DISPLAY)        | 4:0  | 0x0     | H Row Scan Bits 4-0.- These bits define the horizontal scan row, from the top of the characterline, that should be used for underlining. The 5-bit value is equal to the actual number minus one. |
| ADDR_CNT_BY4<br><br>(DISPLAY)      | 5    | 0x0     | Count-by-4:<br>0=Char. Clock<br>1=CountBy4  |
| DOUBLE_WORD<br><br>(HDP) (DISPLAY) | 6    | 0x0     | Double-Word Mode:<br>0=Disable<br>1=DoubleWordMdEna   |

Underline Location Register

**CRT15 - RW - 8 bits - VGACRTIND:0x15**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**CRT15 - RW - 8 bits - VGACRTIND:0x15**

| Field Name    | Bits | Default | Description   |
|---------------|------|---------|---|
| V_BLANK_START | 7:0  | 0x0     | These are the eight low-order bits of the 10-bit vertical blanking start register. Bit 9 is CRT09[5]; bit 8 is CRT07[3]- The 10 bits specify the starting location of the vertical blanking pulse, in units of horizontal scan lines. The value is equal to the actual number of displayed lines minus one. |

Start Vertical Blanking Register

**CRT16 - RW - 8 bits - VGACRTIND:0x16**

| Field Name  | Bits | Default | Description   |
|-------------|------|---------|---|
| V_BLANK_END | 7:0  | 0x0     | These bits define the point at which to trigger the end of the vertical blanking pulse. The location is specified in units of horizontal scan lines.- The value to be stored in this register is the seven low-order bits of the sum of 'pulse width count' plus the content of Start Vertical Blanking register (CRT15) minus one. |

End Vertical Blanking Register

**CRT17 - RW - 8 bits - VGACRTIND:0x17**

| Field Name                   | Bits | Default | Description   |
|------------------------------|------|---------|---|
| RA0_AS_A13B<br>(DISPLAY)     | 0    | 0x0     | Compatibility Mode:   |
| RA1_AS_A14B<br>(DISPLAY)     | 1    | 0x0     | Select Row Scan Counter:  |
| VCOUNT_BY2<br>(DISPLAY)      | 2    | 0x0     | Vertical_by_2 NOTE: When bit 2 is logical one, other vertical register values should be adjusted as well (CRT06, CRT10, CRT12, CRT15, and CRT18). |
| ADDR_CNT_BY2<br>(DISPLAY)    | 3    | 0x0     | Count_by_2: ENGINEERING NOTE: Bit can be written and read, but has no effect.   |
| WRAP_A15TOA0<br>(DISPLAY)    | 5    | 0x0     | Address Wrap: ENGINEERING NOTE: Bit can be written and read, but has no effect.   |
| BYTE_MODE<br>(HDP) (DISPLAY) | 6    | 0x0     | Byte/Word Mode:<br>0=WordMode<br>1=ByteMode   |
| CRTC_SYNC_EN<br>(DISPLAY)    | 7    | 0x0     | H/V Retrace Enable:<br>0=Disable HVSynC<br>1=EnaHVSynC  |

CRT Mode Register

**CRT18 - RW - 8 bits - VGACRTIND:0x18**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**CRT18 - RW - 8 bits - VGACRTIND:0x18**

| Field Name   | Bits | Default | Description  |
|--|------|---------|--|
| LINE_CMP<br><br><i>(mirror bits 0:7 of<br/>CRTC_VLINE_CRNT_VLINE:CRTC_VLINE)</i> | 7:0  | 0x0     | - These bits are the eight low-order of the 10-bit line compare register. Bit 8 is CRT07[4], bit 9 is CRT09[6]. The value of this register is used to disable scrolling on a portion of the display screen, as when split screen is active. When the vertical counter reaches this value, the memory address and row scan counters are cleared.- The screen area above the line specified by the register is commonly called screen A. The screen below is screen B. Screen B cannot be scrolled, but it can panned only together with screen A, controlled by the PEL panning compatibility bit ATTR10[5]. (For a description of this control bit see ATTR10[5].) |

Line Compare Register

**CRT00\_S - RW - 8 bits - VGACRTIND:0x40**

| Field Name   | Bits | Default | Description |
|--|------|---------|-------------|
| H_TOTAL_S<br><br><i>(mirror bits 0:7 of<br/>FP_CRTC_H_TOTAL_DISP:FP_CRTC_H_TO<br/>TAL)</i> | 7:0  | 0x0     |             |

No description available for this register.

**CRT01\_S - RW - 8 bits - VGACRTIND:0x41**

| Field Name   | Bits | Default | Description |
|--|------|---------|-------------|
| H_DISP_END_S<br><br><i>(mirror bits 0:7 of<br/>FP_CRTC_H_TOTAL_DISP:FP_CRTC_H_DIS<br/>P)</i> | 7:0  | 0x0     |             |

No description available for this register.

**CRT02\_S - RW - 8 bits - VGACRTIND:0x42**

| Field Name      | Bits | Default | Description |
|-----------------|------|---------|-------------|
| H_BLANK_START_S | 7:0  | 0x0     |             |

No description available for this register.

**CRT03\_S - RW - 8 bits - VGACRTIND:0x43**

| Field Name  | Bits | Default | Description                              |
|---|------|---------|--|
| H_BLANK_END_S   | 4:0  | 0x0     |  |
| H_DE_SKEW_S   | 6:5  | 0x0     | 0=0Skew<br>1=1Skew<br>2=2Skew<br>3=3Skew |
| CR10CR11_R_DIS_B_M<br><br><i>(mirror of CRT03:CR10CR11_R_DIS_B)</i> | 7    | 0x0     | 0=WrtOnlyToCRT10-11<br>1=WrtRdToCRT10-11 |

No description available for this register.

**CRT04\_S - RW - 8 bits - VGACRTIND:0x44**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**CRT04\_S - RW - 8 bits - VGACRTIND:0x44**

| Field Name   | Bits | Default | Description |
|--|------|---------|-------------|
| H_SYNC_START_S<br><i>(mirror bits 0:7 of<br/>FP_H_SYNC_STRT_WID:FP_H_SYNC_STRT_CHAR)</i> | 7:0  | 0x0     |             |

No description available for this register.

**CRT05\_S - RW - 8 bits - VGACRTIND:0x45**

| Field Name   | Bits | Default | Description |
|--|------|---------|-------------|
| H_SYNC_END_S<br><i>(mirror bits 0:4 of<br/>FP_H_SYNC_STRT_WID:FP_H_SYNC_WID)</i> | 4:0  | 0x0     |             |
| H_SYNC_SKEW_S  | 6:5  | 0x0     |             |
| H_BLANK_END_B5_S   | 7    | 0x0     |             |

No description available for this register.

**CRT06\_S - RW - 8 bits - VGACRTIND:0x46**

| Field Name   | Bits | Default | Description |
|--|------|---------|-------------|
| V_TOTAL_S<br><i>(mirror bits 0:7 of<br/>FP_CRTC_V_TOTAL_DISP:FP_CRTC_V_TO TAL)</i> | 7:0  | 0x0     |             |

No description available for this register.

**CRT07\_S - RW - 8 bits - VGACRTIND:0x47**

| Field Name  | Bits | Default | Description |
|---|------|---------|-------------|
| V_TOTAL_B8_S<br><i>(mirror bits 8:8 of<br/>FP_CRTC_V_TOTAL_DISP:FP_CRTC_V_TO TAL)</i>   | 0    | 0x0     |             |
| V_DISP_END_B8_S<br><i>(mirror bits 8:8 of<br/>FP_CRTC_V_TOTAL_DISP:FP_CRTC_V_DIS P)</i> | 1    | 0x0     |             |
| V_SYNC_START_B8_S<br><i>(mirror bits 8:8 of<br/>FP_V_SYNC_STRT_WID:FP_V_SYNC_STRT )</i> | 2    | 0x0     |             |
| V_BLANK_START_B8_S  | 3    | 0x0     |             |
| LINE_CMP_B8_M<br><i>(mirror bits 8:8 of<br/>CRTC_VLINE_CRNT_VLINE:CRTC_VLINE)</i>       | 4    | 0x0     |             |
| V_TOTAL_B9_S<br><i>(mirror bits 9:9 of<br/>FP_CRTC_V_TOTAL_DISP:FP_CRTC_V_TO TAL)</i>   | 5    | 0x0     |             |
| V_DISP_END_B9_S<br><i>(mirror bits 9:9 of<br/>FP_CRTC_V_TOTAL_DISP:FP_CRTC_V_DIS P)</i> | 6    | 0x0     |             |

**CRT07\_S - RW - 8 bits - VGACRTIND:0x47**

| Field Name  | Bits | Default | Description |
|---|------|---------|-------------|
| V_SYNC_START_B9_S   | 7    | 0x0     |             |
| <i>(mirror bits 9:9 of FP_V_SYNC_STRT_WID:FP_V_SYNC_STRT)</i> |      |         |             |

No description available for this register.

**CRT08\_S - RW - 8 bits - VGACRTIND:0x48**

| Field Name                              | Bits | Default | Description |
|---|------|---------|-------------|
| ROW_SCAN_START_M                        | 4:0  | 0x0     |             |
| <i>(mirror of CRT08:ROW_SCAN_START)</i> |      |         |             |
| BYTE_PAN_M                              | 6:5  | 0x0     |             |
| <i>(mirror of CRT08:BYTE_PAN)</i>       |      |         |             |

No description available for this register.

**CRT09\_S - RW - 8 bits - VGACRTIND:0x49**

| Field Name                                      | Bits | Default | Description                    |
|---|------|---------|--------------------------------|
| MAX_ROW_SCAN_S                                  | 4:0  | 0x0     |                                |
| V_BLANK_START_B9_S                              | 5    | 0x0     |                                |
| LINE_CMP_B9_M                                   | 6    | 0x0     |                                |
| <i>(mirror bits 9:9 of CRT09:LINE_CMP_B9_M)</i> |      |         |                                |
| DOUBLE_CHAR_HEIGHT_M                            | 7    | 0x0     | 0=200LineScan<br>1=400LineScan |
| <i>(mirror of CRT09:DOUBLE_CHAR_HEIGHT)</i>     |      |         |                                |

No description available for this register.

**CRT0A\_S - RW - 8 bits - VGACRTIND:0x4A**

| Field Name                              | Bits | Default | Description   |
|---|------|---------|---------------|
| CURSOR_START_S                          | 4:0  | 0x0     |               |
| CURSOR_DISABLE_M                        | 5    | 0x0     | 0=on<br>1=off |
| <i>(mirror of CRT0A:CURSOR_DISABLE)</i> |      |         |               |

No description available for this register.

**CRT0B\_S - RW - 8 bits - VGACRTIND:0x4B**

| Field Name                           | Bits | Default | Description |
|--------------------------------------|------|---------|-------------|
| CURSOR_END_S                         | 4:0  | 0x0     |             |
| CURSOR_SKEW_M                        | 6:5  | 0x0     |             |
| <i>(mirror of CRT0B:CURSOR_SKEW)</i> |      |         |             |

No description available for this register.

**CRT0C\_S - RW - 8 bits - VGACRTIND:0x4C**

| Field Name                                       | Bits | Default | Description |
|--|------|---------|-------------|
| DISP_START_M                                     | 7:0  | 0x0     |             |
| <i>(mirror bits 11:18 of CRT0C:DISP_START_M)</i> |      |         |             |

No description available for this register.

**CRT0D\_S - RW - 8 bits - VGACRTIND:0x4D**



| Field Name   | Bits | Default | Description |
|--------------|------|---------|-------------|
| DISP_START_M | 7:0  | 0x0     |             |

(mirror bits 3:10 of  
CRTC\_OFFSET:CRTC\_OFFSET)

No description available for this register.

#### CRT0E\_S - RW - 8 bits - VGACRTIND:0x4E

| Field Name      | Bits | Default | Description |
|-----------------|------|---------|-------------|
| CURSOR_LOC_HI_M | 7:0  | 0x0     |             |

(mirror of CRT0E:CURSOR\_LOC\_HI)

No description available for this register.

#### CRT0F\_S - RW - 8 bits - VGACRTIND:0x4F

| Field Name      | Bits | Default | Description |
|-----------------|------|---------|-------------|
| CURSOR_LOC_LO_M | 7:0  | 0x0     |             |

(mirror of CRT0F:CURSOR\_LOC\_LO)

No description available for this register.

#### CRT10\_S - RW - 8 bits - VGACRTIND:0x50

| Field Name     | Bits | Default | Description |
|----------------|------|---------|-------------|
| V_SYNC_START_S | 7:0  | 0x0     |             |

(mirror bits 0:7 of  
FP\_V\_SYNC\_STRT\_WID:FP\_V\_SYNC\_STRT  
)

No description available for this register.

#### CRT11\_S - RW - 8 bits - VGACRTIND:0x51

| Field Name   | Bits | Default | Description |
|--------------|------|---------|-------------|
| V_SYNC_END_S | 3:0  | 0x0     |             |

(mirror bits 0:3 of  
FP\_V\_SYNC\_STRT\_WID:FP\_V\_SYNC\_WID)

|                    |   |     |  |
|--------------------|---|-----|--|
| V_INTR_CLR_M       | 4 | 0x0 | 0=VRetraceIntCleared<br>1=Not Cleared                    |
| V_INTR_EN_M        | 5 | 0x0 | 0=VRetraceIntEna<br>1=Disable                            |
| SEL5_REFRESH_CYC_M | 6 | 0x0 | 0=3 DRAM Refresh/Horz Line<br>1=5 DRAM Refresh/Horz Line |
| C0T7_WR_ONLY_M     | 7 | 0x0 | 0=EnaWrtToCRT00-07<br>1=C0T7B4WrtOnly                    |

(mirror of CRT11:C0T7\_WR\_ONLY)

No description available for this register.

#### CRT12\_S - RW - 8 bits - VGACRTIND:0x52

| Field Name   | Bits | Default | Description |
|--------------|------|---------|-------------|
| V_DISP_END_S | 7:0  | 0x0     |             |

(mirror bits 0:7 of  
FP\_CRTC\_V\_TOTAL\_DISP:FP\_CRTC\_V\_DIS  
P)

No description available for this register.

**CRT13\_S - RW - 8 bits - VGACRTIND:0x53**

| Field Name  | Bits | Default | Description |
|---|------|---------|-------------|
| DISP_PITCH_M<br><br><i>(mirror bits 0:7 of CRTC_PITCH:CRTC_PITCH)</i> | 7:0  | 0x0     |             |

No description available for this register.

**CRT14\_S - RW - 8 bits - VGACRTIND:0x54**

| Field Name   | Bits | Default | Description              |
|--|------|---------|--------------------------|
| UNDRLN_LOC_S<br><br>(DISPLAY)  | 4:0  | 0x0     | Shadow copy UNDRLN_N_LOC |
| ADDR_CNT_BY4_M<br><br><i>(mirror of CRT14:ADDR_CNT_BY4)</i><br><br>(DISPLAY)     | 5    | 0x0     | Mirror of ADDR_CNT_BY4   |
| DOUBLE_WORD_M<br><br><i>(mirror of CRT14:DOUBLE_WORD)</i><br><br>(HDP) (DISPLAY) | 6    | 0x0     | Mirror of DOUBLE_WORD    |

Shadow of Underline Location Register

**CRT15\_S - RW - 8 bits - VGACRTIND:0x55**

| Field Name      | Bits | Default | Description |
|-----------------|------|---------|-------------|
| V_BLANK_START_S | 7:0  | 0x0     |             |

No description available for this register.

**CRT16\_S - RW - 8 bits - VGACRTIND:0x56**

| Field Name    | Bits | Default | Description |
|---------------|------|---------|-------------|
| V_BLANK_END_S | 7:0  | 0x0     |             |

No description available for this register.

**CRT17\_S - RW - 8 bits - VGACRTIND:0x57**

| Field Name   | Bits | Default | Description               |
|--|------|---------|---------------------------|
| RA0_AS_A13B_M<br><br><i>(mirror of CRT17:RA0_AS_A13B)</i><br><br>(DISPLAY)   | 0    | 0x0     | Mirror of RA0_AS_A13B     |
| RA1_AS_A14B_M<br><br><i>(mirror of CRT17:RA1_AS_A14B)</i><br><br>(DISPLAY)   | 1    | 0x0     | Mirror of RA1_AS_A14B     |
| VCOUNT_BY2_S<br><br>(DISPLAY)  | 2    | 0x0     | Shadow copy of VCOUNT_BY2 |
| ADDR_CNT_BY2_M<br><br><i>(mirror of CRT17:ADDR_CNT_BY2)</i><br><br>(DISPLAY) | 3    | 0x0     | Mirror of ADDR_CNT_BY2    |



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**CRT17\_S - RW - 8 bits - VGACRTIND:0x57**

| Field Name   | Bits | Default | Description            |
|--|------|---------|------------------------|
| WRAP_A15TOA0_M<br><i>(mirror of CRT17:WRAP_A15TOA0)</i><br>(DISPLAY) | 5    | 0x0     | Mirror of WRAP_A15TOA0 |
| BYTE_MODE_M<br><i>(mirror of CRT17:BYTE_MODE)</i><br>(HDP) (DISPLAY) | 6    | 0x0     | Mirror of BYTE_MODE    |
| CRTC_SYNC_EN_M<br><i>(mirror of CRT17:CRTC_SYNC_EN)</i><br>(DISPLAY) | 7    | 0x0     | Mirror of CRTC_SYNC_EN |

Shadow of CRT Mode Register

**CRT18\_S - RW - 8 bits - VGACRTIND:0x58**

| Field Name   | Bits | Default | Description |
|--|------|---------|-------------|
| LINE_CMP_M<br><i>(mirror bits 0:7 of CRT17:CRTC_VLINE_CRNT_VLINE:CRTC_VLINE)</i> | 7:0  | 0x0     |             |

No description available for this register.

**17. vgaGrph Detailed Register Reference**

## VGA Graphics Registers

**GRPH8\_IDX - RW - 8 bits - VGA\_IO:0x3CE**

| Field Name   | Bits | Default | Description   |
|--|------|---------|---|
| GRPH_IDX<br>(HDP) (DISPLAY)<br>GRPH Index Register | 3:0  | 0x0     | This index is used to address one of the internal registers of the graphics controller (GRAC) at I/O port 0x3CRF. |

**GRPH8\_DATA - RW - 8 bits - VGA\_IO:0x3CF**

| Field Name   | Bits | Default | Description               |
|--|------|---------|---------------------------|
| GRPH_DATA<br>(HDP) (DISPLAY)<br>GRPH Data Register | 7:0  | 0x0     | GRPH data indirect access |

**GRA05 - RW - 8 bits - VGAGRPHIND:0x5**

| Field Name                   | Bits | Default | Description  |
|------------------------------|------|---------|--|
| GRPH_WRITE_MODE<br>(HDP)     | 1:0  | 0x0     | Write Mode:<br>0=Write mode 0<br>1=Write mode 1<br>2=Write mode 2<br>3=Write mode 3  |
| GRPH_READ1<br>(HDP)          | 3    | 0x0     | Read Mode:<br>0=Read mode 0, byte oriented<br>1=Read mode 1, pixel oriented  |
| CGA_ODDEVEN<br>(HDP)         | 4    | 0x0     | Odd/Even Addressing Enable. Used to enable CGA emulation, this bit enables off/even addressing mode when it is logical one. Normally, this bit and memory mode bit SEQ04[2] are set to agree with each other in enabling odd/even mode emulation.<br>0=Disable Odd/Even Addressing<br>1=Enable Odd/Even Addressing |
| GRPH_OES<br>(HDP) (DISPLAY)  | 5    | 0x0     | Shift Register Mode: This bit controls how data from memory is loaded into the shift registers M0D0:M0D7, M1D0:M1D7; M2D0:M2D7, and M3D0:M3D7 are representations of this data.<br>0=Linear shift mode<br>1=Tiled shift mode   |
| GRPH_PACK<br>(HDP) (DISPLAY) | 6    | 0x0     | 256 Colour Mode. This bit also controls how data from memory is loaded into the shift registers.<br>0=Use shift register mode as per GRPH_OES<br>1=256 color mode, read as packed pixels, ignore GRPH_OES  |

Graphics Mode Register

**18. vgaAttr Detailed Register Reference**

## VGA Attribute Registers

| ATTRX - RW - 8 bits - VGA_IO:0x3C0 |      |         |  |
|------------------------------------|------|---------|--|
| Field Name                         | Bits | Default | Description  |
| ATTR_IDX                           | 4:0  | 0x0     | ATTR Index. This index points to one of the internal registers of the attribute controller (ATTR) at addresses 0x3C1/0x3C0, for the next ATTR read/write operation. Since both the index and data registers are at the same I/O, a pointer to the registers is necessary. This pointer can be initialized to point to the index register by a read of GENS1. |
| ATTR_PAL_RW_ENB                    | 5    | 0x0     | Palette Address Source. After loading the colour palette, this bit should be set to logical 1.<br>0=Processor to load<br>1=Memory data to access   |

Attribute Index Register

| ATTRDW - W - 8 bits - VGA_IO:0x3C0 |      |         |                      |
|------------------------------------|------|---------|----------------------|
| Field Name                         | Bits | Default | Description          |
| ATTR_DATA                          | 7:0  | 0x0     | Attribute Data Write |

Attribute Data Write Register

| ATTRDR - R - 8 bits - VGA_IO:0x3C1 |      |         |                     |
|------------------------------------|------|---------|---------------------|
| Field Name                         | Bits | Default | Description         |
| ATTR_DATA                          | 7:0  | 0x0     | Attribute Data Read |

*(mirror of ATTRDW:ATTR\_DATA)*

Attribute Data Read Register

| ATTR00 - RW - 8 bits - VGAATTRIND:0x0 |      |         |  |
|---------------------------------------|------|---------|--|
| Field Name                            | Bits | Default | Description  |
| ATTR_PAL                              | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register 0

| ATTR01 - RW - 8 bits - VGAATTRIND:0x1 |      |         |  |
|---------------------------------------|------|---------|--|
| Field Name                            | Bits | Default | Description  |
| ATTR_PAL                              | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register 1

| ATTR02 - RW - 8 bits - VGAATTRIND:0x2 |      |         |             |
|---------------------------------------|------|---------|-------------|
| Field Name                            | Bits | Default | Description |

**ATTR02 - RW - 8 bits - VGAATTRIND:0x2**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_PAL   | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register 2

**ATTR03 - RW - 8 bits - VGAATTRIND:0x3**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_PAL   | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register 3

**ATTR04 - RW - 8 bits - VGAATTRIND:0x4**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_PAL   | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register 4

**ATTR05 - RW - 8 bits - VGAATTRIND:0x5**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_PAL   | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register 5

**ATTR06 - RW - 8 bits - VGAATTRIND:0x6**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_PAL   | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register 6

**ATTR07 - RW - 8 bits - VGAATTRIND:0x7**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_PAL   | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register 7

**ATTR08 - RW - 8 bits - VGAATTRIND:0x8**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**ATTR08 - RW - 8 bits - VGAATTRIND:0x8**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_PAL   | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register 8

**ATTR09 - RW - 8 bits - VGAATTRIND:0x9**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_PAL   | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register 9

**ATTR0A - RW - 8 bits - VGAATTRIND:0xA**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_PAL   | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register Ah (10)

**ATTR0B - RW - 8 bits - VGAATTRIND:0xB**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_PAL   | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register Bh (11)

**ATTR0C - RW - 8 bits - VGAATTRIND:0xC**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_PAL   | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register Ch (12)

**ATTR0D - RW - 8 bits - VGAATTRIND:0xD**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_PAL   | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register Dh (13)

**ATTR0E - RW - 8 bits - VGAATTRIND:0xE**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



**ATTR0E - RW - 8 bits - VGAATTRIND:0xE**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_PAL   | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register Eh (14)

**ATTR0F - RW - 8 bits - VGAATTRIND:0xF**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_PAL   | 5:0  | 0x0     | Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1. |

Palette Register Fh (15)

**ATTR10 - RW - 8 bits - VGAATTRIND:0x10**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| ATTR_GRP_MODE   | 0    | 0x0     | Graphics/Alphanumeric Mode.<br>0=Alphanumeric Mode<br>1=Graphic Mode  |
| ATTR_MONO_EN    | 1    | 0x0     | Monochrome/Colour Attributes Select:<br>0=Color Disp<br>1=MonoChrome Disp   |
| ATTR_LGRPH_EN   | 2    | 0x0     | Line Graphics Enable. Must be 0 for character fonts that do not use line graphics character codes for graphics. Zero will force the 9th dot to the background colour. One will allow the 8th bit of the line graphics characters to be stretched to the 9th dot.<br>0=Disable line graphics 8th dot stretch<br>1=Enable line graphics 8th dot stretch |
| ATTR_BLINK_EN   | 3    | 0x0     | Blink Enable/Background Intensity:<br>Selects whether bit 7 of the attribute controls intensity or blinking.<br><br>0=Intensity control<br>1=Blink control  |
| ATTR_PANTOPONLY | 5    | 0x0     | PEL Panning Compatibility:<br>0=Panning both<br>1=Panning only the top half screen  |
| ATTR_PCLKBY2    | 6    | 0x0     | PEL Clock Select:<br>0=Shift register clocked every dot clock<br>1=For mode 13 (256 colour), 8 bits packed to form a pixel  |
| ATTR_CSEL_EN    | 7    | 0x0     | Alternate Colour Source:<br>0=Select ATTR00-0F bit 5:4 as P5 and P4<br>1=Select ATTR14 bit 1:0 as P5 and P4   |

Mode Control Register

**ATTR11 - RW - 8 bits - VGAATTRIND:0x11**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**ATTR11 - RW - 8 bits - VGAATTRIND:0x11**

| Field Name | Bits | Default | Description     |
|------------|------|---------|-----------------|
| ATTR_OVSC  | 7:0  | 0x0     | Overscan Colour |

Overscan Colour Register

**ATTR12 - RW - 8 bits - VGAATTRIND:0x12**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| ATTR_MAP_EN | 3:0  | 0x0     | Enable Colour Map bits.<br>0 = Disables data from respective map from being used for video output.<br>1 = Enables data from respective map for use in video output.  |
| ATTR_VSMUX  | 5:4  | 0x0     | Video Status Mux bits 1:0. These are control bits for the multiplexer on colour bits P0-P7. The bit selection is also indicated at GENS1[5:4]:<br>00 = P2, P0<br>01 = P5, P4<br>10 = P3, P1<br>11 = P7, P6 |

Colour Map Enable Register

**ATTR13 - RW - 8 bits - VGAATTRIND:0x13**

| Field Name | Bits      | Default | Description   |       |           |    |           |       |         |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------|-----------|---------|---|-------|-----------|----|-----------|-------|---------|--|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ATTR_PPAN  | 3:0       | 0x0     | Shift Count Bits 3:0. The shift count value (0-8) indicates how many pixle positions to shift left.<br><br>Shift in respective modes<br><table border="1"> <thead> <tr> <th>Count</th> <th>0+,1+,2+,</th> <th>13</th> <th>All other</th> </tr> </thead> <tbody> <tr> <td>Value</td> <td>3+,7,7+</td> <td></td> <td></td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>2</td> <td>-</td> <td>1</td> </tr> <tr> <td>2</td> <td>3</td> <td>1</td> <td>2</td> </tr> <tr> <td>3</td> <td>4</td> <td>-</td> <td>3</td> </tr> <tr> <td>4</td> <td>5</td> <td>2</td> <td>4</td> </tr> <tr> <td>5</td> <td>6</td> <td>-</td> <td>5</td> </tr> <tr> <td>6</td> <td>7</td> <td>3</td> <td>6</td> </tr> <tr> <td>7</td> <td>8</td> <td>-</td> <td>7</td> </tr> <tr> <td>8</td> <td>0</td> <td>-</td> <td>-</td> </tr> </tbody> </table> | Count | 0+,1+,2+, | 13 | All other | Value | 3+,7,7+ |  |  | 0 | 1 | 0 | 0 | 1 | 2 | - | 1 | 2 | 3 | 1 | 2 | 3 | 4 | - | 3 | 4 | 5 | 2 | 4 | 5 | 6 | - | 5 | 6 | 7 | 3 | 6 | 7 | 8 | - | 7 | 8 | 0 | - | - |
| Count      | 0+,1+,2+, | 13      | All other   |       |           |    |           |       |         |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Value      | 3+,7,7+   |         |   |       |           |    |           |       |         |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 1         | 0       | 0   |       |           |    |           |       |         |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 1          | 2         | -       | 1   |       |           |    |           |       |         |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 2          | 3         | 1       | 2   |       |           |    |           |       |         |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 3          | 4         | -       | 3   |       |           |    |           |       |         |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 4          | 5         | 2       | 4   |       |           |    |           |       |         |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 5          | 6         | -       | 5   |       |           |    |           |       |         |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 6          | 7         | 3       | 6   |       |           |    |           |       |         |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 7          | 8         | -       | 7   |       |           |    |           |       |         |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 8          | 0         | -       | -   |       |           |    |           |       |         |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

Horizontal PEL Panning Register

**ATTR14 - RW - 8 bits - VGAATTRIND:0x14**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ATTR_CSEL1 | 1:0  | 0x0     | Colour bits P5 and P4, respectively. These are the colour output bits (instead of bits 5 and 4 of the internal palette registers ATTR00-0F) when alternate colour source, bit ATTR10[7] is logical 1.  |
| ATTR_CSEL2 | 3:2  | 0x0     | Colour bits P7 and P6, respectively. These two bits are the two high-order bits of the 8-bit colour, used for rapid colour set switching (addressing different parts of the DAC colour lookup table). The lower order bits are in registers ATTR00-0F. |

Colour Select Register



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**19. CRTC Detailed Register Reference**

## CRT Controller Attribute Registers

| <b>CRTC_H_TOTAL_DISP - RW - 32 bits - [MMReg:0x200]</b> |             |                |   |
|---|-------------|----------------|---|
| <b>Field Name</b>                                       | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| CRTC_H_TOTAL  | 9:0         | 0x0            | Horizontal total (pixels * 8)-1. Sum of display width, overscan right, front porch, sync width, back porch and overscan left.<br>This field is programmed with the -1 from the desired size.<br>i.e. for 640 pixels set to 800/8 - 1 = 99 |
| CRTC_H_DISP   | 24:16       | 0x0            | Horizontal display end (pixels * 8)-1. Determines number of visible pixels, not including overscan.<br>This field is programmed with the -1 from the desired size.<br>i.e. for 640 pixels set to 640/8 - 1 = 79                           |

Horizontal Total and Displayed Control

| <b>CRTC_H_SYNC_STRT_WID - RW - 32 bits - [MMReg:0x204]</b> |             |                |  |
|--|-------------|----------------|--|
| <b>Field Name</b>  | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| CRTC_H_SYNC_STRT_PIX                                       | 2:0         | 0x0            | CRT Horizontal sync start delay in pixels. Allows pixel accurate horizontal positioning by delaying sync position within character position set below.   |
| CRTC_H_SYNC_STRT_CHAR                                      | 12:3        | 0x0            | Horizontal sync start (pixels * 8). Sum of display width, overscan right and front porch.<br>This field is programmed with the exact desired character on which to start HSYNC, not -1. i.e. 656/8 = 82                              |
| CRTC_H_SYNC_WID  | 21:16       | 0x0            | Horizontal sync width (pixels * 8)   |
| CRTC_H_SYNC_POL  | 23          | 0x0            | CRT Horizontal sync polarity<br>0 = Active high<br>1 = Active Low<br>0=Active high<br>1=Active low   |
| CRTC_H_SYNC_SKEW_TUNE                                      | 26:24       | 0x0            | Per pixel HSYNC skew tuning value used when manual tuning selected. Value is per display pixel. For VGA display adjustment range varies with VGA mode. For extended display the range is -1 (0x0) to +6 (0x7) pixels.                |
| CRTC_H_SYNC_SKEW_TUNE_MODE                                 | 28          | 0x0            | Used mostly in VGA mode to have HW automatically adjust HSYNC position pixel accurately based on current VGA mode.<br>0=Auto tune the DAC HSYNC pixel skew.<br>1=Manually tune the DAC HSYNC pixel skew using CRTC_H_SYNC_SKEW_TUNE. |

Horizontal Sync Control.

The CRTC\_H\_SYNC\_STRT\_PIX and CRTC\_H\_SYNC\_POL always apply to the CRT Horizontal Sync regardless of other control bits.(DFP\_SYNC\_SEL/CRT\_SYNC\_SEL/CRT\_SYNC\_ALT\_SEL/horz. blanking mode/horz. autocentering)

| <b>CRTC_V_TOTAL_DISP - RW - 32 bits - [MMReg:0x208]</b> |             |                |                    |
|---|-------------|----------------|--------------------|
| <b>Field Name</b>                                       | <b>Bits</b> | <b>Default</b> | <b>Description</b> |

**CRTC\_V\_TOTAL\_DISP - RW - 32 bits - [MMReg:0x208]**

| Field Name   | Bits  | Default | Description  |
|--------------|-------|---------|--|
| CRTC_V_TOTAL | 11:0  | 0x0     | Vertical total (lines-1). Sum of display height, overscan bottom, front porch, sync width, back porch and overscan top.<br>This field is set to one less than the desired number of total lines. |
| CRTC_V_DISP  | 27:16 | 0x0     | Vertical display end (lines-1). Determines number of visible lines, not including overscan.<br>This field is set to one less than the desired number of visible lines.                           |

Vertical Total Control

**CRTC\_V\_SYNC\_STRT\_WID - RW - 32 bits - [MMReg:0x20C]**

| Field Name       | Bits  | Default | Description   |
|------------------|-------|---------|---|
| CRTC_V_SYNC_STRT | 11:0  | 0x0     | Vertical sync start. Sum of display height, overscan bottom and front porch.<br>This field is set the exact line on which VSYNC should start, i.e. not -1 like for CRTC_V_TOTAL or CRTC_V_DISP. |
| CRTC_V_SYNC_WID  | 20:16 | 0x0     | Vertical sync width   |
| CRTC_V_SYNC_POL  | 23    | 0x0     | Vertical sync polarity<br>0 = Active high<br>1 = Active low<br>0=Active high<br>1=Active low  |

Vertical Sync Control

**CRTC\_VLINE\_CRNT\_VLINE - RW - 32 bits - [MMReg:0x210]**

| Field Name          | Bits  | Default | Description  |
|---------------------|-------|---------|--|
| CRTC_VLINE          | 11:0  | 0x0     | Vertical line at which vertical line interrupt is triggered. |
| CRTC_CRNT_VLINE (R) | 27:16 | 0x0     | Current vertical line.                                       |

Display Current Vertical Line

**CRTC\_CRNT\_FRAME - R - 32 bits - [MMReg:0x214]**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| CRTC_CRNT_FRAME | 20:0 | 0x0     | Readback of current value of display frame counter. Used by display time sensitive applications such as video playback. |

Current Frame

**CRTC\_GUI\_TRIG\_VLINE - RW - 32 bits - [MMReg:0x218]**

| Field Name                | Bits | Default | Description  |
|---------------------------|------|---------|--|
| CRTC_GUI_TRIG_VLINE_START | 11:0 | 0x0     | The START (upper in display, lower in memory) for the GUI_TRIG_VLINE compare. First line of display is line 0. |



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**CRTC\_GUI\_TRIG\_VLINE - RW - 32 bits - [MMReg:0x218]**

| Field Name                | Bits  | Default | Description  |
|---------------------------|-------|---------|--|
| CRTC_GUI_TRIG_VLINE_INV   | 15    | 0x0     | Controls whether VLINE region signal is active high or active low. Can be used to stall command stream parser until inside region, or not inside region.<br>0=Active when raster between START and END.<br>1=Active when raster outside START and END.   |
| CRTC_GUI_TRIG_VLINE_END   | 27:16 | 0x0     | The END (lower in display, higher in memory) for the GUI_TRIG_VLINE compare. First line of display is line 0.  |
| CRTC_GUI_TRIG_VLINE_STALL | 30    | 0x0     | If waiting on rising or falling edge of VLINE using WAIT_UNTIL register, then always set the stall to 0. If using WAIT_UNTIL VLINE=1, then always set this stall bit to 1. This bit controls the timing of the signal from the display to the command stream parser during writes to this register.<br>0=Normal operation.<br>1=Force low during write of this register. |
| CRTC_GUI_TRIG_VLINE (R)   | 31    | 0x0     | This signal is active active when the raster is between the START and END. $START \leq \text{raster} \leq END$ . The polarity is controlled as above. This signal goes to the command stream parser as a condition in the WAIT_UNTIL register.<br>0=Current line not between VLINE start and end.<br>1=Current line is between VLINE start and end, inclusive.           |

Trigger to GUI engine activated in certain vertical region of the display, when the raster is between START and END. Normally used to delay rendering operations until the raster has passed a specific point.

**CRTC\_OFFSET\_RIGHT - RW - 32 bits - [MMReg:0x220]**

| Field Name  | Bits | Default | Description  |
|---|------|---------|--|
| CRTC_OFFSET_RIGHT   | 26:0 | 0x0     | Graphics surface origin offset in memory for right eye. Alignment must be as for CRTC_OFFSET.<br>Used only when CRTC_STEREO_OFFSET_EN = 1.<br>This is added to DISP_BASE_ADDR to get the full 32 bit address of the graphics surface.<br><br>NOTE: Bits 0:2 of this field are hardwired to ZERO. |
| CRTC_GUI_TRIG_OFFSET<br><i>(mirror of<br/>CRTC_OFFSET:CRTC_GUI_TRIG_OFFSET)<br/>(R)</i> | 30   | 0x0     | Indicates if visible buffer is last written, or still the previous one.<br>See CRTC_OFFSET register.<br>0=Last CRTC_OFFSET or CRTC_OFFSET_RIGHT written is being displayed<br>1=Last CRTC_OFFSET or CRTC_OFFSET_RIGHT written not yet displayed  |
| CRTC_OFFSET_LOCK<br><i>(mirror of<br/>CRTC_OFFSET:CRTC_OFFSET_LOCK)</i>                 | 31   | 0x0     | Prevents hardware from internally updating certain fields until cleared.<br>See CRTC_OFFSET register.<br>0=Unlock these regs<br>1=Lock'em  |

Right eye visible surface origin. Only used in stereo

**CRTC\_OFFSET - RW - 32 bits - [MMReg:0x224]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**CRTC\_OFFSET - RW - 32 bits - [MMReg:0x224]**

| Field Name               | Bits | Default | Description  |
|--------------------------|------|---------|--|
| CRTC_OFFSET              | 26:0 | 0x0     | Graphics surface origin offset in memory.<br>Must be 8 byte aligned for 4bpp, 8bpp and 24bpp modes.<br>Must be 16 byte aligned for all 16bpp modes. Must be 32 byte aligned for 32bpp mode.<br>When CRTC_STEREO_OFFSET_EN = 1, this is the left eye image.<br>This is added to DISP_BASE_ADDR to get the full 32 bit address of the graphics surface.<br><br>NOTE: Bits 0:2 of this field are hardwired to ZERO. |
| CRTC_GUI_TRIG_OFFSET (R) | 30   | 0x0     | Indicates if visible buffer is last written, or still the previous one.<br>This bit is read only. Goes high when an offset has been written but the corresponding buffer does not appear on screen yet.<br>It goes low again when display starts for that address.<br>0=Last CRTC_OFFSET or CRTC_OFFSET_RIGHT written is being displayed<br>1=Last CRTC_OFFSET or CRTC_OFFSET_RIGHT written not yet displayed    |
| CRTC_OFFSET_LOCK         | 31   | 0x0     | Prevents hardware from internally updating the following fields until cleared: CRTC_OFFSET, CRTC_OFFSET_RIGHT, CRTC_TILE_LINE, CRTC_TILE_LINE_RIGHT.<br>It permits atomic update of CRTC_OFFSET and CRTC_TILE_LINE.<br>Normal operation is with the lock in zero.<br>0=Unlock these regs<br>1=Lock'em  |

Main graphics visible surface origin. Left eye image for stereo

**CRTC\_OFFSET\_CNTL - RW - 32 bits - [MMReg:0x228]**

| Field Name           | Bits | Default | Description   |
|----------------------|------|---------|---|
| CRTC_TILE_LINE       | 3:0  | 0x0     | When CRTC_TILE_EN = 1, this field holds the 4 LSB of the line of the surface where CRTC_OFFSET starts (the 'y' for line 0 of the display, or 'start line'). The display address generator needs to know this to determine the proper pitch to add at the end of each display line. This is normally 0, unless the display is in a virtual desktop mode with tiling enabled.<br>For example, if the surface offset is zero and the display starts in line 3,<br>CRTC_TILE_LINE=0x3<br>CRTC_OFFSET = 0xC0<br>Note that tiles are 8 lines high, but this register must contain ((start line) MOD 16) in order to do the checkerboarding correctly. Do not worry about what checkerboarding is, you shouldn't need to know. |
| CRTC_TILE_LINE_RIGHT | 7:4  | 0x0     | When CRTC_TILE_EN_RIGHT = 1, this field holds the 4 LSB of the line of the surface where CRTC_OFFSET_RIGHT starts. Same as for the left eye with CRTC_TILE_LINE and CRTC_OFFSET. Right fields only used when CRTC_STEREO_OFFSET_EN = 1.   |



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**CRTC\_OFFSET\_CNTL - RW - 32 bits - [MMReg:0x228]**

| Field Name                   | Bits  | Default | Description  |
|------------------------------|-------|---------|--|
| CRTC_TILE_EN_RIGHT           | 14    | 0x0     | Graphics display tiling enable for right eye image. Used only when CRTC_STEREO_OFFSET_EN = 1. Tiling is not supported and should not be enabled in double scan or interlaced display modes. i.e. CRTC_DBL_SCAN_EN=1 or CRTC_INTERLACE_EN=1<br>0=Display Surface uses linear addressing<br>1=Display surface uses tiled addressing  |
| CRTC_TILE_EN                 | 15    | 0x0     | Graphics display tiling enable. When CRTC_STEREO_OFFSET_EN = 1 controls tiling of left eye image only. Tiling is not supported and should not be enabled in double scan or interlaced display modes. i.e. CRTC_DBL_SCAN_EN=1 or CRTC_INTERLACE_EN=1<br>0=Display Surface uses linear addressing<br>1=Display surface uses tiled addressing   |
| CRTC_OFFSET_FLIP_CNTL        | 16    | 0x0     | Selects position within the frame at which new CRTC_OFFSET will be used. Should be normally zero. If set to one, a new offset will be taken at the end of the line instead of the end of the frame.<br><br>0=Use new CRTC_OFFSET on vertical blank<br>1=Use new CRTC_OFFSET on any horizontal blank.<br>Note, this can cause the display to tear.  |
| CRTC_STEREO_OFFSET_EN        | 17    | 0x0     | Enables the use of the stereo display right eye offset and pitch fields.<br>0=No stereoscopic. RIGHT registers not used<br>1=Stereoscopic display enabled. Alternate display between normal (left) and right display surfaces  |
| CRTC_STEREO_SYNC_EN          | 19:18 | 0x0     | Controls function of STEREO_SYNC output signal.<br>0=STEREO_SYNC always low<br>1=STEREO_SYNC alternates. Low=right, high=left<br>2=STEREO_SYNC always high<br>3=STEREO_SYNC alternates. Low=left, high=right   |
| CRTC_STEREO_SYNC_OUT_EN      | 20    | 0x0     | The output enable for the STEREO_SYNC output signal.<br>0=STEREO_SYNC output tri-stated<br>1=STEREO_SYNC output enabled  |
| CRTC_STEREO_SYNC (R)         | 21    | 0x0     | Readback of STEREO_SYNC signal current value.  |
| CRTC_GUI_TRIG_OFFSET_LEFT_EN | 28    | 0x1     | Controls whether or not CRTC_OFFSET affects the CRTC_GUI_TRIG_OFFSET to the WAIT_UNTIL register. If enabled, then wait condition is set on writing CRTC_OFFSET, and cleared only if display starts displaying from CRTC_OFFSET (not if display uses CRTC_OFFSET_RIGHT for next frame).<br>0=Writing CRTC_OFFSET (main/left) does not set CRTC_GUI_TRIG_OFFSET<br>1=Writing CRTC_OFFSET sets CRTC_GUI_TRIG_OFFSET |



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**CRTC\_OFFSET\_CNTL - RW - 32 bits - [MMReg:0x228]**

| Field Name  | Bits | Default | Description  |
|---|------|---------|--|
| CRTC_GUI_TRIG_OFFSET_RIGHT_EN   | 29   | 0x0     | Controls whether or not CRTC_OFFSET_RIGHT affects the CRTC_GUI_TRIG_OFFSET to the WAIT_UNTIL register. If enabled, then wait condition is set on writing CRTC_OFFSET_RIGHT, and cleared only if display starts displaying from CRTC_OFFSET_RIGHT (not if display uses CRTC_OFFSET for next frame).<br>0=Writing CRTC_OFFSET_RIGHT does not set CRTC_GUI_TRIG_OFFSET<br>1=Writing CRTC_OFFSET_RIGHT sets CRTC_GUI_TRIG_OFFSET |
| CRTC_GUI_TRIG_OFFSET<br><i>(mirror of<br/>CRTC_OFFSET:CRTC_GUI_TRIG_OFFSET)<br/>(R)</i> | 30   | 0x0     | Indicates if visible buffer is last written, or still the previous one.<br>See CRTC_OFFSET register.<br>0=Last CRTC_OFFSET or CRTC_OFFSET_RIGHT written is being displayed<br>1=Last CRTC_OFFSET or CRTC_OFFSET_RIGHT written not yet displayed  |
| CRTC_OFFSET_LOCK<br><i>(mirror of<br/>CRTC_OFFSET:CRTC_OFFSET_LOCK)</i>                 | 31   | 0x0     | Prevents hardware from internally updating certain fields until cleared.<br>See CRTC_OFFSET register.<br>0=Unlock these regs<br>1=Lock'em  |

Graphics Display Address Generator Control

**CRTC\_PITCH - RW - 32 bits - [MMReg:0x22C]**

| Field Name       | Bits  | Default | Description   |
|------------------|-------|---------|---|
| CRTC_PITCH       | 10:0  | 0x0     | Display line pitch in (pixels * 8). Note that for 24bpp the display uses pixels * 8 for the pitch, but the rendering engine uses bytes * 8 for the pitch.<br>For tiled display this is the same pitch as used for the surface in the rendering engine (24bpp not supported for tiled). In tiled the pitch must be a multiple of 256 bytes (the tile width). So for 32bpp tiled, the CRTC_PITCH must be a multiple of 64 pixels. Or 128 pixels for 16bpp, or 256 pixels for 8bpp. For stereo display mode, this is the left image pitch. |
| CRTC_PITCH_RIGHT | 26:16 | 0x0     | Programming details same as for CRTC_PITCH. This field only used in stereo display mode for right image pitch.  |

Graphics Display Address Pitch

**CRT\_CRTC\_H\_SYNC\_STRT\_WID - RW - 32 bits - [MMReg:0x258]**

| Field Name                | Bits | Default | Description   |
|---------------------------|------|---------|---|
| CRT_CRTC_H_SYNC_STRT_CHAR | 12:3 | 0x0     | Horizontal sync start position in characters(pixels * 8). Sum of display width, overscan right and front porch.<br>This field is programmed with the exact desired character on which to start HSYNC, not -1. i.e. 656/8 = 82<br>If horizontal autocentering or fixed blank is enabled(see CRTC_MORE_CNTL) this field contains the offset (from the end of the active display/start of horizontal blank) within the blank time of the start of the horizontal sync signal for the CRT (in characters) |

**CRT\_CRTC\_H\_SYNC\_STRT\_WID - RW - 32 bits - [MMReg:0x258]**

| Field Name          | Bits  | Default | Description   |
|---------------------|-------|---------|---|
| CRT_CRTC_H_SYNC_WID | 21:16 | 0x0     | Horizontal sync width in characters(pixels * 8)<br>If horz. autocentering or fixed blank is enabled, this field contains the width (in characters) of the horizontal sync signal for the CRT. |

Alternate Horizontal CRT Sync.

CRT HSync generated using this value when FP\_GEN\_CNTL.CRT\_ALT\_SYNC\_SEL = 1

**CRT\_CRTC\_V\_SYNC\_STRT\_WID - RW - 32 bits - [MMReg:0x25C]**

| Field Name           | Bits  | Default | Description   |
|----------------------|-------|---------|---|
| CRT_CRTC_V_SYNC_STRT | 11:0  | 0x0     | Vertical sync start. Sum of display height, overscan bottom and front porch.<br>If vertical autocentering or fixed blank is enabled(see CRTC_MORE_CNTL) this field contains the offset (from the bottom of the active display/start of vertical blank) within the vertical blank time of the start of the vertical sync signal for the CRT (in lines) |
| CRT_CRTC_V_SYNC_WID  | 20:16 | 0x0     | Vertical sync width (in lines).<br>If vertical autocentering or fixed blank is enabled this field contains the length (in lines) of the vertical sync signal for the CRT  |

Alternate Vertical CRT Sync.

CRT VSync generated using this value when FP\_GEN\_CNTL.CRT\_ALT\_SYNC\_SEL = 1

**CRTC\_MORE\_CNTL - RW - 32 bits - [MMReg:0x27C]**

| Field Name               | Bits | Default | Description   |
|--------------------------|------|---------|---|
| CRTC_HORZ_BLANK_MODE_SEL | 0    | 0x0     | Selects horizontal retrace mode. Either traditional (0) or fixed blank (1).<br>0=CRTC H blank timings are relative to start of active.<br>1=CRTC H blank timings are relative to end of active.   |
| CRTC_VERT_BLANK_MODE_SEL | 1    | 0x0     | Selects vertical retrace mode. Either traditional (0) or fixed blank (1).<br>0=CRTC V blank timings are relative to start of active.<br>1=CRTC V blank timings are relative to end of active.   |
| CRTC_AUTO_HORZ_CENTER_EN | 2    | 0x0     | Enables horizontal auto-centering circuit.<br>See FP_CRTC_H_TOTAL_DISP,<br>FP_CRTC_V_TOTAL_DISP,<br>CRT_CRTC_H_SYNC_STRT_WID,<br>CRT_CRTC_V_SYNC_STRT_WID,<br>FP_H_SYNC_STRT_WID, and FP_V_SYNC_STRT_WID.<br>0=H centering is manual.<br>1=H centering is automatic based on H_DISP and FP_HORZ_PANEL_SIZE. |
| CRTC_AUTO_VERT_CENTER_EN | 3    | 0x0     | Enables vertical auto-centering circuit.<br>0=V centering is manual.<br>1=V centering is automatic based on V_DISP and FP_VERT_PANEL_SIZE.  |
| CRTC_H_CUTOFF_ACTIVE_EN  | 4    | 0x0     | Enables horizontal active size forcing circuit. Uses FP_HORZ_STRETCH.FP_HORZ_PANEL_SIZE<br>0=No corrections to CRTC and/or RMX horizontal timings.<br>1=Horizontal active forced to FP_HORZ_PANEL_SIZE by stretching or cutting off CRTC timings as needed.   |



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**CRTC\_MORE\_CNTL - RW - 32 bits - [MMReg:0x27C]**

| Field Name               | Bits  | Default | Description   |
|--------------------------|-------|---------|---|
| CRTC_V_CUTOFF_ACTIVE_EN  | 5     | 0x0     | Enables vertical active size forcing circuit. Uses FP_VERT_STRETCH.FP_VERT_PANEL_SIZE<br>0=No corrections to CRTC and/or RMX vertical timings.<br>1=Vertical active forced to FP_VERT_PANEL_SIZE by stretching or cutting off CRTC timings as needed.   |
| FORCE_H_EVEN_PIXEL_COUNT | 6     | 0x0     | 0=Normal Horizontal operation of CRTC<br>1=If Horizontal Pixel Count is Odd, Expand Blank by one pixel to ensure even number of pixels  |
| RMX_H_FILT_COEFFICIENT   | 26:24 | 0x0     | 0=Use Horz RMX Ratio to determine Horizontal Alpha Filter Coefficient<br>1=Horizontal RMX Alpha Filter Coefficient is 1<br>2=Horizontal RMX Alpha Filter Coefficient is 2<br>3=Horizontal RMX Alpha Filter Coefficient is 3<br>4=Horizontal RMX Alpha Filter Coefficient is 4<br>5=Horizontal RMX Alpha Filter Coefficient is 5<br>6=Horizontal RMX Alpha Filter Coefficient is 6<br>7=Horizontal RMX Alpha Filter Coefficient is 7 |
| RMX_H_FILTER_EN          | 27    | 0x0     | 0=RMX is standard horizontal alpha-blended scaling.<br>1=RMX is enhanced horizontal alpha-blended scaling.  |
| RMX_V_FILT_COEFFICIENT   | 30:28 | 0x0     | 0=Use Vert RMX Ratio to determine Vertical Alpha Filter Coefficient<br>1=Vertical RMX Alpha Filter Coefficient is 1<br>2=Vertical RMX Alpha Filter Coefficient is 2<br>3=Vertical RMX Alpha Filter Coefficient is 3<br>4=Vertical RMX Alpha Filter Coefficient is 4<br>5=Vertical RMX Alpha Filter Coefficient is 5<br>6=Vertical RMX Alpha Filter Coefficient is 6<br>7=Vertical RMX Alpha Filter Coefficient is 7                 |
| RMX_V_FILTER_EN          | 31    | 0x0     | 0=RMX is standard vertical alpha-blended scaling.<br>1=RMX is enhanced vertical alpha-blended scaling.  |

More CRTC controls

For 'fixed blank' and 'autocentering' modes, refer to registers FP\_CRTC\_H\_TOTAL\_DISP, FP\_CRTC\_V\_TOTAL\_DISP, FP\_H\_SYNC\_STRT\_WID, FP\_V\_SYNC\_STRT\_WID, CRT\_CRTC\_H\_SYNC\_STRT\_WID, and CRT\_CRTC\_V\_SYNC\_STRT\_WID. For 'autocentering' please also refer to FP\_HORZ\_VERT\_ACTIVE. When autocentering is enabled, fixed blanking is also enabled.

**CRTC\_GEN\_CNTL - RW - 32 bits - [IOReg,MMReg:0x50]**

| Field Name                        | Bits | Default | Description  |
|-----------------------------------|------|---------|--|
| CRTC_DBL_SCAN_EN<br><br>(DISPLAY) | 0    | 0x0     | Double scan enable.<br>Double scan only affects the calculation of display addresses by adding the CRTC_PITCH every second line (also applies to the hardware cursor pitch). Enabling double scan does not change the CRTC vertical programming or VSYNC timing. The overscan top & bottom are not affected and remain the number of lines programmed (i.e. not double). The hardware cursor programming remains in terms of physical lines (not logical lines). The cursor vertical position must begin on an even line number when in double scan. The cursor itself is limited to 64 physical lines in height, which means only 32 logical lines. This is because the cursor pitch is only added at the end of odd scan lines, but the CRTC vertical logic stops the cursor after 64 physical lines.<br>0=disable<br>1=enable |



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**CRTC\_GEN\_CNTL - RW - 32 bits - [IOReg,MMReg:0x50]**

| Field Name                     | Bits | Default | Description  |
|--------------------------------|------|---------|--|
| CRTC_INTERLACE_EN<br>(DISPLAY) | 1    | 0x0     | Interlace display mode enable.<br>0=Non-Interlace<br>1=Interlace   |
| CRTC_C_SYNC_EN<br>(DISPLAY)    | 4    | 0x0     | Enables composite sync on horizontal sync output.<br>When this is set, the VSYNC pin should be disabled by setting CRTC_EXT_CNTL.CRTC_VSYNC_TRISTATE=1.<br>0=Disable<br>1=Enable   |
| CRTC_PIX_WIDTH<br>(DISPLAY)    | 11:8 | 0x0     | Display pixel width (actually depth).<br>For 4bpp mode DAC_CNTL.DAC_4BPP_PIX_ORDER selects the order of nibbles within bytes.<br>When R, G, or B components are only 4, 5 or 6 bits, DAC_CNTL.DAC_EXPAND_MODE selects how these components are expanded to 8 bits each for keying and palette lookup.<br>When alpha values are 1 or 4 bits, they are expanded to 8 bits by dynamic expansion of the high order bits to the missing lower order bits.<br>0=Disable pixel clock for primary CRTC<br>1=4bpp Indexed<br>2=8bpp Indexed<br>3=15bpp aRGB 1555<br>4=16bpp RGB 565<br>5=24bpp RGB 888<br>6=32bpp aRGB 8888<br>7=16bpp aRGB 4444<br>8=16bpp aIndex 88 |
| CRTC_ICON_EN<br>(DISPLAY)      | 15   | 0x0     | 0=Disable Hardware Icon<br>1=Enable Hardware Icon  |
| CRTC_CUR_EN<br>(DISPLAY)       | 16   | 0x0     | Hardware cursor enable.<br>This field is double buffered and locked with the CUR_LOCK register field.<br>0=Disable<br>1=Enable   |



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**CRTC\_GEN\_CNTL - RW - 32 bits - [IOReg,MMReg:0x50]**

| Field Name                          | Bits  | Default | Description  |
|-------------------------------------|-------|---------|--|
| CRTC_VSTAT_MODE<br>(DISPLAY)        | 18:17 | 0x0     | Selects the location of the display updating of CRTC_OFFSET and CUR_OFFSET and related fields during the vertical retrace. Also determines where the VGA_VSTATUS update will occur within the vertical retrace for VGA modes.<br>For non-VGA modes only the upper bit of this field is used. When 00 or 01 in non-VGA the updating of the CRTC_OFFSET and the CUR_OFFSET is delayed as long as possible within the vertical retrace until the start of the last line of the retrace. When 10 or 11 in non-VGA the CRTC_OFFSET and CUR_OFFSET are updated at the leading edge of VSYNC, which is normally relatively early in the vertical retrace. No matter how this is set, the update of status bits like WAIT_UNTIL_PFLIP will reflect the actual location of the update. Any writes to CRTC_OFFSET or CUR_OFFSET after the selected point has passed in the vertical retrace will have no affect until the display frame after the next vertical retrace.<br>For VGA modes this field affects the behaviour of page flipping in some applications/games that poll the VGA_VSTATUS flag. This field should be tuned by the BIOS for compatibility with the most games.<br>0=VGA_VSTATUS until vcount= vt total<br>1=VGA_VSTATUS until vblank end, DISP_ADDR loads when vcount=vt otal<br>2=VGA_VSTATUS until vblank end, DISP_ADDR loads when vcount=vtotal<br>3=VGA_VSTATUS until vsync start<br>DISP_ADDR loads in vsync start |
| CRTC_CUR_MODE<br>(DISPLAY)          | 22:20 | 0x0     | Hardware cursor mode.<br>For 2bpp mode, each line of cursor data is stored in memory as 64 bits of AND data followed by 64 bits of XOR data.<br>For color AND/XOR mode, each pixel is stored sequentially in memory as 32bits each in aRGB8888 format with bit 31 of each DWord being the AND bit.<br>For the color alpha modes the format is also 32bpp aRGB8888 with all 8 bits of the alpha being used.<br>All HW cursor lines must be 64 pixels wide and all lines must be stored sequentially in memory.<br>0=Mono + 1 bit AND (2bpp), 64x64<br>1=Color 24bpp + 1 bit AND, 32hx64v<br>2=Color 24bpp + 8 bit alpha, premultiplied alpha, 32hx64v<br>3=Color 24bpp + 8 bit alpha, unmultiplied alpha, 32hx64v   |
| CRTC_EXT_DISP_EN<br>(BIF) (DISPLAY) | 24    | 0x0     | Extended display mode enable. No affect if strapped<br>VGA_DISABLE=1.<br>0=VGA<br>1=Extended   |
| CRTC_EN<br>(DISPLAY)                | 25    | 0x0     | Enables CRT controller.<br>When reset, the CRTC horizontal counter is set to zero, and the vertical counter is set to the current value of CRTC_V_TOTAL_DISP.CRTC_V_DISP.<br>0=Reset<br>1=Enable   |

**CRTC\_GEN\_CNTL - RW - 32 bits - [IOReg,MMReg:0x50]**

| Field Name                          | Bits | Default | Description  |
|-------------------------------------|------|---------|--|
| CRTC_DISP_REQ_EN_B<br><br>(DISPLAY) | 26   | 0x1     | Enables display graphics requests to the memory controller.<br>Affects only graphics and VGA text requests. Does not affect HW cursor, overlay or subpic.<br>When setting this bit, CRTC_EXT_CNTL.CRTC_DISPLAY_DIS is also normally set to blank the screen.<br>Active low.<br>0=Enable<br>1=Disable |

CRTC general controls

**CRTC\_EXT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x54]**

| Field Name                               | Bits | Default | Description   |
|--|------|---------|---|
| CRTC_VGA_XOVERSCAN<br><br>(DISPLAY)      | 0    | 0x0     | Set low for VGA compatible borders. When set high extended overscan registers control border in VGA modes. See also auto-centering in CRTC_MORE_CNTL and FP_GEN_CNTL.CRTC_VGA_XOVERSCAN_COLOR.<br>0=Disable extended overscan in VGA<br>1=Enable extended overscan in VGA |
| VGA_BLINK_RATE<br><br>(DISPLAY)          | 2:1  | 0x0     | Controls number of frames per blink for VGA modes.<br>0=Default VGA blink rate (16 frames)<br>1=1/2 default VGA blink rate (32 frames)<br>2=1/3 default VGA blink rate (48 frames)<br>3=1/4 default VGA blink rate (64 frames)  |
| VGA_ATI_LINEAR<br><br>(HDP) (DISPLAY)    | 3    | 0x0     | Enable linear addressing through VGA memory aperture.<br>0=Disable<br>1=Enable  |
| VGA_128KAP_PAGING<br><br>(HDP) (DISPLAY) | 4    | 0x0     | Enable extended aperture paging in 128K VGA aperture mode.<br>0=Normal<br>1=Enable  |
| VGA_TEXT_132<br><br>(HDP) (DISPLAY)      | 5    | 0x0     | Extended text mode select (linear address 132 column text mode). Set low for VGA compatible 40 or 80 column text modes.<br>0=inActive<br>1=Active   |
| VGA_XCRT_CNT_EN<br><br>(DISPLAY)         | 6    | 0x0     | Extended CRTC display address counter enable. Active High<br>0=Disable<br>1=Enable Ext CRTC Counter   |
| CRTC_HSYNC_DIS<br><br>(DISPLAY)          | 8    | 0x0     | Disables horizontal sync output. Could be used for DPMS signaling, but DISP_PWR_MAN.DISP_PWR_MAN_DPMS is recommended instead.<br>0=Enable<br>1=Disable  |
| CRTC_VSYNC_DIS<br><br>(DISPLAY)          | 9    | 0x0     | Disables vertical sync output. Could be used for DPMS signaling, but DISP_PWR_MAN.DISP_PWR_MAN_DPMS is recommended instead.<br>Note this must remain enabled while using composite SYNC on HSYNC (CRTC_C_SYNC_EN=1).<br>0=Enable<br>1=Disable                             |

**CRTC\_EXT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x54]**

| Field Name                          | Bits  | Default | Description  |
|-------------------------------------|-------|---------|--|
| CRTC_DISPLAY_DIS<br>(DISPLAY)       | 10    | 0x0     | Disables the display, forcing the blanking signal to be active.<br>When blanking the screen with this bit, the overlay, sub-picture, graphics and cursor should also be disabled to save power. See CRTC_DISP_REQ_EN_B, CRTC_CUR_EN, OV0_OVERLAY_EN and SUBPIC_ON.<br>0=Enable<br>1=Blanked  |
| CRTC_SYNC_TRISTATE<br>(DISPLAY)     | 11    | 0x0     | Tristates HSYNC and VSYNC outputs. For individual tristate control, see the next two fields.<br>0=Normal<br>1=Tristate HSYNC and VSYNC outputs   |
| CRTC_HSYNC_TRISTATE<br>(DISPLAY)    | 12    | 0x0     | Tristates HSYNC output.<br>0=Normal HSYNC<br>1=Tristate HSYNC output   |
| CRTC_VSYNC_TRISTATE<br>(DISPLAY)    | 13    | 0x0     | Tristates VSYNC output.<br>This is recommended for use with composite sync mode when only the HSYNC output pin should be enabled.<br>0=Normal VSYNC<br>1=Tristate VSYNC output   |
| CRT_ON<br>(DISPLAY)                 | 15    | 0x0     | 0=CRT OFF<br>1=CRT ON  |
| VGA_CUR_B_TEST<br>(DISPLAY)         | 17    | 0x0     | Test cursor blinking. Only used for diagnostic testing.<br>0=Disable VGA cursor test<br>1=Test VGA cursor blinking   |
| VGA_PACK_DIS<br>(HDP)               | 18    | 0x0     | Controls host write pipe for packed VGA modes (e.g. mode 13). Should only be set high if HW problem with fast writes.<br>0=Fast VGA write in packed modes<br>1=Normal VGA write in packed modes  |
| VGA_MEM_PS_EN<br>(HDP)              | 19    | 0x0     | VGA page select enable:<br>0=Don't use MEM_VGA_WP_SEL and MEM_VGA_RP_SEL registers<br>1=Use MEM_VGA_WP_SEL and MEM_VGA_RP_SEL registers  |
| VCRTC_IDX_MASTER<br>(HDP) (DISPLAY) | 30:24 | 0x0     | VGA CRTC master index. Only bits 5:0 of the VGA CRTC index can be written (or read) in VGA I/O space at 0x3B4 or 0x3D4. Bit 6 controls whether the master or shadow set of VGA CRTC registers is seen in VGA I/O space. The shadow set is for use when supporting panel operation in VGA modes. The BIOS will leave either the master or shadow set active as needed after a mode switch call. |

More CRTC general controls

**CRTC2\_H\_TOTAL\_DISP - RW - 32 bits - [MMReg:0x300]**

| Field Name    | Bits | Default | Description  |
|---------------|------|---------|--|
| CRTC2_H_TOTAL | 9:0  | 0x0     | Horizontal total (pixels * 8)-1. Sum of display width, overscan right, front porch, sync width, back porch and overscan left.<br>This field is programmed with the -1 from the desired size. i.e. for 640 pixels set to 800/8 - 1 = 99 |



**CRTC2\_H\_TOTAL\_DISP - RW - 32 bits - [MMReg:0x300]**

| Field Name   | Bits  | Default | Description   |
|--------------|-------|---------|---|
| CRTC2_H_DISP | 24:16 | 0x0     | Horizontal display end (pixels * 8)-1. Determines number of visible pixels, not including overscan. This field is programmed with the -1 from the desired size. i.e. for 640 pixels set to 640/8 - 1 = 79 |

Secondary display Horizontal Total and Displayed Control

**CRTC2\_H\_SYNC\_STRT\_WID - RW - 32 bits - [MMReg:0x304]**

| Field Name             | Bits  | Default | Description  |
|------------------------|-------|---------|--|
| CRTC2_H_SYNC_STRT_PIX  | 2:0   | 0x0     | CRT Horizontal sync start delay in pixels. Allows pixel accurate horizontal positioning by delaying sync position within character position set below. |
| CRTC2_H_SYNC_STRT_CHAR | 12:3  | 0x0     | Horizontal sync start (pixels * 8). Sum of display width, overscan right and front porch.  |
| CRTC2_H_SYNC_WID       | 21:16 | 0x0     | Horizontal sync width (pixels * 8)   |
| CRTC2_H_SYNC_POL       | 23    | 0x0     | CRT Horizontal sync polarity<br>0 = Active high<br>1 = Active Low<br>0=Active high<br>1=Active low   |

Horizontal Sync Control.

The CRTC2\_H\_SYNC\_STRT\_PIX and CRTC2\_H\_SYNC\_POL always apply to the CRT Horizontal Sync regardless of other control bits.(DFP\_SYNC\_SEL/CRT\_SYNC\_SEL/CRT\_SYNC\_ALT\_SEL/horz. blanking mode/horz. autocentering)

**CRTC2\_V\_TOTAL\_DISP - RW - 32 bits - [MMReg:0x308]**

| Field Name    | Bits  | Default | Description   |
|---------------|-------|---------|---|
| CRTC2_V_TOTAL | 11:0  | 0x0     | Vertical total. Sum of display height, overscan bottom, front porch, sync width, back porch and overscan top. |
| CRTC2_V_DISP  | 27:16 | 0x0     | Vertical display end. Determines number of visible lines, not including overscan.                             |

Vertical Total Control

**CRTC2\_V\_SYNC\_STRT\_WID - RW - 32 bits - [MMReg:0x30C]**

| Field Name        | Bits  | Default | Description  |
|-------------------|-------|---------|--|
| CRTC2_V_SYNC_STRT | 11:0  | 0x0     | Vertical sync start. Sum of display height, overscan bottom and front porch.                 |
| CRTC2_V_SYNC_WID  | 20:16 | 0x0     | Vertical sync width  |
| CRTC2_V_SYNC_POL  | 23    | 0x0     | Vertical sync polarity<br>0 = Active high<br>1 = Active low<br>0=Active high<br>1=Active low |

Vertical Sync Control

**CRTC2\_VLINE\_CRNT\_VLINE - RW - 32 bits - [MMReg:0x310]**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| CRTC2_VLINE | 11:0 | 0x0     | Vertical line at which vertical line interrupt is triggered. |

**CRTC2\_VLINE\_CRNT\_VLINE - RW - 32 bits - [MMReg:0x310]**

| Field Name           | Bits  | Default | Description            |
|----------------------|-------|---------|------------------------|
| CRTC2_CRNT_VLINE (R) | 27:16 | 0x0     | Current vertical line. |

Display Current Vertical Line

**CRTC2\_CRNT\_FRAME - R - 32 bits - [MMReg:0x314]**

| Field Name       | Bits | Default | Description   |
|------------------|------|---------|---|
| CRTC2_CRNT_FRAME | 20:0 | 0x0     | Readback of current value of display frame counter. Used by display time sensitive applications such as video playback. |

Secondary display Current Frame

**CRTC2\_GUI\_TRIG\_VLINE - RW - 32 bits - [MMReg:0x318]**

| Field Name                 | Bits  | Default | Description  |
|----------------------------|-------|---------|--|
| CRTC2_GUI_TRIG_VLINE_START | 11:0  | 0x0     | The START (upper in display, lower in memory) for the GUI_TRIG_VLINE compare. First line of display is line 0.   |
| CRTC2_GUI_TRIG_VLINE_INV   | 15    | 0x0     | Controls whether VLINE region signal is active high or active low. Can be used to stall command stream parser until inside region, or not inside region.<br>0=Active when raster between START and END.<br>1=Active when raster outside START and END.   |
| CRTC2_GUI_TRIG_VLINE_END   | 27:16 | 0x0     | The END (lower in display, higher in memory) for the GUI_TRIG_VLINE compare. First line of display is line 0.  |
| CRTC2_GUI_TRIG_VLINE_STALL | 30    | 0x0     | If waiting on rising or falling edge of VLINE using WAIT_UNTIL register, then always set the stall to 0. If using WAIT_UNTIL VLINE=1, then always set this stall bit to 1. This bit controls the timing of the signal from the display to the command stream parser during writes to this register.<br>0=Normal operation.<br>1=Force low during write of this register. |
| CRTC2_GUI_TRIG_VLINE (R)   | 31    | 0x0     | This signal is active active when the raster is between the START and END. START <= raster <= END. The polarity is controlled as above. This signal goes to the command stream parser as a condition in the WAIT_UNTIL register.<br>0=Current line not between VLINE start and end.<br>1=Current line is between VLINE start and end, inclusive.                         |

Trigger to GUI engine activated in certain vertical region of the display, when the raster is between START and END. Normally used to delay rendering operations until the raster has passed a specific point.

**CRTC2\_OFFSET - RW - 32 bits - [MMReg:0x324]**

| Field Name   | Bits | Default | Description   |
|--------------|------|---------|---|
| CRTC2_OFFSET | 26:0 | 0x0     | Graphics surface origin offset in memory.<br>Must be 8 byte aligned for 4bpp, 8bpp and 24bpp modes.<br>Must be 16 byte aligned for all 16bpp modes. Must be 32 byte aligned for 32bpp mode.<br>This is added to DISP_BASE_ADDR to get the full 32 bit address of the graphics surface.<br><br>NOTE: Bits 0:2 of this field are hardwired to ZERO. |

**CRTC2\_OFFSET - RW - 32 bits - [MMReg:0x324]**

| Field Name                | Bits | Default | Description   |
|---------------------------|------|---------|---|
| CRTC2_GUI_TRIG_OFFSET (R) | 30   | 0x0     | Indicates if visible buffer is last written, or still the previous one.<br>This bit is read only. Goes high when an offset has been written but the corresponding buffer does not appear on screen yet.<br>It goes low again when display starts for that address.<br>0=Last CRTC2_OFFSET or CRTC2_OFFSET_RIGHT written is being displayed<br>1=Last CRTC2_OFFSET or CRTC2_OFFSET_RIGHT written not yet displayed |
| CRTC2_OFFSET_LOCK         | 31   | 0x0     | Prevents hardware from internally updating the following fields until cleared: CRTC2_OFFSET, CRTC2_TILE_LINE.<br>It permits atomic update of CRTC2_OFFSET and CRTC2_TILE_LINE.<br>Normal operation is with the lock in zero.<br>0=Unlock these regs<br>1=Lock'em  |

Secondary graphics visible surface origin.

**CRTC2\_OFFSET\_CNTL - RW - 32 bits - [MMReg:0x328]**

| Field Name                    | Bits | Default | Description   |
|-------------------------------|------|---------|---|
| CRTC2_TILE_LINE               | 3:0  | 0x0     | When CRTC2_TILE_EN = 1, this field holds the 4 LSB of the line of the surface where CRTC2_OFFSET starts (the 'y' for line 0 of the display, or 'start line'). The display address generator needs to know this to determine the proper pitch to add at the end of each display line. This is normally 0, unless the display is in a virtual desktop mode with tiling enabled.<br>For example, if the surface offset is zero and the display starts in line 3,<br>CRTC2_TILE_LINE=0x3<br>CRTC2_OFFSET = 0xC0<br>Note that tiles are 8 lines high, but this register must contain ((start line) MOD 16) in order to do the checkerboarding correctly. Do not worry about what checkerboarding is, you shouldn't need to know. |
| CRTC2_TILE_EN                 | 15   | 0x0     | Graphics display tiling enable.<br>0=Display Surface uses linear addressing<br>1=Display surface uses tiled addressing  |
| CRTC2_OFFSET_FLIP_CNTL        | 16   | 0x0     | Selects position within the frame at which new CRTC2_OFFSET will be used.<br>Should be normally zero. If set to one, a new offset will be taken at the end of the line instead of the end of the frame.<br><br>0=Use new CRTC2_OFFSET on vertical blank<br>1=Use new CRTC2_OFFSET on any horizontal blank.<br>Note, this can cause the display to tear.   |
| CRTC2_GUI_TRIG_OFFSET_LEFT_EN | 28   | 0x1     | Controls whether or not CRTC2_OFFSET affects the CRTC2_GUI_TRIG_OFFSET to the WAIT_UNTIL register.<br>If enabled, then wait condition is set on writing CRTC2_OFFSET, and cleared only if display starts displaying from CRTC2_OFFSET.<br>0=Writing CRTC2_OFFSET (main/left) does not set CRTC2_GUI_TRIG_OFFSET<br>1=Writing CRTC2_OFFSET sets CRTC2_GUI_TRIG_OFFSET  |

**CRTC2\_OFFSET\_CNTL - RW - 32 bits - [MMReg:0x328]**

| Field Name  | Bits | Default | Description  |
|---|------|---------|--|
| CRTC2_GUI_TRIG_OFFSET<br><i>(mirror of<br/>CRTC2_OFFSET:CRTC2_GUI_TRIG_OFFSE<br/>T) (R)</i> | 30   | 0x0     | Indicates if visible buffer is last written, or still the previous one.<br>See CRTC2_OFFSET register.<br>0=Last CRTC_OFFSET or CRTC_OFFSET_RIGHT written is being displayed<br>1=Last CRTC_OFFSET or CRTC_OFFSET_RIGHT written not yet displayed |
| CRTC2_OFFSET_LOCK<br><i>(mirror of<br/>CRTC2_OFFSET:CRTC2_OFFSET_LOCK)</i>                  | 31   | 0x0     | Prevents hardware from internally updating certain fields until cleared.<br>See CRTC2_OFFSET register.<br>0=Unlock these regs<br>1=Lock'em   |

Graphics Display Address Generator Control

**CRTC2\_PITCH - RW - 32 bits - [MMReg:0x32C]**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| CRTC2_PITCH | 10:0 | 0x0     | Display line pitch in (pixels * 8). Note that for 24bpp the display uses pixels * 8 for the pitch, but the rendering engine uses bytes * 8 for the pitch.<br>For tiled display this is the same pitch as used for the surface in the rendering engine (24bpp not supported for tiled). In tiled the pitch must be a multiple of 256 bytes (the tile width). So for 32bpp tiled, the CRTC2_PITCH must be a multiple of 64 pixels. Or 128 pixels for 16bpp, or 256 pixels for 8bpp. For stereo display mode, this is the left image pitch. |

Graphics Display Address Pitch

**CRTC2\_DISPLAY\_BASE\_ADDR - RW - 32 bits - [MMReg:0x33C]**

| Field Name              | Bits | Default | Description  |
|-------------------------|------|---------|--|
| CRTC2_DISPLAY_BASE_ADDR | 31:0 | 0x0     | Base address added to all graphics, cursor and icon requests to the internal memory controller. This should normally be set equal to MC_FB_LOCATION.MC_FB_START. It could be set to other places to allow display out of system (e.g. AGP) memory, but this is not recommended. This is a 4 Megabyte aligned base address.<br><br>NOTE: Bits 0:21 of this field are hardwired to ZERO. |

Secondary display graphics, cursor &amp; icon base address

**CRTC2\_GEN\_CNTL - RW - 32 bits - [MMReg:0x3F8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



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**CRTC2\_GEN\_CNTL - RW - 32 bits - [MMReg:0x3F8]**

| Field Name           | Bits | Default | Description  |
|----------------------|------|---------|--|
| CRTC2_DBL_SCAN_EN    | 0    | 0x0     | Double scan enable.<br>Double scan only affects the calculation of display addresses by adding the CRTC_PITCH every second line (also applies to the hardware cursor pitch). Enabling double scan does not change the CRTC vertical programming or VSYNC timing. The overscan top & bottom are not affected and remain the number of lines programmed (i.e. not double). The hardware cursor programming remains in terms of physical lines (not logical lines). The cursor vertical position must begin on an even line number when in double scan. The cursor itself is limited to 64 physical lines in height, which means only 32 logical lines. This is because the cursor pitch is only added at the end of odd scan lines, but the CRTC vertical logic stops the cursor after 64 physical lines.<br>0=disable<br>1=enable |
| CRTC2_INTERLACE_EN   | 1    | 0x0     | Interlace display mode enable.<br>0=Non-Interlace<br>1=Interlace   |
| CRTC2_SYNC_TRISTATE  | 4    | 0x0     | 0=Normal<br>1=Tristate HSYNC and VSYNC outputs   |
| CRTC2_HSYNC_TRISTATE | 5    | 0x0     | 0=Normal HSYNC<br>1=Tristate HSYNC output  |
| CRTC2_VSYNC_TRISTATE | 6    | 0x0     | 0=Normal VSYNC<br>1=Tristate VSYNC output  |
| CRT2_ON              | 7    | 0x0     | 0=CRT2 OFF - only CRT DAC used for CRT<br>1=CRT2 ON - TV DAC used for second CRT monitor (using CRTC2 path)  |
| CRTC2_PIX_WIDTH      | 11:8 | 0x0     | Display pixel width (actually depth).<br>For 4bpp mode DAC_CNTL.DAC_4BPP_PIX_ORDER selects the order of nibbles within bytes.<br>When R, G, or B components are only 4, 5 or 6 bits, DAC_CNTL.DAC_EXPAND_MODE selects how these components are expanded to 8 bits each for keying and palette lookup.<br>When alpha values are 1 or 4 bits, they are expanded to 8 bits by dynamic expansion of the high order bits to the missing lower order bits.<br>0=Disable pixel clock for secondary CRTC<br>1=Reserved<br>2=8bpp Indexed<br>3=15bpp aRGB 1555<br>4=16bpp RGB 565<br>5=24bpp RGB 888<br>6=32bpp aRGB 8888<br>7=16bpp aRGB 4444<br>8=16bpp aIndex 88   |
| CRTC2_ICON_EN        | 15   | 0x0     | 0=Disable Secondary Hardware Icon<br>1=Enable Secondary Hardware Icon  |
| CRTC2_CUR_EN         | 16   | 0x0     | Hardware cursor enable.<br>This field is double buffered and locked with the CUR_LOCK register field.<br>0=Disable<br>1=Enable   |

**CRTC2\_GEN\_CNTL - RW - 32 bits - [MMReg:0x3F8]**

| Field Name          | Bits  | Default | Description  |
|---------------------|-------|---------|--|
| CRTC2_CUR_MODE      | 22:20 | 0x0     | Hardware cursor mode.<br>For 2bpp mode, each line of cursor data is stored in memory as 64 bits of AND data followed by 64 bits of XOR data.<br>For color AND/XOR mode, each pixel is stored sequentially in memory as 32bits each in aRGB8888 format with bit 31 of each DWord being the AND bit.<br>For the color alpha modes the format is also 32bpp aRGB8888 with all 8 bits of the alpha being used.<br>All HW cursor lines must be 64 pixels wide and all lines must be stored sequentially in memory.<br>0=Mono + 1 bit AND (2bpp), 64x64<br>1=Color 24bpp + 1 bit AND, 32hx64v<br>2=Color 24bpp + 8 bit alpha, premultiplied alpha, 32hx64v<br>3=Color 24bpp + 8 bit alpha, unmultiplied alpha, 32hx64v |
| CRTC2_DISPLAY_DIS   | 23    | 0x0     | 0=Enable<br>1=Blanked  |
| CRTC2_EN            | 25    | 0x0     | Enables CRT controller.<br>When reset, the CRTC horizontal counter is set to zero, and the vertical counter is set to the current value of CRTC2_V_TOTAL_DISP.CRTC2_V_DISP.<br>0=Reset<br>1=Enable   |
| CRTC2_DISP_REQ_EN_B | 26    | 0x1     | Enables display graphics requests to the memory controller.<br>Affects only graphics and VGA text requests. Does not affect HW cursor, overlay or subpic.<br>When setting this bit, CRTC2_EXT_CNTL.CRTC2_DISPLAY_DIS is also normally set to blank the screen.<br>Active low.<br>0=Enable<br>1=Disable   |
| CRTC2_C_SYNC_EN     | 27    | 0x0     | 0=Disable<br>1=Enable  |
| CRTC2_HSYNC_DIS     | 28    | 0x0     | 0=Enable<br>1=Disable  |
| CRTC2_VSYNC_DIS     | 29    | 0x0     | 0=Enable<br>1=Disable  |

Secondary CRTC general controls

**CRTC2\_STATUS - RW - 32 bits - [MMReg:0x3FC]**

| Field Name            | Bits | Default | Description   |
|-----------------------|------|---------|---|
| CRTC2_VBLANK_CUR (R)  | 0    | 0x0     | Indicates if raster currently in vertical blank.<br>0=Not in vertical blank<br>1=In vertical blank  |
| CRTC2_VBLANK_SAVE (R) | 1    | 0x0     | Clearable vertical blank indicator. Used by software to determine if still the same vertical blank as the last time polling (or interrupt) occurred.<br>0=No vertical blank since last clear<br>1=Vertical Blank since last cleared |

**CRTC2\_STATUS - RW - 32 bits - [MMReg:0x3FC]**

| Field Name                  | Bits | Default | Description  |
|-----------------------------|------|---------|--|
| CRTC2_VBLANK_SAVE_CLEAR (W) | 1    | 0x0     | Used to clear CRTC2_VBLANK_SAVE.<br>0=No effect<br>1=Clear CRTC2_VBLANK_SAVE       |
| CRTC2_VLINE_SYNC (R)        | 2    | 0x0     | Indicates if the scan line is even or odd.<br>0=Even scan line<br>1=Odd scan line  |
| CRTC2_FRAME (R)             | 3    | 0x0     | Indicates if even or odd frame currently displayed.<br>0=Even frame<br>1=Odd frame |

Status bits to determine current state of the display.

**CRTC\_STATUS - RW - 32 bits - [IOReg,MMReg:0x5C]**

| Field Name                 | Bits | Default | Description   |
|----------------------------|------|---------|---|
| CRTC_VBLANK_CUR (R)        | 0    | 0x0     | Indicates if raster currently in vertical blank.<br>0=Not in vertical blank<br>1=In vertical blank  |
| CRTC_VBLANK_SAVE (R)       | 1    | 0x0     | Clearable vertical blank indicator. Used by software to determine if still the same vertical blank as the last time polling (or interrupt) occurred.<br>0=No vertical blank since last clear<br>1=Vertical Blank since last cleared |
| CRTC_VBLANK_SAVE_CLEAR (W) | 1    | 0x0     | Used to clear CRTC_VBLANK_SAVE.<br>0=No effect<br>1=Clear CRTC_VBLANK_SAVE  |
| CRTC_VLINE_SYNC (R)        | 2    | 0x0     | Indicates if the scan line is even or odd.<br>0=Even scan line<br>1=Odd scan line   |
| CRTC_FRAME (R)             | 3    | 0x0     | Indicates if even or odd frame currently displayed.<br>0=Even frame<br>1=Odd frame  |

Status bits to determine current state of the display.

**20. ddc Detailed Register Reference**

DDC registers

| <b>GPIO_VGA_DDC - RW - 32 bits - [IOReg,MMReg:0x60]</b> |             |                |  |
|---|-------------|----------------|--|
| <b>Field Name</b>                                       | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| VGA_DDC_DATA_OUTPUT                                     | 0           | 0x0            | Output data bit if output enabled by VGA_DDC_DATA_EN.<br>0=Drive VGA_DDC_DATA low, if enabled.<br>1=Drive VGA_DDC_DATA high, if enabled. |
| VGA_DDC_CLK_OUTPUT                                      | 1           | 0x0            | Output clock bit if output enabled by VGA_DDC_CLK_EN.<br>0=Drive VGA_DDC_CLK low, if enabled.<br>1=Drive VGA_DDC_CLK high, if enabled.   |
| VGA_DDC_DATA_INPUT (R)                                  | 8           | 0x0            | Data bit input.<br>0=VGA_DDC_DATA pin input is low.<br>1=VGA_DDC_DATA pin input is high.   |
| VGA_DDC_CLK_INPUT (R)                                   | 9           | 0x0            | Clock bit input.<br>0=VGA_DDC_CLK pin input is low.<br>1=VGA_DDC_CLK pin input is high.  |
| VGA_DDC_DATA_OUT_EN                                     | 16          | 0x0            | Data pin output enable.<br>0=VGA_DDC_DATA output disabled.<br>1=VGA_DDC_DATA output enabled.   |
| VGA_DDC_CLK_OUT_EN                                      | 17          | 0x0            | Clock pin output enable.<br>0=VGA_DDC_CLK output disabled.<br>1=VGA_DDC_CLK output enabled.  |

Control and read of DDC clock and data lines for analog VGA connector.

| <b>GPIO_DVI_DDC - RW - 32 bits - [IOReg,MMReg:0x64]</b> |             |                |  |
|---|-------------|----------------|--|
| <b>Field Name</b>                                       | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| DVI_DDC_DATA_OUTPUT                                     | 0           | 0x0            | Output data bit if output enabled by DVI_DDC_DATA_EN.<br>0=Drive DVI_DDC_DATA low, if enabled.<br>1=Drive DVI_DDC_DATA high, if enabled. |
| DVI_DDC_CLK_OUTPUT                                      | 1           | 0x0            | Output clock bit if output enabled by DVI_DDC_CLK_EN.<br>0=Drive DVI_DDC_CLK low, if enabled.<br>1=Drive DVI_DDC_CLK high, if enabled.   |
| DVI_DDC_DATA_INPUT (R)                                  | 8           | 0x0            | Data bit input.<br>0=DVI_DDC_DATA pin input is low.<br>1=DVI_DDC_DATA pin input is high.   |
| DVI_DDC_CLK_INPUT (R)                                   | 9           | 0x0            | Clock bit input.<br>0=DVI_DDC_CLK pin input is low.<br>1=DVI_DDC_CLK pin input is high.  |
| DVI_DDC_DATA_OUT_EN                                     | 16          | 0x0            | Data pin output enable.<br>0=DVI_DDC_DATA output disabled.<br>1=DVI_DDC_DATA output enabled.   |
| DVI_DDC_CLK_OUT_EN                                      | 17          | 0x0            | Clock pin output enable.<br>0=DVI_DDC_CLK output disabled.<br>1=DVI_DDC_CLK output enabled.  |

**GPIO\_DVI\_DDC - RW - 32 bits - [IOReg,MMReg:0x64]**

| Field Name   | Bits | Default | Description  |
|--|------|---------|--|
| SW_WANTS_TO_USE_DVI_I2C<br><i>(mirror of DVI_I2C_CNTL_0:SW_WANTS_TO_USE_DVI_I2C) (W)</i> | 20   | 0x0     | 0=Normal<br>1=SW requests to use DVI I2C interface   |
| SW_CAN_USE_DVI_I2C<br><i>(mirror of DVI_I2C_CNTL_0:SW_CAN_USE_DVI_I2C) (R)</i>           | 20   | 0x0     | 0=DVI I2C interface not available<br>1=SW has control of the DVI I2C interface               |
| SW_DONE_USING_DVI_I2C<br><i>(mirror of DVI_I2C_CNTL_0:SW_DONE_USING_DVI_I2C) (W)</i>     | 21   | 0x0     | 0=if SW has control of DVI I2C, free to use it<br>1=indicate SW is done using DVI I2C i/f    |
| HDCP_NEEDS_DVI_I2C<br><i>(mirror of DVI_I2C_CNTL_0:HW_NEEDS_DVI_I2C) (R)</i>             | 21   | 0x0     | 0=no request by H/W for use of DVI I2C<br>1=H/W HDCP requests use of the DVI I2C i/f         |
| ABORT_HDCP_DVI_I2C<br><i>(mirror of DVI_I2C_CNTL_0:ABORT_HW_DVI_I2C) (W)</i>             | 22   | 0x0     | 0=normal operation of H/W using DVI I2C<br>1=abort current H/W HDCP use of DVI I2C interface |
| HW_USING_DVI_I2C<br><i>(mirror of DVI_I2C_CNTL_0:HW_USING_DVI_I2C) (R)</i>               | 22   | 0x0     | 0=DVI I2C i/f not in use by H/W<br>1=HDCP H/W currently using DVI I2C interface              |

Control and read of DDC clock and data lines for digital connector.

**GPIO\_MONID - RW - 32 bits - [IOReg,MMReg:0x68]**

| Field Name             | Bits | Default | Description  |
|------------------------|------|---------|--|
| GPIO_MONID_0_OUTPUT    | 0    | 0x0     | Output data for MONID(0) pin.<br>0=Drive MONID(0) low, if enabled.<br>1=Drive MONID(0) high, if enabled. |
| GPIO_MONID_1_OUTPUT    | 1    | 0x0     | Output data for MONID(1) pin.<br>0=Drive MONID(1) low, if enabled.<br>1=Drive MONID(1) high, if enabled. |
| GPIO_MONID_0_INPUT (R) | 8    | 0x0     | Input data from MONID(0) pin.<br>0=MONID(0) pin input is low.<br>1=MONID(0) pin input is high.           |
| GPIO_MONID_1_INPUT (R) | 9    | 0x0     | Input data from MONID(1) pin.<br>0=MONID(1) pin input is low.<br>1=MONID(1) pin input is high.           |
| GPIO_MONID_0_OUT_EN    | 16   | 0x0     | Output enable for MONID(0) pin.<br>0=MONID(0) output disabled.<br>1=MONID(0) output enabled.             |
| GPIO_MONID_1_OUT_EN    | 17   | 0x0     | Output enable for MONID(1) pin.<br>0=MONID(1) output disabled.<br>1=MONID(1) output enabled.             |

Control and read of MONID general purpose IO pins.

**GPIO\_CRT2\_DDC - RW - 32 bits - [IOReg,MMReg:0x6C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



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**GPIO\_CRT2\_DDC - RW - 32 bits - [IOReg,MMReg:0x6C]**

| Field Name              | Bits | Default | Description   |
|-------------------------|------|---------|---|
| CRT2_DDC_DATA_OUTPUT    | 0    | 0x0     | 0=Drive CRT2_DDC_DATA low, if enabled.<br>1=Drive CRT2_DDC_DATA high, if enabled. |
| CRT2_DDC_CLK_OUTPUT     | 1    | 0x0     | 0=Drive CRT2_DDC_CLK low, if enabled.<br>1=Drive CRT2_DDC_CLK high, if enabled.   |
| CRT2_DDC_DATA_INPUT (R) | 8    | 0x0     | 0=CRT2_DDC_DATA pin input is low.<br>1=CRT2_DDC_DATA pin input is high.           |
| CRT2_DDC_CLK_INPUT (R)  | 9    | 0x0     | 0=CRT2_DDC_CLK pin input is low.<br>1=CRT2_DDC_CLK pin input is high.             |
| CRT2_DDC_DATA_OUT_EN    | 16   | 0x0     | 0=CRT2_DDC_DATA output disabled.<br>1=CRT2_DDC_DATA output enabled.               |
| CRT2_DDC_CLK_OUT_EN     | 17   | 0x0     | 0=CRT2_DDC_CLK output disabled.<br>1=CRT2_DDC_CLK output enabled.                 |

No description available for this register.

**21. Overlay Detailed Register Reference**

## Overlay

| <b>OV0_Y_X_START - RW - 32 bits - [MMReg:0x400]</b> |             |                |   |
|---|-------------|----------------|---|
| <b>Field Name</b>                                   | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| OV0_X_START   | 12:0        | 0x0            | Overlay X starting coordinate relative to ACTIVE screen (0,0) |
| OV0_Y_START   | 28:16       | 0x0            | Overlay Y starting coordinate relative to ACTIVE screen (0,0) |

X/Y coords relative to active display in pixels

| <b>OV0_Y_X_END - RW - 32 bits - [MMReg:0x404]</b> |             |                |   |
|---|-------------|----------------|---|
| <b>Field Name</b>                                 | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| OV0_X_END   | 12:0        | 0x0            | Overlay X ending coordinate relative to ACTIVE screen (0,0) |
| OV0_Y_END   | 28:16       | 0x0            | Overlay X ending coordinate relative to ACTIVE screen (0,0) |

X/Y ending coordinates (inclusive) relative to active display in pixels

| <b>OV0_PIPELINE_CNTL - RW - 32 bits - [MMReg:0x408]</b> |             |                |   |
|---|-------------|----------------|---|
| <b>Field Name</b>                                       | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| OV0_DISP_PIPE_DELAY                                     | 3:0         | 0x8            | Debug field used to adjust overlay window position. Leave at default unless hardware problem requires adjustment as instructed. |

Debug adjustments for overlay window control

| <b>OV0_REG_LOAD_CNTL - RW - 32 bits - [MMReg:0x410]</b> |             |                |  |
|---|-------------|----------------|--|
| <b>Field Name</b>                                       | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| OV0_LOCK  | 0           | 0x0            | <p>If this bit is set, then the start of Display VBlank event that usually updates double buffered registers is ignored. Use this bit to autonomously update scaler and subpicture registers.</p> <p>To use, set this bit, and then poll OV0_LOCK_READBACK until the lock takes effect. In almost all situations the lock should take effect before the first read; however, it is theoretically possible that the lock will not take quickly if various clocks in the chip are programmed to very low frequencies (for power saving for example).</p> <p>Once the lock takes, write registers to update the overlay. Then write the lock bit to zero.</p> <p>The new settings will take effect at the next VBlank rising edge (provided that LOCK is left unset).<br/>           0=NOT LOCKED<br/>           1=LOCKED</p> |



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**OV0\_REG\_LOAD\_CNTL - RW - 32 bits - [MMReg:0x410]**

| Field Name                 | Bits | Default | Description   |
|----------------------------|------|---------|---|
| OV0_VBLANK_DURING_LOCK (R) | 1    | 0x0     | This bit is updated only when OV0_LOCK transitions from 1 to 0. If VBlank occurred while OV0_LOCK was 1, then this bit will be updated to the value one. Otherwise it is updated to the value zero.<br>0=DID NOT HAPPEN<br>1=DID HAPPEN   |
| OV0_STALL_GUI_UNTIL_FLIP   | 2    | 0x0     | The intent here is for the overlay to be able to tell the GUI that it is using the surface that the GUI wants to render to. The overlay will send an 'OV0_SURFACE_IS_FREE' signal to the GUI. It will make this signal go low when there is a danger of front buffer overwrite as determined by software. If software wants to stall the GUI, then it will set OV0_STALL_GUI_UNTIL_FLIP when it locks, updates, and unlocks overlay and subpicture registers. OV0_SURFACE_IS_FREE will go low at unlock and then high during VBlank (when the hardware double buffering flips the registers). The behavior of OV0_SURFACE_IS_FREE is undefined if OV0_STALL_GUI_UNTIL_FLIP is written to when the lock bit is not set.<br><br>OV0_SURFACE_IS_FREE is not an event signal. If it is low the WaitUntilEvent command must stall the GUI until it is high. It does not wait until the signal transitions from low to high. (i.e. If it is already high, there is no stall).<br><br>0=DO NOT STALL<br>1=DO STALL |
| OV0_LOCK_READBACK (R)      | 3    | 0x0     | See OV0_LOCK. This bit indicates whether the lock took effect.<br>0=NOT LOCKED<br>1=LOCKED  |
| OV0_FLIP_READBACK (R)      | 4    | 0x0     | Status indication of whether last submitted overlay flip has occurred yet.<br>0=Flip not yet occurred.<br>1=Flip has occurred.  |

Overlay register load control

**OV0\_SCALE\_CNTL - RW - 32 bits - [MMReg:0x420]**

| Field Name              | Bits | Default | Description   |
|-------------------------|------|---------|---|
| OV0_NO_READ_BEHIND_SCAN | 1    | 0x0     | Recommend set to zero. If set, the data for the next display line is not written to the line buffer until the current line has been read.   |
| OV0_HORZ_PICK_NEAREST   | 2    | 0x0     | Recommend set to zero. If source keying is absolutely needed, then we may need to drop the interpolated scale in order to make the source keyer work.<br>0=BLEND<br>1=FIX H_ALPHA = 0 |
| OV0_VERT_PICK_NEAREST   | 3    | 0x0     | Recommend set to zero. If source keying is absolutely needed, then we may need to drop the interpolated scale in order to make the source keyer work.<br>0=BLEND<br>1=FIX V_ALPHA = 0 |



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**OV0\_SCALE\_CNTL - RW - 32 bits - [MMReg:0x420]**

| Field Name          | Bits  | Default | Description  |
|---------------------|-------|---------|--|
| OV0_SIGNED_UV       | 4     | 0x0     | Support the signed UV source format needed by Apple.<br>0=UNSIGNED<br>1=SIGNED   |
| OV0_GAMMA_SEL       | 7:5   | 0x0     | Select gamma correction factor: (default=0)<br>0 = Brightness Enable<br>1 = Gamma 2.2<br>2 = Gamma 1.8<br>3 = Gamma 1.4<br><br>0=Linear, G=1.0<br>1=G=0.85<br>2=G=1.1<br>3=G=1.2<br>4=G=1.45<br>5=G=1.7<br>6=G=2.2<br>7=G=2.5  |
| OV0_SURFACE_FORMAT  | 11:8  | 0x0     | Scale source pixel format from memory:<br>0-2 = (reserved)<br>3 = 15 bpp aRGB 1555<br>4 = 16 bpp RGB 565<br>5 = (reserved)<br>6 = 32 bpp aRGB 8888<br>7-8 = (reserved)<br>9 = YUV 9<br>10 = YUV 12<br>11 = VYUY422<br>12 = YVYU422<br>13-15 = (reserved)<br>3=15BPP ARGB1555<br>4=16BPP RGB565<br>6=32BPP ARGB8888<br>9=Three plane YUV9<br>10=Three plane YUV12<br>11=Packed VYUY422<br>12=Packed YVYU422<br>13=Two plane YUV12 |
| OV0_ADAPTIVE_DEINT  | 12    | 0x0     | 0=Adaptive de-interlacing is off.<br>1=Adaptive de-interlacing enabled.  |
| OV0_CRTC_SEL        | 14    | 0x0     | 0=Use overlay/scaler on primary CRTC display path<br>1=Use overlay/scaler on secondary CRTC2 display path  |
| OV0_BURST_PER_PLANE | 22:16 | 0x7f    |  |

**OV0\_SCALE\_CNTL - RW - 32 bits - [MMReg:0x420]**

| Field Name             | Bits | Default | Description  |
|------------------------|------|---------|--|
| OV0_DOUBLE_BUFFER_REGS | 24   | 0x0     | Recommend set to 1. Turns on double buffering so that many registers can be updated autonomously in the VBlank. Currently the following fields are double buffered but the list is subject to change as we attempt to reduce the gate count.<br>OV0_V_INC, OV0_P1_V_ACCUM_INIT,<br>OV0_P23_V_ACCUM_INIT,<br>OV0_P1_BLNK_LN_AT_TOP_M1,<br>OV0_P1_ACTIVE_LINES_M1,<br>OV0_P23_BLNK_LN_AT_TOP_M1,<br>OV0_P23_ACTIVE_LINES_M1,<br>OV0_P1_OCTWORDS_PER_LINE_M1,<br>OV0_P2_OCTWORDS_PER_LINE_M1,<br>OV0_P3_OCTWORDS_PER_LINE_M1,<br>OV0_SMART_SWITCH, OV0_BURST_PER_PLANE,<br>OV0_SOFT_EOF_TOGGLE, OV0_DEINT_PAT,<br>OV0_DEINT_PAT_LEN_M1, OV0_P1_H_INC,<br>OV0_P23_H_INC, OV0_P1_H_STEP_BY,<br>OV0_P23_H_STEP_BY, OV0_P1_H_ACCUM_INIT,<br>OV0_PRESHIFT_P1_TO, OV0_P23_H_ACCUM_INIT,<br>OV0_PRESHIFT_P23_TO, OV0_P1_X_START,<br>OV0_P1_X_END, OV0_P2_X_START, OV0_P2_X_END,<br>OV0_P3_X_START, OV0_P3_X_END,<br>OV0_P1_MAX_LN_IN_PER_LN_OUT,<br>OV0_P23_MAX_LN_IN_PER_LN_OUT.<br>0=OFF<br>1=ON |
| OV0_BANDWIDTH (R)      | 26   | 0x0     | 0=NORMAL<br>1=BANDWIDTH LIMIT/ACK  |
| OV0_LIN_TRANS_BYPASS   | 28   | 0x0     | 0=DO NOT BYPASS COLOUR CONVERSION<br>1=BYPASS COLOUR CONVERSION  |
| OV0_INT_EMU            | 29   | 0x0     | Enables experimental deinterlacing hardware which should make displayed video look sharper than 'bobbed' video, but without the feathering artifacts associated with 'weaved' video. It also makes colours richer.<br>0=OFF<br>1=ON  |
| OV0_OVERLAY_EN         | 30   | 0x0     | 0 = Overlay Disable (default=0)<br>1 = Overlay Enable<br>0=DISABLE<br>1=ENABLE   |
| OV0_SOFT_RESET         | 31   | 0x1     | Resets the scaler.<br>0=ENABLE<br>1=RESET  |

General scaler control

**OV0\_V\_INC - RW - 32 bits - [MMReg:0x424]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| OV0_V_INC  | 25:8 | 0x0     | Vertical accumulator increment [17:0]. This is a 6.12 fixed point number. It is used to control the vertical scaling ratio. |

Vertical accumulator increment

**OV0\_P1\_V\_ACCUM\_INIT - RW - 32 bits - [MMReg:0x428]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



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**OV0\_P1\_V\_ACCUM\_INIT - RW - 32 bits - [MMReg:0x428]**

| Field Name                  | Bits  | Default | Description  |
|-----------------------------|-------|---------|--|
| OV0_P1_MAX_LN_IN_PER_LN_OUT | 1:0   | 0x1     | This field supports a new feature which is the ability to read in and blend more than one line for every line output. Using it greatly improves image quality when downscaling vertically. However, memory bandwidth limits the number of lines that can be read in. Do not program the scaler to read in more lines than there is bandwidth to support. The scaler document provides an explanation on determining the available bandwidth. |
| OV0_P1_V_ACCUM_INIT         | 25:15 | 0x0     | This is a 6.5 fixed point number. The integer portion indicates how many lines to fetch and cycle into (and possibly through) through the line buffers in preparation for generating the first display line. The fractional portion indicates the blend of source lines the four tap/two tap filter kernel that is used to generate the first display line.  |

This register is needed to accurately vertically position the source video in the overlay display window, and also to accurately position it relative to the subpicture image.

**OV0\_P23\_V\_ACCUM\_INIT - RW - 32 bits - [MMReg:0x42C]**

| Field Name                   | Bits  | Default | Description  |
|------------------------------|-------|---------|--|
| OV0_P23_MAX_LN_IN_PER_LN_OUT | 1:0   | 0x1     | This field supports a new feature which is the ability to read in and blend more than one line for every line output. Using it greatly improves image quality when downscaling vertically. However, memory bandwidth limits the number of lines that can be read in. Do not program the scaler to read in more lines than there is bandwidth to support. The scaler document provides an explanation on determining the available bandwidth. |
| OV0_P23_V_ACCUM_INIT         | 24:15 | 0x0     | This is a 6.5 fixed point number. The integer portion indicates how many lines (planer U and V lines) to fetch and cycle into (and possibly through) through the line buffers in preparation for generating the first display line. The fractional portion indicates the blend of source lines the four tap/two tap filter kernel that is used to generate the first display line.   |

Please refer to P1\_V\_ACCUM\_INIT. This register is used for the UV components in Planer modes.

**OV0\_P1\_BLANK\_LINES\_AT\_TOP - RW - 32 bits - [MMReg:0x430]**

| Field Name               | Bits  | Default | Description   |
|--------------------------|-------|---------|---|
| OV0_P1_BLNK_LN_AT_TOP_M1 | 11:0  | 0xff    | This is a signed value. Default it to -1 and don't exceed the maximum positive value.   |
| OV0_P1_ACTIVE_LINES_M1   | 27:16 | 0x0     | Program this with the surface height minus one. After the hardware scales and displays the blank lines at top and the active lines, it will continue to scale and display blank lines until it reaches the end of the overlay window. |

Used for DVD letterboxing (when a wide movie is displayed with black borders at the top and bottom). The problem is that software can't provide the black borders using the primary display because subpicture information can be displayed in the black regions. It also is wasteful to allocate extra off screen memory in the frame buffer and fill it with 'black' pixels. Thus use these fields to create the black borders for DVD letterboxing.

**OV0\_P23\_BLANK\_LINES\_AT\_TOP - RW - 32 bits - [MMReg:0x434]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**OV0\_P23\_BLANK\_LINES\_AT\_TOP - RW - 32 bits - [MMReg:0x434]**

| Field Name                | Bits  | Default | Description   |
|---------------------------|-------|---------|---|
| OV0_P23_BLNK_LN_AT_TOP_M1 | 10:0  | 0x7ff   | This is a signed value. Default it to -1 and don't exceed the maximum positive value.   |
| OV0_P23_ACTIVE_LINES_M1   | 26:16 | 0x0     | Program this with the surface height minus one. After the hardware scales and displays the blank lines at top and the active lines, it will continue to scale and display blank lines until it reaches the end of the overlay window. |

Please refer to P1\_BLANK\_LINES\_AT\_TOP. This register is used for the UV components in Planer modes.

**OV0\_BASE\_ADDR - RW - 32 bits - [MMReg:0x43C]**

| Field Name    | Bits | Default | Description   |
|---------------|------|---------|---|
| OV0_BASE_ADDR | 31:0 | 0x0     | This base is added to all overlay address requests to the internal memory controller. Setting this register equal to MC_FB_LOCATION.MC_FB_START positions all overlay surfaces in the frame buffer. Alternatively setting it to MC_AGP_LOCATION.MC_AGP_START positions overlay surfaces in AGP memory. The use of the overlay from AGP is supported, but not recommended. This base address must be a 4 Megabyte aligned value.<br><br>NOTE: Bits 0:21 of this field are hardwired to ZERO. |

Overlay base address

**OV0\_VID\_BUF0\_BASE\_ADRS - RW - 32 bits - [MMReg:0x440]**

| Field Name            | Bits  | Default | Description  |
|-----------------------|-------|---------|--|
| OV0_VID_BUF_PITCH_SEL | 0     | 0x0     | Associates either OV0_VID_BUF_PITCH0_VALUE register or OV0_VID_BUF_PITCH1_VALUE register with this surface or plane of a planer surface.<br>0=SELECT PITCH 0<br>1=SELECT PITCH 1 |
| RESERVED_BIT1         | 1     | 0x0     | reserved for tiling info. No overlay tiling in this ASIC.  |
| OV0_VID_BUF_BASE_ADRS | 26:4  | 0x0     | BASE_ADRS is actually a poor choice of name. This field points to the octaword that contains the top left corner pixel of the region of the surface that you wish to display.    |
| RESERVED_BIT31_28     | 31:28 | 0x0     | reserved for tiling info. No overlay tiling in this ASIC.  |

A surface descriptor register that include the base address (or base offset) of a surface, and some attributes for pitch selection and tiled surface support.

Double buffering (for autonomous overlay updates), or multi-buffering can be achieved by switching between any of the six base address registers using the OV0\_AUTOFLIP\_CNTL register. (Note: for planer surfaces the six registers are interpreted by hardware as two sets of three registers. Thus only OV0\_VID\_BUF0 and OV0\_VID\_BUF3 are valid selections.)

OV0\_VID\_BUF0 can describe any non-planer surface, or it can be used to describe the Y plane of a planer surface.

**OV0\_VID\_BUF1\_BASE\_ADRS - RW - 32 bits - [MMReg:0x444]**

| Field Name            | Bits | Default | Description  |
|-----------------------|------|---------|--|
| OV0_VID_BUF_PITCH_SEL | 0    | 0x0     | Same as in OV0_VID_BUF0_BASE_ADRS.<br>0=SELECT PITCH 0<br>1=SELECT PITCH 1 |
| RESERVED_BIT1         | 1    | 0x0     | reserved for tiling info. No overlay tiling in this ASIC.                  |
| OV0_VID_BUF_BASE_ADRS | 26:4 | 0x0     | Same as in OV0_VID_BUF0_BASE_ADRS.   |

**OV0\_VID\_BUF1\_BASE\_ADRS - RW - 32 bits - [MMReg:0x444]**

| Field Name        | Bits  | Default | Description   |
|-------------------|-------|---------|---|
| RESERVED_BIT31_28 | 31:28 | 0x0     | reserved for tiling info. No overlay tiling in this ASIC. |

OV0\_VID\_BUF1 can describe any non-planer surface, or it can be used to describe the U plane of a planer surface.

**OV0\_VID\_BUF2\_BASE\_ADRS - RW - 32 bits - [MMReg:0x448]**

| Field Name            | Bits  | Default | Description  |
|-----------------------|-------|---------|--|
| OV0_VID_BUF_PITCH_SEL | 0     | 0x0     | Same as in OV0_VID_BUF0_BASE_ADRS.<br>0=SELECT PITCH 0<br>1=SELECT PITCH 1 |
| RESERVED_BIT1         | 1     | 0x0     | reserved for tiling info. No overlay tiling in this ASIC.                  |
| OV0_VID_BUF_BASE_ADRS | 26:4  | 0x0     | Same as in OV0_VID_BUF0_BASE_ADRS.   |
| RESERVED_BIT31_28     | 31:28 | 0x0     | reserved for tiling info. No overlay tiling in this ASIC.                  |

OV0\_VID\_BUF2 can describe any non-planer surface, or it can be used to describe the V plane of a planer surface.

**OV0\_VID\_BUF3\_BASE\_ADRS - RW - 32 bits - [MMReg:0x44C]**

| Field Name            | Bits  | Default | Description  |
|-----------------------|-------|---------|--|
| OV0_VID_BUF_PITCH_SEL | 0     | 0x0     | Same as in OV0_VID_BUF0_BASE_ADRS.<br>0=SELECT PITCH 0<br>1=SELECT PITCH 1 |
| RESERVED_BIT1         | 1     | 0x0     | reserved for tiling info. No overlay tiling in this ASIC.                  |
| OV0_VID_BUF_BASE_ADRS | 26:4  | 0x0     | Same as in OV0_VID_BUF0_BASE_ADRS.   |
| RESERVED_BIT31_28     | 31:28 | 0x0     | reserved for tiling info. No overlay tiling in this ASIC.                  |

OV0\_VID\_BUF3 can describe any non-planer surface, or it can be used to describe the Y plane of a planer surface.

**OV0\_VID\_BUF4\_BASE\_ADRS - RW - 32 bits - [MMReg:0x450]**

| Field Name            | Bits  | Default | Description  |
|-----------------------|-------|---------|--|
| OV0_VID_BUF_PITCH_SEL | 0     | 0x0     | Same as in OV0_VID_BUF0_BASE_ADRS.<br>0=SELECT PITCH 0<br>1=SELECT PITCH 1 |
| RESERVED_BIT1         | 1     | 0x0     | reserved for tiling info. No overlay tiling in this ASIC.                  |
| OV0_VID_BUF_BASE_ADRS | 26:4  | 0x0     | Same as in OV0_VID_BUF0_BASE_ADRS.   |
| RESERVED_BIT31_28     | 31:28 | 0x0     | reserved for tiling info. No overlay tiling in this ASIC.                  |

OV0\_VID\_BUF4 can describe any non-planer surface, or it can be used to describe the U plane of a planer surface.

**OV0\_VID\_BUF5\_BASE\_ADRS - RW - 32 bits - [MMReg:0x454]**

| Field Name            | Bits | Default | Description  |
|-----------------------|------|---------|--|
| OV0_VID_BUF_PITCH_SEL | 0    | 0x0     | Same as in OV0_VID_BUF0_BASE_ADRS.<br>0=SELECT PITCH 0<br>1=SELECT PITCH 1 |
| RESERVED_BIT1         | 1    | 0x0     | reserved for tiling info. No overlay tiling in this ASIC.                  |
| OV0_VID_BUF_BASE_ADRS | 26:4 | 0x0     | Same as in OV0_VID_BUF0_BASE_ADRS.   |

**OV0\_VID\_BUF5\_BASE\_ADRS - RW - 32 bits - [MMReg:0x454]**

| Field Name        | Bits  | Default | Description   |
|-------------------|-------|---------|---|
| RESERVED_BIT31_28 | 31:28 | 0x0     | reserved for tiling info. No overlay tiling in this ASIC. |

OV0\_VID\_BUF5 can describe any non-planer surface, or it can be used to describe the V plane of a planer surface.

**OV0\_VID\_BUF\_PITCH0\_VALUE - RW - 32 bits - [MMReg:0x460]**

| Field Name              | Bits  | Default | Description  |
|-------------------------|-------|---------|--|
| OV0_PITCH_VALUE         | 19:4  | 0x0     | For linear (non-tiled) surfaces, the pitch value is the pitch of the surface, or in the case of planer modes, the pitch of a plane in a surface.<br>For tiled modes, the pitch value is not the pitch. It is a number that the hardware needs to get from the beginning of last line that it read in the previous row of tiles to the beginning first line that it must read in the next row of tiles. To understand this concept, you need a solid understanding of how tiled surfaces are organized in memory. (there is code in the ov0setup.cpp sample code that does the necessary calculations). |
| OV0_PITCH_SKIP_LINES    | 27:26 | 0x0     | Used only if the surface (or plane in planer surface) is tiled. Ignored otherwise.<br><br>When downscaling, or when picking off the even or odd lines of an MPEG frame, it is sometimes desirable to 'double the pitch'. However, unlike linear surfaces, doubling the pitch in a tiled surface doesn't have the desired effect. Therefore, hardware provides a mechanism for skipping lines. Using this field will require that the OV0_PITCH?_VALUE field be changed as well.<br>0=USE EVERY LINE<br>1=USE EVERY 2nd LINE<br>2=USE EVERY 4th LINE<br>3=USE EVERY 8th LINE                            |
| OV0_PITCH_IN_TILES_LSBS | 31:28 | 0x0     | Not used. No overlay tiling in this ASIC.  |

Fields needed for advancing the hardware's line start address pointer from the beginning of one line to the beginning of the next, and for enabling correct checkerboarding in tiled modes.

**OV0\_VID\_BUF\_PITCH1\_VALUE - RW - 32 bits - [MMReg:0x464]**

| Field Name              | Bits  | Default | Description   |
|-------------------------|-------|---------|---|
| OV0_PITCH_VALUE         | 19:4  | 0x0     | See OV0_VID_BUF_PITCH0_VALUE.   |
| OV0_PITCH_SKIP_LINES    | 27:26 | 0x0     | See OV0_VID_BUF_PITCH0_VALUE.<br>0=USE EVERY LINE<br>1=USE EVERY 2nd LINE<br>2=USE EVERY 4th LINE<br>3=USE EVERY 8th LINE |
| OV0_PITCH_IN_TILES_LSBS | 31:28 | 0x0     | Not used. No overlay tiling in this ASIC.   |

A second set of pitch fields that can be used to implement double buffering when changing the pitch, or that can be used to have different pitches for different planes in planer modes (YUV9 and YUV12). Selection of Pitch0/Pitch1 is controlled by the OV0\_VID\_BUF?\_PITCH\_SEL field in the selected OV0\_VID\_BUF?\_BASE\_ADRS register.

**OV0\_AUTO\_FLIP\_CNTRL - RW - 32 bits - [MMReg:0x470]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



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**OV0\_AUTO\_FLIP\_CNTRL - RW - 32 bits - [MMReg:0x470]**

| Field Name              | Bits | Default | Description  |
|-------------------------|------|---------|--|
| OV0_SOFT_BUF_NUM        | 2:0  | 0x0     | A pointer to one of the six base address registers. For non-planer modes valid values are from 0 to 5. For planer modes valid values are 0 and 3.  |
| OV0_SOFT_REPEAT_FIELD   | 3    | 0x0     | 0=LAST FIELD NOT REPEAT<br>1=LAST FIELD IS REPEAT  |
| OV0_SOFT_BUF_ODD        | 4    | 0x0     | For non-interlaced video (e.g. MPEG frames) this field is don't care, but the SHIFT_EVEN_DOWN and SHIFT_ODD_DOWN register fields should be zero. For interlaced video provided by a software application, this field should indicate if the video field is even or odd. If This value is ignored until the internal version of the _EOF_TOGGLE signal changes state.<br>0=EVEN<br>1=ODD  |
| OV0_IGNORE_REPEAT_FIELD | 5    | 0x0     | If a hardware video capture port is selected, and if the video input stream has embedded repeat field flags, then these can be used to reset the deinterlacing pattern. Specifically, the current pattern will be used to select how the field that just arrived and it's two predecessors are displayed. The next time a field arrives, deinterlacing pattern zero will be used.<br><br>Setting this bit will cause the repeat field flags to be ignored.<br><br>If VID_PORT_SELECT is 2 (software), then the hardware assumes that every incoming field has a REPEAT_FIELD attribute. Use this bit to disable that attribute on a field by field basis.<br>0=DON'T IGNORE<br>1=DO IGNORE |
| OV0_SOFT_EOF_TOGGLE     | 6    | 0x0     | After writing SOFT_BUF_NUM and SOFT_BUF_ODD, then change the state of the EOF_TOGGLE bit. The EOF_TOGGLE signal is double buffered, so your change won't happen to the internal version of EOF_TOGGLE (and thus won't be used by hardware) until the start of VBlank, and then only if the LOCK bit is low. However when the internal version does change state, the hardware becomes aware of the new field/frame of video that you describe using SOFT_BUF_NUM and SOFT_BUF_ODD.   |
| OV0_VID_PORT_SELECT     | 9:8  | 0x0     | Selects one of the two capture engines or a software application as the provider of video.<br>0=PORT 0<br>1=reserved<br>2=SOFTWARE   |
| OV0_P1_FIRST_LINE_EVEN  | 16   | 0x0     | If you are weaving two fields together, then you must indicate if the first line that the scaler will fetch is in the field labeled even or the field labeled odd.<br>0=IS ODD<br>1=IS EVEN  |
| OV0_SHIFT_EVEN_DOWN     | 18   | 0x0     | If 'bobbing' video (Called 'Run' Deinterlacing) then this bit allows you to shift the even fields down.  |
| OV0_SHIFT_ODD_DOWN      | 19   | 0x0     | If 'bobbing' video (Called 'Run' Deinterlacing) then this bit allows you to shift the odd fields down.   |

**OV0\_AUTO\_FLIP\_CNTRL - RW - 32 bits - [MMReg:0x470]**

| Field Name           | Bits | Default | Description   |
|----------------------|------|---------|---|
| OV0_FIELD_POL_SOURCE | 23   | 0x0     | 0=Video field polarity taken from next source field.<br>Recommended for bob.<br>1=Video field polarity taken from current source field.<br>Recommended for weave. |

As a video capture port or software application provides new fields or frames of video, information about where these new fields/frames, what they are, and how they should be displayed is passed to the scaler using the AUTO\_FLIP\_CNTRL register.

OV0\_SOFT\_BUF\_NUM, OV0\_SOFT\_BUF\_ODD, and OV0\_IGNORE\_REPEAT\_FIELD are a software application's way of describing new video fields or frames to hardware. These values are ignored until the internal (double buffered) version of the \_EOF\_TOGGLE signal changes state.

If a new video field or frame is created, indicate where it is by writing the address into an unused BASE ADDRESS REGISTER. (If you have already set up a circular buffer then this may already be done). Then write the number of the base address register in OV0\_SOFT\_BUF\_NUM. Also set it's attributes using OV0\_SOFT\_BUF\_ODD and OV0\_IGNORE\_REPEAT\_FIELD. Then change the value of SOFT\_EOF\_TOGGLE to submit the description of the new field to hardware.

The hardware will display some 'combination' of this field and the two previous fields. ('Weave' most recent with next most recent, or 'Weave' the second and third most recent, 'Bob' most recent, or 'Bob' the second most recent)

**OV0\_DEINTERLACE\_PATTERN - RW - 32 bits - [MMReg:0x474]**

| Field Name             | Bits  | Default | Description   |
|------------------------|-------|---------|---|
| OV0_DEINT_PAT          | 19:0  | 0x0     | Ten two bit values. Values are enumerated as follows:<br>0) weave the two most recently submitted fields together and display them,<br>1) weave the second two most recently submitted fields together and display them,<br>2) display only the most recently submitted field (using 'bob' deinterlacing),<br>3) display only the second most recently submitted field (using 'bob' deinterlacing),<br>The scaler documentation provides example patterns of two bit values that can be programmed into this field. This field is double buffered. A two bit value is sampled from the position indicated by the OV0_DEINT_PAT_PNTR at the beginning of a display frame after a new video field is submitted. This two bit value remains in use until a new field is submitted. |
| OV0_DEINT_PAT_PNTR (R) | 27:24 | 0x0     | Read this to find out which two bit value in the pattern the video is currently using.  |
| OV0_DEINT_PAT_LEN_M1   | 31:28 | 0x0     | Set this to 9 if you want to cycle through all ten two bit values, else set it to a lower value.  |

The scaler remembers the last three fields of video that were provided. There are 10 two bit values in the OV0\_DEINTERLACE\_PATTERN register. Each two bit value selects one of four ways that these fields should be displayed.

**OV0\_SUBMIT\_HISTORY - R - 32 bits - [MMReg:0x478]**

| Field Name       | Bits  | Default | Description     |
|------------------|-------|---------|-----------------|
| OV0_NEXT_BUF_NUM | 2:0   | 0x0     |                 |
| OV0_NEXT_IS_ODD  | 4     | 0x0     | 0=EVEN<br>1=ODD |
| OV0_CURR_BUF_NUM | 10:8  | 0x0     |                 |
| OV0_CURR_IS_ODD  | 12    | 0x0     | 0=EVEN<br>1=ODD |
| OV0_PREV_BUF_NUM | 18:16 | 0x0     |                 |

**OV0\_SUBMIT\_HISTORY - R - 32 bits - [MMReg:0x478]**

| Field Name      | Bits | Default | Description     |
|-----------------|------|---------|-----------------|
| OV0_PREV_IS_ODD | 20   | 0x0     | 0=EVEN<br>1=ODD |

No description available for this register.

**OV0\_H\_INC - RW - 32 bits - [MMReg:0x480]**

| Field Name    | Bits  | Default | Description   |
|---------------|-------|---------|---|
| OV0_P1_H_INC  | 13:0  | 0x0     | Horizontal scale increment (1/Scale Ratio) for Y, R, G, and B. It is a 2.12 fixed point number.               |
| OV0_P23_H_INC | 29:16 | 0x0     | Horizontal scale increment (1/Scale Ratio) for U and V (Actually Cb and Cr). It is a 2.12 fixed point number. |

This register indicates how much to scale the Y, R, G, B (P1) or UV (P23) in the horizontal direction. Note that to improve quality when downscaling you should decimate the data first using the 'STEP\_BY' register fields. The decimated data is then scaled by the amount that you indicate using P?\_H\_INC. The CalcH.cpp function provides the decision making code required to do this.

**OV0\_STEP\_BY - RW - 32 bits - [MMReg:0x484]**

| Field Name             | Bits | Default | Description  |
|------------------------|------|---------|--|
| OV0_P1_H_STEP_BY       | 2:0  | 0x0     | P1 refers to the Y in YUV, to G in RGB32, and to RGB in RGB 15/16. In RGB15/16 the value zero (four tap vertical filtering) is not supported.<br>0=STEP BY 1, 4TAP VBLEND<br>1=STEP BY 1, 2TAP VBLEND<br>2=STEP BY 2, 2TAP VBLEND<br>3=STEP BY 4 or 3/5, 2TAP VBLEND<br>4=STEP BY 8 or 7/9 or 6/10, 2TAP VBLEND<br>5=STEP BY 15/17 or 14/18, 2TAP VBLEND |
| OV0_P1_PREDWNSC_RATIO  | 4    | 0x0     | Enables horizontal pre-downscaling for use when horizontal downscale ratio of P1 data is less than 2:1.<br>0=No predownscale, i.e. 1:1<br>1=Predownscale 2:1   |
| OV0_P23_H_STEP_BY      | 10:8 | 0x0     | P23 refers to the UV in YUV, and to RB in RGB32. It is not used in RGB15/16<br>0=PLANER UV STEP BY 1, 4TAP VBLEND<br>1=PLANER UV STEP BY 1, 2TAP VBLEND<br>2=PLANER UV STEP BY 2, 2TAP VBLEND<br>3=PLANER UV STEP BY 4, 2TAP VBLEND<br>4=PLANER UV STEP BY 8, 2TAP VBLEND<br>5=PLANER UV STEP BY 14/18, 2TAP VBLEND                                      |
| OV0_P23_PREDWNSC_RATIO | 12   | 0x0     | Enables horizontal pre-downscaling for use when horizontal downscale ratio of P23 data is less than 2:1. In modes where P23 data is already sub-sampled horizontally, this would only be used when the horizontal scale ratio goes below 4:1.<br>0=No predownscale, i.e. 1:1<br>1=Predownscale 2:1   |

**OV0\_STEP\_BY - RW - 32 bits - [MMReg:0x484]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

Horizontal scaling is performed via a combination of horizontal blending and horizontal decimation. There is a limit to how many source pixels the vertical scalers can provide to the horizontal scalers per output pixel. If H\_STEP\_BY is zero, then the vertical filters perform four tap vertical filtering. If H\_STEP\_BY is greater than zero, then the the vertical scalers reconfigure themselves so that they provide twice as many pixels per clock, but perform only linear two tap vertical filtering to generate those pixels. If H\_STEP\_BY is 2, then the vertical filters fetch only the pixels with and even X coordinate relative to the octword aligned surface base offset. If H\_STEP\_BY is 3, then every 4th pixel is fetched, etc. For ease of implementation reasons, at higher H\_STEP\_BY settings, the spacing between may not be an exact power of two. For example when H\_STEP\_BY is 4, the hardware may step by 7,9,7,9 rather than stepping by 8,8,8,8.

The code to program this field is provided in a function called CalcH.cpp

**OV0\_P1\_H\_ACCUM\_INIT - RW - 32 bits - [MMReg:0x488]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                     |       |     |  |
|---------------------|-------|-----|--|
| OV0_P1_H_ACCUM_INIT | 19:15 | 0x0 | Indicates the blend of source pixels you want in the four tap filter kernal to provide to generate the first display pixel. The ov0setup.cpp program shows how to calculate the correct value. |
|---------------------|-------|-----|--|

|                    |       |     |  |
|--------------------|-------|-----|--|
| OV0_PRESHIFT_P1_TO | 31:28 | 0x2 | Indicates how many source pixels you want to preshift into the horizontal Y four tap filter to generate the first display pixel. Please refer to the documentation for sample code on how to program this field. Typically this value is two or three. |
|--------------------|-------|-----|--|

This register is needed to accurately horizontally position the source video in the overlay display window, and also to accurately position it relative to the subtitle image.

**OV0\_P23\_H\_ACCUM\_INIT - RW - 32 bits - [MMReg:0x48C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                      |       |     |  |
|----------------------|-------|-----|--|
| OV0_P23_H_ACCUM_INIT | 19:15 | 0x0 | Indicates the blend of source pixels you want in the four tap filter kernal to provide to generate the first display pixel. The ov0setup.cpp program shows how to calculate the correct value. |
|----------------------|-------|-----|--|

|                     |       |     |   |
|---------------------|-------|-----|---|
| OV0_PRESHIFT_P23_TO | 30:28 | 0x2 | Indicates how many source pixels you want to preshift into the horizontal U and V four tap filters to generate the first display pixel. Please refer to the documentation for sample code on how to program this field. Typically this value is two or three. |
|---------------------|-------|-----|---|

Please refer to P1\_H\_ACCUM\_INIT. This register is used for the UV components in Planer modes.

**OV0\_P1\_X\_START\_END - RW - 32 bits - [MMReg:0x494]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|              |      |     |   |
|--------------|------|-----|---|
| OV0_P1_X_END | 11:0 | 0x0 | End pixel in an octword aligned line for Y, R, G, and B |
|--------------|------|-----|---|

|                |       |     |   |
|----------------|-------|-----|---|
| OV0_P1_X_START | 19:16 | 0x0 | Start pixel in an octword aligned line for Y, R, G, and B |
|----------------|-------|-----|---|

**OV0\_P1\_X\_START\_END - RW - 32 bits - [MMReg:0x494]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

Fields in the OV0\_VID\_BUF?\_BASE\_ADRS and OV0\_VID\_BUF\_PITCH?\_VALUE registers are used to determine the address of the start octword for each line. The P?\_X\_START\_END registers indicate more accurately where the lines start and ends relative to that first octword. The P?\_X\_START field indicates exactly which pixel in the first octword to start on. The P?\_X\_END field indicates which pixel to end on relative to pixel zero in the first octword. The hardware uses the P?\_X\_END and the SURFACE\_FORMAT fields to determine how many octwords to fetch.

This register allows pixel accurate windowing of the source surface which was not supported in earlier chips. It is now possible to zoom, pan (for DVD pan and scan), and clip the source.

Refer to ov0setup.cpp for sample code on how to program this register. You will notice the the CalcH.cpp routine returns values, P1StepSize and P23StepSize, that indicate the horizontal step when downscaling. These are used to insure that the start and end values are programmed correctly if pixel dropping occurs during horizontal downscaling.

P1 refers to Y, R, G, and B

**OV0\_P2\_X\_START\_END - RW - 32 bits - [MMReg:0x498]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|              |      |     |   |
|--------------|------|-----|---|
| OV0_P2_X_END | 10:0 | 0x0 | End pixel in an octword aligned line for U. |
|--------------|------|-----|---|

|                |       |     |  |
|----------------|-------|-----|--|
| OV0_P2_X_START | 19:16 | 0x0 | Start pixel in an octword aligned line for U |
|----------------|-------|-----|--|

See the P1 description. This register (and its fields) will be renamed OV0\_P23\_X\_START\_END in the near future.

P2 refers to Cb (U)

**OV0\_P3\_X\_START\_END - RW - 32 bits - [MMReg:0x49C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|              |      |     |   |
|--------------|------|-----|---|
| OV0_P3_X_END | 10:0 | 0x0 | End pixel in an octword aligned line for V (program to the same value as OV0_P2_X_END if this register still exists.) |
|--------------|------|-----|---|

|                |       |     |   |
|----------------|-------|-----|---|
| OV0_P3_X_START | 19:16 | 0x0 | Start pixel in an octword aligned line for V (program to the same value as OV0_P2_X_START if this register still exists.) |
|----------------|-------|-----|---|

See the P1 description. Note that you can no longer program the P2(U) and P3(V) start and end points to different values. To support planer surfaces where the U and V planes to share a pitch, make sure that the pitch is a multiple of two octwords. This register is now redundant and will be removed at the earliest opportunity.

P3 refers to Cr (U)

**OV0\_FILTER\_CNTL - RW - 32 bits - [MMReg:0x4A0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                       |   |     |   |
|-----------------------|---|-----|---|
| OV0_HC_COEF_ON_HORZ_Y | 0 | 0x0 | Selects the hard coded upscaling filter coefficients for scaling the Y component horizontally.<br>0=PROGRAMABLE<br>1=HARD CODED |
|-----------------------|---|-----|---|

|                        |   |     |  |
|------------------------|---|-----|--|
| OV0_HC_COEF_ON_HORZ_UV | 1 | 0x0 | Selects the hard coded upscaling filter coefficients for scaling the UV component horizontally.<br>0=PROGRAMABLE<br>1=HARD CODED |
|------------------------|---|-----|--|

|                       |   |     |   |
|-----------------------|---|-----|---|
| OV0_HC_COEF_ON_VERT_Y | 2 | 0x0 | Selects the hard coded upscaling filter coefficients for scaling the Y component vertically. Applies only if the vertical filter engine is performing four tap filtering on the Y.<br>0=PROGRAMABLE<br>1=HARD CODED |
|-----------------------|---|-----|---|

**OV0\_FILTER\_CNTL - RW - 32 bits - [MMReg:0x4A0]**

| Field Name             | Bits | Default | Description  |
|------------------------|------|---------|--|
| OV0_HC_COEF_ON_VERT_UV | 3    | 0x0     | Selects the hard coded upscaling filter coefficients for scaling the UV component vertically. Applies only if the vertical filter engine is performing four tap filtering on the UV.<br>0=PROGRAMMABLE<br>1=HARD CODED |

There are five four tap filters. It is expensive to provide each filter with it's own set of programmable coefficients, so there are hard coded coefficients suitable for upscaling built into the hardware. For example, if you have to use the programmable coefficients to specify a guassian curve for downscaling Y horizontally, but you still want to upsample the UV using the sharper upscaling truncated sync function, then use the hard coded coefficients for the horizontal UV.

**OV0\_FOUR\_TAP\_COEF\_0 - RW - 32 bits - [MMReg:0x4B0]**

| Field Name       | Bits  | Default | Description  |
|------------------|-------|---------|--|
| OV0_COEF_0TH_TAP | 3:0   | 0x0     | This filter coefficient is a four bit signed value in the range of -8 to +7. |
| OV0_COEF_1ST_TAP | 14:8  | 0x0     | This filter coefficient is a four bit signed value in the range - 8 to +47.  |
| OV0_COEF_2ND_TAP | 22:16 | 0x0     | This filter coefficient is a four bit signed value in the range - 8 to +47.  |
| OV0_COEF_3RD_TAP | 27:24 | 0x0     | This filter coefficient is a four bit signed value in the range of -8 to +7. |

Coefficients used for phase 0/8. 0TH\_TAP means the left most of top most pixel in a set of four will be multiplied by this coefficient.

**OV0\_FOUR\_TAP\_COEF\_1 - RW - 32 bits - [MMReg:0x4B4]**

| Field Name       | Bits  | Default | Description  |
|------------------|-------|---------|--|
| OV0_COEF_0TH_TAP | 3:0   | 0x0     | This filter coefficient is a four bit signed value in the range of -8 to +7. |
| OV0_COEF_1ST_TAP | 14:8  | 0x0     | This filter coefficient is a four bit signed value in the range - 8 to +47.  |
| OV0_COEF_2ND_TAP | 22:16 | 0x0     | This filter coefficient is a four bit signed value in the range - 8 to +47.  |
| OV0_COEF_3RD_TAP | 27:24 | 0x0     | This filter coefficient is a four bit signed value in the range of -8 to +7. |

Coefficients used for phase 1/8 and 5/8 when swapped. 0TH\_TAP means the left most of top most pixel in a set of four will be multiplied by this coefficient when the coefficients aren't swapped.

**OV0\_FOUR\_TAP\_COEF\_2 - RW - 32 bits - [MMReg:0x4B8]**

| Field Name       | Bits  | Default | Description  |
|------------------|-------|---------|--|
| OV0_COEF_0TH_TAP | 3:0   | 0x0     | This filter coefficient is a four bit signed value in the range of -8 to +7. |
| OV0_COEF_1ST_TAP | 14:8  | 0x0     | This filter coefficient is a four bit signed value in the range - 8 to +47.  |
| OV0_COEF_2ND_TAP | 22:16 | 0x0     | This filter coefficient is a four bit signed value in the range - 8 to +47.  |

**OV0\_FOUR\_TAP\_COEF\_2 - RW - 32 bits - [MMReg:0x4B8]**

| Field Name       | Bits  | Default | Description  |
|------------------|-------|---------|--|
| OV0_COEF_3RD_TAP | 27:24 | 0x0     | This filter coefficient is a four bit signed value in the range of -8 to +7. |

Coefficients used for phase 2/8 and 6/8 when swapped. 0TH\_TAP means the left most of top most pixel in a set of four will be multiplied by this coefficient when the coefficients aren't swapped.

**OV0\_FOUR\_TAP\_COEF\_3 - RW - 32 bits - [MMReg:0x4BC]**

| Field Name       | Bits  | Default | Description  |
|------------------|-------|---------|--|
| OV0_COEF_0TH_TAP | 3:0   | 0x0     | This filter coefficient is a four bit signed value in the range of -8 to +7. |
| OV0_COEF_1ST_TAP | 14:8  | 0x0     | This filter coefficient is a four bit signed value in the range -8 to +47.   |
| OV0_COEF_2ND_TAP | 22:16 | 0x0     | This filter coefficient is a four bit signed value in the range -8 to +47.   |
| OV0_COEF_3RD_TAP | 27:24 | 0x0     | This filter coefficient is a four bit signed value in the range of -8 to +7. |

Coefficients used for phase 3/8 and 7/8 when swapped. 0TH\_TAP means the left most of top most pixel in a set of four will be multiplied by this coefficient when the coefficients aren't swapped.

**OV0\_FOUR\_TAP\_COEF\_4 - RW - 32 bits - [MMReg:0x4C0]**

| Field Name       | Bits  | Default | Description  |
|------------------|-------|---------|--|
| OV0_COEF_0TH_TAP | 3:0   | 0x0     | This filter coefficient is a four bit signed value in the range of -8 to +7. |
| OV0_COEF_1ST_TAP | 14:8  | 0x0     | This filter coefficient is a four bit signed value in the range -8 to +47.   |
| OV0_COEF_2ND_TAP | 22:16 | 0x0     | This filter coefficient is a four bit signed value in the range -8 to +47.   |
| OV0_COEF_3RD_TAP | 27:24 | 0x0     | This filter coefficient is a four bit signed value in the range of -8 to +7. |

Coefficients used for phase 4/8. 0TH\_TAP means the left most of top most pixel in a set of four will be multiplied by this coefficient.

**OV0\_FLAG\_CNTRL - RW - 32 bits - [MMReg:0x4DC]**

| Field Name          | Bits | Default | Description   |
|---------------------|------|---------|---|
| OV0_HI_PRI_MCREQ    | 3:0  | 0x8     |   |
| OV0_HI_PRI_FORCE    | 8    | 0x0     | 0=NO FORCE<br>1=FORCE   |
| OV0_LUMA_10BIT_EN   | 12   | 0x0     | 0=H filter produces 8 bits for luma<br>1=H filter produces 10 bits for luma     |
| OV0_CHROMA_10BIT_EN | 13   | 0x0     | 0=H filter produces 8 bits for chroma<br>1=H filter produces 10 bits for chroma |

No description available for this register.

**OV0\_SLICE\_CNTL - RW - 32 bits - [MMReg:0x4E0]**

| Field Name          | Bits | Default | Description |
|---------------------|------|---------|-------------|
| OV0_SLICE_LAST_LINE | 6:0  | 0x0     |             |

**OV0\_SLICE\_CNTL - RW - 32 bits - [MMReg:0x4E0]**

| Field Name             | Bits | Default | Description                                |
|------------------------|------|---------|--|
| OV0_SLICEDONE_STAT (R) | 30   | 0x0     | 0=Not done with slice.<br>1=Slice is done. |
| OV0_MPEG_EOF_TOGGLE    | 31   | 0x0     |  |

No description available for this register.

**OV0\_VID\_KEY\_CLR\_LOW - RW - 32 bits - [MMReg:0x4E4]**

| Field Name              | Bits  | Default | Description  |
|-------------------------|-------|---------|--|
| OV0_VID_KEY_Cb_BLUE_LOW | 9:0   | 0x0     | Overlay/subpicture keyer Cb or blue component lower limit. |
| OV0_VID_KEY_Y_GREEN_LOW | 19:10 | 0x0     | Overlay/subpicture keyer Y or green component lower limit. |
| OV0_VID_KEY_Cr_RED_LOW  | 29:20 | 0x0     | Overlay/subpicture keyer Cr or red component lower limit.  |

Overlay/subpicture range keyer lower limits. The overlay/subpicture blend unit output where keying is done is 30bpp. This is the data before color conversion or gamma adjustment.

**OV0\_VID\_KEY\_CLR\_HIGH - RW - 32 bits - [MMReg:0x4E8]**

| Field Name               | Bits  | Default | Description  |
|--------------------------|-------|---------|--|
| OV0_VID_KEY_Cb_BLUE_HIGH | 9:0   | 0x0     | Overlay/subpicture keyer Cb or blue component upper limit. |
| OV0_VID_KEY_Y_GREEN_HIGH | 19:10 | 0x0     | Overlay/subpicture keyer Y or green component upper limit. |
| OV0_VID_KEY_Cr_RED_HIGH  | 29:20 | 0x0     | Overlay/subpicture keyer Cr or red component upper limit.  |

Overlay/subpicture range keyer upper limits. The overlay/subpicture blend unit output where keying is done is 30bpp. This is the data before color conversion or gamma adjustment.

**OV0\_GRP\_KEY\_CLR\_LOW - RW - 32 bits - [MMReg:0x4EC]**

| Field Name            | Bits  | Default | Description                                 |
|-----------------------|-------|---------|---|
| OV0_GRP_KEY_BLUE_LOW  | 7:0   | 0x0     | Graphics keyer blue component lower limit.  |
| OV0_GRP_KEY_GREEN_LOW | 15:8  | 0x0     | Graphics keyer green component lower limit. |
| OV0_GRP_KEY_RED_LOW   | 23:16 | 0x0     | Graphics keyer red component lower limit.   |
| OV0_GRP_KEY_ALPHA_LOW | 31:24 | 0x0     | Graphics keyer alpha component lower limit. |

Graphics range keyer lower limits. Note in some modes expansion is needed to create an 8 bit red, green, blue or alpha from the 4, 5, or 6 bits stored in the frame buffer. This is controlled by DAC\_CNTL.DAC\_EXPAND\_MODE. Graphics keying is always done on 8 bit post-expanded data. For pixel depths that do not have alpha, set the ALPHA\_LOW to 0x00. To key on only the alpha channel in 15 or 32 bpp, set the color lower limits to 0x00.

**OV0\_GRP\_KEY\_CLR\_HIGH - RW - 32 bits - [MMReg:0x4F0]**

| Field Name             | Bits  | Default | Description                                 |
|------------------------|-------|---------|---|
| OV0_GRP_KEY_BLUE_HIGH  | 7:0   | 0x0     | Graphics keyer blue component upper limit.  |
| OV0_GRP_KEY_GREEN_HIGH | 15:8  | 0x0     | Graphics keyer green component upper limit. |
| OV0_GRP_KEY_RED_HIGH   | 23:16 | 0x0     | Graphics keyer red component upper limit.   |
| OV0_GRP_KEY_ALPHA_HIGH | 31:24 | 0x0     | Graphics keyer alpha component upper limit. |

**OV0\_GRP\_KEY\_CLR\_HIGH - RW - 32 bits - [MMReg:0x4F0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

Graphics range keyer upper limits. Note in some modes expansion is needed to create an 8 bit red, green, blue or alpha from the 4, 5, or 6 bits stored in the frame buffer. This is controlled by DAC\_CNTL.DAC\_EXPAND\_MODE. Graphics keying is always done on 8 bit post-expanded data. For pixel depths that do not have alpha, set the ALPHA\_HIGH to 0xFF. To key on only the alpha channel in 15 or 32 bpp, set the color high limits to 0xFF.

**OV0\_KEY\_CNTL - RW - 32 bits - [MMReg:0x4F4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                     |     |     |  |
|---------------------|-----|-----|--|
| OV0_VIDEO_KEY_FN    | 1:0 | 0x0 | Selects overlay keyer result equation. Result used as stated in OV0_CMP_MIX.<br>0=VID_KEY = FALSE = 0<br>1=VID_KEY = TRUE = 1<br>2=VID_KEY = (VID_Cr_BLUE in range) AND (VID_Cb_GREEN in range) AND (VID_Y_RED in range)<br>3=VID_KEY = not [(VID_Cr_BLUE in range) AND (VID_Cb_GREEN in range) AND (VID_Y_RED in range)]  |
| OV0_GRAPHICS_KEY_FN | 5:4 | 0x0 | Selects graphics keyer result equation. Result used as stated in OV0_CMP_MIX.<br>0=GRPH_KEY = FALSE = 0<br>1=GRPH_KEY = TRUE = 1<br>2=GPPH_KEY = (GRPH_BLUE in range) AND (GRPH_GREEN in range) AND (GRPH_RED in range) AND (GRPH_ALPHA in range)<br>3=GRPH_KEY = not [(GRPH_BLUE in range) AND (GRPH_GREEN in range) AND (GRPH_RED in range) AND (GRPH_ALPHA in range)] |
| OV0_CMP_MIX         | 8   | 0x0 | Selects final mix of graphics and video keys. Result used as stated in DISP_MERGE_CNTL.DISP_ALPHA_MODE.<br>0=GRPH_VID_KEY = GRPH_KEY or VID_KEY<br>1=GRPH_VID_KEY = GRPH_KEY and VID_KEY   |

Graphics/overlay keyer control

**OV0\_TEST - RW - 32 bits - [MMReg:0x4F8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                             |       |     |  |
|-----------------------------|-------|-----|--|
| OV0_MIN_OFFSET_EN           | 1     | 0x0 |  |
| OV0_SUBPIC_ONLY             | 3     | 0x0 | Forces the subpicture data on.<br>0=NORMAL<br>1=PURE SUBPICTURE DATA   |
| OV0_SWAP_UV                 | 5     | 0x0 | This field will swap the U and V components (and also the R and B components in RGB modes).<br>0=NO SWAP<br>1=SWAP |
| OV0_NOROUNDUP               | 6     | 0x0 | 0=ROUND UP HORZ & VERT FIR<br>1=DO NOT ROUND UP HORZ & VERT FIR  |
| OV0_ADAPTIVE_DEINT_ADJ      | 13:12 | 0x0 |  |
| OV0_READ_BEHIND_SCAN_MARGIN | 22:16 | 0x0 |  |

Test registers for the scaler.

**OV0\_LIN\_TRANS\_A - RW - 32 bits - [MMReg:0xD20]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                    |      |     |  |
|--------------------|------|-----|--|
| OV0_LIN_TRANS_Cb_R | 15:4 | 0x0 | Overlay linear transform unit coefficient for Cb of R. Format S3.8 (-8.00...+7.99) |
|--------------------|------|-----|--|

**OVO\_LIN\_TRANS\_A - RW - 32 bits - [MMReg:0xD20]**

| Field Name        | Bits  | Default | Description  |
|-------------------|-------|---------|--|
| OVO_LIN_TRANS_Y_R | 31:20 | 0x12a   | Overlay linear transform unit coefficient for Y of R. Format S3.8 (-8.00..+7.99) |

Overlay linear transform unit coefficient group A

**OVO\_LIN\_TRANS\_B - RW - 32 bits - [MMReg:0xD24]**

| Field Name          | Bits  | Default | Description  |
|---------------------|-------|---------|--|
| OVO_LIN_TRANS_OFF_R | 12:0  | 0x190e  | Overlay linear transform unit coefficient offset of R. Format S11.1 (-2048.0..+2047.5) |
| OVO_LIN_TRANS_Cr_R  | 31:20 | 0x199   | Overlay linear transform unit coefficient for Cr of R. Format S3.8 (-8.00..+7.99)      |

Overlay linear transform unit coefficient group B

**OVO\_LIN\_TRANS\_C - RW - 32 bits - [MMReg:0xD28]**

| Field Name         | Bits  | Default | Description   |
|--------------------|-------|---------|---|
| OVO_LIN_TRANS_Cb_G | 15:4  | 0xf9c   | Overlay linear transform unit coefficient for Cb of G. Format S3.8 (-8.00..+7.99) |
| OVO_LIN_TRANS_Y_G  | 31:20 | 0x12a   | Overlay linear transform unit coefficient for Y of G. Format S3.8 (-8.00..+7.99)  |

Overlay linear transform unit coefficient group C

**OVO\_LIN\_TRANS\_D - RW - 32 bits - [MMReg:0xD2C]**

| Field Name          | Bits  | Default | Description  |
|---------------------|-------|---------|--|
| OVO_LIN_TRANS_OFF_G | 12:0  | 0x442   | Overlay linear transform unit coefficient offset of G. Format S11.1 (-2048.0..+2047.5) |
| OVO_LIN_TRANS_Cr_G  | 31:20 | 0xf30   | Overlay linear transform unit coefficient for Cr of G. Format S3.8 (-8.00..+7.99)      |

Overlay linear transform unit coefficient group D

**OVO\_LIN\_TRANS\_E - RW - 32 bits - [MMReg:0xD30]**

| Field Name         | Bits  | Default | Description   |
|--------------------|-------|---------|---|
| OVO_LIN_TRANS_Cb_B | 15:4  | 0x204   | Overlay linear transform unit coefficient for Cb of B. Format S3.8 (-8.00..+7.99) |
| OVO_LIN_TRANS_Y_B  | 31:20 | 0x12a   | Overlay linear transform unit coefficient for Y of B. Format S3.8 (-8.00..+7.99)  |

Overlay linear transform unit coefficient group E

**OVO\_LIN\_TRANS\_F - RW - 32 bits - [MMReg:0xD34]**

| Field Name          | Bits  | Default | Description  |
|---------------------|-------|---------|--|
| OVO_LIN_TRANS_OFF_B | 12:0  | 0x175f  | Overlay linear transform unit coefficient offset of B. Format S11.1 (-2048.0..+2047.5) |
| OVO_LIN_TRANS_Cr_B  | 31:20 | 0x0     | Overlay linear transform unit coefficient for Cr of B. Format S3.8 (-8.00..+7.99)      |

Overlay linear transform unit coefficient group F

**OV0\_GAMMA\_0\_F - RW - 32 bits - [MMReg:0xD40]**

| Field Name           | Bits  | Default | Description  |
|----------------------|-------|---------|--|
| OV0_GAMMA_0_F_OFFSET | 8:0   | 0x0     | Overlay gamma correction non-linear offset for input 0-F. Format 8.1 (0.0..+255.5) |
| OV0_GAMMA_0_F_SLOPE  | 26:16 | 0x100   | Overlay gamma correction non-linear slope for input 0-F. Format 3.8 (0.00..+7.99)  |

Overlay gamma correction non-linear offset and slope for input 0-F

**OV0\_GAMMA\_10\_1F - RW - 32 bits - [MMReg:0xD44]**

| Field Name             | Bits  | Default | Description  |
|------------------------|-------|---------|--|
| OV0_GAMMA_10_1F_OFFSET | 8:0   | 0x20    | Overlay gamma correction non-linear offset for input 10-1F. Format 8.1 (0.0..+255.5) |
| OV0_GAMMA_10_1F_SLOPE  | 26:16 | 0x100   | Overlay gamma correction non-linear slope for input 10-1F. Format 3.8 (0.00..+7.99)  |

Overlay gamma correction non-linear offset and slope for input 10-1F

**OV0\_GAMMA\_20\_3F - RW - 32 bits - [MMReg:0xD48]**

| Field Name             | Bits  | Default | Description  |
|------------------------|-------|---------|--|
| OV0_GAMMA_20_3F_OFFSET | 9:0   | 0x40    | Overlay gamma correction non-linear offset for input 20-3F. Format 9.1 (0.0..+511.5) |
| OV0_GAMMA_20_3F_SLOPE  | 25:16 | 0x100   | Overlay gamma correction non-linear slope for input 20-3F. Format 2.8 (0.00..+3.99)  |

Overlay gamma correction non-linear offset and slope for input 20-3F

**OV0\_GAMMA\_40\_7F - RW - 32 bits - [MMReg:0xD4C]**

| Field Name             | Bits  | Default | Description  |
|------------------------|-------|---------|--|
| OV0_GAMMA_40_7F_OFFSET | 9:0   | 0x80    | Overlay gamma correction non-linear offset for input 40-7F. Format 9.1 (0.0..+511.5) |
| OV0_GAMMA_40_7F_SLOPE  | 24:16 | 0x100   | Overlay gamma correction non-linear slope for input 40-7F. Format 1.8 (0.00..+1.99)  |

Overlay gamma correction non-linear offset and slope for input 40-7F

**OV0\_GAMMA\_380\_3BF - RW - 32 bits - [MMReg:0xD50]**

| Field Name               | Bits  | Default | Description  |
|--------------------------|-------|---------|--|
| OV0_GAMMA_380_3BF_OFFSET | 8:0   | 0x100   | Overlay gamma correction non-linear offset for input 380-3BF. Format 8.1 + 0x300 integer added by HW (+768.0..+1023.5) |
| OV0_GAMMA_380_3BF_SLOPE  | 24:16 | 0x100   | Overlay gamma correction non-linear slope for input 380-3BF. Format 1.8 (0.00..+1.99)                                  |

Overlay gamma correction non-linear offset and slope for input 380-3BF

**OV0\_GAMMA\_3C0\_3FF - RW - 32 bits - [MMReg:0xD54]**

| Field Name               | Bits | Default | Description  |
|--------------------------|------|---------|--|
| OV0_GAMMA_3C0_3FF_OFFSET | 8:0  | 0x100   | Overlay gamma correction non-linear offset for input 3C0-3FF. Format 8.1 + 0x300 integer added by HW (+768.0..+1023.5) |



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**OV0\_GAMMA\_3C0\_3FF - RW - 32 bits - [MMReg:0xD54]**

| Field Name              | Bits  | Default | Description   |
|-------------------------|-------|---------|---|
| OV0_GAMMA_3C0_3FF_SLOPE | 24:16 | 0x100   | Overlay gamma correction non-linear slope for input 3C0-3FF. Format 1.8 (0.00..+1.99) |

Overlay gamma correction non-linear offset and slope for input 3C0-3FF

**OV1\_Y\_X\_START - RW - 32 bits - [MMReg:0x600]**

| Field Name  | Bits  | Default | Description   |
|-------------|-------|---------|---|
| OV1_X_START | 12:0  | 0x0     | Overlay X ending coordinate relative to secondary ACTIVE screen (0,0) |
| OV1_Y_START | 28:16 | 0x0     | Overlay Y ending coordinate relative to secondary ACTIVE screen (0,0) |

X/Y coords relative to active secondary display in pixels

**OV1\_Y\_X\_END - RW - 32 bits - [MMReg:0x604]**

| Field Name | Bits  | Default | Description   |
|------------|-------|---------|---|
| OV1_X_END  | 12:0  | 0x0     | Overlay X ending coordinate relative to secondary ACTIVE screen (0,0) |
| OV1_Y_END  | 28:16 | 0x0     | Overlay X ending coordinate relative to secondary ACTIVE screen (0,0) |

X/Y ending coordinates (inclusive) relative to secondary active display in pixels

**OV1\_PIPELINE\_CNTL - RW - 32 bits - [MMReg:0x608]**

| Field Name          | Bits | Default | Description   |
|---------------------|------|---------|---|
| OV1_DISP_PIPE_DELAY | 3:0  | 0x8     | Secondary display debug field used to adjust overlay window position. Leave at default unless hardware problem requires adjustment as instructed. |

Secondary display debug adjustments for overlay window control

**22. cursor Detailed Register Reference**

## Cursor

| CUR_OFFSET - RW - 32 bits - [MMReg:0x260] |      |         |  |
|---|------|---------|--|
| Field Name                                | Bits | Default | Description  |
| CUR_OFFSET                                | 26:0 | 0x0     | Hardware cursor address offset.<br>For monochrome cursors (CRTC_CUR_MODE = 00), this value must be a 16 byte aligned address. For color cursor modes it must be a 256 byte aligned address.<br>The CUR_OFFSET is relative to the DISP_BASE_ADDRESS, meaning the active display pointed to by CRTC_OFFSET and the cursor must be in the same region of memory.<br>This value is adjusted to move the cursor off the top edge of the display. See the CUR_VERT_OFF description.<br><br>NOTE: Bits 0:3 of this field are hardwired to ZERO. |
| CUR_LOCK                                  | 31   | 0x0     | Locks the HWC_EN, CUR_OFFSET, CUR_HORZ_VERT_POSN and CUR_HORZ_VERT_OFF registers to allow tear free atomic updating of the cursor shape and/or position.<br>Moving the cursor around on the top and/or left edges, or changing the shape, requires multiple register writes. If these were done without setting CUR_LOCK, then flicker could occur.<br>0=Unlocked<br>1=Locked  |

Location of the hardware cursor image.

| CUR_HORZ_VERT_POSN - RW - 32 bits - [MMReg:0x264]  |       |         |   |
|--|-------|---------|---|
| Field Name   | Bits  | Default | Description   |
| CUR_VERT_POSN                                      | 11:0  | 0x0     | Cursor vertical position.<br>To move the cursor off the top edge set CUR_VERT_POSN=0 and see the CUR_VERT_OFF description.<br>When CRTC_GEN_CNTL.CRTC_DBL_SCAN_EN=1 the logical position from the OS must be converted to a physical position to program here by multiplying by 2. i.e. no odd values should be used in double scan mode.                                     |
| CUR_HORZ_POSN                                      | 29:16 | 0x0     | Cursor horizontal position. To move the cursor off the left edge set CUR_HORZ_POSN=0 and see the CUR_HORZ_OFF description.  |
| CUR_LOCK<br><i>(mirror of CUR_OFFSET:CUR_LOCK)</i> | 31    | 0x0     | Locks the HWC_EN, CUR_OFFSET, CUR_HORZ_VERT_POSN and CUR_HORZ_VERT_OFF registers to allow tear free atomic updating of the cursor shape and/or position.<br>Moving the cursor around on the top and/or left edges, or changing the shape, requires multiple register writes. If these were done without setting CUR_LOCK, then flicker could occur.<br>0=Unlocked<br>1=Locked |

Sets the screen position of the top left pixel of the visible part of the hardware cursor.

| CUR_HORZ_VERT_OFF - RW - 32 bits - [MMReg:0x268] |      |         |             |
|--|------|---------|-------------|
| Field Name                                       | Bits | Default | Description |

**CUR\_HORZ\_VERT\_OFF - RW - 32 bits - [MMReg:0x268]**

| Field Name   | Bits  | Default | Description  |
|--|-------|---------|--|
| CUR_VERT_OFF                                       | 5:0   | 0x0     | Cursor vertical offset. Height of cursor is (64-CUR_VERT_OFF).<br>To move the cursor off the top of the display, set CUR_VERT_POSN to 0, add 16*(number of lines to move off the top) to CUR_OFFSET, and increase CUR_VERT_OFF by the same number of lines.<br>When is double scan display (CRTC_DBL_SCAN_EN=1) the height of the cursor is limited to 32 logical lines, but 64 physical lines. i.e. the image in memory can be up to 32 lines high, but will cover 64 physical lines of the display.<br>Also in double scan mode the height of the cursor must be even in physical lines. i.e. this field must be even. |
| CUR_HORZ_OFF                                       | 21:16 | 0x0     | Cursor horizontal offset. Width of the cursor is always 64 pixels. CUR_HORZ_OFF controls how far into the cursor map from the left is 'pixel 0'.<br>The horizontal position on the display of 'pixel 0' is set by CUR_HORZ_POSN. Therefore to move the cursor off the left edge of the display, set the CUR_HORZ_POSN to zero, and increase the CUR_HORZ_OFF by the number of pixels off the left edge.  |
| CUR_LOCK<br><i>(mirror of CUR_OFFSET:CUR_LOCK)</i> | 31    | 0x0     | Locks the HWC_EN, CUR_OFFSET, CUR_HORZ_VERT_POSN and CUR_HORZ_VERT_OFF registers to allow tear free atomic updating of the cursor shape and/or position.<br>Moving<br>0=Unlocked<br>1=Locked   |

Controls the size of the hardware cursor mask in memory, and used to move the cursor off the top and/or left edges of the display.

**CUR\_CLR0 - RW - 32 bits - [MMReg:0x26C]**

| Field Name | Bits  | Default | Description                        |
|------------|-------|---------|------------------------------------|
| CUR_CLR0_B | 7:0   | 0x0     | Blue component of cursor color 0.  |
| CUR_CLR0_G | 15:8  | 0x0     | Green component of cursor color 0. |
| CUR_CLR0_R | 23:16 | 0x0     | Red component of cursor color 0.   |

Hardware cursor color 0. Always 24bpp, independent of graphics mode.  
For monochrome cursor only.

**CUR\_CLR1 - RW - 32 bits - [MMReg:0x270]**

| Field Name | Bits  | Default | Description                        |
|------------|-------|---------|------------------------------------|
| CUR_CLR1_B | 7:0   | 0x0     | Blue component of cursor color 1.  |
| CUR_CLR1_G | 15:8  | 0x0     | Green component of cursor color 1. |
| CUR_CLR1_R | 23:16 | 0x0     | Red component of cursor color 1.   |

Hardware cursor color 1. Always 24bpp, independent of graphics mode.  
For monochrome cursor only.

**CUR2\_OFFSET - RW - 32 bits - [MMReg:0x360]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**CUR2\_OFFSET - RW - 32 bits - [MMReg:0x360]**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| CUR2_OFFSET | 26:0 | 0x0     | Hardware cursor address offset.<br>For monochrome cursors (CRTC2_CUR_MODE = 00), this value must be a 16 byte aligned address. For color cursor modes it must be a 256 byte aligned address.<br>The CUR_OFFSET is relative to the DISP_BASE_ADDRESS, meaning the active display pointed to by CRTC2_OFFSET and the cursor must be in the same region of memory.<br>This value is adjusted to move the cursor off the top edge of the display. See the CUR_VERT_OFF description.<br><br>NOTE: Bits 0:3 of this field are hardwired to ZERO. |
| CUR2_LOCK   | 31   | 0x0     | Locks the HWC_EN, CUR_OFFSET, CUR_HORZ_VERT_POSN and CUR_HORZ_VERT_OFF registers to allow tear free atomic updating of the cursor shape and/or position.<br>Moving the cursor around on the top and/or left edges, or changing the shape, requires multiple register writes. If these were done without setting CUR_LOCK, then flicker could occur.<br>0=Unlocked<br>1=Locked  |

Location of the secondary hardware cursor image.

**CUR2\_HORZ\_VERT\_POSN - RW - 32 bits - [MMReg:0x364]**

| Field Name  | Bits  | Default | Description   |
|---|-------|---------|---|
| CUR2_VERT_POSN  | 11:0  | 0x0     | Cursor vertical position.<br>To move the cursor off the top edge set CUR_VERT_POSN=0 and see the CUR_VERT_OFF description.<br>When CRTC2_GEN_CNTL.CRTC2_DBL_SCAN_EN=1 the logical position from the OS must be converted to a physical position to program here by multiplying by 2. i.e. no odd values should be used in double scan mode.                                   |
| CUR2_HORZ_POSN  | 29:16 | 0x0     | Cursor horizontal position. To move the cursor off the left edge set CUR_HORZ_POSN=0 and see the CUR_HORZ_OFF description.  |
| CUR2_LOCK<br><i>(mirror of CUR2_OFFSET:CUR2_LOCK)</i> | 31    | 0x0     | Locks the HWC_EN, CUR_OFFSET, CUR_HORZ_VERT_POSN and CUR_HORZ_VERT_OFF registers to allow tear free atomic updating of the cursor shape and/or position.<br>Moving the cursor around on the top and/or left edges, or changing the shape, requires multiple register writes. If these were done without setting CUR_LOCK, then flicker could occur.<br>0=Unlocked<br>1=Locked |

Sets the screen position of the top left pixel of the visible part of the secondary hardware cursor.

**CUR2\_HORZ\_VERT\_OFF - RW - 32 bits - [MMReg:0x368]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**CUR2\_HORZ\_VERT\_OFF - RW - 32 bits - [MMReg:0x368]**

| Field Name  | Bits  | Default | Description   |
|---|-------|---------|---|
| CUR2_VERT_OFF   | 5:0   | 0x0     | Cursor vertical offset. Height of cursor is (64-CUR_VERT_OFF).<br>To move the cursor off the top of the display, set CUR_VERT_POSN to 0, add 16*(number of lines to move off the top) to CUR_OFFSET, and increase CUR_VERT_OFF by the same number of lines.<br>When is double scan display (CRTC2_DBL_SCAN_EN=1) the height of the cursor is limited to 32 logical lines, but 64 physical lines. i.e. the image in memory can be up to 32 lines high, but will cover 64 physical lines of the display.<br>Also in double scan mode the height of the cursor must be even in physical lines. i.e. this field must be even. |
| CUR2_HORZ_OFF   | 21:16 | 0x0     | Cursor horizontal offset. Width of the cursor is always 64 pixels. CUR_HORZ_OFF controls how far into the cursor map from the left is 'pixel 0'.<br>The horizontal position on the display of 'pixel 0' is set by CUR_HORZ_POSN. Therefore to move the cursor off the left edge of the display, set the CUR_HORZ_POSN to zero, and increase the CUR_HORZ_OFF by the number of pixels off the left edge.   |
| CUR2_LOCK<br><i>(mirror of CUR2_OFFSET:CUR2_LOCK)</i> | 31    | 0x0     | Locks the HWC_EN, CUR_OFFSET, CUR_HORZ_VERT_POSN and CUR_HORZ_VERT_OFF registers to allow tear free atomic updating of the cursor shape and/or position.<br>Moving<br>0=Unlocked<br>1=Locked  |

Controls the size of the secondary hardware cursor mask in memory, and used to move the cursor off the top and/or left edges of the display.

**CUR2\_CLR0 - RW - 32 bits - [MMReg:0x36C]**

| Field Name  | Bits  | Default | Description                        |
|-------------|-------|---------|------------------------------------|
| CUR2_CLR0_B | 7:0   | 0x0     | Blue component of cursor color 0.  |
| CUR2_CLR0_G | 15:8  | 0x0     | Green component of cursor color 0. |
| CUR2_CLR0_R | 23:16 | 0x0     | Red component of cursor color 0.   |

Location of the secondary hardware cursor image.

**CUR2\_CLR1 - RW - 32 bits - [MMReg:0x370]**

| Field Name  | Bits  | Default | Description                        |
|-------------|-------|---------|------------------------------------|
| CUR2_CLR1_B | 7:0   | 0x0     | Blue component of cursor color 1.  |
| CUR2_CLR1_G | 15:8  | 0x0     | Green component of cursor color 1. |
| CUR2_CLR1_R | 23:16 | 0x0     | Red component of cursor color 1.   |

Hardware cursor color 1. Always 24bpp, independent of graphics mode.  
For monochrome cursor only.

**23. overscan Detailed Register Reference**

## Overscan

**OVR2\_CLR - RW - 32 bits - [MMReg:0x330]**

| Field Name | Bits  | Default | Description                      |
|------------|-------|---------|----------------------------------|
| OVR2_CLR_B | 7:0   | 0x0     | Blue component overscan colour.  |
| OVR2_CLR_G | 15:8  | 0x0     | Green component overscan colour. |
| OVR2_CLR_R | 23:16 | 0x0     | Red component overscan colour.   |

Secondary display Overscan color. Always 24 bit, independent of pixel depth.

**OVR2\_WID\_LEFT\_RIGHT - RW - 32 bits - [MMReg:0x334]**

| Field Name     | Bits  | Default | Description                           |
|----------------|-------|---------|---------------------------------------|
| OVR2_WID_RIGHT | 6:0   | 0x0     | Right overscan width (in pixels * 8). |
| OVR2_WID_LEFT  | 22:16 | 0x0     | Left overscan width (in pixels * 8).  |

Secondary display Overscan border left/right width control.

**OVR2\_WID\_TOP\_BOTTOM - RW - 32 bits - [MMReg:0x338]**

| Field Name      | Bits  | Default | Description                            |
|-----------------|-------|---------|--|
| OVR2_WID_BOTTOM | 9:0   | 0x0     | Bottom overscan width (in scan lines). |
| OVR2_WID_TOP    | 25:16 | 0x0     | Top overscan width (in scan lines).    |

Secondary display Overscan border top/bottom width control.

**OVR\_CLR - RW - 32 bits - [MMReg:0x230]**

| Field Name | Bits  | Default | Description                      |
|------------|-------|---------|----------------------------------|
| OVR_CLR_B  | 7:0   | 0x0     | Blue component overscan colour.  |
| OVR_CLR_G  | 15:8  | 0x0     | Green component overscan colour. |
| OVR_CLR_R  | 23:16 | 0x0     | Red component overscan colour.   |

Overscan color. Always 24 bit, independent of pixel depth.

**OVR\_WID\_LEFT\_RIGHT - RW - 32 bits - [MMReg:0x234]**

| Field Name    | Bits  | Default | Description                           |
|---------------|-------|---------|---------------------------------------|
| OVR_WID_RIGHT | 6:0   | 0x0     | Right overscan width (in pixels * 8). |
| OVR_WID_LEFT  | 22:16 | 0x0     | Left overscan width (in pixels * 8).  |

Overscan border left/right width control.

**OVR\_WID\_TOP\_BOTTOM - RW - 32 bits - [MMReg:0x238]**

| Field Name     | Bits  | Default | Description                            |
|----------------|-------|---------|--|
| OVR_WID_BOTTOM | 9:0   | 0x0     | Bottom overscan width (in scan lines). |
| OVR_WID_TOP    | 25:16 | 0x0     | Top overscan width (in scan lines).    |

Overscan border top/bottom width control.



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**24. hwicon Detailed Register Reference**

Hardware icon

| ICON_OFFSET - RW - 32 bits - [MMReg:0x2B0] |      |         |   |
|--|------|---------|---|
| Field Name                                 | Bits | Default | Description   |
| ICON_OFFSET                                | 26:0 | 0x0     | Primary display hardware icon origin offset in memory. Must be 8 byte aligned for 4bpp, 8bpp and 24bpp modes. Must be 16 byte aligned for all 16bpp modes. Must be 32 byte aligned for 32bpp mode. When CRTC_STEREO_OFFSET_EN = 1, this is the left eye image. This is added to DISP_BASE_ADDR to get the full 32 bit address of the graphics surface.<br><br>NOTE: Bits 0:4 of this field are hardwired to ZERO. |
| BLANK_SCREEN1                              | 27   | 0x0     | Blank screen except for ICON on primary display<br>0=Normal<br>1=Blank Screen Except for Icon on primary display  |
| DONT_DS_ICON                               | 28   | 0x0     | Double scan primary hardware icon<br>0=Expand icon in double scan mode<br>1=Do not expand icon in double scan mode  |
| ICON_LOCK                                  | 31   | 0x0     | 0=Unlocked<br>1=Locked  |

Location of primary display hardware icon image

| ICON_HORZ_VERT_POSN - RW - 32 bits - [MMReg:0x2B4] |       |         |  |
|--|-------|---------|--|
| Field Name   | Bits  | Default | Description  |
| ICON_VERT_POSN                                     | 11:0  | 0x0     | Icon vertical position   |
| ICON_HORZ_POSN                                     | 27:16 | 0x0     | Icon horizontal position   |
| ICON_LOCK  | 31    | 0x0     | 0=Unlocked<br>1=Locked<br><br><i>(mirror of ICON_OFFSET:ICON_LOCK)</i> |

Primary display hardware icon horizontal and vertical positions

| ICON_HORZ_VERT_OFF - RW - 32 bits - [MMReg:0x2B8] |       |         |  |
|---|-------|---------|--|
| Field Name  | Bits  | Default | Description  |
| ICON_VERT_OFF                                     | 6:0   | 0x0     | Icon vertical offset   |
| ICON_HORZ_OFF                                     | 22:16 | 0x0     | Icon horizontal offset   |
| ICON_LOCK   | 31    | 0x0     | 0=Unlocked<br>1=Locked<br><br><i>(mirror of ICON_OFFSET:ICON_LOCK)</i> |

Primary display hardware icon horizontal and vertical offsets

| ICON_CLR0 - RW - 32 bits - [MMReg:0x2BC] |       |         |                                      |
|--|-------|---------|--------------------------------------|
| Field Name                               | Bits  | Default | Description                          |
| ICON_CLR0_B                              | 7:0   | 0x0     | Primary hardware icon blue colour 0  |
| ICON_CLR0_G                              | 15:8  | 0x0     | Primary hardware icon green colour 0 |
| ICON_CLR0_R                              | 23:16 | 0x0     | Primary hardware icon red colour 0   |

**ICON\_CLR0 - RW - 32 bits - [MMReg:0x2BC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

Primary hardware icon colour 0 register

**ICON\_CLR1 - RW - 32 bits - [MMReg:0x2C0]**

| Field Name  | Bits  | Default | Description                          |
|-------------|-------|---------|--------------------------------------|
| ICON_CLR1_B | 7:0   | 0x0     | Primary hardware icon blue colour 1  |
| ICON_CLR1_G | 15:8  | 0x0     | Primary hardware icon green colour 1 |
| ICON_CLR1_R | 23:16 | 0x0     | Primary hardware icon red colour 1   |

Primary hardware icon colour 1 register

**ICON2\_OFFSET - RW - 32 bits - [MMReg:0x3B0]**

| Field Name    | Bits | Default | Description   |
|---------------|------|---------|---|
| ICON2_OFFSET  | 26:0 | 0x0     | Secondary display hardware icon origin offset in memory. Must be 8 byte aligned for 4bpp, 8bpp and 24bpp modes. Must be 16 byte aligned for all 16bpp modes. Must be 32 byte aligned for 32bpp mode. This is added to DISP_BASE_ADDR to get the full 32 bit address of the graphics surface.<br><br>NOTE: Bits 0:4 of this field are hardwired to ZERO. |
| BLANK_SCREEN2 | 27   | 0x0     | Blank screen except for ICON on secondary display<br>0=Normal<br>1=Blank Screen Except for Icon on secondary display  |
| DONT_DS_ICON2 | 28   | 0x0     | Double scan secondary hardware icon<br>0=Expand icon in double scan mode<br>1=Do not expand icon in double scan mode  |
| ICON2_LOCK    | 31   | 0x0     | 0=Unlocked<br>1=Locked  |

Location of secondary display hardware icon image

**ICON2\_HORZ\_VERT\_POSN - RW - 32 bits - [MMReg:0x3B4]**

| Field Name      | Bits  | Default | Description  |
|-----------------|-------|---------|--|
| ICON2_VERT_POSN | 11:0  | 0x0     | Icon vertical position   |
| ICON2_HORZ_POSN | 27:16 | 0x0     | Icon horizontal position   |
| ICON2_LOCK      | 31    | 0x0     | 0=Unlocked<br>1=Locked<br><br><i>(mirror of ICON2_OFFSET:ICON2_LOCK)</i> |

Secondary display hardware icon horizontal and vertical positions

**ICON2\_HORZ\_VERT\_OFF - RW - 32 bits - [MMReg:0x3B8]**

| Field Name     | Bits  | Default | Description  |
|----------------|-------|---------|--|
| ICON2_VERT_OFF | 6:0   | 0x0     | Icon vertical offset   |
| ICON2_HORZ_OFF | 22:16 | 0x0     | Icon horizontal offset   |
| ICON2_LOCK     | 31    | 0x0     | 0=Unlocked<br>1=Locked<br><br><i>(mirror of ICON2_OFFSET:ICON2_LOCK)</i> |

Secondary display hardware icon horizontal and vertical offsets

**ICON2\_CLR0 - RW - 32 bits - [MMReg:0x3BC]**

| Field Name   | Bits  | Default | Description                            |
|--------------|-------|---------|--|
| ICON2_CLR0_B | 7:0   | 0x0     | Secondary hardware icon blue colour 0  |
| ICON2_CLR0_G | 15:8  | 0x0     | Secondary hardware icon green colour 0 |
| ICON2_CLR0_R | 23:16 | 0x0     | Secondary hardware icon red colour 0   |

Secondary hardware icon colour 0 register

**ICON2\_CLR1 - RW - 32 bits - [MMReg:0x3C0]**

| Field Name   | Bits  | Default | Description                            |
|--------------|-------|---------|--|
| ICON2_CLR1_B | 7:0   | 0x0     | Secondary hardware icon blue colour 1  |
| ICON2_CLR1_G | 15:8  | 0x0     | Secondary hardware icon green colour 1 |
| ICON2_CLR1_R | 23:16 | 0x0     | Secondary hardware icon red colour 1   |

Secondary hardware icon colour 1 register

**25. CLKCNTL Detailed Register Reference**

Clock control registers

| <b>CLOCK_CNTL_INDEX - RW - 32 bits - [IOReg,MMReg:0x8]</b> |             |                |   |
|--|-------------|----------------|---|
| <b>Field Name</b>  | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| PLL_ADDR<br>(DISPLAY) (CG) (CGM)                           | 5:0         | 0x0            | Indirect CG and PLL register index  |
| PLL_WR_EN<br>(DISPLAY) (CG) (CGM)                          | 7           | 0x0            | Indirect CG and PLL register write enable<br>0=Disable writes to CLOCK_CNTL_DATA<br>1=Enable writing to CLOCK_CNTL_DATA   |
| PPLL_DIV_SEL<br>(DISPLAY) (CG) (CGM)                       | 9:8         | 0x0            | Pixel clock PLL feedback division selection for non-VGA modes. Used when CRTC_GEN_CNTL.CRTC_EXT_DISP_EN=1. See GENMO_WT.VGA_CKSEL for pixel clock selection when VGA mode active.<br>0=PPLL_DIV0<br>1=PPLL_DIV1<br>2=PPLL_DIV2<br>3=PPLL_DIV3 |

CG and PLL indirect register control

| <b>CLOCK_CNTL_DATA - RW - 32 bits - [IOReg,MMReg:0xC]</b> |             |                |   |
|---|-------------|----------------|---|
| <b>Field Name</b>   | <b>Bits</b> | <b>Default</b> | <b>Description</b>                              |
| PLL_DATA<br>(DISPLAY) (CG) (CGM)                          | 31:0        | 0x0            | Data for write to CG and PLL indirect registers |

Data for write to CG and PLL indirect registers

| <b>PPLL_DIV_0 - RW - 32 bits - CLKIND:0x4</b>   |             |                |  |
|---|-------------|----------------|--|
| <b>Field Name</b>   | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| PPLL_FB0_DIV<br>(CG)  | 10:0        | 0x1bb          | Feedback divider for pixel clock PLL.<br>PLL output to post divider is $PPIIClk = PPLL\_REF * PPLL\_FBx\_DIV / PPLL\_REF\_DIV$ .<br>PPIIClk required to always run in the 350 MHz $\geq$ PPIIClk $\geq$ 125 MHz range. For slower pixel clocks use the PPLL_POSTx_DIV field.<br>The PPLL_FBx_DIV setting must be $\geq$ 4. |
| PPLL_ATOMIC_UPDATE_W<br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i><br>(W)<br>(CG) | 15          | 0x0            | If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.  |
| PPLL_ATOMIC_UPDATE_R<br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i><br>(R)<br>(CG) | 15          | 0x0            | Readback of atomic update status.  |
| PPLL_POST0_DIV<br>(DISPLAY)   | 18:16       | 0x0            | Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided.  |

Pixel clock PLL feedback and post division selection 0

**PPLL\_DIV\_1 - RW - 32 bits - CLKIND:0x5**

| Field Name  | Bits  | Default | Description   |
|---|-------|---------|---|
| PPLL_FB1_DIV<br>(CG)  | 10:0  | 0x1f2   | Feedback divider for pixel clock PLL.<br>PLL output to post divider is PPIIClk = PPLL_REF * PPLL_FBx_DIV / PPLL_REF_DIV.<br>PPIIClk required to always run in the 350 MHz >= PPIIClk >= 125 MHz range. For slower pixel clocks us the PPLL_POSTx_DIV field.<br>The PPLL_FBx_DIV setting must be >= 4. |
| PPLL_ATOMIC_UPDATE_W<br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i><br>(W)<br>(CG) | 15    | 0x0     | If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.   |
| PPLL_ATOMIC_UPDATE_R<br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i><br>(R)<br>(CG) | 15    | 0x0     | Readback of atomic update status.   |
| PPLL_POST1_DIV<br>(DISPLAY)   | 18:16 | 0x0     | Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided.   |

Pixel clock PLL feedback and post division selection 1

**PPLL\_DIV\_2 - RW - 32 bits - CLKIND:0x6**

| Field Name  | Bits  | Default | Description   |
|---|-------|---------|---|
| PPLL_FB2_DIV<br>(CG)  | 10:0  | 0x1bb   | Feedback divider for pixel clock PLL.<br>PLL output to post divider is PPIIClk = PPLL_REF * PPLL_FBx_DIV / PPLL_REF_DIV.<br>PPIIClk required to always run in the 350 MHz >= PPIIClk >= 125 MHz range. For slower pixel clocks us the PPLL_POSTx_DIV field.<br>The PPLL_FBx_DIV setting must be >= 4. |
| PPLL_ATOMIC_UPDATE_W<br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i><br>(W)<br>(CG) | 15    | 0x0     | If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.   |
| PPLL_ATOMIC_UPDATE_R<br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i><br>(R)<br>(CG) | 15    | 0x0     | Readback of atomic update status.   |
| PPLL_POST2_DIV<br>(DISPLAY)   | 18:16 | 0x0     | Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided.   |

Pixel clock PLL feedback and post division selection 2

**PPLL\_DIV\_3 - RW - 32 bits - CLKIND:0x7**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**PPLL\_DIV\_3 - RW - 32 bits - CLKIND:0x7**

| Field Name  | Bits  | Default | Description   |
|---|-------|---------|---|
| PPLL_FB3_DIV<br>(CG)  | 10:0  | 0x1bb   | Feedback divider for pixel clock PLL.<br>PLL output to post divider is PPIIClk = PPLL_REF * PPLL_FBx_DIV / PPLL_REF_DIV.<br>PPIIClk required to always run in the 350 MHz >= PPIIClk >= 125 MHz range. For slower pixel clocks us the PPLL_POSTx_DIV field.<br>The PPLL_FBx_DIV setting must be >= 4. |
| PPLL_ATOMIC_UPDATE_W<br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_W)</i><br>(W)<br>(CG) | 15    | 0x0     | If atomic update enabled, then controls movement of reference and feedback dividers from pending to active buffers.   |
| PPLL_ATOMIC_UPDATE_R<br><i>(mirror of PPLL_REF_DIV:PPLL_ATOMIC_UPDATE_R)</i><br>(R)<br>(CG) | 15    | 0x0     | Readback of atomic update status.   |
| PPLL_POST3_DIV<br>(DISPLAY)   | 18:16 | 0x0     | Post divider for pixel clock. See VCLK_SRC_SEL for source of clock that is divided.   |

Pixel clock PLL feedback and post division selection 3

**VCLK\_ECP\_CNTL - RW - 32 bits - CLKIND:0x8**

| Field Name            | Bits | Default | Description  |
|-----------------------|------|---------|--|
| VCLK_SRC_SEL          | 1:0  | 0x0     | Selects source of PIXCLK. The output of this mux selection is post divided by PPLL_POSTx_DIV to create the final PIXCLK.<br>If set to BYTE_CLK, then see BYTE_CLK_POST_DIV below to select the PIXCLK source.<br>Both the clock source you are switching to and from must be running, or the switch will not occur.<br>0=CPUCLK<br>1=PSCANCLK<br>2=BYTE_CLK<br>3=PPIIClk |
| VCLK_INVERT           | 4    | 0x0     | Used to invert PPIIClk to get opposite duty cycle. Only takes effect when VCLK_SRC_SEL is using PPIIClk, and PPLL_POSTx_DIV is divide-by-1. Don't care in other cases.<br>0=Not Invert<br>1=Invert   |
| PIXCLK_SRC_INVERT     | 5    | 0x0     | Used to invert PIXCLK_SRC to get opposite duty cycle.<br>0=Not Invert<br>1=Invert  |
| PIXCLK_ALWAYS_ONb     | 6    | 0x0     | 0=PIXCLK is on regardless of CRTC_PIX_WIDTH field (should be set to zero in VGA mode)<br>1=PIXCLK is off if CRTC_PIX_WIDTH is 0 otherwise PIXCLK is on   |
| PIXCLK_DAC_ALWAYS_ONb | 7    | 0x0     | 0=PIXCLK is always on<br>1=PIXCLK is off during blank time   |

**VCLK\_ECP\_CNTL - RW - 32 bits - CLKIND:0x8**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| ECP_DIV         | 9:8  | 0x0     | OV0CLK clock speed select.<br>Should always be set to 00 for PIXCLK <= 175 MHz and to 01 for PIXCLK > 175 MHz. When set to 01, the overlay and subpic horizontal scale parameters must be adjusted for the extra horizontal replication this causes. Settings 10 and 11 are reserved.<br>0=VCLK<br>1=VCLK/2 |
| ECP_FORCE_ON    | 18   | 0x0     | Controls the dynamic clock control for the back-end overlay/scaler. Set to low for power reduction.<br>0=SCALER ACTIVITY<br>1=CONTINUOUS  |
| SUBCLK_FORCE_ON | 19   | 0x0     | 0=SUBPIC ACTIVITY<br>1=CONTINUOUS   |

General controls for the display clocks.

VCLK is the pixel, or dot, clock.

ECP is the overlay/scaler clock.

**PIXCLKS\_CNTL - RW - 32 bits - CLKIND:0x2D**

| Field Name                 | Bits | Default | Description   |
|----------------------------|------|---------|---|
| PIX2CLK_SRC_SEL            | 1:0  | 0x0     | 0=PIX2CLK_SRC = CPUCLK (input pin)<br>1=PIX2CLK_SRC = PSCANCLK (input pin)<br>2=Reserved<br>3=PIX2CLK_SRC = P2PIIClk    |
| PIX2CLK_INVERT             | 4    | 0x0     | 0=Not Invert<br>1=Invert  |
| PIX2CLK_SRC_INVERT         | 5    | 0x0     | 0=Not Invert<br>1=Invert  |
| PIX2CLK_ALWAYS_ONb         | 6    | 0x0     | 0=PIX2CLK is on regardless of CRTC2_PIX_WIDTH field<br>1=PIX2CLK is off if CRTC2_PIX_WIDTH is 0 otherwise PIX2CLK is on |
| PIX2CLK_DAC_ALWAYS_ONb     | 7    | 0x0     | 0=PIX2CLK is always on<br>1=PIX2CLK is off during blank time  |
| PIXCLK_TV_SRC_SEL          | 8    | 0x0     | 0=PIXCLK_TV = PIXCLK<br>1=PIXCLK_TV = PIX2CLK   |
| PIXCLK_BLEND_ALWAYS_ONb    | 11   | 0x0     | 0=1 = Enable dynamic stopping for PIXCLK_BLEND  |
| PIXCLK_GV_ALWAYS_ONb       | 12   | 0x0     | 0=1 = Enable dynamic stopping for PIXCLK_GV   |
| PIXCLK_DIG_TMDS_ALWAYS_ONb | 13   | 0x0     |   |
| PIXCLK_LVDS_ALWAYS_ONb     | 14   | 0x0     |   |
| PIXCLK_TMDS_ALWAYS_ONb     | 15   | 0x0     |   |

No description available for this register.

**PLL\_TEST\_CNTL - RW - 32 bits - CLKIND:0x13**

| Field Name                | Bits | Default | Description  |
|---------------------------|------|---------|--|
| TST_SRC_SEL<br>(CG) (CGM) | 6:0  | 0x0     | Select different clock source to readable counter and as test clock output |

**PLL\_TEST\_CNTL - RW - 32 bits - CLKIND:0x13**

| Field Name                    | Bits  | Default | Description   |
|-------------------------------|-------|---------|---|
| TST_SRC_INV<br>(CG) (CGM)     | 7     | 0x0     | Invert test clock output                              |
| TST_DIVIDERS<br>(CG) (CGM)    | 8     | 0x0     | Enable driver test                                    |
| PLL_MASK_READ_B<br>(CG) (CGM) | 9     | 0x1     | Mask test clock output and 3 LSBs of readable counter |
| TESTCLK_MUX_SEL<br>(CG)       | 12    | 0x0     | 0=cg<br>1=cgm   |
| ANALOG_MON<br>(DISPLAY)       | 23:15 | 0x0     |   |
| TEST_COUNT (R)<br>(CG) (CGM)  | 31:24 | 0x0     | Readable counter read back                            |

CG and PLL test control

**P2PLL\_DIV\_0 - RW - 32 bits - CLKIND:0x2C**

| Field Name  | Bits  | Default | Description  |
|---|-------|---------|--|
| P2PLL_FB_DIV<br>(CG)  | 10:0  | 0x0     |  |
| P2PLL_ATOMIC_UPDATE_W<br><i>(mirror of P2PLL_REF_DIV:P2PLL_ATOMIC_UPDATE_W)</i> (W)<br>(CG) | 15    | 0x0     |  |
| P2PLL_ATOMIC_UPDATE_R<br><i>(mirror of P2PLL_REF_DIV:P2PLL_ATOMIC_UPDATE_R)</i> (R)<br>(CG) | 15    | 0x0     |  |
| P2PLL_POST_DIV<br>(DISPLAY)   | 18:16 | 0x0     | 0=V2CLK = V2CLK_SRC<br>1=V2CLK = V2CLK_SRC/2<br>2=V2CLK = V2CLK_SRC/4<br>3=V2CLK = V2CLK_SRC/8<br>4=V2CLK = V2CLK_SRC/3<br>5=reserved<br>6=V2CLK = V2CLK_SRC/6<br>7=V2CLK = V2CLK_SRC/12 |

No description available for this register.

**26. TMDS Detailed Register Reference**

TMDS registers

| <b>TMDS_CNTL - RW - 32 bits - [MMReg:0x294]</b> |             |                |  |
|---|-------------|----------------|--|
| <b>Field Name</b>                               | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| TMDS_CTL0                                       | 0           | 0x0            | Control signal for TMDS (encoded in Green channel)   |
| TMDS_CTL1                                       | 1           | 0x0            | Control signal for TMDS (encoded in Green channel)   |
| TMDS_CTL2                                       | 2           | 0x0            | Control signal for TMDS (encoded in Red channel)   |
| TMDS_CTL3                                       | 3           | 0x0            | Control signal for TMDS (encoded in Red channel)   |
| TMDS_DEBUG_HSYNC                                | 4           | 0x0            | Debug mode HSYNC control   |
| TMDS_DEBUG_VSYNC                                | 5           | 0x0            | Debug mode VSYNC control   |
| TMDS_DEBUG_DE                                   | 6           | 0x0            | Debug mode Display Enable  |
| TMDS_DEBUG_EN                                   | 7           | 0x0            | Debug mode enable  |
| TMDS_CTL_FB_SEL                                 | 9:8         | 0x0            | Select input of CTL0 for TMDS  |
| TMDS_CTL_FB_DEL                                 | 11:10       | 0x0            | Select delay of CTL0 for TMDS  |
| TMDS_STEREO_SYNC_CTL_SEL                        | 13:12       | 0x0            | 0=TMDS CTL registers have normal functionality<br>1=Stereosync will use TMDS CTL1 register<br>2=Stereosync will use TMDS CTL2 register<br>3=Stereosync will use TMDS CTL3 register |
| TMDS_SYNC_CHAR_EN                               | 19:16       | 0x0            | SYNC character enable. Each of the bit represents use of register defined sync character. Bit x= 1 means SYNC_CHARx is defined by register   |
| TMDS_SYNC_CONT                                  | 24          | 0x1            | TMDS synchronization control   |
| TMDS_DPCUM_TST                                  | 25          | 0x0            | Dcbalancer test enable   |
| TMDS_DPCUM_IN                                   | 29:26       | 0x0            | Dcbalancer test input  |
| TMDS_CRC_EN                                     | 30          | 0x0            | Enable CRC calculation   |
| TMDS_RB_SWITCH_EN                               | 31          | 0x0            | Switch Red and Blue encoding position  |

Control register for TMDS encoder timing and others

| <b>TMDS_SYNC_CHAR_SETA - RW - 32 bits - [MMReg:0x298]</b> |             |                |  |
|---|-------------|----------------|--|
| <b>Field Name</b>   | <b>Bits</b> | <b>Default</b> | <b>Description</b>                         |
| TMDS_SYNC_CHAR0   | 9:0         | 0x354          | TMDS SYNC Character 0 (Default 1101010100) |
| TMDS_SYNC_CHAR1   | 25:16       | 0x154          | TMDS SYNC Character 1 (Default 0101010100) |

TMDS SYNC Character set A

| <b>TMDS_SYNC_CHAR_SETB - RW - 32 bits - [MMReg:0x29C]</b> |             |                |  |
|---|-------------|----------------|--|
| <b>Field Name</b>   | <b>Bits</b> | <b>Default</b> | <b>Description</b>                         |
| TMDS_SYNC_CHAR2   | 9:0         | 0xab           | TMDS SYNC Character 2 (Default 0010101011) |

**TMDS\_SYNC\_CHAR\_SETB - RW - 32 bits - [MMReg:0x29C]**

| Field Name      | Bits  | Default | Description                                |
|-----------------|-------|---------|--|
| TMDS_SYNC_CHAR3 | 25:16 | 0x2ab   | TMDS SYNC Character 3 (Default 1010101011) |

TMDS SYNC character set b

**TMDS\_CRC - R - 32 bits - [MMReg:0x2A0]**

| Field Name  | Bits | Default | Description                    |
|-------------|------|---------|--------------------------------|
| TMDS_CRCRGB | 29:0 | 0x0     | 30bits RGB combined CRC result |

TMDS CRC read back

**TMDS\_TRANSMITTER\_CNTL - RW - 32 bits - [MMReg:0x2A4]**

| Field Name        | Bits  | Default | Description  |
|-------------------|-------|---------|--|
| TMDS_PLEN         | 0     | 0x0     | TMDS transmitter's PLL enable. This can power down the PLL   |
| TMDS_PLLRST       | 1     | 0x1     | TMDS transmitter's PLL reset. PLL will start the locking acquisition process once this signal becomes LOW                        |
| TMDS_MODE_SEL     | 3:2   | 0x0     |  |
| TMDS_REGSEL       | 5:4   | 0x0     | TMDS_REG output select one of the four channels  |
| TMDS_HALF_CLK_RST | 6     | 0x0     |  |
| TMDS_RAN_PAT_RST  | 7     | 0x1     |  |
| TMDS_TSTPIX       | 17:8  | 0x0     | TMDS transmitter test pixel. This signals replace pixel value when TSTEN is HIGH   |
| TMDS_REG (R)      | 27:18 | 0x0     | Output of shift registers. These are the outputs of the 10 shift registers from one of the channels during test mode (Read only) |
| ICHSEL            | 28    | 0x1     |  |
| ITCLKSEL          | 29    | 0x0     |  |
| TMDS_RAN_PAT_SEL  | 30    | 0x0     |  |

TMDS transmitter control register

**TMDS\_PLL\_CNTL - RW - 32 bits - [MMReg:0x2A8]**

| Field Name  | Bits | Default | Description   |
|-------------|------|---------|---|
| TMDS_PLLPCP | 2:0  | 0x4     | TMDS PLL charge-pump gain control   |
| TMDS_PLLPVG | 5:3  | 0x4     | TMDS PLL VCO gain control   |
| TMDS_PLLPDC | 7:6  | 0x2     | TMDS PLL duty cycle control   |
| TMDS_PLLPVS | 11:8 | 0x6     | TMDS driver voltage swing control. Select the Rext from 300ohm to 1000ohm in 50ohm step which is equivalent to 250 to 720 mV swing. |

TMDS PLL control register

**TMDS\_PATTERN\_GEN\_SEED - RW - 32 bits - [MMReg:0x2AC]**

| Field Name   | Bits | Default      | Description |
|--------------|------|--------------|-------------|
| PATTERN_SEED | 23:0 | 0x22222<br>2 |             |

No description available for this register.

**27. LVDS Detailed Register Reference**

LVDS registers

| LVDS_DIGTMSD_CRC - R - 32 bits - [MMReg:0x2CC] |       |         |  |
|--|-------|---------|--|
| Field Name                                     | Bits  | Default | Description                                      |
| LVDS_CRC_SIG_RGB                               | 23:0  | 0x0     | CRC signature for red, green and blue components |
| LVDS_CRC_SIG_C                                 | 26:24 | 0x0     | CRC signature for control signals                |

CRC signature for LVDS or Digital TMDS output

| LVDS_GEN_CNTL - RW - 32 bits - [MMReg:0x2D0] |      |         |   |
|--|------|---------|---|
| Field Name                                   | Bits | Default | Description   |
| LVDS_ON                                      | 0    | 0x0     | 0=LVDS OFF<br>1=LVDS ON   |
| LVDS_DISPLAY_DIS                             | 1    | 0x0     | 0=Normal<br>1=Force LVDS data to 0  |
| LVDS_PANEL_TYPE                              | 2    | 0x0     | 0=TFT single pixel per clock<br>1=TFT dual pixel per clock                                      |
| LVDS_PANEL_FORMAT                            | 3    | 0x1     | 0=18 bit per pixel TFT panel - 666 RGB<br>1=24 bit per pixel TFT panel - 888 RGB                |
| LVDS_NO_OF_GREY                              | 5:4  | 0x0     | 0=No frame modulation<br>1=2 levels of grey support<br>2=4 levels of grey support<br>3=reserved |
| LVDS_RST_FM                                  | 6    | 0x0     | 0=Enable frame modulation circuitry to function<br>1=Reset frame modulation circuit             |
| LVDS_EN                                      | 7    | 0x0     | 0=On chip LVDS interface is disabled<br>1=On chip LVDS interface is enabled                     |
| LVDS_BL_MOD_LEVEL                            | 15:8 | 0x0     |   |
| LVDS_BL_MOD_EN                               | 16   | 0x0     | 0=Disable LVDS backlight modulation<br>1=Enable LVDS backlight modulation                       |
| LVDS_BL_CLK_SEL                              | 17   | 0x0     | 0=29MHz Backlight Modulation Clock<br>1=29MHz divided by 3 Backlight Modulation Clock           |
| LVDS_DIGON                                   | 18   | 0x0     | 0=LVDS digital voltage off<br>1=LVDS digital voltage on   |
| LVDS_BLON                                    | 19   | 0x0     | 0=LVDS backlight voltage off<br>1=LVDS backlight voltage on                                     |
| LVDS_FP_POL                                  | 20   | 0x0     | 0=active high Frame Pulse / Vsync<br>1=active low Frame Pulse / Vsync                           |
| LVDS_LP_POL                                  | 21   | 0x0     | 0=active high Line Pulse / Hsync<br>1=active low Line Pulse / Hsync                             |
| LVDS_DTM_POL                                 | 22   | 0x0     | 0=active high Display Enable / MOD<br>1=active low Display Enable / MOD                         |
| LVDS_SRC_SEL                                 | 23   | 0x0     | 0=Select Primary (CRTC1) display path<br>1=Select Secondary (CRTC2) display path                |

**LVDS\_GEN\_CNTL - RW - 32 bits - [MMReg:0x2D0]**

| Field Name         | Bits  | Default | Description  |
|--------------------|-------|---------|--|
| LVDS_RESERVED_BITS | 26:24 | 0x0     |  |
| LVDS_FPD_EN        | 27    | 0x1     | 0=use LDI format for 888 RGB<br>1=use FPD format for 888 RGB |
| LVDS_HSYNC_DELAY   | 31:28 | 0x0     |  |

No description available for this register.

**LVDS\_PLL\_CNTL - RW - 32 bits - [MMReg:0x2D4]**

| Field Name             | Bits  | Default | Description  |
|------------------------|-------|---------|--|
| LVDS_CRC_DE_ONLY       | 0     | 0x0     | 0=LVDS CRC includes DE and blank period<br>1=LVDS CRC includes DE period only  |
| LVDS_LVPVS             | 4:1   | 0x6     |  |
| LVDS_LPPVG             | 7:5   | 0x4     |  |
| LVDS_LPPDC             | 9:8   | 0x2     |  |
| LVDS_LPPCP             | 12:10 | 0x4     |  |
| LVDS_SS_DISP_EN        | 13    | 0x0     | 0=Disable jitter whole display path<br>1=Enable jitter whole display path  |
| LVDS_PRG               | 15:14 | 0x0     |  |
| LVDS_PLL_EN            | 16    | 0x0     | 0=Disable LVDS PLL<br>1=Enable LVDS PLL  |
| LVDS_PLL_RESET         | 17    | 0x0     | 0=Unreset LVDS PLL<br>1=Reset LVDS PLL   |
| LVDS_PREAMPH_EN        | 18    | 0x0     | 0=Disable LVDS preamphsis<br>1=Enables LVDS preamphsis   |
| LVDS_CRC_EN            | 20    | 0x0     |  |
| LVDS_CRC_UP24          | 21    | 0x0     | 0=Selects lower 30bit (24+syncs,etc) of lvds data as source for LCD2ENG CRC<br>1=Selects upper 30bit (24+syncs,etc) of lvds data as source for LCD2ENG CRC |
| LVDS_TEST_DATA_OUT (R) | 24:22 | 0x0     |  |
| LVDS_TEST_DATA_SEL     | 26:25 | 0x0     |  |
| LCDENG_TEST_MODE       | 31:28 | 0x0     | 0000 = Normal<br>0001 = Eye pattern<br>1010 = Test mode 0<br>1011 = Test mode 1<br>x1xx = Use test clock for LVDS macro                                    |

No description available for this register.

**LVDS\_SS\_GEN\_CNTL - RW - 32 bits - [MMReg:0x2EC]**

| Field Name      | Bits | Default | Description  |
|-----------------|------|---------|--|
| SS_EXT_EN       | 1    | 0x0     | 0=Disable External Spread Spectrum<br>1=Enable External Spread Spectrum                                  |
| SS_EXT_SEL      | 2    | 0x0     | 0=Use External Spread Spectrum on Primary Display<br>1=Use External Spread Spectrum on Secondary Display |
| SS_BUF_EN       | 3    | 0x0     | 0=Disable Spread Spectrum Buffer<br>1=Enable Spread Spectrum Buffer                                      |
| SS_BUF_OFFSET   | 10:4 | 0x2     | Initial SS buffer read address   |
| SS_BUF_RESET_EN | 11   | 0x0     |  |



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**LVDS\_SS\_GEN\_CNTL - RW - 32 bits - [MMReg:0x2EC]**

| Field Name         | Bits  | Default | Description  |
|--------------------|-------|---------|--|
| SS_BUF_STRENGTH    | 13:12 | 0x2     | 0=Minimum drive. ~74 ohms.<br>1=Matched impedance drive. ~63 ohms.<br>2=Optimal drive. ~47 ohms.<br>3=Maximum drive. ~42 ohms. |
| LVDSPWR_STRENGTH   | 15:14 | 0x2     | 0=Minimum drive. ~74 ohms.<br>1=Matched impedance drive. ~63 ohms.<br>2=Optimal drive. ~47 ohms.<br>3=Maximum drive. ~42 ohms. |
| LVDS_PWRSEQ_DELAY1 | 19:16 | 0x2     | Delay from DIGON active to lvds data active  |
| LVDS_PWRSEQ_DELAY2 | 23:20 | 0x3     | Delay from lvds data active to BLON active   |
| LVDS_CLK_PATTERN   | 30:24 | 0x63    | Data pattern for clock channel. Default value is 0x63  |

Auxiliary window horizontal controls

**28. DVI Detailed Register Reference**

DVI

| <b>DVI_I2C_CNTL_0 - RW - 32 bits - [MMReg:0x2E0]</b> |             |                |  |
|--|-------------|----------------|--|
| <b>Field Name</b>                                    | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| I2C_DONE   | 0           | 0x0            | 0=I2c is busy<br>1=transfer is complete  |
| I2C_NACK   | 1           | 0x0            | 1=Slave did not issue acknowledge  |
| I2C_HALT   | 2           | 0x0            | 1=Time-out condition, transfer is halted   |
| I2C_SOFT_RST   | 5           | 0x0            | 0=Normal<br>1=Resets i2c controller  |
| I2C_DRIVE_EN   | 6           | 0x0            | 0=Pullup by external resistor<br>1=I2C pads drive SDA  |
| I2C_DRIVE_SEL  | 7           | 0x0            | 0=Drive for 10MCLKs<br>1=20MCLKS   |
| I2C_START  | 8           | 0x0            | 0=No start<br>1=Start  |
| I2C_STOP   | 9           | 0x0            | 0=No stop<br>1=Stop  |
| I2C_RECEIVE  | 10          | 0x0            | 0=Send<br>1=Receive  |
| I2C_ABORT  | 11          | 0x0            | 0=No abort<br>1=Abort  |
| I2C_GO   | 12          | 0x0            |  |
| SW_WANTS_TO_USE_DVI_I2C (W)                          | 13          | 0x0            | 0=Normal<br>1=SW requests to use DVI I2C interface   |
| SW_CAN_USE_DVI_I2C (R)                               | 13          | 0x0            | 0=DVI I2C interface not available<br>1=SW has control of the DVI I2C interface               |
| SW_DONE_USING_DVI_I2C (W)                            | 14          | 0x0            | 0=if SW has control of DVI I2C, free to use it<br>1=indicate SW is done using DVI I2C i/f    |
| HW_NEEDS_DVI_I2C (R)                                 | 14          | 0x0            | 0=no request by H/W for use of DVI I2C<br>1=H/W HDCP requests use of the DVI I2C i/f         |
| ABORT_HW_DVI_I2C (W)                                 | 15          | 0x0            | 0=normal operation of H/W using DVI I2C<br>1=abort current H/W HDCP use of DVI I2C interface |
| HW_USING_DVI_I2C (R)                                 | 15          | 0x0            | 0=DVI I2C i/f not in use by H/W<br>1=HDCP H/W currently using DVI I2C interface              |
| I2C_PRESCALE   | 31:16       | 0x0            |  |

No description available for this register.

| <b>DVI_I2C_CNTL_1 - RW - 32 bits - [MMReg:0x2E4]</b> |             |                |                    |
|--|-------------|----------------|--------------------|
| <b>Field Name</b>                                    | <b>Bits</b> | <b>Default</b> | <b>Description</b> |
| I2C_DATA_COUNT                                       | 3:0         | 0x0            |                    |
| I2C_ADDR_COUNT                                       | 10:8        | 0x0            |                    |



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**DVI\_I2C\_CNTL\_1 - RW - 32 bits - [MMReg:0x2E4]**

| Field Name     | Bits  | Default | Description   |
|----------------|-------|---------|---|
| I2C_SEL        | 16    | 0x0     | 0=Pullup by external resistor<br>1=I2C pads drive SCL |
| I2C_EN         | 17    | 0x0     |   |
| I2C_TIME_LIMIT | 31:24 | 0x0     |   |

No description available for this register.

**DVI\_I2C\_DATA - RW - 32 bits - [MMReg:0x2E8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| I2C_DATA   | 7:0  | 0x0     |             |

No description available for this register.

**29. flatPanel Detailed Register Reference**

Flat panel registers

| <b>FP_H2_SYNC_STRT_WID - RW - 32 bits - [MMReg:0x3C4]</b> |             |                |   |
|---|-------------|----------------|---|
| <b>Field Name</b>   | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| FP_H2_SYNC_STRT_PIX                                       | 2:0         | 0x0            | DFP Horizontal sync start delay in pixels. Allows pixel accurate horizontal positioning by delaying sync position by the specified number of pixels.  |
| FP_H2_SYNC_STRT_CHAR                                      | 12:3        | 0x0            | DFP Horizontal sync start position (pixels * 8). Sum of display width, overscan right and front porch. This field is programmed with the exact desired character on which to start HSYNC, not -1. i.e. 656/8 = 82. If horizontal fixed blank or autocentering (see CRTC_MORE_CNTL) is enabled, this register field contains the offset (from then end of the active display/start of horizontal blank) within the blank time of the start of the horizontal sync signal for the DFP (in characters) |
| FP_H2_SYNC_WID  | 21:16       | 0x0            | DFP Horizontal sync width (pixels * 8). If horz. fixed blank or autocentering is enabled this register field contains the width (in characters) of the horizontal sync signal for the DFP.  |
| FP_H2_SYNC_POL  | 23          | 0x0            | DFP Horizontal sync polarity<br>0=Active high<br>1=Active low<br>0=Active high<br>1=Active low  |

Secondary display shadow Horizontal Sync for Digital Flat Panels.

Used for DFP HSYNC when FP\_GEN\_CNTL.DFP\_SYNC\_SEL=1 and used for CRT HSYNC when

FP\_GEN\_CNTL.CRT\_SYNC\_SEL=1.

The FP\_H\_SYNC\_STRT\_PIX and FP\_H\_SYNC\_POL always apply to the DFP Horizontal Sync regardless of other control bits.(DFP\_SYNC\_SEL/CRT\_SYNC\_SEL/horizontal blanking mode/horz. autocentering)

| <b>FP_V2_SYNC_STRT_WID - RW - 32 bits - [MMReg:0x3C8]</b> |             |                |  |
|---|-------------|----------------|--|
| <b>Field Name</b>   | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| FP_V2_SYNC_STRT   | 11:0        | 0x0            | DFP Vertical sync start position (in lines). Sum of display height, overscan bottom and front porch. If vertical fixed blank or autocentering is enabled(see CRTC_MORE_CNTL) this field contains the offset(from the bottom of the active display/start of vertical blank) within the vertical blank time of the start of the vertical sync signal for the DFP(in lines) |
| FP_V2_SYNC_WID  | 20:16       | 0x0            | DFP Vertical sync width(in lines). If vert. fixed blank or autocentering is enabled this field contains the length (in lines) of the vertical sync signal for the DFP  |
| FP_V2_SYNC_POL  | 23          | 0x0            | DFP Vertical sync polarity<br>0=Active high<br>1=Active low<br>0=Active high<br>1=Active low   |

Secondary display shadow Vertical Sync for Digital Flat Panels

**FP\_GEN\_CNTL - RW - 32 bits - [MMReg:0x284]**

| Field Name          | Bits | Default | Description   |
|---------------------|------|---------|---|
| FP_ON               | 0    | 0x0     | 0=Resets TMDS block and turns of PIXCLK_TMDS<br>1=Turns on PIXCLK_TMDS and removes reset to TMDS block  |
| FP_BLANK_EN         | 1    | 0x0     | 0 = Normal operation.<br>1 = Send black pixel data to TMDS encoder to blank screen. No effect on DE or SYNCs.<br>0=Normal operation.<br>1=Black data to TMDS encoder. No effect on DE or SYNCs.   |
| TMDS_EN             | 2    | 0x0     | 0 = TMDS interface is disabled.<br>1 = TMDS interface is enabled.<br>This bit can be cleared if the hardware detects a hot plug disconnect of the DFP and FP_DETECT_EN=1.<br>0=TMDS interface is disabled. This bit can be cleared by hot plug disconnect if FP_DETECT_EN=1.<br>1=TMDS interface is enabled.  |
| PANEL_FORMAT        | 3    | 0x1     | Panel format: (default=0)<br>0 = 18 bit per pixel TFT panel - 666 RGB.<br>1 = 24 bit per pixel TFT panel - 888 RGB<br>0=18 bit per pixel TFT panel - 666 RGB<br>1=24 bit per pixel TFT panel - 888 RGB  |
| NO_OF_GREY          | 5:4  | 0x0     | Grey level select:<br>0 = No frame modulation.<br>1 = 2 levels of grey support.<br>2 = 4 levels of grey support.<br>3 = reserved<br>0=No frame modulation.<br>1=2 levels of grey support.<br>2=4 levels of grey support.<br>3=reserved  |
| FP_RST_FM           | 6    | 0x0     | Frame modulation reset.<br>0 = EnaFMCir.<br>1 = ResetFMCir<br>0=Frame modulator ready.<br>1=Reset frame modualtor circuit.  |
| FP_EN_TMDS (R)      | 7    | 0x0     | Read-only bit that indicates TMDS status.<br>0 = TMDS interface is disabled. Either by TMDS_EN written with 0, or hot plug disconnect detected.<br>1 = TMDS interface is enabled. Also requires TMDS macro to be properly set up.<br>0=TMDS interface is disabled. Either by TMDS_EN written with 0, or hot plug disconnect detected.<br>1=TMDS interface is enabled. Also requires TMDS macro to be properly set up. |
| FP_DETECT_SENSE (R) | 8    | 0x0     | 0 = No hot plug panel connected or panel that does not support hot plug is connected.<br>1 = Hot plug panel is connected.<br>0=No hot plug panel connected or panel that does not support hot plug is connected.<br>1=Hot plug panel is connected.  |

**FP\_GEN\_CNTL - RW - 32 bits - [MMReg:0x284]**

| Field Name               | Bits | Default | Description  |
|--------------------------|------|---------|--|
| FP_DETECT_INT_POL        | 9    | 0x0     | 0 = Generate interrupt on hot plug disconnect.<br>1 = Generate interrupt on hot plug connect.<br>Requires interrupt to be enabled(GEN_INT_CNTL.FP_DETECT_MASK)<br>0=Generate interrupt on hot plug disconnect.<br>1=Generate interrupt on hot plug connect.  |
| FP_DETECT_EN             | 12   | 0x0     | 0 = Hot plug detection has no affect on TMDS transmitter enable/disable.<br>1 = Hot plug detection can disable TMDS transmitter. Transmitter enable only possible by SW.<br>0=Hot plug detection has no affect on TMDS transmitter enable/disable.<br>1=Hot plug detection can disable TMDS transmitter. Transmitter enable only possible by SW.   |
| FP_SRC_SEL               | 13   | 0x0     | 0=Select Primary (CRTC1) display path<br>1=Select Secondary (CRTC2) display path   |
| FP_USE_VGA_HVSYNC        | 14   | 0x1     | 0 = TMDS H&V SYNC based only on FP_x_SYNC_STRT_WID registers. For VGA modes, this will not be adjusted for pixel data delays through VGA logic.<br>1 = TMDS H&V SYNC adjusted in VGA modes for delays through VGA pixel data logic.<br>0=TMDS H&V SYNC based only on FP_x_SYNC_STRT_WID. For VGA modes, this will not be adjusted for pixel data delays through VGA logic.<br>1=TMDS H&V SYNC adjusted in VGA modes for delays through VGA pixel data logic. |
| FP_USE_VGA_SYNC_POLARITY | 15   | 0x0     | 0 = TMDS H&V SYNC polarities determined by FP_x_SYNC_POL fields.<br>1 = TMDS H&V SYNC polarities determined by VGA_xSYNC regs in VGA modes, and FP_x_SYNC_POL fields in non-VGA modes.<br>0=TMDS H&V SYNC polarities determined by FP_x_SYNC_POL fields.<br>1=TMDS H&V SYNC polarities determined by VGA_xSYNC regs in VGA modes, and FP_x_SYNC_POL fields in non-VGA modes.   |
| CRTC_DONT_SHADOW_VPAR    | 16   | 0x0     | 0 = Use Shadowed Vertical CRT values. DFP VSYNC calculated from shadow CRT VSYNC register values. If FP_USE_SHADOW_EN=1 uses shadowed V_BLANK_START, V_BLANK_END, and V_TOTAL.<br>1 = Use non-shadowed vertical CRT values. DFP VSYNC calculated from non-shadowed vertical CRT values. If FP_USE_SHADOW_EN=1, uses non-shadowed V_BLANK_START, V_BLANK_END, and V_TOTAL.<br>0=Use Shadowed<br>1=Use non-shadowed  |
| CRTC_DONT_SHADOW_HEND    | 17   | 0x0     | 0 = If FP_USE_SHADOW_EN=1 then use shadowed versions of H_DISP_END, H_BLANK_START, and H_BLANK_END CRT registers<br>1 = Use non-shadowed CRT register values regardless of value of FP_USE_SHADOW_EN<br>0=Use Shadowed HorzDispEnd<br>1=Use non-shadowed HorzDispEnd   |



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**FP\_GEN\_CNTL - RW - 32 bits - [MMReg:0x284]**

| Field Name               | Bits | Default | Description   |
|--------------------------|------|---------|---|
| CRTC_USE_SHADOWED_VEND   | 18   | 0x0     | 0 = use non-shadow V_DISP_END register value<br>1 = if FP_USE_SHADOW_EN=1 then use shadow CRT V_DISP_END_S register value, else use non-shadow value<br>0=disable<br>1=use shadowed VEND  |
| CRTC_USE_SHADOWED_ROWCUR | 19   | 0x0     | 0 = use normal CRT register values<br>1 = use shadowed MAX_ROW_SCAN, CURSOR_START, CURSOR_END, and UNDRLN_LOC CRT registers<br>0=disable<br>1=use shadowed RowCur   |
| RMX_HVSYNC_CONTROL_EN    | 20   | 0x0     | 0 = Use standard syncs generated for CRT and DFP HSYNC and VSYNC outputs<br>1 = Use syncs generated in RMX logic for CRT and DFP HSYNC and VSYNC outputs. While this will also work when RMX is disabled, it should only be used with RMX enabled<br>0=Use standard syncs generated for CRT and DFP HSYNC and VSYNC outputs<br>1=Use syncs generated in RMX logic for CRT and DFP HSYNC and VSYNC outputs |
| DFP_SYNC_SEL             | 21   | 0x0     | 0=Use standard(non-shadow) values for DFP syncs(with auto-scaling panels or at native resolution)<br>1=Use shadow(DFP) registers for DFP syncs<br>0=Use non-shadow values for DFP syncs<br>1=Use shadow(LCD) values for DFP syncs   |
| CRTC_LOCK_8DOT           | 22   | 0x0     | 0=Normal VGA text is 8 or 9 dot depending on SEQ01.SEQ_DOT8. 1=Force VGA text to 8 dot. Used when Horizontal RMX is enabled<br>0=Normal VGA text 8 or 9 dot.<br>1=Force VGA text to 8 dot.  |
| CRT_SYNC_SEL             | 23   | 0x0     | 0=Use standard (non-shadow) values for CRT syncs in normal operation.<br>1=Use shadow(DFP) values for CRT syncs in centring/RMX modes (registers with FP_ name prefix)<br>0=Use non-shadow values for CRT syncs in centring mode<br>1=Use shadow(LCD) values for CRT syncs in centring mode   |
| FP_USE_SHADOW_EN         | 24   | 0x0     | 0=Use standard CRTC registers to calculate CRT display parameters.<br>1=Use shadow CRT registers (mirrored with the registers with a FP_ name prefix) to calculate CRT parameters.<br>0=Disable<br>1=Enable   |
| DONT_RST_CHAREN          | 25   | 0x0     | 0 = stop CHAREN if SEQ00=0<br>1 = when SEQ00=0 CHAREN is not stopped. Use with RMX.<br>0=stop CHAREN if SEQ00=0<br>1=Don't  |

**FP\_GEN\_CNTL - RW - 32 bits - [MMReg:0x284]**

| Field Name                           | Bits | Default | Description   |
|--------------------------------------|------|---------|---|
| CRT_SYNC_ALT_SEL                     | 26   | 0x0     | 0 = value of CRT_SYNC_SEL determines which register values are used to generate CRT horz. & vert. sync start and width.<br>1 = Alternate CRT shadow register values (CRT_CRTC_H_SYNC_STRT_WID and CRT_CRTC_V_SYNC_STRT_WID) are used to generate CRT sync start and width in centering/RMX modes.<br>0=Use CRT_SYNC_SEL to choose CRT sync start and width.<br>1=Use alternate CRT shadow values for CRT sync start and width in centering mode (CRT_CRTC_H_SYNC_STRT_WID and CRT_CRTC_V_SYNC_STRT_WID) |
| CRTC_USE_NONSHADOW_HPARAMS_FOR_BLANK | 27   | 0x0     | 0 = disabled (normal operation)<br>1 = makes left overscan width in VGA equal the value in non-shadow CRT registers when shadowing is enabled. When FP_USE_SHADOW_EN=1 and in VGA mode, the horizontal blank end(left overscan width) is calculated from the non-shadow CRT values. $H\_BLANK\_END = H\_TOTAL(shadow) - (H\_TOTAL(non-shadow) - H\_BLANK\_END(non-shadow))$<br>0=Left overscan calculated from shadow H parameters.<br>1=Left overscan calculated from non-shadow H parameters.         |
| CRTC_USE_NONSHADOW_VPARAMS_FOR_BLANK | 28   | 0x0     | 0 = disabled (normal operation)<br>1 = makes top overscan width in VGA equal the value in non-shadow CRT registers when shadowing is enabled. When FP_USE_SHADOW_EN=1 and in VGA mode, the vertical blank end(top overscan width) is calculated from the non-shadow CRT values. $V\_BLANK\_END = V\_TOTAL(shadow) - (V\_TOTAL(non-shadow) - V\_BLANK\_END(non-shadow))$<br>0=Top overscan calculated from shadow V parameters.<br>1=Top overscan calculated from non-shadow V parameters.               |
| CRTC_VGA_XOVERSCAN_COLOR             | 29   | 0x0     | 0 = use extended overscan color (OVR_CLR register) for overscan pixels in VGA mode when extended overscan is enabled(CRTC_VGA_XOVERSCAN = 1).<br>1 = use VGA overscan color for overscan pixels in VGA mode when extended overscan enabled.<br>0=Use extended overscan color when doing extended overscan in VGA mode.<br>1=Use VGA overscan color when doing extended overscan in VGA mode.  |
| CRTC_VGA_XOVERSCAN_DIVBY2_EN         | 30   | 0x0     | 0 = in VGA mode, when CRTC_EXT_CNTL.CRTC_VGA_XOVERSCAN=1 and SEQ_PCLKBY2=1 then OVR_LEFT/RIGHT register values are used.<br>1 = in VGA mode, when CRTC_EXT_CNTL.CRTC_VGA_XOVERSCAN=1 and SEQ_PCLKBY2=1, then OVR_LEFT/RIGHT register values are divided by 2<br>0=When VGA and extended overscan and SEQ_PCLKBY2=1, then OVR_WID_LEFT/RIGHT are used directly.<br>1=When VGA and extended overscan and SEQ_PCLKBY2=1, then OVR_WID_LEFT/RIGHT are divided by 2.   |

Digital Flat Panel(DFP) general controls

**FP2\_GEN\_CNTL - RW - 32 bits - [MMReg:0x288]**

| Field Name           | Bits  | Default | Description   |
|----------------------|-------|---------|---|
| FP2_BLANK_EN         | 1     | 0x0     | 0=Normal operation.<br>1=Black data to TMDS encoder. No effect on DE or SYNCs.  |
| FP2_ON               | 2     | 0x0     |   |
| FP2_PANEL_FORMAT     | 3     | 0x1     | 0=18 bit per pixel TFT panel - 666 RGB<br>1=24 bit per pixel TFT panel - 888 RGB                                      |
| FP2_NO_OF_GREY       | 5:4   | 0x0     | 0=No frame modulation.<br>1=2 levels of grey support.<br>2=4 levels of grey support.<br>3=reserved                    |
| FP2_RST_FM           | 6     | 0x0     | 0=Frame modulator ready.<br>1=Reset frame modulator circuit.  |
| FP2_DETECT_SENSE (R) | 8     | 0x0     | 0=No hot plug panel connected or panel that does not support hot plug is connected.<br>1=Hot plug panel is connected. |
| FP2_DETECT_INT_POL   | 9     | 0x0     | 0=Generate interrupt on hot plug disconnect.<br>1=Generate interrupt on hot plug connect.                             |
| FP2_SRC_SEL          | 13    | 0x0     | 0=Select Primary (CRTC1) display path<br>1=Select Secondary (CRTC2) display path                                      |
| FP2_FP_POL           | 16    | 0x0     | 0=Active High Frame Pulse<br>1=Active Low Frame Pulse   |
| FP2_LP_POL           | 17    | 0x0     | 0=Active High Line Pulse<br>1=Active Low Line Pulse   |
| FP2_SCK_POL          | 18    | 0x0     | 0=Active High Shift Clock<br>1=Active Low Shift Clock   |
| FP2_LCD_CNTL         | 21:19 | 0x0     |   |
| FP2_PAD_FLOP_EN      | 22    | 0x0     | 0=To Enable flops in pads.  |
| FP2_CRC_EN           | 23    | 0x0     |   |
| FP2_CRC_READ_EN      | 24    | 0x0     |   |

No description available for this register.

**FP\_HORZ\_STRETCH - RW - 32 bits - [MMReg:0x28C]**

| Field Name            | Bits | Default | Description  |
|-----------------------|------|---------|--|
| FP_HORZ_STRETCH_RATIO | 15:0 | 0x0     | Horizontal RMX Stretch Ratio. When FP_HORZ_STRETCH_MODE = 0 (pixel replication), the value in this register is shifted out serially (LSB first, i.e. bit 0). If the value of the bit shifted out is a '0' then the next real (pre-replication) display pixel is loaded and displayed. If the bit shifted out is a '1' then the last pixel loaded will be duplicated and displayed. The bit shifter is looped back to bit 0 after either bit 9, 11, 12, 14, or 15 depending on the value of FP_LOOP_STRETCH. In pixel-replication mode, bit 0 of the ratio must always be set to '0'.<br>When FP_HORZ_STRETCH_MODE = 1 (blending), valid values for the ratio are 1 to 4095.<br>Ratio = ( (Active display width in characters (including overscan)) / (Panel width in characters)) x 4096 ) |

**FP\_HORZ\_STRETCH - RW - 32 bits - [MMReg:0x28C]**

| Field Name              | Bits  | Default | Description  |
|-------------------------|-------|---------|--|
| FP_HORZ_PANEL_SIZE      | 24:16 | 0x0     | Digital Flat Panel (DFP) width in characters = ((panel width in pixels/8) - 1). Used when Automatic RMX Horizontal Ratio enabled   |
| FP_HORZ_STRETCH_EN      | 25    | 0x0     | 0 = Disable Horizontal RMX.<br>1 = Enable Horz. RMX.<br>0=Horizontal stretching disabled.<br>1=Horizontal stretching enabled.  |
| FP_HORZ_STRETCH_MODE    | 26    | 0x0     | Panel horizontal stretch mode:<br>0 = pixel replication.<br>1 = horizontal blending.<br>0=Disables horizontal filter, giving pixel replication.<br>1=Enables horizontal filter blending.   |
| FP_AUTO_HORZ_RATIO      | 27    | 0x0     | 0=Use FP_HORZ_STRETCH_RATIO as Hratio for RMX.<br>1=Use auto-calculated ratio for Hratio. Works in both VGA and Extended modes.<br>0=Use FP_HORZ_STRETCH_RATIO as Hratio for RMX. Required selection for non-VGA modes.<br>1=Use auto-calculated ratio for Hratio. Only available in VGA modes.  |
| FP_LOOP_STRETCH         | 30:28 | 0x0     | Panel horizontal 'pixel replication' loop back select:<br>0 = after bit 9 loop back to bit 0.<br>1 = after bit 11 loop back to bit 0.<br>2 = after bit 12 loop back to bit 0.<br>3 = after bit 14 loop back to bit 0.<br>4 = after bit 15 loop back to bit 0<br>0=Loop bit 0 back to bit 9<br>1=Loop bit 0 back to bit 11<br>2=Loop bit 0 back to bit 12<br>3=Loop bit 0 back to bit 14<br>4=Loop bit 0 back to bit 15 |
| RMX_AUTO_RATIO_HORZ_INC | 31    | 0x1     | 0=Horizontal auto ratio result truncated, i.e. rounded down.<br>1=Horizontal auto ratio result truncated, and then incremented by 1 i.e. rounded up.<br>0=Horizontal auto ratio result truncated, i.e. rounded down.<br>1=Horizontal auto ratio result truncated, and then incremented by 1.   |

Panel Horizontal Ratiometric(RMX) stretch control register

**FP\_VERT\_STRETCH - RW - 32 bits - [MMReg:0x290]**

| Field Name            | Bits  | Default | Description  |
|-----------------------|-------|---------|--|
| FP_VERT_STRETCH_RATIO | 11:0  | 0x0     | For both values of FP_VERT_STRETCH_MODE, valid values for the ratio are 1 to 4095.<br>Ratio = (((Active display height in lines (including overscan)) / (Panel height in lines)) x 4096) |
| FP_VERT_PANEL_SIZE    | 23:12 | 0x0     | DFP height in lines = (panel height in lines - 1)  |
| FP_VERT_STRETCH_EN    | 25    | 0x0     | 0 = Disable Vertical RMX.<br>1 = Enable Vert. RMX<br>0=Vertical stretching disabled.<br>1=Vertical stretching enabled.   |

**FP\_VERT\_STRETCH - RW - 32 bits - [MMReg:0x290]**

| Field Name              | Bits | Default | Description  |
|-------------------------|------|---------|--|
| FP_VERT_STRETCH_MODE    | 26   | 0x0     | Panel vertical stretch mode:<br>0 = line replication.<br>1 = vertical blending<br>0=Disables vertical filter, giving line replication.<br>1=Enables vertical filter blending.  |
| FP_AUTO_VERT_RATIO      | 27   | 0x0     | 0 = Use FP_VERT_STRETCH_RATIO as Vratio for RMX.<br>1 = use auto-calculated vertical ratio. Works in both VGA and Extended modes.<br>0=Use FP_VERT_STRETCH_RATIO register field.<br>Required selection for non-VGA modes.<br>1=Auto calculate vertical ratio. Only available in VGA modes. |
| RMX_H_FILTER_INIT       | 28   | 0x0     | 0=first filter tap is black.<br>1=first filter tap is first pixel.   |
| RMX_V_FILTER_INIT       | 29   | 0x0     | 0=first filter tap is black.<br>1=first filter tap is first pixel.   |
| RMX_AUTO_RATIO_VERT_INC | 31   | 0x1     | 0 = Vertical auto ratio result truncated(i.e. rounded down).<br>1 = Vertical auto ratio result truncated, and then incremented by 1 (i.e. rounded up).<br>0=Vertical auto ratio result truncated, i.e. rounded down.<br>1=Vertical auto ratio result truncated, and then incremented by 1. |

Panel Vertical Ratiometric(RMX) stretch control register

**FP\_H\_SYNC\_STRT\_WID - RW - 32 bits - [MMReg:0x2C4]**

| Field Name          | Bits  | Default | Description   |
|---------------------|-------|---------|---|
| FP_H_SYNC_STRT_PIX  | 2:0   | 0x0     | DFP Horizontal sync start delay in pixels. Allows pixel accurate horizontal positioning by delaying sync position by the specified number of pixels.  |
| FP_H_SYNC_STRT_CHAR | 12:3  | 0x0     | DFP Horizontal sync start position (pixels * 8). Sum of display width, overscan right and front porch.<br>This field is programmed with the exact desired character on which to start HSYNC, not -1. i.e. 656/8 = 82<br>If horizontal fixed blank or auto-centering (see CRTC_MORE_CNTL) is enabled, this register field contains the offset (from then end of the active display/start of horizontal blank) within the blank time of the start of the horizontal sync signal for the DFP (in characters) |
| FP_H_SYNC_WID       | 21:16 | 0x0     | DFP Horizontal sync width (pixels * 8).<br>If horz. fixed blank or auto-centering is enabled this register field contains the width (in characters) of the horizontal sync signal for the DFP.  |
| FP_H_SYNC_POL       | 23    | 0x0     | DFP Horizontal sync polarity<br>0=Active high<br>1=Active low<br>0=Active high<br>1=Active low  |

Shadow Horizontal Sync for Digital Flat Panels.

Used for DFP HSYNC when FP\_GEN\_CNTL.DFP\_SYNC\_SEL=1 and used for CRT HSYNC when

FP\_GEN\_CNTL.CRT\_SYNC\_SEL=1.

The FP\_H\_SYNC\_STRT\_PIX and FP\_H\_SYNC\_POL always apply to the DFP Horizontal Sync regardless of other control bits.(DFP\_SYNC\_SEL/CRT\_SYNC\_SEL/horizontal blanking mode/horz. auto-centering)

**FP\_V\_SYNC\_STRT\_WID - RW - 32 bits - [MMReg:0x2C8]**

| Field Name     | Bits  | Default | Description  |
|----------------|-------|---------|--|
| FP_V_SYNC_STRT | 11:0  | 0x0     | DFP Vertical sync start position (in lines). Sum of display height, overscan bottom and front porch.<br>If vertical fixed blank or auto-centering is enabled(see CRTC_MORE_CNTL) this field contains the offset(from the bottom of the active display/start of vertical blank) within the vertical blank time of the start of the vertical sync signal for the DFP(in lines) |
| FP_V_SYNC_WID  | 20:16 | 0x0     | DFP Vertical sync width(in lines).<br>If vert. fixed blank or auto-centering is enabled this field contains the length (in lines) of the vertical sync signal for the DFP  |
| FP_V_SYNC_POL  | 23    | 0x0     | DFP Vertical sync polarity<br>0=Active high<br>1=Active low<br>0=Active high<br>1=Active low   |

Shadow Vertical Sync for Digital Flat Panels

**FP\_HORZ\_VERT\_ACTIVE - RW - 32 bits - [MMReg:0x278]**

| Field Name          | Bits  | Default | Description  |
|---------------------|-------|---------|--|
| FP_VERT_ACTIVE_SIZE | 11:0  | 0x0     | Vertical Active Display size (usually panel native height) in lines when vert. auto-centering is enabled.                                |
| FP_HORZ_ACTIVE_SIZE | 24:16 | 0x0     | Horizontal Active Display size (usually panel native width) in characters (8 pixels per character) when horz. auto-centering is enabled. |

Active Display Size registers for auto-centering.

Using auto-centering in combination with ratiometric expansion and auto-ratio calculation should enable ratiometric expansion while preserving the aspect ratio of the original image.

**FP\_CRTC\_H\_TOTAL\_DISP - RW - 32 bits - [MMReg:0x250]**

| Field Name      | Bits  | Default | Description  |
|-----------------|-------|---------|--|
| FP_CRTC_H_TOTAL | 9:0   | 0x0     | Horizontal total ((pixels * 8)-1). Sum of display width, overscan right, front porch, sync width, back porch and overscan left.<br>If horizontal auto-centering or horizontal fixed blank is enabled(see CRTC_MORE_CNTL), this field contains the width of the horizontal blanking time(in characters) |
| FP_CRTC_H_DISP  | 24:16 | 0x0     | Horizontal display end ((pixels * 8)-1). Determines number of visible pixels, not including overscan.  |

DFP Shadow Horizontal Display/Horizontal Total.

These values are used when FP\_GEN\_CNTL.FP\_USE\_SHADOW\_EN = 1

**FP\_CRTC\_V\_TOTAL\_DISP - RW - 32 bits - [MMReg:0x254]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



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**FP\_CRTC\_V\_TOTAL\_DISP - RW - 32 bits - [MMReg:0x254]**

| Field Name      | Bits  | Default | Description   |
|-----------------|-------|---------|---|
| FP_CRTC_V_TOTAL | 11:0  | 0x0     | Vertical total(lines-1). Sum of display height, overscan bottom, front porch, sync width, back porch and overscan top.<br>If vertical autocentering or vertical fixed blank is enabled(see CRTC_MORE_CNTL) this field contains the length of the vertical blanking time(in lines) |
| FP_CRTC_V_DISP  | 27:16 | 0x0     | Vertical display end(lines-1). Determines number of visible lines, not including overscan.  |

DFP Shadow Vertical Display/Vertical Total registers.

These values are used when FP\_GEN\_CNTL.FP\_USE\_SHADOW\_EN = 1



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**30. Palette Detailed Register Reference**

| <b>PALETTE_INDEX - RW - 32 bits - [IOReg,MMReg:0xB0]</b> |             |                |  |
|--|-------------|----------------|--|
| <b>Field Name</b>  | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| PALETTE_W_INDEX  | 7:0         | 0x0            | Write: Sets starting index for palette writes. Auto-increments on each write to PALETTE_DATA.<br>Read: Indicates index where next write to PALETTE_DATA will be written. |
| PALETTE_R_INDEX  | 23:16       | 0x0            | Write: Sets starting index for palette reads. Auto-increments on each read from PALETTE_DATA.<br>Read: Indicates index where next read from PALETTE_DATA will be read.   |

Display palette read and write index setting.

Recommend using byte writes to set either read mode or write mode for the palette. If both bytes are written at once, the write index will win and read index will be ignored. Note there is only one internal index register, so writing to one of them changes the read for both.

| <b>PALETTE_DATA - RW - 32 bits - [IOReg,MMReg:0xB4]</b> |             |                |                     |
|---|-------------|----------------|---------------------|
| <b>Field Name</b>                                       | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| PALETTE_DATA_B  | 7:0         | 0x0            | Blue palette data.  |
| PALETTE_DATA_G  | 15:8        | 0x0            | Green palette data. |
| PALETTE_DATA_R  | 23:16       | 0x0            | Red palette data.   |

Display palette data read/write in 24bpp format for backward compatibility. Note DAC\_CNTL.DAC\_8BIT\_EN affects this register. For all three colors 8 bit write data is expanded to 10 bits by replicating msbs to the missing lsbs. On reads only the top 8 bits of each 10 bit color in the internal palette are returned. For best results, use PALETTE\_30\_DATA instead of this register.

| <b>PALETTE_30_DATA - RW - 32 bits - [IOReg,MMReg:0xB8]</b> |             |                |                     |
|--|-------------|----------------|---------------------|
| <b>Field Name</b>  | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| PALETTE_DATA_B   | 9:0         | 0x0            | Blue palette data.  |
| PALETTE_DATA_G   | 19:10       | 0x0            | Green palette data. |
| PALETTE_DATA_R   | 29:20       | 0x0            | Red palette data.   |

Display palette 30 bit data read/write. Use register instead of PALETTE\_DATA to take advantage of the 30 bit DACs and improved gamma correction.

**31. RMX Detailed Register Reference**

## Ratiometric Expansion Registers

| <b>RMX_HORZ_PHASE - RW - 32 bits - [MMReg:0xDBC]</b> |             |                |   |
|--|-------------|----------------|---|
| <b>Field Name</b>                                    | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| RMX_HORZ_START_PHASE                                 | 11:0        | 0x0            | Ratiometric expander horizontal accumulator start phase. Horizontal filter accumulator resets to this value at the start of each line. This is normally set to zero, but can be used to fix certain large expansion cases where the expanded image otherwise comes out one pixel too large. |
| RMX_H_ACC_INIT                                       | 12          | 0x0            | 0=start accumulator at ratio.<br>1=use h phase register for accumulator init.   |
| RMX_V_ACC_INIT                                       | 13          | 0x0            | 0=start accumulator at ratio.<br>1=use v phase register for accumulator init.   |
| RMX_VERT_START_PHASE                                 | 27:16       | 0x0            | Ratiometric expander vertical accumulator start phase. Vertical filter accumulator resets to this value at the start of each frame. This is normally set to zero, but can be used to fix certain large expansion cases where the expanded image otherwise comes out one pixel too large.    |

Ratiometric expander accumulator horizontal and vertical start phases

**32. AUXWin Detailed Register Reference**

## Auxilliary Window Control Registers

| <b>AUX_WINDOW_HORZ_CNTL - RW - 32 bits - [MMReg:0x2D8]</b>               |             |                |   |
|--|-------------|----------------|---|
| <b>Field Name</b>  | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| AUX_WIN_HORZ_START   | 11:0        | 0x0            | Pixel coordinate of left edge of auxiliary window.  |
| AUX_WIN_HORZ_END   | 23:12       | 0x0            | Pixel coordinate of right edge of auxiliary window.   |
| AUX_WIN_EN   | 24          | 0x0            | Auxiliary window enable/disable.<br>0=Disable<br>1=Enable   |
| AUX_WIN_OUT_DELAY  | 28:25       | 0x5            | Pixel accurate adjustment of AUXWIN position. Allows it to delayed relative to the RGB signals from the DAC.<br>Available settings are:<br>000 = -5 pixels<br>001 = -4 pixels<br>010 = -3 pixels<br>011 = -2 pixels<br>100 = -1 pixel<br>101 = 0 pixels<br>110 = +1 pixels<br>111 = +2 pixels |
| RESERVED   | 30          | 0x1            | Not used in this ASIC   |
| AUX_WIN_LOCK<br><i>(mirror of<br/>AUX_WINDOW_VERT_CNTL:AUX_WIN_LOCK)</i> | 31          | 0x0            | Locks AUX_WIN register fields to allow atomic update of all fields at once when unlocked.<br>0 = not locked, 1 = locked<br>0=don't lock<br>1=lock   |

Auxiliary window horizontal controls

| <b>AUX_WINDOW_VERT_CNTL - RW - 32 bits - [MMReg:0x2DC]</b> |             |                |   |
|--|-------------|----------------|---|
| <b>Field Name</b>  | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| AUX_WIN_VERT_START   | 11:0        | 0x0            | Line coordinate of top edge of auxiliary window.  |
| AUX_WIN_VERT_END   | 27:16       | 0x0            | Line coordinate of bottom edge of auxiliary window.   |
| AUX_WINDOW_POL   | 30          | 0x0            | Selects whether AUXWIN output is high or low when raster inside window coordinates.<br>0 = active high<br>1 = active low<br>0=Active high<br>1=Active low |
| AUX_WIN_LOCK   | 31          | 0x0            | Locks AUX_WIN register fields to allow atomic update of all fields at once when unlocked.<br>0 = not locked, 1 = locked<br>0=don't lock<br>1=lock         |

Auxiliary window vertical controls

**33. Snapshot Detailed Register Reference**

## Snapshot Control Registers

**SNAPSHOT\_VH\_COUNTS - R - 32 bits - [MMReg:0x240]**

| Field Name      | Bits  | Default | Description |
|-----------------|-------|---------|-------------|
| SNAPSHOT_HCOUNT | 9:0   | 0x0     |             |
| SNAPSHOT_VCOUNT | 27:16 | 0x0     |             |

No description available for this register.

**SNAPSHOT\_F\_COUNT - R - 32 bits - [MMReg:0x244]**

| Field Name       | Bits | Default | Description |
|------------------|------|---------|-------------|
| SNAPSHOT_F_COUNT | 20:0 | 0x0     |             |

No description available for this register.

**N\_VIF\_COUNT - RW - 32 bits - [MMReg:0x248]**

| Field Name         | Bits | Default | Description |
|--------------------|------|---------|-------------|
| N_VIF_COUNT_VAL    | 9:0  | 0x0     |             |
| GENLOCK_SOURCE_SEL | 31   | 0x0     |             |

No description available for this register.

**SNAPSHOT\_VIF\_COUNT - RW - 32 bits - [MMReg:0x24C]**

| Field Name                 | Bits  | Default | Description |
|----------------------------|-------|---------|-------------|
| LSNAPSHOT_VIF_COUNT (R)    | 9:0   | 0x0     |             |
| USNAPSHOT_VIF_COUNT (R)    | 20:10 | 0x0     |             |
| AUTO_SNAPSHOT_TAKEN_RD (R) | 24    | 0x0     |             |
| AUTO_SNAPSHOT_TAKEN_WR (W) | 24    | 0x0     |             |
| MANUAL_SNAPSHOT_NOW        | 25    | 0x0     |             |

No description available for this register.

**SNAPSHOT2\_VH\_COUNTS - R - 32 bits - [MMReg:0x340]**

| Field Name       | Bits  | Default | Description |
|------------------|-------|---------|-------------|
| SNAPSHOT2_HCOUNT | 9:0   | 0x0     |             |
| SNAPSHOT2_VCOUNT | 27:16 | 0x0     |             |

No description available for this register.

**SNAPSHOT2\_F\_COUNT - R - 32 bits - [MMReg:0x344]**

| Field Name        | Bits | Default | Description |
|-------------------|------|---------|-------------|
| SNAPSHOT2_F_COUNT | 20:0 | 0x0     |             |

No description available for this register.

**N\_VIF2\_COUNT - RW - 32 bits - [MMReg:0x348]**

| Field Name          | Bits | Default | Description |
|---------------------|------|---------|-------------|
| N_VIF2_COUNT_VAL    | 9:0  | 0x0     |             |
| GENLOCK2_SOURCE_SEL | 31   | 0x0     |             |

No description available for this register.

**SNAPSHOT2\_VIF\_COUNT - RW - 32 bits - [MMReg:0x34C]**

| Field Name                  | Bits  | Default | Description |
|-----------------------------|-------|---------|-------------|
| LSNAPSHOT2_VIF_COUNT (R)    | 9:0   | 0x0     |             |
| USNAPSHOT2_VIF_COUNT (R)    | 20:10 | 0x0     |             |
| AUTO_SNAPSHOT2_TAKEN_RD (R) | 24    | 0x0     |             |



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**SNAPSHOT2\_VIF\_COUNT - RW - 32 bits - [MMReg:0x34C]**

| Field Name                  | Bits | Default | Description |
|-----------------------------|------|---------|-------------|
| AUTO_SNAPSHOT2_TAKEN_WR (W) | 24   | 0x0     |             |
| MANUAL_SNAPSHOT2_NOW        | 25   | 0x0     |             |

No description available for this register.

**34. HDPcontrol Detailed Register Reference**

HDP Control Registers.

| HOST_PATH_CNTL - RW - 32 bits - [MMReg:0x130] |       |         |   |
|---|-------|---------|---|
| Field Name                                    | Bits  | Default | Description   |
| HDP_APER_CNTL                                 | 23    | 0x0     | Selects how the two PCI linear memory apertures map into the internal 32bit address space of the graphics controller.<br>0=Both host apertures map to same area in MC address space (starting at MC_FB_START). Surface ranges are limited to the size of CONFIG_APER_SIZE.<br>1=Two host apertures are mapped one above the other in MC address space starting at MC_FP_START. i.e. they become one big aperture. Surface ranges can cover the double size of CONFIG_APER_SIZE. |
| HP_LIN_RD_CACHE_DIS                           | 24    | 0x0     | Selects whether to disable HDP prefetching.<br>0=Linear aperture reads taken from HostDataPath cache, if possible.<br>1=Linear aperture reads always sent to memory.  |
| HP_RBBM_LOCK_DIS                              | 25    | 0x0     | Controls coherency between linear aperture cycles and register cycles that affect linear aperture operation (e.g. changing SURFACE registers or VGA write/read mode).<br>This field should normally be 0 to ensure proper coherency, and should be changed only if needed to avoid deadlock problems.<br>0=The RBBM write requests will be held until the data pipe is idle.<br>1=The RBBM write requests will not be held.   |
| HDP_SOFT_RESET                                | 26    | 0x0     | Software reset for HDP.<br>0=HDP running in normal operating mode<br>1=Soft Reset to HDP  |
| HDP_WRITE_COMBINER_TIMEOUT                    | 30:28 | 0x0     | Controls internal timeout for write combining optimization. This allows separate dword writes to be combined into octawords before sending to the internal memory controller. This reduces bandwidth cost of slave writes and increases performance.<br>It is recommended this register be set to 0x7 (28 BCLKs) unless otherwise noted.<br>0=0 BCLK<br>1=4 BCLK<br>2=8 BCLK<br>3=12 BCLK<br>4=16 BCLK<br>5=20 BCLK<br>6=24 BCLK<br>7=28 BCLK                                   |
| HP_TEST_RST_CNTL                              | 31    | 0x0     | For HW test and debugging only. No use to software.   |

Controls for the Merged Register Bus internal to the controller for non-FIFOed register writes, and all register reads

| MEM_VGA_WP_SEL - RW - 32 bits - [IOReg,MMReg:0x38] |       |         |   |
|--|-------|---------|---|
| Field Name   | Bits  | Default | Description   |
| MEM_VGA_WPS0                                       | 11:0  | 0x0     | Write page pointer for lower 32 KByte aperture into 128 MByte video memory. |
| MEM_VGA_WPS1                                       | 27:16 | 0x0     | Write page pointer for upper 32 KByte aperture into 128 MByte video memory. |

**MEM\_VGA\_WP\_SEL - RW - 32 bits - [IOReg,MMReg:0x38]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

Two write page pointers used for the two small 32K apertures at 0xA000 and 0xA800. Pages are selectable only on 32K boundaries.

**MEM\_VGA\_RP\_SEL - RW - 32 bits - [IOReg,MMReg:0x3C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|              |      |     |  |
|--------------|------|-----|--|
| MEM_VGA_RPS0 | 11:0 | 0x0 | Read page pointer for lower 32 KByte aperture into 128 MByte video memory. |
|--------------|------|-----|--|

|              |       |     |  |
|--------------|-------|-----|--|
| MEM_VGA_RPS1 | 27:16 | 0x0 | Read page pointer for upper 32 KByte aperture into 128 MByte video memory. |
|--------------|-------|-----|--|

Two read page pointers used for the two small 32K apertures at 0xA000 and 0xA800. Pages are selectable only on 32K boundaries.

**SW\_SEMAPHORE - RW - 32 bits - [MMReg:0x13C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|              |      |     |   |
|--------------|------|-----|---|
| SW_SEMAPHORE | 15:0 | 0x0 | Scratch register for use by software to implement status flags and semaphores. No affect on the hardware. |
|--------------|------|-----|---|

Scratch register

**GEN\_INT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x40]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                               |   |     |   |
|-------------------------------|---|-----|---|
| CRTC_VBLANK_MASK<br>(DISPLAY) | 0 | 0x0 | Vertical blank interrupt mask.<br>0=Disable<br>1=Enable |
|-------------------------------|---|-----|---|

|                              |   |     |  |
|------------------------------|---|-----|--|
| CRTC_VLINE_MASK<br>(DISPLAY) | 1 | 0x0 | Vertical line interrupt mask.<br>0=Disable<br>1=Enable |
|------------------------------|---|-----|--|

|                              |   |     |  |
|------------------------------|---|-----|--|
| CRTC_VSYNC_MASK<br>(DISPLAY) | 2 | 0x0 | Vertical sync interrupt mask.<br>0=Disable<br>1=Enable |
|------------------------------|---|-----|--|

|                            |   |     |   |
|----------------------------|---|-----|---|
| SNAPSHOT_MASK<br>(DISPLAY) | 3 | 0x0 | Snapshot interrupt mask.<br>0=Disable<br>1=Enable |
|----------------------------|---|-----|---|

|                             |   |     |  |
|-----------------------------|---|-----|--|
| FP_DETECT_MASK<br>(DISPLAY) | 4 | 0x0 | Hot plug detect (HPD) interrupt mask.<br>0=Disable<br>1=Enable |
|-----------------------------|---|-----|--|

|                               |   |     |                       |
|-------------------------------|---|-----|-----------------------|
| CRTC2_VLINE_MASK<br>(DISPLAY) | 5 | 0x0 | 0=Disable<br>1=Enable |
|-------------------------------|---|-----|-----------------------|

|                               |   |     |                       |
|-------------------------------|---|-----|-----------------------|
| CRTC2_VSYNC_MASK<br>(DISPLAY) | 6 | 0x0 | 0=Disable<br>1=Enable |
|-------------------------------|---|-----|-----------------------|

|                             |   |     |                       |
|-----------------------------|---|-----|-----------------------|
| SNAPSHOT2_MASK<br>(DISPLAY) | 7 | 0x0 | 0=Disable<br>1=Enable |
|-----------------------------|---|-----|-----------------------|

|                                |   |     |                       |
|--------------------------------|---|-----|-----------------------|
| CRTC2_VBLANK_MASK<br>(DISPLAY) | 9 | 0x0 | 0=Disable<br>1=Enable |
|--------------------------------|---|-----|-----------------------|

|                              |    |     |                       |
|------------------------------|----|-----|-----------------------|
| FP2_DETECT_MASK<br>(DISPLAY) | 10 | 0x0 | 0=Disable<br>1=Enable |
|------------------------------|----|-----|-----------------------|

**GEN\_INT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x40]**

| Field Name                            | Bits | Default | Description  |
|---------------------------------------|------|---------|--|
| VSYNC_DIFF_OVER_LIMIT_MASK<br>(TVOUT) | 11   | 0x0     | 0=Disable<br>1=Enable  |
| DMA_VIPH0_INT_EN<br>(VIP)             | 12   | 0x0     | 0=Disable<br>1=Enable  |
| DMA_VIPH1_INT_EN<br>(VIP)             | 13   | 0x0     | 0=Disable<br>1=Enable  |
| DMA_VIPH2_INT_EN<br>(VIP)             | 14   | 0x0     | 0=Disable<br>1=Enable  |
| DMA_VIPH3_INT_EN<br>(VIP)             | 15   | 0x0     | 0=Disable<br>1=Enable  |
| I2C_INT_EN<br>(VIP)                   | 17   | 0x0     | 0=Disable<br>1=Enable  |
| GUI_IDLE_MASK<br>(RBBM)               | 19   | 0x0     | GUI idle interrupt mask.<br>0=Disable<br>1=Enable                  |
| VIPH_INT_EN<br>(VIP)                  | 24   | 0x0     | 0=Disable<br>1=Enable  |
| SW_INT_EN<br>(HDP)                    | 25   | 0x0     | Software interrupt mask.<br>0=Disable<br>1=Enable                  |
| GEYSERVILLE_MASK<br>(VIP)             | 27   | 0x0     | 0=Disable<br>1=Enable  |
| HDCP_AUTHORIZED_INT_MASK<br>(DISPLAY) | 28   | 0x0     | 0=Disable<br>1=Enable  |
| DVI_I2C_INT_MASK<br>(DISPLAY)         | 29   | 0x0     | 0=Disable<br>1=Enable  |
| GUIDMA_MASK<br>(CP)                   | 30   | 0x0     | GUI DMA channel interrupt mask.<br>0=Disable<br>1=Enable           |
| VIDDMA_MASK<br>(CP)                   | 31   | 0x0     | Video capture DMA channel interrupt mask.<br>0=Disable<br>1=Enable |

General Interrupt Control register.

The MASK/EN fields control whether the respective status bits are enabled to drive the system interrupt pin. Even if enabled here, the interrupt line is not driven unless enabled in the PCI configuration space.

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                           | Bits | Default | Description  |
|--------------------------------------|------|---------|--|
| CRTC_VBLANK_STAT (R)<br>(DISPLAY)    | 0    | 0x0     | Vertical blank interrupt. Set when display in vertical retrace.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| CRTC_VBLANK_STAT_AK (W)<br>(DISPLAY) | 0    | 0x0     | Vertical blank interrupt acknowledge.<br>0=No effect<br>1=Clear status   |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                           | Bits | Default | Description  |
|--------------------------------------|------|---------|--|
| CRTC_VLINE_STAT (R)<br>(DISPLAY)     | 1    | 0x0     | Vertical line interrupt. Set on display line on programmed by the CRTC_VLINE_CRNT_VLINE.CRTC_VLINE register.<br>0=No event<br>1=Event has occurred, interrupting if enabled      |
| CRTC_VLINE_STAT_AK (W)<br>(DISPLAY)  | 1    | 0x0     | Vertical line interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| CRTC_VSYNC_STAT (R)<br>(DISPLAY)     | 2    | 0x0     | Vertical sync interrupt. Set on start of VSYNC at the DAC.<br>0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC_VSYNC_STAT_AK (W)<br>(DISPLAY)  | 2    | 0x0     | Vertical sync interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| SNAPSHOT_STAT (R)<br>(DISPLAY)       | 3    | 0x0     | Snapshot interrupt. Set as controlled by SNAPSHOT_VIF_COUNT register.<br>0=No event<br>1=Event has occurred, interrupting if enabled   |
| SNAPSHOT_STAT_AK (W)<br>(DISPLAY)    | 3    | 0x0     | Snapshot interrupt acknowledge.<br>0=No effect<br>1=Clear status   |
| FP_DETECT_STAT (R)<br>(DISPLAY)      | 4    | 0x0     | Hot plug detect (HPD) interrupt. Set on HPD connect or disconnect as controlled by FP_GEN_CNTL.FP_DETECT_INT_POL.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| FP_DETECT_STAT_AK (W)<br>(DISPLAY)   | 4    | 0x0     | Hot plug detect (HPD) interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| CRTC2_VLINE_STAT (R)<br>(DISPLAY)    | 5    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC2_VLINE_STAT_AK (W)<br>(DISPLAY) | 5    | 0x0     | 0=No effect<br>1=Clear status  |
| CRTC2_VSYNC_STAT (R)<br>(DISPLAY)    | 6    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC2_VSYNC_STAT_AK (W)<br>(DISPLAY) | 6    | 0x0     | 0=No effect<br>1=Clear status  |
| SNAPSHOT2_STAT (R)<br>(DISPLAY)      | 7    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| SNAPSHOT2_STAT_AK (W)<br>(DISPLAY)   | 7    | 0x0     | 0=No effect<br>1=Clear status  |
| CAPO_INT_ACTIVE (R)<br>(VIP)         | 8    | 0x0     | Capture port 0 has active interrupt(s).<br>0=Capture port 0 not source of any active interrupt<br>1=Capture port 0 has active interrupt(s)                                       |
| CRTC2_VBLANK_STAT (R)<br>(DISPLAY)   | 9    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                                   | Bits | Default | Description   |
|--|------|---------|---|
| CRTC2_VBLANK_STAT_AK (W)<br>(DISPLAY)        | 9    | 0x0     | 0=No effect<br>1=Clear status   |
| FP2_DETECT_STAT (R)<br>(DISPLAY)             | 10   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| FP2_DETECT_STAT_AK (W)<br>(DISPLAY)          | 10   | 0x0     | 0=No effect<br>1=Clear status   |
| VSYNC_DIFF_OVER_LIMIT_STAT (R)<br>(TVOUT)    | 11   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| VSYNC_DIFF_OVER_LIMIT_STAT_AK (W)<br>(TVOUT) | 11   | 0x0     | 0=No effect<br>1=Clear status   |
| DMA_VIPH0_INT (R)<br>(VIP)                   | 12   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DMA_VIPH0_INT_AK (W)<br>(VIP)                | 12   | 0x0     | 0=No effect<br>1=Clear status   |
| DMA_VIPH1_INT (R)<br>(VIP)                   | 13   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DMA_VIPH1_INT_AK (W)<br>(VIP)                | 13   | 0x0     | 0=No effect<br>1=Clear status   |
| DMA_VIPH2_INT (R)<br>(VIP)                   | 14   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DMA_VIPH2_INT_AK (W)<br>(VIP)                | 14   | 0x0     | 0=No effect<br>1=Clear status   |
| DMA_VIPH3_INT (R)<br>(VIP)                   | 15   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DMA_VIPH3_INT_AK (W)<br>(VIP)                | 15   | 0x0     | 0=No effect<br>1=Clear status   |
| I2C_INT (R)<br>(VIP)                         | 17   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| I2C_INT_AK (W)<br>(VIP)                      | 17   | 0x0     | 0=No effect<br>1=Clear status   |
| GUI_IDLE_STAT (R)<br>(RBBM)                  | 19   | 0x1     | GUI idle interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled  |
| GUI_IDLE_STAT_AK (W)<br>(RBBM)               | 19   | 0x0     | GUI idle interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| VIPH_INT (R)<br>(VIP)                        | 24   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| SW_INT (R)<br>(HDP)                          | 25   | 0x0     | Software interrupt. General purpose interrupt that can only be set by software event by writing to SW_INT_SET.<br>0=No event<br>1=Event has occurred, interrupting if enabled |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                                | Bits | Default | Description   |
|---|------|---------|---|
| SW_INT_AK (W)<br>(HDP)                    | 25   | 0x0     | Software interrupt acknowledge.<br>0=No effect<br>1=Clear SW_INT (set low)                          |
| SW_INT_SET (W)<br>(HDP)                   | 26   | 0x0     | Software interrupt trigger.<br>0=No effect<br>1=Set SW_INT active (high)                            |
| GEYSERVILLE_STAT (R)<br>(VIP)             | 27   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| GEYSERVILLE_STAT_AK (W)<br>(VIP)          | 27   | 0x0     | 0=No effect<br>1=Clear status   |
| HDCP_AUTHORIZED_INT_STAT (R)<br>(DISPLAY) | 28   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| HDCP_AUTHORIZED_INT_AK (W)<br>(DISPLAY)   | 28   | 0x0     | 0=No effect<br>1=Clear status   |
| DVI_I2C_INT_STAT (R)<br>(DISPLAY)         | 29   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DVI_I2C_INT_AK (W)<br>(DISPLAY)           | 29   | 0x0     | 0=No effect<br>1=Clear status   |
| GUIDMA_STAT (R)<br>(CP)                   | 30   | 0x0     | GUI DMA channel interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled           |
| GUIDMA_AK (W)<br>(CP)                     | 30   | 0x0     | GUI DMA channel interrupt acknowledge.<br>0=No effect<br>1=Clear status                             |
| VIDDMA_STAT (R)<br>(CP)                   | 31   | 0x0     | Video capture DMA channel interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| VIDDMA_AK (W)<br>(CP)                     | 31   | 0x0     | Video capture DMA channel interrupt acknowledge.<br>0=No effect<br>1=Clear status                   |

General Interrupt Status register.

These fields can be polled and acknowledged even if interrupts are disabled, or the respective fields are masked in the GEN\_INT\_CNTL register.

**CRTC\_EXT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x54]**

| Field Name                      | Bits | Default | Description   |
|---------------------------------|------|---------|---|
| CRTC_VGA_XOVERSCAN<br>(DISPLAY) | 0    | 0x0     | Set low for VGA compatible borders. When set high extended overscan registers control border in VGA modes. See also auto-centering in CRTC_MORE_CNTL and FP_GEN_CNTL.CRTC_VGA_XOVERSCAN_COLOR.<br>0=Disable extended overscan in VGA<br>1=Enable extended overscan in VGA |
| VGA_BLINK_RATE<br>(DISPLAY)     | 2:1  | 0x0     | Controls number of frames per blink for VGA modes.<br>0=Default VGA blink rate (16 frames)<br>1=1/2 default VGA blink rate (32 frames)<br>2=1/3 default VGA blink rate (48 frames)<br>3=1/4 default VGA blink rate (64 frames)  |



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**CRTC\_EXT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x54]**

| Field Name                           | Bits | Default | Description   |
|--------------------------------------|------|---------|---|
| VGA_ATI_LINEAR<br>(HDP) (DISPLAY)    | 3    | 0x0     | Enable linear addressing through VGA memory aperture.<br>0=Disable<br>1=Enable  |
| VGA_128KAP_PAGING<br>(HDP) (DISPLAY) | 4    | 0x0     | Enable extended aperture paging in 128K VGA aperture mode.<br>0=Normal<br>1=Enable  |
| VGA_TEXT_132<br>(HDP) (DISPLAY)      | 5    | 0x0     | Extended text mode select (linear address 132 column text mode). Set low for VGA compatible 40 or 80 column text modes.<br>0=inActive<br>1=Active   |
| VGA_XCRT_CNT_EN<br>(DISPLAY)         | 6    | 0x0     | Extended CRTC display address counter enable. Active High<br>0=Disable<br>1=Enable Ext CRTC Counter   |
| CRTC_HSYNC_DIS<br>(DISPLAY)          | 8    | 0x0     | Disables horizontal sync output. Could be used for DPMS signaling, but DISP_PWR_MAN.DISP_PWR_MAN_DPMS is recommended instead.<br>0=Enable<br>1=Disable  |
| CRTC_VSYNC_DIS<br>(DISPLAY)          | 9    | 0x0     | Disables vertical sync output. Could be used for DPMS signaling, but DISP_PWR_MAN.DISP_PWR_MAN_DPMS is recommended instead.<br>Note this must remain enabled while using composite SYNC on HSYNC (CRTC_C_SYNC_EN=1).<br>0=Enable<br>1=Disable   |
| CRTC_DISPLAY_DIS<br>(DISPLAY)        | 10   | 0x0     | Disables the display, forcing the blanking signal to be active.<br>When blanking the screen with this bit, the overlay, sub-picture, graphics and cursor should also be disabled to save power. See CRTC_DISP_REQ_EN_B, CRTC_CUR_EN, OV0_OVERLAY_EN and SUBPIC_ON.<br>0=Enable<br>1=Blanked |
| CRTC_SYNC_TRISTATE<br>(DISPLAY)      | 11   | 0x0     | Tristates HSYNC and VSYNC outputs. For individual tristate control, see the next two fields.<br>0=Normal<br>1=Tristate HSYNC and VSYNC outputs  |
| CRTC_HSYNC_TRISTATE<br>(DISPLAY)     | 12   | 0x0     | Tristates HSYNC output.<br>0=Normal HSYNC<br>1=Tristate HSYNC output  |
| CRTC_VSYNC_TRISTATE<br>(DISPLAY)     | 13   | 0x0     | Tristates VSYNC output.<br>This is recommended for use with composite sync mode when only the HSYNC output pin should be enabled.<br>0=Normal VSYNC<br>1=Tristate VSYNC output  |
| CRT_ON<br>(DISPLAY)                  | 15   | 0x0     | 0=CRT OFF<br>1=CRT ON   |

**CRTC\_EXT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x54]**

| Field Name                          | Bits  | Default | Description  |
|-------------------------------------|-------|---------|--|
| VGA_CUR_B_TEST<br>(DISPLAY)         | 17    | 0x0     | Test cursor blinking. Only used for diagnostic testing.<br>0=Disable VGA cursor test<br>1=Test VGA cursor blinking   |
| VGA_PACK_DIS<br>(HDP)               | 18    | 0x0     | Controls host write pipe for packed VGA modes (e.g. mode 13). Should only be set high if HW problem with fast writes.<br>0=Fast VGA write in packed modes<br>1=Normal VGA write in packed modes  |
| VGA_MEM_PS_EN<br>(HDP)              | 19    | 0x0     | VGA page select enable:<br>0=Don't use MEM_VGA_WP_SEL and MEM_VGA_RP_SEL registers<br>1=Use MEM_VGA_WP_SEL and MEM_VGA_RP_SEL registers  |
| VCRTC_IDX_MASTER<br>(HDP) (DISPLAY) | 30:24 | 0x0     | VGA CRTC master index. Only bits 5:0 of the VGA CRTC index can be written (or read) in VGA I/O space at 0x3B4 or 0x3D4. Bit 6 controls whether the master or shadow set of VGA CRTC registers is seen in VGA I/O space. The shadow set is for use when supporting panel operation in VGA modes. The BIOS will leave either the master or shadow set active as needed after a mode switch call. |

More CRTC general controls

**GENMO\_RD - R - 8 bits - VGA\_IO:0x3CC**

| Field Name  | Bits | Default | Description   |
|---|------|---------|---|
| GENMO_MONO_ADDRESS_B<br><i>(mirror of GENMO_WT:GENMO_MONO_ADDRESS_B)</i><br>(BIF) | 0    | 0x0     | VGA addressing mode.  |
| VGA_RAM_EN<br><i>(mirror of GENMO_WT:VGA_RAM_EN)</i><br>(BIF)                     | 1    | 0x0     | Enables/Disables CPU access to video RAM at VGA aperture.   |
| VGA_CKSEL<br><i>(mirror of GENMO_WT:VGA_CKSEL)</i><br>(DISPLAY)                   | 3:2  | 0x0     | Selects pixel clock frequency to use.   |
| ODD_EVEN_MD_PGSEL<br><i>(mirror of GENMO_WT:ODD_EVEN_MD_PGSEL)</i><br>(HDP)       | 5    | 0x0     | This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled. Used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory.                       |
| VGA_HSYNC_POL<br><i>(mirror of GENMO_WT:VGA_HSYNC_POL)</i><br>(DISPLAY)           | 6    | 0x0     | Determines polarity of horizontal sync (HSYNC) for VGA modes.<br>0 = HSYNC pulse active high<br>1 = HSYNC pulse active low<br>The convention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes. |



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**GENMO\_RD - R - 8 bits - VGA\_IO:0x3CC**

| Field Name  | Bits | Default | Description  |
|---|------|---------|--|
| VGA_VSYNC_POL<br><i>(mirror of GENMO_WT:VGA_VSYNC_POL)</i><br><br>(DISPLAY) | 7    | 0x0     | Determines polarity of vertical sync (VSYNC) for VGA modes.<br>0 = VSYNC pulse active high<br>1 = VSYNC pulse active low<br>The covention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes. |

Miscellaneous Output Register (Read)

**GENMO\_WT - W - 8 bits - VGA\_IO:0x3C2**

| Field Name                        | Bits | Default | Description  |
|-----------------------------------|------|---------|--|
| GENMO_MONO_ADDRESS_B<br><br>(BIF) | 0    | 0x0     | VGA addressing mode.<br>0=Monochrome emulation, regs at 0x3Bx<br>1=Color/Graphic emulation, regs at 0x3Dx  |
| VGA_RAM_EN<br><br>(BIF)           | 1    | 0x0     | Enables/Disables CPU access to video RAM at VGA aperture.<br>0=Disable<br>1=Enable   |
| VGA_CKSEL<br><br>(DISPLAY)        | 3:2  | 0x0     | Selects pixel clock frequency to use in VGA modes. Used when CRTC_GEN_CNTL.CRTC_EXT_DISP_EN=0. See CLOCK_CNTL_INDEX.PPLL_DIV_SEL for non-VGA mode pixel clock selection.<br>0=25.1744MHz (640 Pels)<br>1=28.3212MHz (720 Pels)<br>2=Reserved<br>3=Reserved   |
| ODD_EVEN_MD_PGSEL<br><br>(HDP)    | 5    | 0x0     | This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled.<br>Used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory.<br>0=Selects odd (high) memory locations<br>1=Selects even (low) memory locations |
| VGA_HSYNC_POL<br><br>(DISPLAY)    | 6    | 0x0     | Determines polarity of horizontal sync (HSYNC) for VGA modes.<br>0 = HSYNC pulse active high<br>1 = HSYNC pulse active low<br>The covention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes.   |
| VGA_VSYNC_POL<br><br>(DISPLAY)    | 7    | 0x0     | Determines polarity of vertical sync (VSYNC) for VGA modes.<br>0 = VSYNC pulse active high<br>1 = VSYNC pulse active low<br>The covention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes.   |

Miscellaneous Output Register (Write)

**MC\_FB\_LOCATION - RW - 32 bits - [MMReg:0x148]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



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**MC\_FB\_LOCATION - RW - 32 bits - [MMReg:0x148]**

| Field Name                | Bits  | Default | Description  |
|---------------------------|-------|---------|--|
| MC_FB_START<br>(MC) (HDP) | 15:0  | 0x0     | Start of local frame buffer section of 32 bit internal address space. Recommend setting this register to same as CONFIG_APER_0_BASE.APER_0_BASE shr 16.<br><br>NOTE: Bits 0:5 of this field are hardwired to ZERO.                         |
| MC_FB_TOP<br>(MC)         | 31:16 | 0x3f    | End of local frame buffer section of 32 bit internal address space. Recommend setting this register to (CONFIG_APER_0_BASE.APER_0_BASE + CONFIG_APER_SIZE.APER_SIZE - 1) shr 16.<br><br>NOTE: Bits 0:5 of this field are hardwired to ONE. |

This register defines the location of the frame buffer in the internal address space. The internal address space has 32 address bits. Minimum Frame buffer size for Rage 5 is 2 MB, and the start location is required to be on a 4 MB boundary. Therefore START(21:0) must be 0x000000 and TOP(21:0) must be 0x3FFFFFF. Only the 16 MSBs of each are loaded in the register.

**35. VGA GRPH Detailed Register Reference**

VGA Graphics Controller Registers.

**GRPH8\_IDX - RW - 8 bits - VGA\_IO:0x3CE**

| Field Name   | Bits | Default | Description   |
|--|------|---------|---|
| GRPH_IDX<br>(HDP) (DISPLAY)<br>GRPH Index Register | 3:0  | 0x0     | This index is used to address one of the internal registers of the graphics controller (GRAC) at I/O port 0x3CRF. |

**GRPH8\_DATA - RW - 8 bits - VGA\_IO:0x3CF**

| Field Name   | Bits | Default | Description               |
|--|------|---------|---------------------------|
| GRPH_DATA<br>(HDP) (DISPLAY)<br>GRPH Data Register | 7:0  | 0x0     | GRPH data indirect access |

**GRA00 - RW - 8 bits - VGAGRPHIND:0x0**

| Field Name      | Bits | Default | Description     |
|-----------------|------|---------|-----------------|
| GRPH_SET_RESET0 | 0    | 0x0     | Set/Reset Map 0 |
| GRPH_SET_RESET1 | 1    | 0x0     | Set/Reset Map 1 |
| GRPH_SET_RESET2 | 2    | 0x0     | Set/Reset Map 2 |
| GRPH_SET_RESET3 | 3    | 0x0     | Set/Reset Map 3 |

Set/Reset Register

**GRA01 - RW - 8 bits - VGAGRPHIND:0x1**

| Field Name          | Bits | Default | Description            |
|---------------------|------|---------|------------------------|
| GRPH_SET_RESET_ENA0 | 0    | 0x0     | Enable Set/Reset Map 0 |
| GRPH_SET_RESET_ENA1 | 1    | 0x0     | Enable Set/Reset Map 1 |
| GRPH_SET_RESET_ENA2 | 2    | 0x0     | Enable Set/Reset Map 2 |
| GRPH_SET_RESET_ENA3 | 3    | 0x0     | Enable Set/Reset Map 3 |

Enable Set/Reset Register

**GRA02 - RW - 8 bits - VGAGRPHIND:0x2**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| GRPH_CCOMP | 3:0  | 0x0     | Colour Compare Map bits 3:0. In Read mode (GRA05[3] being logical 1), the 4 bits from this register are compared with the 4-bit PEL value (made up of one bit from each map), from bit positions 0 through 7. As long as the colour don't care bits (GRA07[0:3]) for the respective maps are logical 1's, the compare takes place only on those bits of the PEL value, and the CPU reads a one for a match in that bit position. If Colour Don't Care bit for one map is a logical zero, the latched data from the map is excluded from the compare, and only the remaining three bits are compared to generate bus data. |

Colour Compare Register

**GRA03 - RW - 8 bits - VGAGRPHIND:0x3**

| Field Name  | Bits | Default | Description   |
|-------------|------|---------|---|
| GRPH_ROTATE | 2:0  | 0x0     | Rotate Count Bits 2-0. Specifies the number of bit positions that the CPU data is to be rotated to the right, before doing the function selected by bits 3 and 4 above and subsequencey bit mask select and write operations. Rotation is carried out only in write modes 0 and 3. In these two modes, the CPU data is rotated first, the operated only the function bits GRA03[4:3], the updated by the bit mask register GRA05. |
| GRPH_FN_SEL | 4:3  | 0x0     | Function Select Bits 1 and 2. These funcitons are performed on the CPU data before the selected bits are updated by the bit mask register, and then written to the display buffers.<br>0=Replace<br>1=AND<br>2=OR<br>3=XOR  |

Data Rotate Register

**GRA04 - RW - 8 bits - VGAGRPHIND:0x4**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| GRPH_RMAP  | 1:0  | 0x0     | Read Mode 0 Only: GRA controller returns the contents of one of the four latched buffer bytes to CPU each time a CPU read loads these latches. The 2 bits (0 and 1) define a value that represents the bit map where CPU is to read data - usefull in transferring bit map data between the maps and system RAM. |

Read Map Select Register

**GRA05 - RW - 8 bits - VGAGRPHIND:0x5**

| Field Name                  | Bits | Default | Description  |
|-----------------------------|------|---------|--|
| GRPH_WRITE_MODE<br>(HDP)    | 1:0  | 0x0     | Write Mode:<br>0=Write mode 0<br>1=Write mode 1<br>2=Write mode 2<br>3=Write mode 3  |
| GRPH_READ1<br>(HDP)         | 3    | 0x0     | Read Mode:<br>0=Read mode 0, byte oriented<br>1=Read mode 1, pixel oriented  |
| CGA_ODDEVEN<br>(HDP)        | 4    | 0x0     | Odd/Even Addressing Enable. Used to enable CGA emulation, this bit enables off/even addressing mode when it is logical one. Normally, this bit and memory mode bit SEQ04[2] are set to agree with each other in enabling odd/even mode emulation.<br>0=Disable Odd/Even Addressing<br>1=Enable Odd/Even Addressing |
| GRPH_OES<br>(HDP) (DISPLAY) | 5    | 0x0     | Shift Register Mode: This bit controls how data from memory is loaded into the shift registers M0D0:M0D7, M1D0:M1D7; M2D0:M2D7, and M3D0:M3D7 are representations of this data.<br>0=Linear shift mode<br>1=Tiled shift mode   |



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**GRA05 - RW - 8 bits - VGAGRPHIND:0x5**

| Field Name                   | Bits | Default | Description   |
|------------------------------|------|---------|---|
| GRPH_PACK<br>(HDP) (DISPLAY) | 6    | 0x0     | 256 Colour Mode. This bit also controls how data from memory is loaded into the shift registers.<br>0=Use shift register mode as per GRPH_OES<br>1=256 color mode, read as packed pixels, ignore GRPH_OES |

Graphics Mode Register

**GRA06 - RW - 8 bits - VGAGRPHIND:0x6**

| Field Name    | Bits | Default | Description  |
|---------------|------|---------|--|
| GRPH_GRAPHICS | 0    | 0x0     | Graphics/Alphanumeric Mode<br>0=Alpha Numeric Mode<br>1=Graphics Mode                                    |
| GRPH_ODDEVEN  | 1    | 0x0     | Chains Odd Maps to Even<br>0=Normal<br>1=Chain Odd maps to Even  |
| GRPH_ADRSEL   | 3:2  | 0x0     | Memory Map Read Bits 1 and 0, respectively.<br>0=A0000-128K<br>1=A0000-64K<br>2=B0000-32K<br>3=B8000-32K |

Graphics Miscellaneous Register

**GRA07 - RW - 8 bits - VGAGRPHIND:0x7**

| Field Name  | Bits | Default | Description   |
|-------------|------|---------|---|
| GRPH_XCARE0 | 0    | 0x0     | Ignore Map 0<br>0=Ignore map 0<br>1=Use map 0 for read mode 1 |
| GRPH_XCARE1 | 1    | 0x0     | Ignore Map 1<br>0=Ignore map 1<br>1=Use map 1 for read mode 1 |
| GRPH_XCARE2 | 2    | 0x0     | Ignore Map 2<br>0=Ignore map 2<br>1=Use map 2 for read mode 1 |
| GRPH_XCARE3 | 3    | 0x0     | Ignore Map 3<br>0=Ignore map 3<br>1=Use map 3 for read mode 1 |

Colour Don't Care Register

**GRA08 - RW - 8 bits - VGAGRPHIND:0x8**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| GRPH_BMSK  | 7:0  | 0x0     | Bit Mask    |

Bit Mask Register

**36. VGA\_SEQ Detailed Register Reference**

VGA Sequencer Registers.

**SEQ8\_IDX - RW - 8 bits - VGA\_IO:0x3C4**

| Field Name                 | Bits | Default | Description  |
|----------------------------|------|---------|--|
| SEQ_IDX<br>(HDP) (DISPLAY) | 2:0  | 0x0     | This index points to one of the sequencer registers (SEQ_) at I/O port address 0x3C5, for the next SEQ read/write operation. |

SEQ Index Register

**SEQ8\_DATA - RW - 8 bits - VGA\_IO:0x3C5**

| Field Name                  | Bits | Default | Description              |
|-----------------------------|------|---------|--------------------------|
| SEQ_DATA<br>(HDP) (DISPLAY) | 7:0  | 0x0     | SEQ data indirect access |

SEQ Data Register

**SEQ02 - RW - 8 bits - VGASEQIND:0x2**

| Field Name  | Bits | Default | Description   |
|-------------|------|---------|---|
| SEQ_MAP0_EN | 0    | 0x0     | Enable map 0<br>0=Disable write to memory map 0<br>1=Enable write to memory map 0 |
| SEQ_MAP1_EN | 1    | 0x0     | Enable map 1<br>0=Disable write to memory map 1<br>1=Enable write to memory map 1 |
| SEQ_MAP2_EN | 2    | 0x0     | Enable map 2<br>0=Disable write to memory map 2<br>1=Enable write to memory map 2 |
| SEQ_MAP3_EN | 3    | 0x0     | Enable map 3<br>0=Disable write to memory map 3<br>1=Enable write to memory map 3 |

Map Mask Register

**SEQ04 - RW - 8 bits - VGASEQIND:0x4**

| Field Name  | Bits | Default | Description   |
|-------------|------|---------|---|
| SEQ_256K    | 1    | 0x0     | Extended memory - 1 indicates 256 KB of video memory is present. It also enables the character map selection in SEQ03.<br>0=64KB memory present. Has no effect since 256KB always available<br>1=256KB memory present |
| SEQ_ODDEVEN | 2    | 0x0     | Odd/Even<br>0=Even CPU address (A0=0) accesses maps 0 and 2.<br>Odd address accesses maps 1 and 3<br>1=Enables sequential access to maps for odd/even modes. SEQ02 (Map Mask) selects which maps are used             |



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**SEQ04 - RW - 8 bits - VGASEQIND:0x4**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SEQ_CHAIN  | 3    | 0x0     | Chain (when logical 1, it takes priority over off/even mode bits SEQ04[2] and GRA05[4]. Unlike odd/even mode, SEQ04[2] is the only bit used to enable chain mode (double odd/even). Chain does not affect CRTIC access to video memory. Odd/even bit SEQ04[2] should be the opposite of GRA05[4].<br>0=Enables sequential access to maps. SEQ02 (Map Mask) selects which maps are used<br>1=For 256 color modes. Map select by CPU address bits A1:A0 |

Memory Mode Register

**37. VGA CRT Detailed Register Reference**

VGA CRT Controller Registers.

**CRTC8\_IDX - RW - 8 bits - [VGA\_IO:0x3B4] [VGA\_IO:0x3D4]**

| Field Name   | Bits | Default | Description   |
|--|------|---------|---|
| VCRTC_IDX<br><i>(mirror bits 0:5 of<br/>CRTC_EXT_CNTL:VCRTC_IDX_MASTER)</i><br><br>(HDP) (DISPLAY) | 5:0  | 0x0     | This index points to one of the internal registers of the CRT controller (CRTC) at address 0x3?5, for the next CRTC read/write operation. |

CRT Index Register

**CRTC8\_DATA - RW - 8 bits - [VGA\_IO:0x3B5] [VGA\_IO:0x3D5]**

| Field Name                        | Bits | Default | Description               |
|-----------------------------------|------|---------|---------------------------|
| VCRTC_DATA<br><br>(HDP) (DISPLAY) | 7:0  | 0x0     | CRTC data indirect access |

CRTC Data Register

**CRT14 - RW - 8 bits - VGACRTIND:0x14**

| Field Name                         | Bits | Default | Description   |
|------------------------------------|------|---------|---|
| UNDRLN_LOC<br><br>(DISPLAY)        | 4:0  | 0x0     | H Row Scan Bits 4-0.- These bits define the horizontal scan row, from the top of the characterline, that should be used for underlining. The 5-bit value is equal to the actual number minus one. |
| ADDR_CNT_BY4<br><br>(DISPLAY)      | 5    | 0x0     | Count-by-4:<br>0=Char. Clock<br>1=CountBy4  |
| DOUBLE_WORD<br><br>(HDP) (DISPLAY) | 6    | 0x0     | Double-Word Mode:<br>0=Disable<br>1=DoubleWordMdEna   |

Underline Location Register

**CRT17 - RW - 8 bits - VGACRTIND:0x17**

| Field Name                    | Bits | Default | Description   |
|-------------------------------|------|---------|---|
| RA0_AS_A13B<br><br>(DISPLAY)  | 0    | 0x0     | Compatibility Mode:   |
| RA1_AS_A14B<br><br>(DISPLAY)  | 1    | 0x0     | Select Row Scan Counter:  |
| VCOUNT_BY2<br><br>(DISPLAY)   | 2    | 0x0     | Vertical_by_2 NOTE: When bit 2 is logical one, other vertical register values should be adjusted as well (CRT06, CRT10, CRT12, CRT15, and CRT18). |
| ADDR_CNT_BY2<br><br>(DISPLAY) | 3    | 0x0     | Count_by_2: ENGINEERING NOTE: Bit can be written and read, but has no effect.   |
| WRAP_A15TOA0<br><br>(DISPLAY) | 5    | 0x0     | Address Wrap: ENGINEERING NOTE: Bit can be written and read, but has no effect.   |

**CRT17 - RW - 8 bits - VGACRTIND:0x17**

| Field Name                   | Bits | Default | Description  |
|------------------------------|------|---------|--|
| BYTE_MODE<br>(HDP) (DISPLAY) | 6    | 0x0     | Byte/Word Mode:<br>0=WordMode<br>1=ByteMode            |
| CRTC_SYNC_EN<br>(DISPLAY)    | 7    | 0x0     | H/V Retrace Enable:<br>0=Disable HVSynC<br>1=EnaHVSynC |

CRT Mode Register

**CRT1E - R - 8 bits - VGACRTIND:0x1E**

| Field Name   | Bits | Default | Description  |
|--------------|------|---------|--|
| GRPH_DEC_RD1 | 1    | 0x0     | This register is used to read back the graphics controller index decode. |

Graphics Controller Index Decode Register

**CRT1F - R - 8 bits - VGACRTIND:0x1F**

| Field Name   | Bits | Default | Description  |
|--------------|------|---------|--|
| GRPH_DEC_RD0 | 7:0  | 0x0     | This register is used to read back the graphics controller index decode. |

Graphics Controller Index Decode Register

**CRT22 - R - 8 bits - VGACRTIND:0x22**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| GRPH_LATCH_DATA | 7:0  | 0x0     | This register is used to read the data in the Graphics Controller CPU data latches. The Graphics Controller Read Map Select register bits 0 and 1 determines which byte is read back. |

RAM Data Latch Readback Register

**CRT14\_S - RW - 8 bits - VGACRTIND:0x54**

| Field Name   | Bits | Default | Description              |
|--|------|---------|--------------------------|
| UNDRLN_LOC_S<br>(DISPLAY)  | 4:0  | 0x0     | Shadow copy UNDRLN_N_LOC |
| ADDR_CNT_BY4_M<br><i>(mirror of CRT14:ADDR_CNT_BY4)</i><br>(DISPLAY)     | 5    | 0x0     | Mirror of ADDR_CNT_BY4   |
| DOUBLE_WORD_M<br><i>(mirror of CRT14:DOUBLE_WORD)</i><br>(HDP) (DISPLAY) | 6    | 0x0     | Mirror of DOUBLE_WORD    |

Shadow of Underline Location Register

**CRT17\_S - RW - 8 bits - VGACRTIND:0x57**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**CRT17\_S - RW - 8 bits - VGACRTIND:0x57**

| Field Name   | Bits | Default | Description               |
|--|------|---------|---------------------------|
| RA0_AS_A13B_M<br><i>(mirror of CRT17:RA0_AS_A13B)</i><br>(DISPLAY)   | 0    | 0x0     | Mirror of RA0_AS_A13B     |
| RA1_AS_A14B_M<br><i>(mirror of CRT17:RA1_AS_A14B)</i><br>(DISPLAY)   | 1    | 0x0     | Mirror of RA1_AS_A14B     |
| VCOUNT_BY2_S<br>(DISPLAY)  | 2    | 0x0     | Shadow copy of VCOUNT_BY2 |
| ADDR_CNT_BY2_M<br><i>(mirror of CRT17:ADDR_CNT_BY2)</i><br>(DISPLAY) | 3    | 0x0     | Mirror of ADDR_CNT_BY2    |
| WRAP_A15TOA0_M<br><i>(mirror of CRT17:WRAP_A15TOA0)</i><br>(DISPLAY) | 5    | 0x0     | Mirror of WRAP_A15TOA0    |
| BYTE_MODE_M<br><i>(mirror of CRT17:BYTE_MODE)</i><br>(HDP) (DISPLAY) | 6    | 0x0     | Mirror of BYTE_MODE       |
| CRTC_SYNC_EN_M<br><i>(mirror of CRT17:CRTC_SYNC_EN)</i><br>(DISPLAY) | 7    | 0x0     | Mirror of CRTC_SYNC_EN    |

Shadow of CRT Mode Register

**CRT1E\_S - R - 8 bits - VGACRTIND:0x5E**

| Field Name  | Bits | Default | Description            |
|---|------|---------|------------------------|
| GRPH_DEC_RD1_M<br><i>(mirror of CRT1E:GRPH_DEC_RD1)</i> | 1    | 0x0     | Mirror of GRPH_DEC_RD1 |

Shadow of CRT1E

**CRT1F\_S - R - 8 bits - VGACRTIND:0x5F**

| Field Name  | Bits | Default | Description            |
|---|------|---------|------------------------|
| GRPH_DEC_RD0_M<br><i>(mirror of CRT1F:GRPH_DEC_RD0)</i> | 7:0  | 0x0     | Mirror of GRPH_DEC_RD0 |

Shadow of CRT1F

**CRT22\_S - R - 8 bits - VGACRTIND:0x62**

| Field Name  | Bits | Default | Description               |
|---|------|---------|---------------------------|
| GRPH_LATCH_DATA_M<br><i>(mirror of CRT22:GRPH_LATCH_DATA)</i> | 7:0  | 0x0     | Mirror of GRPH_LATCH_DATA |

Shadow of CRT22

**38. Tiling Detailed Register Reference**

Frame Buffer Tiling Control Registers.

| <b>SURFACE_CNTL - RW - 32 bits - [MMReg:0xB00]</b> |             |                |  |
|--|-------------|----------------|--|
| <b>Field Name</b>                                  | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| SURF_TRANSLATION_DIS                               | 8           | 0x1            | Disable register for Tiling address translation.<br>0=Enable tiling translation based on SURFACE registers.<br>1=Disable tiling based on SURFACE registers.<br>Swapping still based on SURFACE comparisons and settings. |
| NONSURF_AP0_SWP                                    | 21:20       | 0x0            | Endian Swap control for Aperture 0 accesses not in a surface. Always used when SURF_TRANSLATION_DIS is set to 1.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.    |
| NONSURF_AP1_SWP                                    | 23:22       | 0x0            | Endian Swap control for Aperture 1 accesses not in a surface. Always used when SURF_TRANSLATION_DIS is set to 1.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.    |

General Tiling Control Registers

| <b>SURFACE_ACCESS_FLAGS - R - 32 bits - [MMReg:0xBF8]</b> |             |                |   |
|---|-------------|----------------|---|
| <b>Field Name</b>   | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| SURF0_WRITE_FLAG  | 0           | 0x0            | Indicates if write to surface 0 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared. |
| SURF1_WRITE_FLAG  | 1           | 0x0            | Indicates if write to surface 1 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared. |
| SURF2_WRITE_FLAG  | 2           | 0x0            | Indicates if write to surface 2 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared. |
| SURF3_WRITE_FLAG  | 3           | 0x0            | Indicates if write to surface 3 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared. |
| SURF4_WRITE_FLAG  | 4           | 0x0            | Indicates if write to surface 4 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared. |
| SURF5_WRITE_FLAG  | 5           | 0x0            | Indicates if write to surface 5 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared. |
| SURF6_WRITE_FLAG  | 6           | 0x0            | Indicates if write to surface 6 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared. |

**SURFACE\_ACCESS\_FLAGS - R - 32 bits - [MMReg:0xBF8]**

| Field Name         | Bits | Default | Description  |
|--------------------|------|---------|--|
| SURF7_WRITE_FLAG   | 7    | 0x0     | Indicates if write to surface 7 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared.                          |
| NONSURF_WRITE_FLAG | 8    | 0x0     | Indicates if write to address that missed all surfaces since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared.   |
| LINEAR_WRITE_FLAG  | 9    | 0x0     | Indicates if write to anywhere in linear memory aperture since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared. |
| VGA_WRITE_FLAG     | 10   | 0x0     | Indicates if write to anywhere in VGA memory aperture since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared.    |
| SURF0_READ_FLAG    | 16   | 0x0     | Indicates if read to surface 0 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.                             |
| SURF1_READ_FLAG    | 17   | 0x0     | Indicates if read to surface 1 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.                             |
| SURF2_READ_FLAG    | 18   | 0x0     | Indicates if read to surface 2 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.                             |
| SURF3_READ_FLAG    | 19   | 0x0     | Indicates if read to surface 3 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.                             |
| SURF4_READ_FLAG    | 20   | 0x0     | Indicates if read to surface 4 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.                             |
| SURF5_READ_FLAG    | 21   | 0x0     | Indicates if read to surface 5 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.                             |
| SURF6_READ_FLAG    | 22   | 0x0     | Indicates if read to surface 6 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.                             |
| SURF7_READ_FLAG    | 23   | 0x0     | Indicates if read to surface 7 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.                             |
| NONSURF_READ_FLAG  | 24   | 0x0     | Indicates if read to address that missed all surfaces since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.      |
| LINEAR_READ_FLAG   | 25   | 0x0     | Indicates if read to anywhere in linear memory aperture since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.    |

**SURFACE\_ACCESS\_FLAGS - R - 32 bits - [MMReg:0xBF8]**

| Field Name    | Bits | Default | Description  |
|---------------|------|---------|--|
| VGA_READ_FLAG | 26   | 0x0     | Indicates if read to anywhere in VGA memory aperture since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared. |

Flags to indicate write or read access to memory surfaces

**SURFACE\_ACCESS\_CLR - W - 32 bits - [MMReg:0xBFC]**

| Field Name             | Bits | Default | Description  |
|------------------------|------|---------|--|
| SURF0_WRITE_FLAG_CLR   | 0    | 0x0     | Used to clear SURF0_WRITE_FLAG.<br>0=Do not clear this write flag.<br>1=Clear this write flag.   |
| SURF1_WRITE_FLAG_CLR   | 1    | 0x0     | Used to clear SURF1_WRITE_FLAG.<br>0=Do not clear this write flag.<br>1=Clear this write flag.   |
| SURF2_WRITE_FLAG_CLR   | 2    | 0x0     | Used to clear SURF2_WRITE_FLAG.<br>0=Do not clear this write flag.<br>1=Clear this write flag.   |
| SURF3_WRITE_FLAG_CLR   | 3    | 0x0     | Used to clear SURF3_WRITE_FLAG.<br>0=Do not clear this write flag.<br>1=Clear this write flag.   |
| SURF4_WRITE_FLAG_CLR   | 4    | 0x0     | Used to clear SURF4_WRITE_FLAG.<br>0=Do not clear this write flag.<br>1=Clear this write flag.   |
| SURF5_WRITE_FLAG_CLR   | 5    | 0x0     | Used to clear SURF5_WRITE_FLAG.<br>0=Do not clear this write flag.<br>1=Clear this write flag.   |
| SURF6_WRITE_FLAG_CLR   | 6    | 0x0     | Used to clear SURF6_WRITE_FLAG.<br>0=Do not clear this write flag.<br>1=Clear this write flag.   |
| SURF7_WRITE_FLAG_CLR   | 7    | 0x0     | Used to clear SURF7_WRITE_FLAG.<br>0=Do not clear this write flag.<br>1=Clear this write flag.   |
| NONSURF_WRITE_FLAG_CLR | 8    | 0x0     | Used to clear NONSURF_WRITE_FLAG.<br>0=Do not clear this write flag.<br>1=Clear this write flag. |
| LINEAR_WRITE_FLAG_CLR  | 9    | 0x0     | Used to clear LINEAR_WRITE_FLAG.<br>0=Do not clear this write flag.<br>1=Clear this write flag.  |
| VGA_WRITE_FLAG_CLR     | 10   | 0x0     | Used to clear VGA_WRITE_FLAG.<br>0=Do not clear this write flag.<br>1=Clear this write flag.     |
| SURF0_READ_FLAG_CLR    | 16   | 0x0     | Used to clear SURF0_READ_FLAG.<br>0=Do not clear this read flag.<br>1=Clear this read flag.      |
| SURF1_READ_FLAG_CLR    | 17   | 0x0     | Used to clear SURF1_READ_FLAG.<br>0=Do not clear this read flag.<br>1=Clear this read flag.      |

**SURFACE\_ACCESS\_CLR - W - 32 bits - [MMReg:0xBFC]**

| Field Name            | Bits | Default | Description   |
|-----------------------|------|---------|---|
| SURF2_READ_FLAG_CLR   | 18   | 0x0     | Used to clear SURF2_READ_FLAG.<br>0=Do not clear this read flag.<br>1=Clear this read flag.   |
| SURF3_READ_FLAG_CLR   | 19   | 0x0     | Used to clear SURF3_READ_FLAG.<br>0=Do not clear this read flag.<br>1=Clear this read flag.   |
| SURF4_READ_FLAG_CLR   | 20   | 0x0     | Used to clear SURF4_READ_FLAG.<br>0=Do not clear this read flag.<br>1=Clear this read flag.   |
| SURF5_READ_FLAG_CLR   | 21   | 0x0     | Used to clear SURF5_READ_FLAG.<br>0=Do not clear this read flag.<br>1=Clear this read flag.   |
| SURF6_READ_FLAG_CLR   | 22   | 0x0     | Used to clear SURF6_READ_FLAG.<br>0=Do not clear this read flag.<br>1=Clear this read flag.   |
| SURF7_READ_FLAG_CLR   | 23   | 0x0     | Used to clear SURF7_READ_FLAG.<br>0=Do not clear this read flag.<br>1=Clear this read flag.   |
| NONSURF_READ_FLAG_CLR | 24   | 0x0     | Used to clear NONSURF_READ_FLAG.<br>0=Do not clear this read flag.<br>1=Clear this read flag. |
| LINEAR_READ_FLAG_CLR  | 25   | 0x0     | Used to clear LINEAR_READ_FLAG.<br>0=Do not clear this read flag.<br>1=Clear this read flag.  |
| VGA_READ_FLAG_CLR     | 26   | 0x0     | Used to clear VGA_READ_FLAG.<br>0=Do not clear this read flag.<br>1=Clear this read flag.     |

Clear bits for SURFACE\_ACCESS\_FLAGS register

**SURFACE0\_LOWER\_BOUND - RW - 32 bits - [MMReg:0xB04]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_LOWER | 27:0 | 0x0     | Starting address of lowest tile in Surface 0.<br><br>NOTE: Bits 0:10 of this field are hardwired to ZERO. |

Surface 0 Lower Bound Register

**SURFACE1\_LOWER\_BOUND - RW - 32 bits - [MMReg:0xB14]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_LOWER | 27:0 | 0x0     | Starting address of lowest tile in Surface 1.<br><br>NOTE: Bits 0:10 of this field are hardwired to ZERO. |

Surface 1 Lower Bound Register

**SURFACE2\_LOWER\_BOUND - RW - 32 bits - [MMReg:0xB24]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_LOWER | 27:0 | 0x0     | Starting address of lowest tile in Surface 2.<br><br>NOTE: Bits 0:10 of this field are hardwired to ZERO. |

Surface 2 Lower Bound Register

**SURFACE3\_LOWER\_BOUND - RW - 32 bits - [MMReg:0xB34]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_LOWER | 27:0 | 0x0     | Starting address of lowest tile in Surface 3.<br><br>NOTE: Bits 0:10 of this field are hardwired to ZERO. |

Surface 3 Lower Bound Register

**SURFACE4\_LOWER\_BOUND - RW - 32 bits - [MMReg:0xB44]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_LOWER | 27:0 | 0x0     | Starting address of lowest tile in Surface 4.<br><br>NOTE: Bits 0:10 of this field are hardwired to ZERO. |

Surface 4 Lower Bound Register

**SURFACE5\_LOWER\_BOUND - RW - 32 bits - [MMReg:0xB54]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_LOWER | 27:0 | 0x0     | Starting address of lowest tile in Surface 5.<br><br>NOTE: Bits 0:10 of this field are hardwired to ZERO. |

Surface 5 Lower Bound Register

**SURFACE6\_LOWER\_BOUND - RW - 32 bits - [MMReg:0xB64]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_LOWER | 27:0 | 0x0     | Starting address of lowest tile in Surface 6.<br><br>NOTE: Bits 0:10 of this field are hardwired to ZERO. |

Surface 6 Lower Bound Register

**SURFACE7\_LOWER\_BOUND - RW - 32 bits - [MMReg:0xB74]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_LOWER | 27:0 | 0x0     | Starting address of lowest tile in Surface 7.<br><br>NOTE: Bits 0:10 of this field are hardwired to ZERO. |

Surface 7 Lower Bound Register

**SURFACE0\_UPPER\_BOUND - RW - 32 bits - [MMReg:0xB08]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_UPPER | 27:0 | 0x7ff   | Starting address of highest tile in Surface 0.<br><br>NOTE: Bits 0:10 of this field are hardwired to ONE. |

Surface 0 Upper Bound Register

**SURFACE1\_UPPER\_BOUND - RW - 32 bits - [MMReg:0xB18]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_UPPER | 27:0 | 0x7ff   | Starting address of highest tile in Surface 1.<br><br>NOTE: Bits 0:10 of this field are hardwired to ONE. |

Surface 1 Upper Bound Register

**SURFACE2\_UPPER\_BOUND - RW - 32 bits - [MMReg:0xB28]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**SURFACE2\_UPPER\_BOUND - RW - 32 bits - [MMReg:0xB28]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_UPPER | 27:0 | 0x7ff   | Starting address of highest tile in Surface 2.<br><br>NOTE: Bits 0:10 of this field are hardwired to ONE. |

Surface 2 Upper Bound Register

**SURFACE3\_UPPER\_BOUND - RW - 32 bits - [MMReg:0xB38]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_UPPER | 27:0 | 0x7ff   | Starting address of highest tile in Surface 3.<br><br>NOTE: Bits 0:10 of this field are hardwired to ONE. |

Surface 3 Upper Bound Register

**SURFACE4\_UPPER\_BOUND - RW - 32 bits - [MMReg:0xB48]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_UPPER | 27:0 | 0x7ff   | Starting address of highest tile in Surface 4.<br><br>NOTE: Bits 0:10 of this field are hardwired to ONE. |

Surface 4 Upper Bound Register

**SURFACE5\_UPPER\_BOUND - RW - 32 bits - [MMReg:0xB58]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_UPPER | 27:0 | 0x7ff   | Starting address of highest tile in Surface 5.<br><br>NOTE: Bits 0:10 of this field are hardwired to ONE. |

Surface 5 Upper Bound Register

**SURFACE6\_UPPER\_BOUND - RW - 32 bits - [MMReg:0xB68]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_UPPER | 27:0 | 0x7ff   | Starting address of highest tile in Surface 6.<br><br>NOTE: Bits 0:10 of this field are hardwired to ONE. |

Surface 6 Upper Bound Register

**SURFACE7\_UPPER\_BOUND - RW - 32 bits - [MMReg:0xB78]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SURF_UPPER | 27:0 | 0x7ff   | Starting address of highest tile in Surface 7.<br><br>NOTE: Bits 0:10 of this field are hardwired to ONE. |

Surface 7 Upper Bound Register

**SURFACE0\_INFO - RW - 32 bits - [MMReg:0xB0C]**

| Field Name     | Bits | Default | Description   |
|----------------|------|---------|---|
| SURF0_PITCHSEL | 9:0  | 0x0     | Pitch in octawords (16 bytes) of Surface 0. A value of 0 disables tiling in Surface 0.<br>For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512.<br>For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514.<br>For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257.<br>Pitch bits less than min increment are ignored. |

**SURFACE0\_INFO - RW - 32 bits - [MMReg:0xB0C]**

| Field Name   | Bits  | Default | Description   |
|--|-------|---------|---|
| SURF0_TILE_MODE  | 17:16 | 0x0     | Mode of tiling for Surface 0. Set SURF0_PITCHSEL to 0 to disable tiling surface 0.<br>0=Disable MicroTiling<br>1=Enable MicroTiling<br>2=32 bit Z tiling<br>3=16 bit Z tiling |
| SURF0_AP0_SWP  | 21:20 | 0x0     | Endian swap control for Aperture 0 accesses in Surface 0.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.                |
| SURF0_AP1_SWP  | 23:22 | 0x0     | Endian swap control for Aperture 1 accesses in Surface 0.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.                |
| SURF0_WRITE_FLAG<br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF0_WRITE_FLAG) (R)</i> | 24    | 0x0     | Indicates if write to surface 0 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared.   |
| SURF0_READ_FLAG<br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF0_READ_FLAG) (R)</i>   | 25    | 0x0     | Indicates if read to surface 0 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.  |

Control register for Surface 0

**SURFACE1\_INFO - RW - 32 bits - [MMReg:0xB1C]**

| Field Name   | Bits  | Default | Description   |
|--|-------|---------|---|
| SURF1_PITCHSEL   | 9:0   | 0x0     | Pitch in octawords (16 bytes) of Surface 1. A value of 0 disables tiling in Surface 0.<br>For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512.<br>For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514.<br>For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257.<br>Pitch bits less than min increment are ignored. |
| SURF1_TILE_MODE  | 17:16 | 0x0     | Mode of tiling for Surface 1. Set SURF1_PITCHSEL to 0 to disable tiling surface 1.<br>0=Disable MicroTiling<br>1=Enable MicroTiling<br>2=32 bit Z tiling<br>3=16 bit Z tiling   |
| SURF1_AP0_SWP  | 21:20 | 0x0     | Endian swap control for Aperture 0 accesses in Surface 1.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.  |
| SURF1_AP1_SWP  | 23:22 | 0x0     | Endian swap control for Aperture 1 accesses in Surface 1.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.  |
| SURF1_WRITE_FLAG<br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF1_WRITE_FLAG) (R)</i> | 24    | 0x0     | Indicates if write to surface 1 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared.   |

**SURFACE1\_INFO - RW - 32 bits - [MMReg:0xB1C]**

| Field Name   | Bits | Default | Description  |
|--|------|---------|--|
| SURF1_READ_FLAG<br><br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF1_READ_FLAG) (R)</i> | 25   | 0x0     | Indicates if read to surface 1 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared. |

Control register for Surface 1

**SURFACE2\_INFO - RW - 32 bits - [MMReg:0xB2C]**

| Field Name   | Bits  | Default | Description   |
|--|-------|---------|---|
| SURF2_PITCHSEL   | 9:0   | 0x0     | Pitch in octawords (16 bytes) of Surface 2. A value of 0 disables tiling in Surface 0.<br>For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512.<br>For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514.<br>For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257.<br>Pitch bits less than min increment are ignored. |
| SURF2_TILE_MODE  | 17:16 | 0x0     | Mode of tiling for Surface 2. Set SURF2_PITCHSEL to 0 to disable tiling surface 2.<br>0=Disable MicroTiling<br>1=Enable MicroTiling<br>2=32 bit Z tiling<br>3=16 bit Z tiling   |
| SURF2_AP0_SWP  | 21:20 | 0x0     | Endian swap control for Aperture 0 accesses in Surface 2.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.  |
| SURF2_AP1_SWP  | 23:22 | 0x0     | Endian swap control for Aperture 1 accesses in Surface 2.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.  |
| SURF2_WRITE_FLAG<br><br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF2_WRITE_FLAG) (R)</i> | 24    | 0x0     | Indicates if write to surface 2 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared.   |
| SURF2_READ_FLAG<br><br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF2_READ_FLAG) (R)</i>   | 25    | 0x0     | Indicates if read to surface 2 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.  |

Control register for Surface 2

**SURFACE3\_INFO - RW - 32 bits - [MMReg:0xB3C]**

| Field Name     | Bits | Default | Description   |
|----------------|------|---------|---|
| SURF3_PITCHSEL | 9:0  | 0x0     | Pitch in octawords (16 bytes) of Surface 3. A value of 0 disables tiling in Surface 0.<br>For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512.<br>For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514.<br>For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257.<br>Pitch bits less than min increment are ignored. |



| SURFACE3_INFO - RW - 32 bits - [MMReg:0xB3C]                                     |       |         |   |
|--|-------|---------|---|
| Field Name   | Bits  | Default | Description   |
| SURF3_TILE_MODE  | 17:16 | 0x0     | Mode of tiling for Surface 3. Set SURF3_PITCHSEL to 0 to disable tiling surface 3.<br>0=Disable MicroTiling<br>1=Enable MicroTiling<br>2=32 bit Z tiling<br>3=16 bit Z tiling |
| SURF3_AP0_SWP  | 21:20 | 0x0     | Endian swap control for Aperture 0 accesses in Surface 3.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.                |
| SURF3_AP1_SWP  | 23:22 | 0x0     | Endian swap control for Aperture 1 accesses in Surface 3.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.                |
| SURF3_WRITE_FLAG<br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF3_WRITE_FLAG) (R)</i> | 24    | 0x0     | Indicates if write to surface 3 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared.   |
| SURF3_READ_FLAG<br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF3_READ_FLAG) (R)</i>   | 25    | 0x0     | Indicates if read to surface 3 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.  |

Control register for Surface 3

| SURFACE4_INFO - RW - 32 bits - [MMReg:0xB4C]                                     |       |         |   |
|--|-------|---------|---|
| Field Name   | Bits  | Default | Description   |
| SURF4_PITCHSEL   | 9:0   | 0x0     | Pitch in octawords (16 bytes) of Surface 4. A value of 0 disables tiling in Surface 0.<br>For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512.<br>For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514.<br>For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257.<br>Pitch bits less than min increment are ignored. |
| SURF4_TILE_MODE  | 17:16 | 0x0     | Mode of tiling for Surface 4. Set SURF4_PITCHSEL to 0 to disable tiling surface 4.<br>0=Disable MicroTiling<br>1=Enable MicroTiling<br>2=32 bit Z tiling<br>3=16 bit Z tiling   |
| SURF4_AP0_SWP  | 21:20 | 0x0     | Endian swap control for Aperture 0 accesses in Surface 4.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.  |
| SURF4_AP1_SWP  | 23:22 | 0x0     | Endian swap control for Aperture 1 accesses in Surface 4.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.  |
| SURF4_WRITE_FLAG<br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF4_WRITE_FLAG) (R)</i> | 24    | 0x0     | Indicates if write to surface 4 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared.   |

**SURFACE4\_INFO - RW - 32 bits - [MMReg:0xB4C]**

| Field Name   | Bits | Default | Description  |
|--|------|---------|--|
| SURF4_READ_FLAG<br><br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF4_READ_FLAG) (R)</i> | 25   | 0x0     | Indicates if read to surface 4 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared. |

Control register for Surface 4

**SURFACE5\_INFO - RW - 32 bits - [MMReg:0xB5C]**

| Field Name   | Bits  | Default | Description   |
|--|-------|---------|---|
| SURF5_PITCHSEL   | 9:0   | 0x0     | Pitch in octawords (16 bytes) of Surface 5. A value of 0 disables tiling in Surface 0.<br>For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512.<br>For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514.<br>For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257.<br>Pitch bits less than min increment are ignored. |
| SURF5_TILE_MODE  | 17:16 | 0x0     | Mode of tiling for Surface 5. Set SURF5_PITCHSEL to 0 to disable tiling surface 5.<br>0=Disable MicroTiling<br>1=Enable MicroTiling<br>2=32 bit Z tiling<br>3=16 bit Z tiling   |
| SURF5_AP0_SWP  | 21:20 | 0x0     | Endian swap control for Aperture 0 accesses in Surface 5.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.  |
| SURF5_AP1_SWP  | 23:22 | 0x0     | Endian swap control for Aperture 1 accesses in Surface 5.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.  |
| SURF5_WRITE_FLAG<br><br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF5_WRITE_FLAG) (R)</i> | 24    | 0x0     | Indicates if write to surface 5 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared.   |
| SURF5_READ_FLAG<br><br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF5_READ_FLAG) (R)</i>   | 25    | 0x0     | Indicates if read to surface 5 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.  |

Control register for Surface 5

**SURFACE6\_INFO - RW - 32 bits - [MMReg:0xB6C]**

| Field Name     | Bits | Default | Description   |
|----------------|------|---------|---|
| SURF6_PITCHSEL | 9:0  | 0x0     | Pitch in octawords (16 bytes) of Surface 6. A value of 0 disables tiling in Surface 0.<br>For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512.<br>For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514.<br>For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257.<br>Pitch bits less than min increment are ignored. |



| SURFACE6_INFO - RW - 32 bits - [MMReg:0xB6C]                                     |       |         |   |
|--|-------|---------|---|
| Field Name   | Bits  | Default | Description   |
| SURF6_TILE_MODE  | 17:16 | 0x0     | Mode of tiling for Surface 6. Set SURF6_PITCHSEL to 0 to disable tiling surface 6.<br>0=Disable MicroTiling<br>1=Enable MicroTiling<br>2=32 bit Z tiling<br>3=16 bit Z tiling |
| SURF6_AP0_SWP  | 21:20 | 0x0     | Endian swap control for Aperture 0 accesses in Surface 6.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.                |
| SURF6_AP1_SWP  | 23:22 | 0x0     | Endian swap control for Aperture 1 accesses in Surface 6.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.                |
| SURF6_WRITE_FLAG<br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF6_WRITE_FLAG) (R)</i> | 24    | 0x0     | Indicates if write to surface 6 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared.   |
| SURF6_READ_FLAG<br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF6_READ_FLAG) (R)</i>   | 25    | 0x0     | Indicates if read to surface 6 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared.  |

Control register for Surface 6

| SURFACE7_INFO - RW - 32 bits - [MMReg:0xB7C]                                     |       |         |   |
|--|-------|---------|---|
| Field Name   | Bits  | Default | Description   |
| SURF7_PITCHSEL   | 9:0   | 0x0     | Pitch in octawords (16 bytes) of Surface 7. A value of 0 disables tiling in Surface 0.<br>For color macro tiling and color macro&micro tiling the pitch must be in 16 octaword increments from 16 to 512.<br>For 32-bit Z tiling the pitch must be in 2 octaword increments from 2 to 514.<br>For 16-bit Z tiling the pitch may be in 1 octaword increments from 1 to 257.<br>Pitch bits less than min increment are ignored. |
| SURF7_TILE_MODE  | 17:16 | 0x0     | Mode of tiling for Surface 7. Set SURF7_PITCHSEL to 0 to disable tiling surface 7.<br>0=Disable MicroTiling<br>1=Enable MicroTiling<br>2=32 bit Z tiling<br>3=16 bit Z tiling   |
| SURF7_AP0_SWP  | 21:20 | 0x0     | Endian swap control for Aperture 0 accesses in Surface 7.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.  |
| SURF7_AP1_SWP  | 23:22 | 0x0     | Endian swap control for Aperture 1 accesses in Surface 7.<br>0=Little endian: no swapping.<br>1=Big endian: 16-bit swapping.<br>2=Big endian: 32-bit swapping.  |
| SURF7_WRITE_FLAG<br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF7_WRITE_FLAG) (R)</i> | 24    | 0x0     | Indicates if write to surface 7 since last cleared.<br>0=No write since last cleared.<br>1=Write occurred since last cleared.   |



ORIGINATE DATE

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**SURFACE7\_INFO - RW - 32 bits - [MMReg:0xB7C]**

| Field Name   | Bits | Default | Description  |
|--|------|---------|--|
| SURF7_READ_FLAG<br><i>(mirror of SURFACE_ACCESS_FLAGS:SURF7_READ_FLAG) (R)</i> | 25   | 0x0     | Indicates if read to surface 7 since last cleared.<br>0=No read since last cleared.<br>1=Read occurred since last cleared. |

Control register for Surface 7

**39. Capture Detailed Register Reference**

Registers to facilitate the capture of input video data

| FCP_CNTL - RW - 32 bits - [MMReg:0x910] |      |         |  |
|---|------|---------|--|
| Field Name                              | Bits | Default | Description  |
| FCP0_SRC_SEL                            | 2:0  | 0x4     | PCICLK,PCLK, PCLKb, HREF, GND, HREFb.<br>0=PCICLK<br>1=PCLK<br>2=PCLKb<br>3=HREF<br>4=GND<br>5=HREFb |

Capture Port FCP clock mux control

| GEN_INT_STATUS - RW - 32 bits - [IOReg,MMReg:0x44] |      |         |  |
|--|------|---------|--|
| Field Name   | Bits | Default | Description  |
| CRTC_VBLANK_STAT (R)<br>(DISPLAY)                  | 0    | 0x0     | Vertical blank interrupt. Set when display in vertical retrace.<br>0=No event<br>1=Event has occurred, interrupting if enabled   |
| CRTC_VBLANK_STAT_AK (W)<br>(DISPLAY)               | 0    | 0x0     | Vertical blank interrupt acknowledge.<br>0=No effect<br>1=Clear status   |
| CRTC_VLINE_STAT (R)<br>(DISPLAY)                   | 1    | 0x0     | Vertical line interrupt. Set on display line on programmed by the CRTC_VLINE_CRNT_VLINE.CRTC_VLINE register.<br>0=No event<br>1=Event has occurred, interrupting if enabled      |
| CRTC_VLINE_STAT_AK (W)<br>(DISPLAY)                | 1    | 0x0     | Vertical line interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| CRTC_VSYNC_STAT (R)<br>(DISPLAY)                   | 2    | 0x0     | Vertical sync interrupt. Set on start of VSYNC at the DAC.<br>0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC_VSYNC_STAT_AK (W)<br>(DISPLAY)                | 2    | 0x0     | Vertical sync interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| SNAPSHOT_STAT (R)<br>(DISPLAY)                     | 3    | 0x0     | Snapshot interrupt. Set as controlled by SNAPSHOT_VIF_COUNT register.<br>0=No event<br>1=Event has occurred, interrupting if enabled   |
| SNAPSHOT_STAT_AK (W)<br>(DISPLAY)                  | 3    | 0x0     | Snapshot interrupt acknowledge.<br>0=No effect<br>1=Clear status   |
| FP_DETECT_STAT (R)<br>(DISPLAY)                    | 4    | 0x0     | Hot plug detect (HPD) interrupt. Set on HPD connect or disconnect as controlled by FP_GEN_CNTL.FP_DETECT_INT_POL.<br>0=No event<br>1=Event has occurred, interrupting if enabled |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                                   | Bits | Default | Description  |
|--|------|---------|--|
| FP_DETECT_STAT_AK (W)<br>(DISPLAY)           | 4    | 0x0     | Hot plug detect (HPD) interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| CRTC2_VLINE_STAT (R)<br>(DISPLAY)            | 5    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC2_VLINE_STAT_AK (W)<br>(DISPLAY)         | 5    | 0x0     | 0=No effect<br>1=Clear status  |
| CRTC2_VSYNC_STAT (R)<br>(DISPLAY)            | 6    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC2_VSYNC_STAT_AK (W)<br>(DISPLAY)         | 6    | 0x0     | 0=No effect<br>1=Clear status  |
| SNAPSHOT2_STAT (R)<br>(DISPLAY)              | 7    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| SNAPSHOT2_STAT_AK (W)<br>(DISPLAY)           | 7    | 0x0     | 0=No effect<br>1=Clear status  |
| CAPO_INT_ACTIVE (R)<br>(VIP)                 | 8    | 0x0     | Capture port 0 has active interrupt(s).<br>0=Capture port 0 not source of any active interrupt<br>1=Capture port 0 has active interrupt(s) |
| CRTC2_VBLANK_STAT (R)<br>(DISPLAY)           | 9    | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| CRTC2_VBLANK_STAT_AK (W)<br>(DISPLAY)        | 9    | 0x0     | 0=No effect<br>1=Clear status  |
| FP2_DETECT_STAT (R)<br>(DISPLAY)             | 10   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| FP2_DETECT_STAT_AK (W)<br>(DISPLAY)          | 10   | 0x0     | 0=No effect<br>1=Clear status  |
| VSYNC_DIFF_OVER_LIMIT_STAT (R)<br>(TVOUT)    | 11   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| VSYNC_DIFF_OVER_LIMIT_STAT_AK (W)<br>(TVOUT) | 11   | 0x0     | 0=No effect<br>1=Clear status  |
| DMA_VIPH0_INT (R)<br>(VIP)                   | 12   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| DMA_VIPH0_INT_AK (W)<br>(VIP)                | 12   | 0x0     | 0=No effect<br>1=Clear status  |
| DMA_VIPH1_INT (R)<br>(VIP)                   | 13   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| DMA_VIPH1_INT_AK (W)<br>(VIP)                | 13   | 0x0     | 0=No effect<br>1=Clear status  |
| DMA_VIPH2_INT (R)<br>(VIP)                   | 14   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled  |
| DMA_VIPH2_INT_AK (W)<br>(VIP)                | 14   | 0x0     | 0=No effect<br>1=Clear status  |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name                                | Bits | Default | Description   |
|---|------|---------|---|
| DMA_VIPH3_INT (R)<br>(VIP)                | 15   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DMA_VIPH3_INT_AK (W)<br>(VIP)             | 15   | 0x0     | 0=No effect<br>1=Clear status   |
| I2C_INT (R)<br>(VIP)                      | 17   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| I2C_INT_AK (W)<br>(VIP)                   | 17   | 0x0     | 0=No effect<br>1=Clear status   |
| GUI_IDLE_STAT (R)<br>(RBBM)               | 19   | 0x1     | GUI idle interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled  |
| GUI_IDLE_STAT_AK (W)<br>(RBBM)            | 19   | 0x0     | GUI idle interrupt acknowledge.<br>0=No effect<br>1=Clear status  |
| VIPH_INT (R)<br>(VIP)                     | 24   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| SW_INT (R)<br>(HDP)                       | 25   | 0x0     | Software interrupt. General purpose interrupt that can only be set by software event by writing to SW_INT_SET.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| SW_INT_AK (W)<br>(HDP)                    | 25   | 0x0     | Software interrupt acknowledge.<br>0=No effect<br>1=Clear SW_INT (set low)  |
| SW_INT_SET (W)<br>(HDP)                   | 26   | 0x0     | Software interrupt trigger.<br>0=No effect<br>1=Set SW_INT active (high)  |
| GEYSERVILLE_STAT (R)<br>(VIP)             | 27   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| GEYSERVILLE_STAT_AK (W)<br>(VIP)          | 27   | 0x0     | 0=No effect<br>1=Clear status   |
| HDCP_AUTHORIZED_INT_STAT (R)<br>(DISPLAY) | 28   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| HDCP_AUTHORIZED_INT_AK (W)<br>(DISPLAY)   | 28   | 0x0     | 0=No effect<br>1=Clear status   |
| DVI_I2C_INT_STAT (R)<br>(DISPLAY)         | 29   | 0x0     | 0=No event<br>1=Event has occurred, interrupting if enabled   |
| DVI_I2C_INT_AK (W)<br>(DISPLAY)           | 29   | 0x0     | 0=No effect<br>1=Clear status   |
| GUIDMA_STAT (R)<br>(CP)                   | 30   | 0x0     | GUI DMA channel interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled   |
| GUIDMA_AK (W)<br>(CP)                     | 30   | 0x0     | GUI DMA channel interrupt acknowledge.<br>0=No effect<br>1=Clear status   |

**GEN\_INT\_STATUS - RW - 32 bits - [IOReg,MMReg:0x44]**

| Field Name              | Bits | Default | Description   |
|-------------------------|------|---------|---|
| VIDDMA_STAT (R)<br>(CP) | 31   | 0x0     | Video capture DMA channel interrupt.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| VIDDMA_AK (W)<br>(CP)   | 31   | 0x0     | Video capture DMA channel interrupt acknowledge.<br>0=No effect<br>1=Clear status                   |

General Interrupt Status register.

These fields can be polled and acknowledged even if interrupts are disabled, or the respective fields are masked in the GEN\_INT\_CNTL register.

**CAPO\_BUF0\_OFFSET - RW - 32 bits - [MMReg:0x920]**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| CAP_BUF0_OFFSET | 31:0 | 0x0     | Capture Port 0 Buffer 0 starting address<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO. |

Capture Port 0 Buffer 0 starting address

**CAPO\_BUF1\_OFFSET - RW - 32 bits - [MMReg:0x924]**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| CAP_BUF1_OFFSET | 31:0 | 0x0     | Capture Port 0 Buffer 1 starting address<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO. |

Capture Port 0 Buffer 1 starting address

**CAPO\_BUF0\_EVEN\_OFFSET - RW - 32 bits - [MMReg:0x928]**

| Field Name           | Bits | Default | Description  |
|----------------------|------|---------|--|
| CAP_BUF0_EVEN_OFFSET | 31:0 | 0x0     | Capture Port 0 Buffer 0 even frame starting address<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO. |

Capture Port 0 Buffer 0 even frame starting address

**CAPO\_BUF1\_EVEN\_OFFSET - RW - 32 bits - [MMReg:0x92C]**

| Field Name           | Bits | Default | Description  |
|----------------------|------|---------|--|
| CAP_BUF1_EVEN_OFFSET | 31:0 | 0x0     | Capture Port 0 Buffer 1 even frame starting address<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO. |

Capture Port 0 Buffer 1 even frame starting address

**CAPO\_BUF\_PITCH - RW - 32 bits - [MMReg:0x930]**

| Field Name    | Bits | Default | Description  |
|---------------|------|---------|--|
| CAP_BUF_PITCH | 11:0 | 0x0     | Capture 0 buffer's pitch.<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO. |

Capture 0 buffer's pitch.

**CAPO\_V\_WINDOW - RW - 32 bits - [MMReg:0x934]**

| Field Name  | Bits  | Default | Description                           |
|-------------|-------|---------|---------------------------------------|
| CAP_V_START | 11:0  | 0x0     | Vertical window starting line number. |
| CAP_V_END   | 27:16 | 0x0     | Vertical window end line number.      |

Capture 0's Vertical window.

**CAPO\_H\_WINDOW - RW - 32 bits - [MMReg:0x938]**

| Field Name  | Bits  | Default | Description   |
|-------------|-------|---------|---|
| CAP_H_START | 11:0  | 0x0     | Horizontal window's start.  |
| CAP_H_WIDTH | 27:16 | 0x0     | Horizontal window's width.<br>NOTE: Bits 0:1 of this field are hardwired to ZERO. |

Capture 0's Horizontal window.

**CAPO\_VBI0\_OFFSET - RW - 32 bits - [MMReg:0x93C]**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| CAP_VBI0_OFFSET | 31:0 | 0x0     | Capture 0 VBI 0 buffer's starting address.<br>NOTE: Bits 0:1 of this field are hardwired to ZERO. |

Capture 0 VBI 0 buffer's starting address.

**CAPO\_VBI1\_OFFSET - RW - 32 bits - [MMReg:0x940]**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| CAP_VBI1_OFFSET | 31:0 | 0x0     | Capture 0 VBI 1 buffer's starting address.<br>NOTE: Bits 0:1 of this field are hardwired to ZERO. |

Capture 0 VBI 1 buffer's starting address.

**CAPO\_VBI\_V\_WINDOW - RW - 32 bits - [MMReg:0x944]**

| Field Name      | Bits  | Default | Description                     |
|-----------------|-------|---------|---------------------------------|
| CAP_VBI_V_START | 11:0  | 0x0     | Capture 0 VBI's Vertical start. |
| CAP_VBI_V_END   | 27:16 | 0x0     | Capture 0 VBI's Vertical End.   |

Capture 0 VBI's vertical window

**CAPO\_VBI\_H\_WINDOW - RW - 32 bits - [MMReg:0x948]**

| Field Name      | Bits  | Default | Description  |
|-----------------|-------|---------|--|
| CAP_VBI_H_START | 11:0  | 0x0     | Capture 0 VBI's Horizontal start.  |
| CAP_VBI_H_WIDTH | 27:16 | 0x0     | Capture 0 VBI's Horizontal Width.<br>NOTE: Bits 0:1 of this field are hardwired to ZERO. |

Capture 0 VBI's horizontal window

**CAPO\_PORT\_MODE\_CNTL - RW - 32 bits - [MMReg:0x94C]**

| Field Name         | Bits | Default | Description   |
|--------------------|------|---------|---|
| CAP_PORT_WIDTH     | 1    | 0x0     | Capture 0 port width.<br>0=8 bits<br>1=16 bits                                  |
| CAP_PORT_BYTE_USED | 2    | 0x0     | In 8 bit width mode, which byte used.<br>0=lower byte used<br>1=upper byte used |

Capture 0 mode control register.

**CAPO\_TRIG\_CNTL - RW - 32 bits - [MMReg:0x950]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**CAP0\_TRIG\_CNTL - RW - 32 bits - [MMReg:0x950]**

| Field Name        | Bits | Default | Description  |
|-------------------|------|---------|--|
| CAP_TRIGGER_R (R) | 1:0  | 0x0     | Read only. Capture status.<br>0=capture complete<br>1=capture pending<br>2=capture in progress |
| CAP_TRIGGER_W (W) | 0    | 0x0     | Write only. Start capture next frame.<br>0=no action<br>1=capture next field/frame             |
| CAP_EN            | 4    | 0x0     | Capture 0 enable.<br>0=disable<br>1=enable   |
| CAP_VSYNC_CNT (R) | 15:8 | 0x0     | Read only. VSYNC counter.  |
| CAP_VSYNC_CLR     | 16   | 0x0     | Reset the VSYNC counter.   |

Capture 0 trigger control.

**CAP0\_CONFIG - RW - 32 bits - [MMReg:0x958]**

| Field Name            | Bits | Default | Description  |
|-----------------------|------|---------|--|
| CAP_INPUT_MODE        | 0    | 0x0     | Input mode.<br>0=OneShot trigger mode<br>1=Enable continuous capture |
| CAP_START_FIELD       | 1    | 0x0     | Starting field.<br>0=Odd<br>1=Even                                   |
| CAP_START_BUF_R (R)   | 2    | 0x0     | Read only. Current starting buffer.<br>0=Buffer 0<br>1=Buffer 1      |
| CAP_START_BUF_W (W)   | 3    | 0x0     | Write only. Control starting buffer.<br>0=Buffer 0<br>1=Buffer 1     |
| CAP_BUF_TYPE          | 5:4  | 0x0     | Buffer type.<br>0=Field<br>1=Alternating<br>2=Frame                  |
| CAP_ONESHOT_MODE      | 6    | 0x0     | ONESHOT mode.<br>0=FIELD<br>1=FRAME                                  |
| CAP_BUF_MODE          | 8:7  | 0x0     | Capture 0 buffer mode.<br>0=Single<br>1=Double<br>2=Triple           |
| CAP_MIRROR_EN         | 9    | 0x0     | Capture 0 mirroring function enable.<br>0=Normal<br>1=Mirror         |
| CAP_ONESHOT_MIRROR_EN | 10   | 0x0     | ONESHOT buffer mirroring function enable.<br>0=Normal<br>1=Mirror    |
| CAP_VIDEO_SIGNED_UV   | 11   | 0x0     | Enable conversion to signed value.<br>1=Convert to signed            |

**CAP0\_CONFIG - RW - 32 bits - [MMReg:0x958]**

| Field Name                | Bits  | Default | Description  |
|---------------------------|-------|---------|--|
| CAP_ANC_DECODE_EN         | 12    | 0x0     | ANC enable.<br>0=disable<br>1=enable   |
| CAP_VBI_EN                | 13    | 0x0     | VBI enable.<br>0=disable<br>1=enable   |
| CAP_SOFT_PULL_DOWN_EN     | 14    | 0x0     | Software pull down enable.<br>0=disable<br>1=enable  |
| CAP_VIP_EXTEND_FLAG_EN    | 15    | 0x0     | Extended flag enable.<br>0=DISABLE<br>1=ENABLE   |
| CAP_FAKE_FIELD_EN         | 16    | 0x1     | Fake field enable.<br>0=DISABLE<br>1=ENABLE  |
| CAP_FIELD_START_LINE_DIFF | 18:17 | 0x0     | Odd, Even frame line number differences.<br>0=EQUAL<br>1=ODD_ONE_MORE_LINE<br>2=EVEN_ONE_MORE_LINE     |
| CAP_HORZ_DOWN             | 20:19 | 0x0     | Horizontal decimation.<br>0=Normal<br>1=x2<br>2=x4   |
| CAP_VERT_DOWN             | 22:21 | 0x0     | Vertical decimation.<br>0=Normal<br>1=x2<br>2=x4   |
| CAP_STREAM_FORMAT         | 25:23 | 0x0     | Video stream format.<br>0=Brooktree<br>1=CCIR 656<br>2=Zoom Video<br>3=16bit VIP<br>4=TRANSPORT STREAM |
| CAP_HDWNS_DEC             | 26    | 0x1     | Horizontal downscaler or decimator.<br>0=downscaler<br>1=decimator                                     |
| CAP_VIDEO_IN_FORMAT       | 29    | 0x0     | Input format.<br>0=YVYU422<br>1=VYUY422  |
| VBI_HORZ_DOWN             | 31:30 | 0x0     | 0=Normal<br>1=x2<br>2=x4   |

Capture 0 configuration register.

**CAP0\_ANC0\_OFFSET - RW - 32 bits - [MMReg:0x95C]**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| CAP_ANC0_OFFSET | 31:0 | 0x0     | Starting address<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO. |

Capture 0 ANC 0 starting address.

**CAP0 Anc1 Offset - RW - 32 bits - [MMReg:0x960]**

| Field Name      | Bits | Default | Description      |
|-----------------|------|---------|------------------|
| CAP Anc1_Offset | 31:0 | 0x0     | Starting address |

NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 Anc 1 starting address.

**CAP0 Anc H Window - RW - 32 bits - [MMReg:0x964]**

| Field Name    | Bits | Default | Description   |
|---------------|------|---------|---------------|
| CAP Anc Width | 11:0 | 0x0     | Window width. |

NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 Anc horizontal window.

**CAP0 Video Sync Test - RW - 32 bits - [MMReg:0x968]**

| Field Name         | Bits | Default | Description                                    |
|--------------------|------|---------|--|
| CAP_Test_Vid_Sof   | 0    | 0x0     | Start of field.                                |
| CAP_Test_Vid_Eof   | 1    | 0x0     | End of field.                                  |
| CAP_Test_Vid_Eol   | 2    | 0x0     | End of line.                                   |
| CAP_Test_Vid_Field | 3    | 0x0     | Odd/Even field.<br>0=Even Field<br>1=Odd Field |
| CAP_Test_Sync_En   | 5    | 0x0     | Test sync enable.<br>0=Normal<br>1=Test Mode   |

Capture port 0 sync test.

**CAP0 Oneshot Buf Offset - RW - 32 bits - [MMReg:0x96C]**

| Field Name             | Bits | Default | Description                      |
|------------------------|------|---------|----------------------------------|
| CAP Oneshot_Buf_Offset | 31:0 | 0x0     | ONESHOT buffer starting address. |

NOTE: Bits 0:1 of this field are hardwired to ZERO.

ONESHOT buffer starting address.

**CAP0 Buf Status - R - 32 bits - [MMReg:0x970]**

| Field Name         | Bits | Default | Description                                     |
|--------------------|------|---------|---|
| CAP_Pre_Vid_Buf    | 1:0  | 0x0     | Read only. Previous capture buffer.             |
| CAP_Cur_Vid_Buf    | 3:2  | 0x0     | Read only. Current Capture buffer.              |
| CAP_Pre_Field      | 4    | 0x0     | Read only. Previous field.                      |
| CAP_Cur_Field      | 5    | 0x0     | Read only. Current field.                       |
| CAP_Pre_Vbi_Buf    | 7:6  | 0x0     | Read only. Previous VBI buffer.                 |
| CAP_Cur_Vbi_Buf    | 9:8  | 0x0     | Read only. Current VBI buffer.                  |
| CAP_Vbi_Buf_Status | 10   | 0x0     | Read only. VBI busy status.<br>0=done<br>1=busy |

**CAPO\_BUF\_STATUS - R - 32 bits - [MMReg:0x970]**

| Field Name               | Bits  | Default | Description  |
|--------------------------|-------|---------|--|
| CAP_PRE_ANC_BUF          | 12:11 | 0x0     | Read only. Previous ANC buffer.  |
| CAP_CUR_ANC_BUF          | 14:13 | 0x0     | Read only. Current ANC buffer.   |
| CAP_ANC_BUF_STATUS       | 15    | 0x0     | Read only. Buffer busy status.<br>0=done<br>1=busy                                 |
| CAP_ANC_PRE_BUF_CNT      | 27:16 | 0x0     | Read only. Buffer count.   |
| CAP_VIP_INC              | 28    | 0x0     | Read only. Interlaced or not.<br>0=INTERLACED<br>1=NON_INTERLACED                  |
| CAP_VIP_PRE_REPEAT_FIELD | 29    | 0x0     | Read only. Previous buffer is new/repeat field.<br>0=new_field<br>1=repeated_field |
| CAP_CAP_BUF_STATUS       | 30    | 0x0     | Read only. Capture buffer busy status.<br>0=done<br>1=busy                         |

Capture 0 buffer status.

**CAPO\_VBI2\_OFFSET - RW - 32 bits - [MMReg:0x980]**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| CAP_VBI2_OFFSET | 31:0 | 0x0     | Capture 0 VBI 2 buffer's starting address.<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO. |

Capture 0 VBI 2 buffer's starting address.

**CAPO\_VBI3\_OFFSET - RW - 32 bits - [MMReg:0x984]**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| CAP_VBI3_OFFSET | 31:0 | 0x0     | Capture 0 VBI 3 buffer's starting address.<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO. |

Capture 0 VBI 3 buffer's starting address.

**CAPO\_ANC2\_OFFSET - RW - 32 bits - [MMReg:0x988]**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| CAP_ANC2_OFFSET | 31:0 | 0x0     | Starting address<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO. |

Capture 0 ANC 2 starting address.

**CAPO\_ANC3\_OFFSET - RW - 32 bits - [MMReg:0x98C]**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| CAP_ANC3_OFFSET | 31:0 | 0x0     | Starting address<br><br>NOTE: Bits 0:1 of this field are hardwired to ZERO. |

Capture 0 ANC 3 starting address.

**VID\_BUFFER\_CONTROL - RW - 32 bits - [MMReg:0x900]**

| Field Name             | Bits | Default | Description                  |
|------------------------|------|---------|------------------------------|
| CAPO_BUFFER_WATER_MARK | 5:0  | 0x10    | Capture 0 buffer water mark. |

**VID\_BUFFER\_CONTROL - RW - 32 bits - [MMReg:0x900]**

| Field Name            | Bits  | Default | Description   |
|-----------------------|-------|---------|---|
| FULL_BUFFER_EN        | 16    | 0x0     | 1= The shared buffer is dedicated to one capture only.<br>0=DISABLE<br>1=ENABLE |
| CAP0 Anc_VBI_Quad_Buf | 17    | 0x0     | 0=Dual buffer<br>1=Quadruple buffer   |
| VID_BUFFER_RESET      | 20    | 0x0     | Reset the buffer pointers.<br>0=NOT RESET<br>1=RESET                            |
| CAP_SWAP              | 22:21 | 0x0     | Capture Port Swap control.  |
| CAP0_BUFFER_EMPTY (R) | 24    | 0x0     | Capture 0's buffer empty status.<br>0=EMPTY<br>1=NOT EMPTY                      |

Video Capture port buffer control.

**VIDEOMUX\_CNTL - RW - 32 bits - [MMReg:0x190]**

| Field Name             | Bits  | Default | Description   |
|------------------------|-------|---------|---|
| VIPH_INT_SEL           | 0     | 0x0     | 0=If VIP host port interrupt using input instead of polling, then MONID(1) pin used as interrupt input.<br>1=If VIP host port interrupt using input instead of polling, then I2C clock pin used as interrupt input. |
| ROM_CLK_DIVIDE         | 20:16 | 0x5     | ROM clock divider   |
| STR_ROMCLK             | 21    | 0x0     | Extend ROM cycle  |
| VIP_INTERNAL_DEBUG_SEL | 24:22 | 0x0     |   |
| GEYSERVILLE_SENSE (R)  | 25    | 0x0     |   |
| GEYSERVILLE_INT_POL    | 26    | 0x0     |   |

GPIO pin mux control

**CAP\_INT\_STATUS - RW - 32 bits - [MMReg:0x90C]**

| Field Name                | Bits | Default | Description   |
|---------------------------|------|---------|---|
| CAP0_BUF0_INT (R)         | 0    | 0x0     | Read only. Buffer 0 interrupt status.<br>0=No event<br>1=Event has occurred, interrupting if enabled            |
| CAP0_BUF0_INT_AK (W)      | 0    | 0x0     | Buf0 interrupt acknowledgment.<br>0=No effect<br>1=Clear status   |
| CAP0_BUF0_EVEN_INT (R)    | 1    | 0x0     | Read only. Buffer 0 even frame interrupt status.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| CAP0_BUF0_EVEN_INT_AK (W) | 1    | 0x0     | Buf0 even frame buffer interrupt acknowledgment.<br>0=No effect<br>1=Clear status                               |
| CAP0_BUF1_INT (R)         | 2    | 0x0     | Read only. Buffer 1 interrupt status.<br>0=No event<br>1=Event has occurred, interrupting if enabled            |
| CAP0_BUF1_INT_AK (W)      | 2    | 0x0     | Buf1 interrupt acknowledgment.<br>0=No effect<br>1=Clear status   |

**CAP\_INT\_STATUS - RW - 32 bits - [MMReg:0x90C]**

| Field Name                | Bits | Default | Description   |
|---------------------------|------|---------|---|
| CAPO_BUF1_EVEN_INT (R)    | 3    | 0x0     | Read only. Buffer 1 even frame interrupt status.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| CAPO_BUF1_EVEN_INT_AK (W) | 3    | 0x0     | Buf1 even frame buffer interrupt acknowledgment.<br>0=No effect<br>1=Clear status                               |
| CAPO_VBI0_INT (R)         | 4    | 0x0     | Read only. VBI buffer 0 interrupt status.<br>0=No event<br>1=Event has occurred, interrupting if enabled        |
| CAPO_VBI0_INT_AK (W)      | 4    | 0x0     | VBI buffer 0 interrupt acknowledgment.<br>0=No effect<br>1=Clear status   |
| CAPO_VBI1_INT (R)         | 5    | 0x0     | Read only. VBI buffer 1 interrupt status.<br>0=No event<br>1=Event has occurred, interrupting if enabled        |
| CAPO_VBI1_INT_AK (W)      | 5    | 0x0     | VBI buffer 1 interrupt acknowledgment.<br>0=No effect<br>1=Clear status   |
| CAPO_ONESHOT_INT (R)      | 6    | 0x0     | Read only. ONESHOT buffer interrupt status.<br>0=No event<br>1=Event has occurred, interrupting if enabled      |
| CAPO_ONESHOT_INT_AK (W)   | 6    | 0x0     | ONESHOT buffer interrupt acknowledgment.<br>0=No effect<br>1=Clear status                                       |
| CAPO_ANC0_INT (R)         | 7    | 0x0     | Read only. ANC buffer 0 interrupt status.<br>0=No event<br>1=Event has occurred, interrupting if enabled        |
| CAPO_ANC0_INT_AK (W)      | 7    | 0x0     | ANC buffer 0 interrupt acknowledgment.<br>0=No effect<br>1=Clear status   |
| CAPO_ANC1_INT (R)         | 8    | 0x0     | Read only. ANC buffer 1 interrupt status.<br>0=No event<br>1=Event has occurred, interrupting if enabled        |
| CAPO_ANC1_INT_AK (W)      | 8    | 0x0     | ANC buffer 1 interrupt acknowledgment.<br>0=No effect<br>1=Clear status   |
| CAPO_VBI2_INT (R)         | 9    | 0x0     | Read only. VBI buffer 2 interrupt status.<br>0=No event<br>1=Event has occurred, interrupting if enabled        |
| CAPO_VBI2_INT_AK (W)      | 9    | 0x0     | VBI buffer 2 interrupt acknowledgment.<br>0=No effect<br>1=Clear status   |
| CAPO_VBI3_INT (R)         | 10   | 0x0     | Read only. VBI buffer 3 interrupt status.<br>0=No event<br>1=Event has occurred, interrupting if enabled        |
| CAPO_VBI3_INT_AK (W)      | 10   | 0x0     | VBI buffer 3 interrupt acknowledgment.<br>0=No effect<br>1=Clear status   |

**CAP\_INT\_STATUS - RW - 32 bits - [MMReg:0x90C]**

| Field Name           | Bits | Default | Description  |
|----------------------|------|---------|--|
| CAPO_ANC2_INT (R)    | 11   | 0x0     | Read only. ANC buffer 2 interrupt status.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| CAPO_ANC2_INT_AK (W) | 11   | 0x0     | ANC buffer 2 interrupt acknowledgment.<br>0=No effect<br>1=Clear status                                  |
| CAPO_ANC3_INT (R)    | 12   | 0x0     | Read only. ANC buffer 3 interrupt status.<br>0=No event<br>1=Event has occurred, interrupting if enabled |
| CAPO_ANC3_INT_AK (W) | 12   | 0x0     | ANC buffer 3 interrupt acknowledgment.<br>0=No effect<br>1=Clear status                                  |

Capture port interrupt control.

**CAP\_INT\_CNTL - RW - 32 bits - [MMReg:0x908]**

| Field Name            | Bits | Default | Description  |
|-----------------------|------|---------|--|
| CAPO_BUF0_INT_EN      | 0    | 0x0     | Capture 0 Buffer 0 Interrupt enable.<br>0=Disable<br>1=Enable            |
| CAPO_BUF0_EVEN_INT_EN | 1    | 0x0     | Capture 0 Buffer 0 even frame Interrupt enable.<br>0=Disable<br>1=Enable |
| CAPO_BUF1_INT_EN      | 2    | 0x0     | Capture 0 Buffer 1 Interrupt enable.<br>0=Disable<br>1=Enable            |
| CAPO_BUF1_EVEN_INT_EN | 3    | 0x0     | Capture 0 Buffer 1 even frame Interrupt enable.<br>0=Disable<br>1=Enable |
| CAPO_VBI0_INT_EN      | 4    | 0x0     | Capture 0 VBI Buffer 0 Interrupt enable.<br>0=Disable<br>1=Enable        |
| CAPO_VBI1_INT_EN      | 5    | 0x0     | Capture 0 VBI Buffer 1 Interrupt enable.<br>0=Disable<br>1=Enable        |
| CAPO_ONESHOT_INT_EN   | 6    | 0x0     | Capture 0 ONESHOT Buffer Interrupt enable.<br>0=Disable<br>1=Enable      |
| CAPO_ANC0_INT_EN      | 7    | 0x0     | Capture 0 ANC Buffer 0 Interrupt enable.<br>0=Disable<br>1=Enable        |
| CAPO_ANC1_INT_EN      | 8    | 0x0     | Capture 0 ANC Buffer 1 Interrupt enable.<br>0=Disable<br>1=Enable        |
| CAPO_VBI2_INT_EN      | 9    | 0x0     | Capture 0 VBI Buffer 2 Interrupt enable.<br>0=Disable<br>1=Enable        |



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**CAP\_INT\_CNTL - RW - 32 bits - [MMReg:0x908]**

| Field Name       | Bits | Default | Description   |
|------------------|------|---------|---|
| CAP0_VBI3_INT_EN | 10   | 0x0     | Capture 0 VBI Buffer 3 Interrupt enable.<br>0=Disable<br>1=Enable |
| CAP0_ANC2_INT_EN | 11   | 0x0     | Capture 0 ANC Buffer 2 Interrupt enable.<br>0=Disable<br>1=Enable |
| CAP0_ANC3_INT_EN | 12   | 0x0     | Capture 0 ANC Buffer 3 Interrupt enable.<br>0=Disable<br>1=Enable |

Video Capture port interrupt control register

**GEN\_INT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x40]**

| Field Name                            | Bits | Default | Description  |
|---------------------------------------|------|---------|--|
| CRTC_VBLANK_MASK<br>(DISPLAY)         | 0    | 0x0     | Vertical blank interrupt mask.<br>0=Disable<br>1=Enable        |
| CRTC_VLINE_MASK<br>(DISPLAY)          | 1    | 0x0     | Vertical line interrupt mask.<br>0=Disable<br>1=Enable         |
| CRTC_VSYNC_MASK<br>(DISPLAY)          | 2    | 0x0     | Vertical sync interrupt mask.<br>0=Disable<br>1=Enable         |
| SNAPSHOT_MASK<br>(DISPLAY)            | 3    | 0x0     | Snapshot interrupt mask.<br>0=Disable<br>1=Enable              |
| FP_DETECT_MASK<br>(DISPLAY)           | 4    | 0x0     | Hot plug detect (HPD) interrupt mask.<br>0=Disable<br>1=Enable |
| CRTC2_VLINE_MASK<br>(DISPLAY)         | 5    | 0x0     | 0=Disable<br>1=Enable  |
| CRTC2_VSYNC_MASK<br>(DISPLAY)         | 6    | 0x0     | 0=Disable<br>1=Enable  |
| SNAPSHOT2_MASK<br>(DISPLAY)           | 7    | 0x0     | 0=Disable<br>1=Enable  |
| CRTC2_VBLANK_MASK<br>(DISPLAY)        | 9    | 0x0     | 0=Disable<br>1=Enable  |
| FP2_DETECT_MASK<br>(DISPLAY)          | 10   | 0x0     | 0=Disable<br>1=Enable  |
| VSYNC_DIFF_OVER_LIMIT_MASK<br>(TVOUT) | 11   | 0x0     | 0=Disable<br>1=Enable  |
| DMA_VIPH0_INT_EN<br>(VIP)             | 12   | 0x0     | 0=Disable<br>1=Enable  |
| DMA_VIPH1_INT_EN<br>(VIP)             | 13   | 0x0     | 0=Disable<br>1=Enable  |

**GEN\_INT\_CNTL - RW - 32 bits - [IOReg,MMReg:0x40]**

| Field Name                            | Bits | Default | Description  |
|---------------------------------------|------|---------|--|
| DMA_VIPH2_INT_EN<br>(VIP)             | 14   | 0x0     | 0=Disable<br>1=Enable  |
| DMA_VIPH3_INT_EN<br>(VIP)             | 15   | 0x0     | 0=Disable<br>1=Enable  |
| I2C_INT_EN<br>(VIP)                   | 17   | 0x0     | 0=Disable<br>1=Enable  |
| GUI_IDLE_MASK<br>(RBBM)               | 19   | 0x0     | GUI idle interrupt mask.<br>0=Disable<br>1=Enable                  |
| VIPH_INT_EN<br>(VIP)                  | 24   | 0x0     | 0=Disable<br>1=Enable  |
| SW_INT_EN<br>(HDP)                    | 25   | 0x0     | Software interrupt mask.<br>0=Disable<br>1=Enable                  |
| GEYSERVILLE_MASK<br>(VIP)             | 27   | 0x0     | 0=Disable<br>1=Enable  |
| HDCP_AUTHORIZED_INT_MASK<br>(DISPLAY) | 28   | 0x0     | 0=Disable<br>1=Enable  |
| DVI_I2C_INT_MASK<br>(DISPLAY)         | 29   | 0x0     | 0=Disable<br>1=Enable  |
| GUIDMA_MASK<br>(CP)                   | 30   | 0x0     | GUI DMA channel interrupt mask.<br>0=Disable<br>1=Enable           |
| VIDDMA_MASK<br>(CP)                   | 31   | 0x0     | Video capture DMA channel interrupt mask.<br>0=Disable<br>1=Enable |

General Interrupt Control register.

The MASK/EN fields control whether the respective status bits are enabled to drive the system interrupt pin. Even if enabled here, the interrupt line is not driven unless enabled in the PCI configuration space.

**EXTERN\_TRIG\_CNTL - RW - 32 bits - [MMReg:0x1BC]**

| Field Name           | Bits | Default | Description   |
|----------------------|------|---------|---|
| EXTERN_TRIG_CLR (W)  | 0    | 0x0     | 0=Write 0 has no affect.<br>1=Write 1 sets EXTERN_TRIG to 0. This can then be used with WAIT_UNTIL(19) to stall until external signal pulses. |
| EXTERN_TRIG_READ (R) | 1    | 0x0     | 0=Read 1 indicates WAIT condition not active.<br>1=Read 0 indicates WAIT condition active.  |

No description available for this register.

**40. GPIO Detailed Register Reference**

General Purpose IO Control Registers.

| <b>CONFIG_XSTRAP - R - 32 bits - [IOReg,MMReg:0xE4]</b> |             |                |  |
|---|-------------|----------------|--|
| <b>Field Name</b>                                       | <b>Bits</b> | <b>Default</b> | <b>Description</b>                                     |
| VGA_DISABLE   | 0           | 0x0            | VGA controller capability disable.                     |
| BLANK_ROM   | 2           | 0x0            | Blank Rom on board.                                    |
| ENINTB  | 3           | 0x0            | Enable Interrup.                                       |
| MULTI_FUNC  | 5:4         | 0x0            |  |
| AGPSKEW   | 7:6         | 0x0            | AGP1x clock feedback phaseadjustment wrt refclk.       |
| X1CLK_SKEW  | 9:8         | 0x0            | Clock phase adjustment between x1clk and x2clk.        |
| VIP_DEVICE  | 13          | 0x0            |  |
| ID_DISABLE  | 14          | 0x0            | Shut down the chip by not responding to config cycles. |
| AP_SIZE   | 17:16       | 0x0            |  |
| ROMIDCFG  | 23:20       | 0x0            |  |
| BUSCFG  | 26:24       | 0x0            |  |

Strap read back.

| <b>GPIOPAD_MASK - RW - 32 bits - [MMReg:0x198]</b> |             |                |                    |
|--|-------------|----------------|--------------------|
| <b>Field Name</b>                                  | <b>Bits</b> | <b>Default</b> | <b>Description</b> |
| GPIO_MASK  | 15:0        | 0x0            |                    |

No description available for this register.

| <b>GPIOPAD_A - RW - 32 bits - [MMReg:0x19C]</b> |             |                |                    |
|---|-------------|----------------|--------------------|
| <b>Field Name</b>                               | <b>Bits</b> | <b>Default</b> | <b>Description</b> |
| GPIO_A  | 15:0        | 0x0            |                    |

No description available for this register.

| <b>GPIOPAD_EN - RW - 32 bits - [MMReg:0x1A0]</b> |             |                |                    |
|--|-------------|----------------|--------------------|
| <b>Field Name</b>                                | <b>Bits</b> | <b>Default</b> | <b>Description</b> |
| GPIO_EN  | 15:0        | 0x0            |                    |

No description available for this register.

| <b>GPIOPAD_Y - R - 32 bits - [MMReg:0x1A4]</b> |             |                |                    |
|--|-------------|----------------|--------------------|
| <b>Field Name</b>                              | <b>Bits</b> | <b>Default</b> | <b>Description</b> |
| GPIO_Y   | 15:0        | 0x0            |                    |

No description available for this register.

| <b>VIPPAD_STRENGTH - RW - 32 bits - [MMReg:0x194]</b> |             |                |  |
|---|-------------|----------------|--|
| <b>Field Name</b>                                     | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| ZV_LCDDATA_STRENGTH                                   | 1:0         | 0x2            | 0=Minimum drive. ~74 ohms.<br>1=Matched impedance drive. ~63 ohms.<br>2=Optimal drive. ~47 ohms.<br>3=Maximum drive. ~42 ohms. |

**VIPPAD\_STRENGTH - RW - 32 bits - [MMReg:0x194]**

| Field Name          | Bits  | Default | Description  |
|---------------------|-------|---------|--|
| ZV_LCDCNTL_STRENGTH | 9:8   | 0x2     | 0=Minimum drive. ~74 ohms.<br>1=Matched impedance drive. ~63 ohms.<br>2=Optimal drive. ~47 ohms.<br>3=Maximum drive. ~42 ohms. |
| GPIO_STRENGTH       | 13:12 | 0x2     | 0=Minimum drive. ~74 ohms.<br>1=Matched impedance drive. ~63 ohms.<br>2=Optimal drive. ~47 ohms.<br>3=Maximum drive. ~42 ohms. |

No description available for this register.

**ZV\_LCDPAD\_MASK - RW - 32 bits - [MMReg:0x1A8]**

| Field Name      | Bits  | Default | Description |
|-----------------|-------|---------|-------------|
| ZV_LCDDATA_MASK | 23:0  | 0x0     |             |
| ZV_LCDCNTL_MASK | 27:24 | 0x0     |             |

No description available for this register.

**ZV\_LCDPAD\_A - RW - 32 bits - [MMReg:0x1AC]**

| Field Name   | Bits  | Default | Description |
|--------------|-------|---------|-------------|
| ZV_LCDDATA_A | 23:0  | 0x0     |             |
| ZV_LCDCNTL_A | 27:24 | 0x0     |             |

No description available for this register.

**ZV\_LCDPAD\_EN - RW - 32 bits - [MMReg:0x1B0]**

| Field Name    | Bits  | Default | Description |
|---------------|-------|---------|-------------|
| ZV_LCDDATA_EN | 23:0  | 0x0     |             |
| ZV_LCDCNTL_EN | 27:24 | 0x0     |             |

No description available for this register.

**ZV\_LCDPAD\_Y - R - 32 bits - [MMReg:0x1B4]**

| Field Name   | Bits  | Default | Description |
|--------------|-------|---------|-------------|
| ZV_LCDDATA_Y | 23:0  | 0x0     |             |
| ZV_LCDCNTL_Y | 27:24 | 0x0     |             |

No description available for this register.

**41. ROM Detailed Register Reference**

ROM registers

| <b>SEEPROM_CNTL1 - RW - 32 bits - [MMReg:0x1C0]</b> |             |                |  |
|---|-------------|----------------|--|
| <b>Field Name</b>                                   | <b>Bits</b> | <b>Default</b> | <b>Description</b>   |
| WRITE_ENABLE  | 0           | 0x0            | Set WRITE_ENABLE to be the command field   |
| WRITE_DISABLE                                       | 1           | 0x0            | Set WRITE_DISABLE to be the command field  |
| READ_CONFIG   | 2           | 0x0            | Set READ_CONFIG to be the command field  |
| WRITE_CONFIG  | 3           | 0x0            | Set WRITE_CONFIG to be the command field   |
| READ_STATUS   | 4           | 0x0            | Set READ_STATUS to be the command field  |
| SECT_TO_SRAM  | 5           | 0x0            | Set SECT_TO_SRAM to be the command field   |
| READY_BUSY (R)                                      | 7           | 0x0            | Status bit that reflects the status of the HOLD/READY_BUSY bus   |
| SEEPROM_BUSY (R)                                    | 8           | 0x0            | Status bit that indicates the status of the SPI state machine  |
| BCNT_OVER_WTE_EN                                    | 9           | 0x0            | This bit must be set to '1' for burst ROM write/read. This bit works coherently with the BYTE_CNT.   |
| RB_MASKB  | 10          | 0x0            |  |
| SOFT_RESET  | 11          | 0x0            |  |
| STATE_IDLEb (R)                                     | 12          | 0x0            |  |
| BYTE_CNT  | 23:16       | 0xff           | The BYTE_CNT works coherently with the BCNT_OVER_WTE_EN. Programming the BYTE_CNT has no effect if BCNT_OVER_WTE_EN is '0'. The BYTE_CNT can be programmed to tell the SPI state machine how many byte will be sent/read.<br><br>BYTE_CNT = 0 means 1 byte will be sent<br>' '<br>BYTE_CNT = 255 means 256 byte will be sent |
| SCK_PRESCALE  | 31:24       | 0x4            | This changes the SCK period with this function:<br>SCK period = (SCK_PRESCALE + 1) * 2 * (SYSTEM CLOCK period)   |

First SPI Serial ROM Control register

| <b>SEEPROM_CNTL2 - RW - 32 bits - [MMReg:0x1C4]</b> |             |                |                    |
|---|-------------|----------------|--------------------|
| <b>Field Name</b>                                   | <b>Bits</b> | <b>Default</b> | <b>Description</b> |
| WAIT_CYCLE  | 7:0         | 0x5            |                    |
| AUTO_ADDR_SAMPLE                                    | 8           | 0x1            |                    |
| SEC_COMMAND   | 23:16       | 0x0            |                    |

Second SPI Serial ROM Control register

**42. Render Backend 2D****RB2D\_ROP - R - 32 bits - [MMReg:0x3400]**

| Field Name | Bits  | Default | Description   |
|------------|-------|---------|---|
| ROP        | 23:16 | none    | 3D ROP, ROP2 code for 3D fragments. This value is replicated into 2 nibbles to form the equivalent ROP3 code to control the ROP3 logic. |

ROP control register , Windows 3.1 ROP code.

**RB2D\_CLRCMP\_SRC - R - 32 bits - [MMReg:0x3408]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| CLRCMP_SRC | 31:0 | none    | Color Compare Source , Comparison color for source. The format of this color is based on the 2D destination data format. |

Color Compare Source , Comparison color for source.

**RB2D\_CLRCMP\_DST - R - 32 bits - [MMReg:0x340C]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| CLRCMP_DST | 31:0 | none    | Color Compare Dest , Comparison color for destination. The format of this color is based on the 2D destination data format. |

Color Compare Dest , Comparison color for destination.

**RB2D\_CLRCMP\_FLIPE - R - 32 bits - [MMReg:0x3410]**

| Field Name   | Bits | Default | Description   |
|--------------|------|---------|---|
| CLRCMP_FLIPE | 31:0 | none    | Color Compare Flip, This shadows E2_SRC_FRGD_CLR and is written via the DP_SRC_FRGD_CLR register location. This is the foreground color. When RB2D_CLRCMP_CNTL.FCN_SRC = 7, a '1' in bit location n means enable flipping on bit n. |

Color Compare Flip, Color Compare flip register.

**RB2D\_CLRCMP\_CNTL - R - 32 bits - [MMReg:0x3414]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| FCN_SRC    | 2:0  | none    | Color Compare Source Function, Specifies the function to perform on the source color compare.<br>0=False (cmp_false, always draw)<br>1=True (cmp_true, never draw)<br>2=RESERVED<br>3=RESERVED<br>4=SRC == CLRCMP_SRC (do not draw if equal)<br>5=SRC != CLRCMP_SRC (draw if equal)<br>6=RESERVED<br>7=SRC == CLRCMP_SRC and FLIP |

**RB2D\_CLRCMP\_CNTL - R - 32 bits - [MMReg:0x3414]**

| Field Name | Bits  | Default | Description  |
|------------|-------|---------|--|
| FCN_DST    | 10:8  | none    | Color Compare Destination Function, Specifies the function to perform on the source color compare.<br>0=False (cmp_false, always draw)<br>1=True (cmp_true, never draw)<br>2=RESERVED<br>3=RESERVED<br>4=SRC == CLRCMP_SRC (do not draw if equal)<br>5=SRC != CLRCMP_SRC (draw if equal)<br>6=RESERVED<br>7=RESERVED |
| SRC        | 25:24 | none    | Color Compare Function Select, Selects which color compare results to use in the final compare results.<br>0=Destination<br>1=Source<br>2=Src AND Dst<br>3=Hilite  |

Color Compare Control, Controls the color compare logic.

**RB2D\_CLRCMP\_MSK - R - 32 bits - [MMReg:0x3418]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| CLRCMP_MSK | 31:0 | none    | Color Compare Mask, This is ANDed with source and destination before compare. |

Color Compare Mask, This is ANDed with source and destination before compare.

**RB2D\_WRITEMASK - R - 32 bits - [MMReg:0x341C]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| WRITEMASK  | 31:0 | none    | Write Mask, This is a bit mask that should be set with byte alignment for better performance. |

Write Mask, This is a bit mask.

**RB2D\_DATATYPE - R - 32 bits - [MMReg:0x3420]**

| Field Name        | Bits | Default | Description   |
|-------------------|------|---------|---|
| DP_DST_DATATYPE   | 3:0  | none    | 2D Destination Datatype, Shadow of the E2_DST_DATATYPE field in 2D pipe. Written via DP_DATATYPE register address in the 2D pipe. |
| DP_BRUSH_DATATYPE | 11:8 | none    | Brush Datatype, Shadow of the E2_DST_DATATYPE field in 2D pipe. Written via DP_DATATYPE register address in the 2D pipe.          |

2D Data Formats, Denotes format of 2D destination and brush.

**RB2D\_GUI\_MASTER\_CNTL - R - 32 bits - [MMReg:0x3424]**

| Field Name   | Bits | Default | Description  |
|--|------|---------|--|
| GMC_BRUSH_DATATYPE<br><i>(mirror of<br/>RB2D_DATATYPE:DP_BRUSH_DATATYPE)</i> | 7:4  | none    | GMC_BRUSH_DATATYPE shadow, Shadow of GMC_BRUSH_DATATYPE field of DP_GUI_MASTER_CNTL register in 2D pipe. Value of this field is loaded into RB2D_DATATYPE.DP_BRUSH_DATATYPE. |

**RB2D\_GUI\_MASTER\_CNTL - R - 32 bits - [MMReg:0x3424]**

| Field Name   | Bits  | Default | Description  |
|--|-------|---------|--|
| GMC_DST_DATATYPE<br><i>(mirror of RB2D_DATATYPE:DP_DST_DATATYPE)</i> | 11:8  | none    | GMC_DST_DATATYPE shadow, Shadow of GMC_DST_DATATYPE field of DP_GUI_MASTER_CNTL register in 2D pipe. Value of this field is loaded into RB2D_DATATYPE.DP_DST_DATATYPE. |
| GMC_ROP<br><i>(mirror of RB2D_ROP:ROP)</i>                           | 23:16 | none    |  |
| GMC_CLR_CMP_FCN_DIS  | 28    | none    | GMC_CLR_CMP_FCN_DIS shadow, Clear RB2D_CLRCMP_CNTL if set, else does nothing. Shadow of GMC_CLR_CMP_FCN_DIS field of DP_GUI_MASTER_CNTL register in 2D pipe.           |
| GMC_WR_MSK_DIS   | 30    | none    | GMC_WR_MASK_DIS shadow, Sets RB2D_WRITEMASK to 0xFFFFFFFF if set, else does nothing. Shadow of GMC_WR_MASK_DIS field of DP_GUI_MASTER_CNTL register in 2D pipe.        |

GUI Master Control, Master control register for 2D operations

**RB2D\_BRUSHDATA\_0 - R - 32 bits - [MMReg:0x3500]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_1 - R - 32 bits - [MMReg:0x3504]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_2 - R - 32 bits - [MMReg:0x3508]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_3 - R - 32 bits - [MMReg:0x350C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_4 - R - 32 bits - [MMReg:0x3510]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_5 - R - 32 bits - [MMReg:0x3514]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_6 - R - 32 bits - [MMReg:0x3518]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

**RB2D\_BRUSHDATA\_6 - R - 32 bits - [MMReg:0x3518]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

No description available for this register.

**RB2D\_BRUSHDATA\_7 - R - 32 bits - [MMReg:0x351C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

BRUSHDATA

31:0

none

No description available for this register.

**RB2D\_BRUSHDATA\_8 - R - 32 bits - [MMReg:0x3520]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

BRUSHDATA

31:0

none

No description available for this register.

**RB2D\_BRUSHDATA\_9 - R - 32 bits - [MMReg:0x3524]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

BRUSHDATA

31:0

none

No description available for this register.

**RB2D\_BRUSHDATA\_10 - R - 32 bits - [MMReg:0x3528]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

BRUSHDATA

31:0

none

No description available for this register.

**RB2D\_BRUSHDATA\_11 - R - 32 bits - [MMReg:0x352C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

BRUSHDATA

31:0

none

No description available for this register.

**RB2D\_BRUSHDATA\_12 - R - 32 bits - [MMReg:0x3530]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

BRUSHDATA

31:0

none

No description available for this register.

**RB2D\_BRUSHDATA\_13 - R - 32 bits - [MMReg:0x3534]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

BRUSHDATA

31:0

none

No description available for this register.

**RB2D\_BRUSHDATA\_14 - R - 32 bits - [MMReg:0x3538]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

BRUSHDATA

31:0

none

No description available for this register.

**RB2D\_BRUSHDATA\_15 - R - 32 bits - [MMReg:0x353C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

BRUSHDATA

31:0

none

No description available for this register.

**RB2D\_BRUSHDATA\_16 - R - 32 bits - [MMReg:0x3540]**



| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_17 - R - 32 bits - [MMReg:0x3544]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_18 - R - 32 bits - [MMReg:0x3548]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_19 - R - 32 bits - [MMReg:0x354C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_20 - R - 32 bits - [MMReg:0x3550]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_21 - R - 32 bits - [MMReg:0x3554]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_22 - R - 32 bits - [MMReg:0x3558]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_23 - R - 32 bits - [MMReg:0x355C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_24 - R - 32 bits - [MMReg:0x3560]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_25 - R - 32 bits - [MMReg:0x3564]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_26 - R - 32 bits - [MMReg:0x3568]**



| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_27 - R - 32 bits - [MMReg:0x356C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_28 - R - 32 bits - [MMReg:0x3570]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_29 - R - 32 bits - [MMReg:0x3574]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_30 - R - 32 bits - [MMReg:0x3578]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_31 - R - 32 bits - [MMReg:0x357C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_32 - R - 32 bits - [MMReg:0x3580]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_33 - R - 32 bits - [MMReg:0x3584]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_34 - R - 32 bits - [MMReg:0x3588]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_35 - R - 32 bits - [MMReg:0x358C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_36 - R - 32 bits - [MMReg:0x3590]**



| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_37 - R - 32 bits - [MMReg:0x3594]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_38 - R - 32 bits - [MMReg:0x3598]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_39 - R - 32 bits - [MMReg:0x359C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_40 - R - 32 bits - [MMReg:0x35A0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_41 - R - 32 bits - [MMReg:0x35A4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_42 - R - 32 bits - [MMReg:0x35A8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_43 - R - 32 bits - [MMReg:0x35AC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_44 - R - 32 bits - [MMReg:0x35B0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_45 - R - 32 bits - [MMReg:0x35B4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_46 - R - 32 bits - [MMReg:0x35B8]**



| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_47 - R - 32 bits - [MMReg:0x35BC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_48 - R - 32 bits - [MMReg:0x35C0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_49 - R - 32 bits - [MMReg:0x35C4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_50 - R - 32 bits - [MMReg:0x35C8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_51 - R - 32 bits - [MMReg:0x35CC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_52 - R - 32 bits - [MMReg:0x35D0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_53 - R - 32 bits - [MMReg:0x35D4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_54 - R - 32 bits - [MMReg:0x35D8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_55 - R - 32 bits - [MMReg:0x35DC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_56 - R - 32 bits - [MMReg:0x35E0]**



| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_57 - R - 32 bits - [MMReg:0x35E4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_58 - R - 32 bits - [MMReg:0x35E8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_59 - R - 32 bits - [MMReg:0x35EC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_60 - R - 32 bits - [MMReg:0x35F0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_61 - R - 32 bits - [MMReg:0x35F4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_62 - R - 32 bits - [MMReg:0x35F8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_BRUSHDATA\_63 - R - 32 bits - [MMReg:0x35FC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSHDATA  | 31:0 | none    |             |

No description available for this register.

**RB2D\_DSTCACHE\_MODE - R - 32 bits - [MMReg:0x3428]**

| Field Name   | Bits | Default | Description   |
|--|------|---------|---|
| DC_BYPASS<br><i>(mirror of<br/>RB3D_DSTCACHE_MODE:DC_BYPASS)</i> | 1:0  | none    | Dst Cache Bypass, Disables cache when set. This field is cleared to 0 on reset so that by default, both destination caches are enabled.<br>0=3D cache enabled, 2D cache enabled (Default)<br>1=3D cache enabled, 2D cache disabled<br>2=3D cache disabled, 2D cache enabled<br>3=3D cache disabled, 2D cache disabled |

**RB2D\_DSTCACHE\_MODE - R - 32 bits - [MMReg:0x3428]**

| Field Name   | Bits | Default | Description   |
|--|------|---------|---|
| DC_LINE_SIZE<br><i>(mirror of RB3D_DSTCACHE_MODE:DC_LINE_SIZE)</i>               | 3:2  | none    | 0=256-bit 3D, 256-bit 2D lines (Default)<br>1=256-bit 3D, 128-bit 2D lines<br>2=128-bit 3D, 256-bit 2D lines<br>3=128-bit 3D, 128-bit 2D lines  |
| DC_AUTOFLUSH_ENABLE<br><i>(mirror of RB3D_DSTCACHE_MODE:DC_AUTOFLUSH_ENABLE)</i> | 9:8  | none    | 0=No autoflush 3D, no autoflush 2D<br>1=No autoflush 3D, autoflush 2D<br>2=Autoflush 3D, no autoflush 2D<br>3=Autoflush 3D, autoflush 2D (Default)  |
| DC_FORCE_RMW<br><i>(mirror of RB3D_DSTCACHE_MODE:DC_FORCE_RMW)</i>               | 16   | none    | Dst Cache Force Read-Modify-Write, Controls whether or not to optimize for write-only Dst modes. This bit is reset to 0 and is intended for debug purposes only.<br>0=Write-only Enabled<br>1=Write-only Disabled |
| DC_DISABLE_RI_FILL<br><i>(mirror of RB3D_DSTCACHE_MODE:DC_DISABLE_RI_FILL)</i>   | 24   | none    | 0=Enabled<br>1=Disabled   |
| DC_DISABLE_RI_READ<br><i>(mirror of RB3D_DSTCACHE_MODE:DC_DISABLE_RI_READ)</i>   | 25   | none    | 0=Enabled<br>1=Disabled   |

Dst Cache Mode, Alias to RB3D\_CACHE\_MODE Dst Cache Bypass, Alias to RB3D\_CACHE\_MODE.DC\_BYPASS Dst Cache Force Read-Modify-Write, Alias to RB3D\_CACHE\_MODE.DC\_FORCE\_RMW Dst Cache Disable Fill Check, Alias to RB3D\_CACHE\_MODE.DC\_RI\_FILL Dst Cache Disable Read Check, Alias to RB3D\_CACHE\_MODE.DC\_RI\_READ

**RB2D\_DSTCACHE\_CTLSTAT - R - 32 bits - [MMReg:0x342C]**

| Field Name  | Bits | Default | Description   |
|---|------|---------|---|
| DC_FLUSH<br><i>(mirror of RB3D_DSTCACHE_CTLSTAT:DC_FLUSH)</i> | 1:0  | none    | Dst Cache Flush, Setting this bit flushes dirty data from the 2D and/or 3D Dst Cache. Unless the DC_FREE bits are also set, the tags in the cache remain valid. A purge is achieved by setting both DC_FLUSH and DC_FREE. These are sticky bits that clear themselves at the end of the flush operation.<br>0=No effect<br>1=Flush dirty 2D Dst Data<br>2=Flush dirty 2D Dst Data<br>3=Flush all dirty Dst Data |
| DC_FREE<br><i>(mirror of RB3D_DSTCACHE_CTLSTAT:DC_FREE)</i>   | 3:2  | none    | Dst Cache Free, Setting this bit invalidates the 2D and/or 3D Dst Cache tags. Unless the DC_FLUSH bit is also set, the cache lines are not written to memory. A purge is achieved by setting both DC_FLUSH and DC_FREE. These are sticky bits that clear themselves at the end of the flush operation.<br>0=No effect<br>1=Free 2D Dst tags<br>2=Free 3D Dst tags<br>3=Free all Dst tags                        |
| DC_BUSY<br><i>(mirror of RB3D_DSTCACHE_CTLSTAT:DC_BUSY)</i>   | 31   | none    | Dst Cache Busy.<br>0=Idle<br>1=Busy   |

Dst Cache Control and Status, Alias to RB3D\_CACHE\_MODE Dst Cache Flush, Alias to RB3D\_CACHE\_MODE.DC\_FLUSH Dst Cache Free, Alias to RB3D\_CACHE\_MODE.DC\_FREE Dst Cache Read Invalidate, Alias to RB3D\_CACHE\_MODE.DC\_RI Dst Cache Busy, Alias to RB3D\_CACHE\_MODE.DC\_BUSY

**RB2D\_SRC\_ENDIAN - R - 32 bits - [MMReg:0x3430]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| SRC_ENDIAN | 1:0  | none    | 0=No swap<br>1=Word swap<br>2=Dword swap<br>3=RESERVED |

No description available for this register.

**RB2D\_DST\_ENDIAN - R - 32 bits - [MMReg:0x3434]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| DST_ENDIAN | 1:0  | none    | 0=No swap<br>1=Word swap<br>2=Dword swap<br>3=RESERVED |

No description available for this register.

**RB2D\_PD1\_DATA - RW - 32 bits - [MMReg:0x3438]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| PD1_DATA   | 31:0 | none    |             |

No description available for this register.

**RB2D\_PD1\_ADDR - RW - 32 bits - [MMReg:0x343C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| PD1_ADDR   | 2:0  | none    |             |

No description available for this register.

**RB2D\_WRITEBACK\_DATA\_LO - RW - 32 bits - [MMReg:0x3450]**

| Field Name   | Bits | Default | Description   |
|--|------|---------|---|
| WRITEBACK_DATA_LO<br><i>(mirror of<br/>RB3D_WRITEBACK_DATA_LO:WRITEBACK_DATA_LO)</i> | 31:0 | none    | Write-back Data Register Lo , Lower DWORD for write-back. The transfer to memory occurs when WRITEBACK_ADDR is written. |

Write-back Data Register Lo, Alias to RB3D\_WRITEBACK\_DATA\_LO. Write-back Data Register Lo, Alias to RB3D\_WRITEBACK\_DATA\_LO.WRITEBACK\_DATA\_LO.

**RB2D\_WRITEBACK\_DATA\_HI - RW - 32 bits - [MMReg:0x3454]**

| Field Name   | Bits | Default | Description   |
|--|------|---------|---|
| WRITEBACK_DATA_HI<br><i>(mirror of<br/>RB3D_WRITEBACK_DATA_HI:WRITEBACK_DATA_HI)</i> | 31:0 | none    | Write-back Data Register Hi , Upper DWORD for registers write-back. The transfer to memory occurs when WRITEBACK_ADDR is written. |

Write-back Data Register Hi , Alias to RB3D\_WRITEBACK\_DATA\_HI Write-back Data Register Hi , Alias to RB3D\_WRITEBACK\_DATA\_HI.WRITEBACK\_DATA\_HI.

**RB2D\_WRITEBACK\_ADDR - RW - 32 bits - [MMReg:0x3458]**

| Field Name  | Bits | Default | Description   |
|---|------|---------|---|
| WRITEBACK_ADDR<br><i>(mirror of<br/>RB3D_WRITEBACK_ADDR:WRITEBACK_ADDR)</i> | 31:3 | none    | Write-back Address Register , Address to write DWORDS to. The transfer to memory occurs when WRITEBACK_ADDR is written. The 64-bits pointed to by this address is written with WRITEBACK_DATA_HI and WRITEBACK_DATA_LO. |



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5 September, 2001

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7 September, 2001

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**RB2D\_WRITEBACK\_ADDR - RW - 32 bits - [MMReg:0x3458]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

Write-back Address Register , Alias to RB3D\_WRITEBACK\_ADDR. Write-back Address Register , Alias to RB3D\_WRITEBACK\_ADDR.WRITEBACK\_ADDR.

**43. Render Backend 3D**

| <b>RB3D_BLENDCTL - RW - 32 bits - [MMReg:0x1C20] [MMReg:0x3220]</b> |             |                |   |
|---|-------------|----------------|---|
| <b>Field Name</b>   | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| COMB_FCN  | 13:12       | none           | Combine Function , Allows modification of how the SRCBLEND and DESTBLEND are combined.<br>0=Add and Clamp<br>1=Add but no Clamp<br>2=Subtract Dst from Src, and Clamp<br>3=Subtract Dst from Src, and don't Clamp   |
| SRCBLEND  | 21:16       | none           | Source Blend Function , Alpha blending function (SRC).<br>0=RESERVED<br>1=D3D_ZERO<br>2=D3D_ONE<br>3=D3D_SRCCOLOR<br>4=D3D_INVSRCOLOR<br>5=D3D_SRCALPHA<br>6=D3D_INVSRCALPHA<br>7=D3D_DESTALPHA<br>8=D3D_INVDESTALPHA<br>9=D3D_DESTCOLOR<br>10=D3D_INVDESTCOLOR<br>11=D3D_SRCALPHASAT<br>12=D3D_BOTHSRCALPHA<br>13=D3D_BOTHINVSRCALPHA<br>14=RESERVED<br>15=RESERVED<br>16=RESERVED<br>17=RESERVED<br>18=RESERVED<br>19=RESERVED<br>20=RESERVED<br>21=RESERVED<br>22=RESERVED<br>23=RESERVED<br>24=RESERVED<br>25=RESERVED<br>26=RESERVED<br>27=RESERVED<br>28=RESERVED<br>29=RESERVED<br>30=RESERVED<br>31=RESERVED<br>32=GL_ZERO<br>33=GL_ONE<br>34=GL_SRC_COLOR<br>35=GL_ONE_MINUS_SRC_COLOR<br>36=GL_DST_COLOR<br>37=GL_ONE_MINUS_DST_COLOR<br>38=GL_SRC_ALPHA<br>39=GL_ONE_MINUS_SRC_ALPHA<br>40=GL_DST_ALPHA<br>41=GL_ONE_MINUS_DST_ALPHA<br>42=GL_SRC_ALPHA_SATURATE<br>43=RESERVED<br>44=RESERVED<br>45=RESERVED<br>46=RESERVED<br>47=RESERVED<br>48=RESERVED<br>49=RESERVED<br>50=RESERVED |



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**RB3D\_BLENDCTL - RW - 32 bits - [MMReg:0x1C20] [MMReg:0x3220]**

| Field Name | Bits  | Default | Description   |
|------------|-------|---------|---|
|            |       |         | 51=RESERVED<br>52=RESERVED<br>53=RESERVED<br>54=RESERVED<br>55=RESERVED<br>56=RESERVED<br>57=RESERVED<br>58=RESERVED<br>59=RESERVED<br>60=RESERVED<br>61=RESERVED<br>62=RESERVED<br>63=RESERVED   |
| DESTBLEND  | 29:24 | none    | Destination Blend Function , Alpha blending function (DST).<br>0=RESERVED<br>1=D3D_ZERO<br>2=D3D_ONE<br>3=D3D_SRCCOLOR<br>4=D3D_INVSRCOLOR<br>5=D3D_SRCALPHA<br>6=D3D_INVSRCALPHA<br>7=D3D_DESTALPHA<br>8=D3D_INVDESTALPHA<br>9=D3D_DESTCOLOR<br>10=D3D_INVDESTCOLOR<br>11=RESERVED<br>12=RESERVED<br>13=RESERVED<br>14=RESERVED<br>15=RESERVED<br>16=RESERVED<br>17=RESERVED<br>18=RESERVED<br>19=RESERVED<br>20=RESERVED<br>21=RESERVED<br>22=RESERVED<br>23=RESERVED<br>24=RESERVED<br>25=RESERVED<br>26=RESERVED<br>27=RESERVED<br>28=RESERVED<br>29=RESERVED<br>30=RESERVED<br>31=RESERVED<br>32=GL_ZERO<br>33=GL_ONE<br>34=GL_SRC_COLOR<br>35=GL_ONE_MINUS_SRC_COLOR<br>36=GL_DST_COLOR<br>37=GL_ONE_MINUS_DST_COLOR<br>38=GL_SRC_ALPHA<br>39=GL_ONE_MINUS_SRC_ALPHA<br>40=GL_DST_ALPHA<br>41=GL_ONE_MINUS_DST_ALPHA<br>42=RESERVED<br>43=RESERVED<br>44=RESERVED<br>45=RESERVED<br>46=RESERVED<br>47=RESERVED<br>48=RESERVED |

**RB3D\_BLENDCTRL - RW - 32 bits - [MMReg:0x1C20] [MMReg:0x3220]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
|            |      |         | 49=RESERVED<br>50=RESERVED<br>51=RESERVED<br>52=RESERVED<br>53=RESERVED<br>54=RESERVED<br>55=RESERVED<br>56=RESERVED<br>57=RESERVED<br>58=RESERVED<br>59=RESERVED<br>60=RESERVED<br>61=RESERVED<br>62=RESERVED<br>63=RESERVED |

Blend Control , Alpha Blend Control.

**RB3D\_DEPTHOFFSET - RW - 32 bits - [MMReg:0x1C24] [MMReg:0x3224]**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| DEPTHOFFSET | 31:4 | none    | Z Buffer Offset Address , 128-bit aligned address. This is a virtual address which maps to different memory regions according to bits [31:30]. When tiling, the offset must be tile-aligned. (2KB, [10:4] all zeros) |

Z Buffer Offset Address , 128-bit aligned address.

**RB3D\_DEPTHPITCH - RW - 32 bits - [MMReg:0x1C28] [MMReg:0x3228]**

| Field Name  | Bits  | Default | Description  |
|-------------|-------|---------|--|
| DEPTHPITCH  | 12:3  | none    | Z Buffer Pitch , Pitch is specified in multiples of 8-pixels. When tiling, the pitch must be tile-aligned. Since pitch is in 8-pixels, the bits which must be zero varies. |
| DEPTHENDIAN | 19:18 | none    | 0=No swap<br>1=Word swap<br>2=Dword swap<br>3=RESERVED   |

Z Buffer Pitch , Pitch in 8-pixels

**RB3D\_ZSTENCILCNTL - RW - 32 bits - [MMReg:0x1C2C] [MMReg:0x322C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



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**RB3D\_ZSTENCILCNTL - RW - 32 bits - [MMReg:0x1C2C] [MMReg:0x322C]**

| Field Name  | Bits  | Default | Description  |
|-------------|-------|---------|--|
| DEPTHFORMAT | 3:0   | none    | Z pixel format , If RB3D_ZSTENCILCNTL.STENCILENABLE is set, the depth format is changed to the nearest 24-bpp mode.<br>0=16-bit Integer Z<br>1=RESERVED<br>2=24-bit Integer Z<br>3=24-bit Floating Point Z<br>4=32-bit Integer Z<br>5=32-bit Floating Point Z<br>6=RESERVED<br>7=16-bit Floating Point W<br>8=RESERVED<br>9=24-bit Floating Point W<br>10=RESERVED<br>11=32-bit Floating Point W<br>12=RESERVED<br>13=RESERVED<br>14=RESERVED<br>15=RESERVED |
| ZFUNC       | 6:4   | none    | Z Function , Specific Z test to be enabled. A passing Z test will overwrite the existing value with the interpolator Z value. A failing test will leave the existing Z value and color value unmodified. If stenciling is enables, the stencil values may be overwritten even in the case of a failing test.<br>0=Never<br>1=Less<br>2=Less or Equal<br>3=Equal<br>4=Greater or Equal<br>5=Greater Than<br>6=Not Equal<br>7=Always                           |
| STENCILFUNC | 14:12 | none    | Stencil Function , Specific stencil test to be enabled.<br>0=Never<br>1=Less<br>2=Less or Equal<br>3=Equal<br>4=Greater or Equal<br>5=Greater<br>6=Not Equal<br>7=Always   |
| STENCILFAIL | 18:16 | none    | Stencil Fail Op , Stencil value to be written if the stencil test fails. Note that values are clamped after this operation to between 0 and 255.<br>0=Keep: New value = Old value<br>1=Zero: New value = 0<br>2=Replace: New value = STENCILREF<br>3=Increment: New value++<br>4=Decrement: New value--<br>5=Invert new value: New value = !Old value<br>6=RESERVED<br>7=RESERVED  |

**RB3D\_ZSTENCILCNTL - RW - 32 bits - [MMReg:0x1C2C] [MMReg:0x322C]**

| Field Name   | Bits  | Default | Description   |
|--------------|-------|---------|---|
| STENCILZPASS | 22:20 | none    | Stencil Z Pass Op , Stencil value to be written if the stencil test passes and (the Z test passes or the Z enable is 0). Note that values are clamped after this operation to between 0 and 255.<br>0=Keep: New value = Old value<br>1=Zero: New value = 0<br>2=Replace: New value = STENCILREF<br>3=Increment: New value++<br>4=Decrement: New value--<br>5=Invert new value: New value = !Old value<br>6=RESERVED<br>7=RESERVED |
| STENCILZFAIL | 26:24 | none    | Stencil Z Fail Op , Stencil value to be written if the stencil test passes and the Z test fails. Note that values are clamped after this operation to between 0 and 255.<br>0=Keep: New value = Old value<br>1=Zero: New value = 0<br>2=Replace: New value = STENCILREF<br>3=Increment: New value++<br>4=Decrement: New value--<br>5=Invert new value: New value = !Old value<br>6=RESERVED<br>7=RESERVED                         |
| ZWRITEENABLE | 30    | 0x0     | Z Write Enable , Enables writing of the Z planes.<br>0=Disable<br>1=Enable  |

Z/Stencil Control , Controls Z and stencil logic.

**RB3D\_CNTL - RW - 32 bits - [MMReg:0x1C3C] [MMReg:0x323C]**

| Field Name         | Bits | Default | Description   |
|--------------------|------|---------|---|
| ALPHA_BLEND_ENABLE | 0    | none    | 0=Disabled<br>1=Enabled   |
| PLANE_MASK_ENABLE  | 1    | none    | 0=Disabled<br>1=Enabled   |
| DITHER_ENABLE      | 2    | none    | 0=Disabled<br>1=Enabled   |
| ROUND_ENABLE       | 3    | none    | 0=Disabled<br>1=Enabled   |
| SCALE_DITHER       | 4    | none    | 0=X error diffusion<br>1=Enabled  |
| DITHER_INIT        | 5    | none    | 0=Use current error<br>1=Reset at start of line   |
| ROP_ENABLE         | 6    | none    | 3D ROP Enable , Enables raster operations for 3D fragments. Disabling 3D ROP is equivalent to setting RB3D_ROPCNTL.ROP to 0xC (SRCCOPY).<br>0=Disabled<br>1=Enabled |



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**RB3D\_CNTL - RW - 32 bits - [MMReg:0x1C3C] [MMReg:0x323C]**

| Field Name            | Bits  | Default | Description   |
|-----------------------|-------|---------|---|
| STENCIL_ENABLE        | 7     | none    | 0=Disabled<br>1=Enabled   |
| Z_ENABLE              | 8     | none    | 0=Disabled<br>1=Enabled   |
| DEPTHXY_OFFSET_ENABLE | 9     | none    | 0=Disabled<br>1=Enabled   |
| COLORFORMAT           | 13:10 | none    | 3D Destination Datatype , Specifies destination pixel width.<br>0=RESERVED<br>1=RESERVED<br>2=RESERVED<br>3=ARGB1555<br>4=RGB565<br>5=RESERVED<br>6=ARGB8888<br>7=RGB332<br>8=Y8<br>9=RGB8<br>10=RESERVED<br>11=YUV422 packed (VYUY)<br>12=YUV422 packed (YVYU)<br>13=RESERVED<br>14=aYUV444<br>15=ARGB4444 |
| CLRCMP_FLIPE_ENABLE   | 14    | none    | 0=Disabled<br>1=Enabled   |
|                       |       |         |   |

No description available for this register.

**RB3D\_COLOROFFSET - RW - 32 bits - [MMReg:0x1C40] [MMReg:0x3240]**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| COLOROFFSET | 31:4 | none    | 3D Destination Offset Address , 128-bit aligned address. This is a virtual address which maps to different memory regions according to bits [31:30]. When tiling, the offset must be tile-aligned. (2KB, [10:4] all zeros) |

3D Destination Offset Address , 128-bit aligned address.

**RB3D\_COLORPITCH - RW - 32 bits - [MMReg:0x1C48] [MMReg:0x3248]**

| Field Name  | Bits  | Default | Description  |
|-------------|-------|---------|--|
| COLORPITCH  | 12:3  | none    | 3D Destination Pitch , Pitch is specified in multiples of 8-pixels. When tiling, the pitch must be tile-aligned. Since pitch is in 8-pixels, the bits which must be zero varies. |
|             |       |         |  |
| COLORENDIAN | 19:18 | none    | 0=No swap<br>1=Word swap<br>2=Dword swap<br>3=RESERVED   |

3D Destination Pitch , Pitch in 8-pixels

**RB3D\_DEPTHXY\_OFFSET - RW - 32 bits - [MMReg:0x1D60]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**RB3D\_DEPTHXY\_OFFSET - RW - 32 bits - [MMReg:0x1D60]**

| Field Name    | Bits  | Default | Description |
|---------------|-------|---------|-------------|
| DEPTHX_OFFSET | 11:0  | none    |             |
| DEPTHY_OFFSET | 27:16 | none    |             |

No description available for this register.

**RB3D\_CLRCMP\_FLIPE - RW - 32 bits - [MMReg:0x1D64]**

| Field Name   | Bits | Default | Description  |
|--------------|------|---------|--|
| CLRCMP_FLIPE | 31:0 | none    | Color Compare Flip , This shadows E2_SRC_FRGD_CLR and is written via the DP_SRC_FRGD_CLR register location. This is the foreground color. When RB2D_CLRCMP_CNTL.FCN_SRC = 7, a '1' in bit location n means enable flipping on bit n. |

No description available for this register.

**RB3D\_CLRCMP\_CLR - RW - 32 bits - [MMReg:0x1D68]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| CLRCMP_CLR | 31:0 | none    |             |

No description available for this register.

**RB3D\_CLRCMP\_MSK - RW - 32 bits - [MMReg:0x1D6C]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| CLRCMP_MSK | 31:0 | none    | Color Compare Mask , This is ANDed with source and destination before compare. |

No description available for this register.

**RB3D\_STENCILREFMASK - RW - 32 bits - [MMReg:0x1D7C]**

| Field Name       | Bits  | Default | Description   |
|------------------|-------|---------|---|
| STENCILREF       | 7:0   | none    | Stencil Reference , An unsigned 8-bit value that is used as a reference stencil value.  |
| STENCILMASK      | 23:16 | none    | Stencil Mask , This value is ANDed with both reference and the current stencil values prior to the stencil test.  |
| STENCILWRITEMASK | 31:24 | none    | Stencil Write Mask , This value gates writing particular bits of the stencil values. Any particular bit must be '1' to allow writing of that stencil plane. |

No description available for this register.

**RB3D\_ROPCNTL - RW - 32 bits - [MMReg:0x1D80]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| ROP        | 11:8 | none    | 3D ROP , ROP2 code for 3D fragments. This value is replicated into 2 nibbles to form the equivalent ROP3 code to control the ROP3 logic. |

3D ROP Control , Control for 3D ROP2 operations

**RB3D\_PLANEMASK - RW - 32 bits - [MMReg:0x1D84]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| PLANEMASK  | 31:0 | none    | 3D Plane Mask , Bit mask for 3D destination writes. For vest performance, the mask should be byte-aligned. |

3D Plane Mask , Bit mask for 3D destination writes.

**RB3D\_ZCACHE\_CTLSTAT - RW - 32 bits - [MMReg:0x3254]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| ZC_FLUSH   | 0    | none    | Z Cache Flush , Setting this bit flushes dirty data from the Z cache. Unless the ZC_FREE bit is also set, the tags in the cache remain valid. A purge is achieved by setting both ZC_FLUSH and ZC_FREE. This is a sticky bit that clears itself at the end of the flush operation.<br>0=No effect<br>1=Flush dirty Z data |
| ZC_FREE    | 2    | none    | Z Cache Free , Setting this bit invalidates the Z cache tags. Unless the ZC_FLUSH bit is also set, the cache lines are not written to memory. A purge is achieved by setting both ZC_FLUSH and ZC_FREE. This is a sticky bit that clears itself at the end of the flush operation.<br>0=No effect<br>1=Free Z tags        |
| ZC_BUSY    | 31   | none    | Z Cache Busy ,<br>0=Idle<br>1=Busy  |

Z Cache Control and Status , Contains cache controls and status.

**RB3D\_DSTCACHE\_CTLSTAT - RW - 32 bits - [MMReg:0x325C]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| DC_FLUSH   | 1:0  | none    | Dst Cache Flush , Setting this bit flushes dirty data from the 2D and/or 3D Dst Cache. Unless the DC_FREE bits are also set, the tags in the cache remain valid. A purge is achieved by setting both DC_FLUSH and DC_FREE. These are sticky bits that clear themselves at the end of the flush operation.<br>0=No effect<br>1=Flush dirty 2D Dst Data<br>2=Flush dirty 2D Dst Data<br>3=Flush all dirty Dst Data |
| DC_FREE    | 3:2  | none    | Dst Cache Free , Setting this bit invalidates the 2D and/or 3D Dst Cache tags. Unless the DC_FLUSH bit is also set, the cache lines are not written to memory. A purge is achieved by setting both DC_FLUSH and DC_FREE. These are sticky bits that clear themselves at the end of the flush operation.<br>0=No effect<br>1=Free 2D Dst tags<br>2=Free 3D Dst tags<br>3=Free all Dst tags                        |
| DC_BUSY    | 31   | none    | Dst Cache Busy ,<br>0=Idle<br>1=Busy   |

Dst Cache Control and Status , Contains cache controls and status.

**44. Setup Engine**

| <b>SE_CNTL - RW - 32 bits - [MMReg:0x1C4C] [MMReg:0x2088]</b> |             |                |   |
|---|-------------|----------------|---|
| <b>Field Name</b>   | <b>Bits</b> | <b>Default</b> | <b>Description</b>  |
| FFACE_CULL_DIR  | 0           | none           | Direction of front-facing triangles. Used to control culling.<br>0 = Front facing triangles are clockwise<br>1 = Front facing triangles are counter-clockwise   |
| BFACE_CULL_FCN  | 2:1         | none           | Back-facing Cull Function.<br>0 = Don't Draw back-facing triangles<br>1 = Reserved<br>2 = Reserved<br>3 = Draw back-facing triangles.   |
| FFACE_CULL_FCN  | 4:3         | none           | Front-facing Cull Function.<br>0 = Don't Draw front-facing triangles.<br>1 = Reserved<br>2 = Reserved<br>3 = Draw front-facing triangles.   |
| BADVTX_CULL_DISABLE   | 5           | 0x0            | Disable culling of primitives with 'bad' coordinates or 'bad' parameters.<br>0 = Raster primitives that use a vertex which contains an out-of-range X or Y coordinate are not drawn. Also, raster primitives that use a vertex which contains at least one parameter that is NaN (Not A Number) are not drawn.<br>1 = These types of primitives are drawn.<br>Default = 0 |
| FLAT_SHADE_VTX  | 7:6         | none           | Indicates which of the three vertices (by arrival order, before sorting) should be used for color components that have their SHADE_FCN set to 'Flat Shade' mode.<br>0 = Use Vertex 0<br>1 = Use Vertex 1<br>2 = Use Vertex 2<br>3 = Last Vertex   |
| DIFFUSE_SHADE_FCN   | 9:8         | none           | Controls shading for diffuse RGB components.<br>0 = Solid: use corresponding '_SOLID' register for the color.<br>1 = Flat: use corresponding color from vertex specified by FLAT_SHADE_VTX.<br>2 = Gouraud<br>3 = Reserved.   |
| ALPHA_SHADE_FCN   | 11:10       | none           | Controls shading for alpha component.<br>Same encoding as DIFFUSE_SHADE_FCN.  |
| SPECULAR_SHADE_FCN  | 13:12       | none           | Controls shading for specular RGB components.<br>Same encoding as DIFFUSE_SHADE_FCN.  |
| FOG_SHADE_FCN   | 15:14       | none           | Controls shading for fog component.<br>Same encoding as DIFFUSE_SHADE_FCN.  |
| ZBIAS_EN_POINT  | 16          | none           | Enables Z Bias for the '3-Vertex Point List' primitive.   |
| ZBIAS_EN_LINE   | 17          | none           | Enables Z Bias for the '3-Vertex Line List' primitive.  |
| ZBIAS_EN_TRI  | 18          | none           | Enables Z Bias for all types of triangle primitives.  |

**SE\_CNTL - RW - 32 bits - [MMReg:0x1C4C] [MMReg:0x2088]**

| Field Name      | Bits  | Default | Description  |
|-----------------|-------|---------|--|
| WIDELINE_EN     | 20    | none    | Enables lines wider than 1.0 pixels.<br>0 = All lines are drawn as one pixel wide.<br>1 = All lines are drawn with the width specified in the SE_LINE_WIDTH register.  |
| VPORT_XY_XFEN   | 24    | none    | Viewport Transform Enable for X,Y coordinates.   |
| VPORT_Z_XFEN    | 25    | none    | Viewport Transform Enable for Z coordinates.   |
| VTX_PIXCENTER   | 27    | none    | Specifies where the pixel center of the incoming vertex is.<br>0 = Pixel center at 0.0 (D3D)<br>1 = Pixel center at 0.5 (OGL)<br>The drawing engine itself has pixel centers at 0.5, so if this bit is '0', the Setup Engine will add 0.5 to the X,Y coordinates to move the incoming vertex onto our internal grid. |
| ROUND_MODE      | 29:28 | none    | Controls conversion of X,Y coordinates from IEEE -to-fixed-point.<br>0 = Truncate (OGL)<br>1 = Round<br>2 = Round to Even. (D3D)<br>3 = Round to Odd.  |
| ROUND_PRECISION | 31:30 | none    | Controls conversion of X,Y coordinates from IEEE -to-fixed-point.<br>0 = Round to 1/16th pixel grid<br>1 = Round to 1/8th pixel grid<br>2 = Round to 1/4 pixel grid<br>3 = Round to 1/2 pixel grid.  |

Setup Engine Control

**SE\_COORD\_FMT - RW - 32 bits - [MMReg:0x1C50] [MMReg:0x208C]**

| Field Name            | Bits | Default | Description  |
|-----------------------|------|---------|--|
| VTX_XY_FMT            | 0    | none    | 1 = Indicates that the incoming X,Y have already been multiplied by 1/W0.<br>0 = The Setup Engine will multiply the X,Y coordinates by 1/W0. |
| VTX_Z_FMT             | 1    | none    | 1 = Indicates that the incoming Z has already been multiplied by 1/W0.<br>0 = The Setup Engine will multiply the Z coordinate by 1/W0.       |
| VTX_ST0_NONPARAMETRIC | 8    | none    | Indicates if the first set of S,T coordinates are non-parametric, that is, they have already been multiplied by the texture size.            |
| VTX_ST1_NONPARAMETRIC | 9    | none    | Indicates if the second set of S,T coordinates are non-parametric, that is, they have already been multiplied by the texture size.           |
| VTX_ST2_NONPARAMETRIC | 10   | none    | Indicates if the third set of S,T coordinates are non-parametric, that is, they have already been multiplied by the texture size.            |
| VTX_ST3_NONPARAMETRIC | 11   | none    | Reserved for expansion   |
| VTX_W0_NORMALIZE      | 12   | none    | Indicates that the Setup Engine must multiply 1/W0 by VTX_W0_RANGE.  |



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**SE\_COORD\_FMT - RW - 32 bits - [MMReg:0x1C50] [MMReg:0x208C]**

| Field Name     | Bits | Default | Description  |
|----------------|------|---------|--|
| VTX_W0_FMT     | 16   | none    | Indicates that the incoming W0 is not 1/W0. If ON, the Setup Engine will perform the reciprocal to get 1/W0.   |
| VTX_ST0_FMT    | 17   | none    | Indicates if the first set of S,T,Q coordinates have already been multiplied by 1/W0.  |
| VTX_ST1_FMT    | 19   | none    | Indicates if the second set of S,T,Q coordinates have already been multiplied by 1/W0.   |
| VTX_ST2_FMT    | 21   | none    | Indicates if the third set of S,T,Q coordinates have already been multiplied by 1/W0.  |
| VTX_ST3_FMT    | 23   | none    | Reserved for expansion   |
| TEX1_W_ROUTING | 26   | none    | Indicates whether W for coordinate set 1 comes from vertex parameter W0 or Q1. This bit is only present for Rage128-compatibility; it is similar in function to the SEC_SRC_SEL_W bit. For non-Rage128 drivers, this bit should be set to '1'.<br>0 = use W0<br>1 = use Q1 |

Setup Engine Coordinate Format

**SE\_VPORT\_XSCALE - RW - 32 bits - [MMReg:0x1D98] [MMReg:0x2098]**

| Field Name   | Bits | Default | Description   |
|--------------|------|---------|---|
| VPORT_XSCALE | 31:0 | none    | Viewport Scale Factor for X coordinates. An IEEE float. |

Setup Engine Viewport X Scale Factor

**SE\_VPORT\_XOFFSET - RW - 32 bits - [MMReg:0x1D9C] [MMReg:0x209C]**

| Field Name    | Bits | Default | Description                                       |
|---------------|------|---------|---|
| VPORT_XOFFSET | 31:0 | none    | Viewport Offset for X coordinates. An IEEE float. |

Setup Engine Viewport X Offset

**SE\_VPORT\_YSCALE - RW - 32 bits - [MMReg:0x1DA0] [MMReg:0x20A0]**

| Field Name   | Bits | Default | Description   |
|--------------|------|---------|---|
| VPORT_YSCALE | 31:0 | none    | Viewport Scale Factor for Y coordinates. An IEEE float. |

Setup Engine Viewport Y Scale Factor

**SE\_VPORT\_YOFFSET - RW - 32 bits - [MMReg:0x1DA4] [MMReg:0x20A4]**

| Field Name    | Bits | Default | Description                                       |
|---------------|------|---------|---|
| VPORT_YOFFSET | 31:0 | none    | Viewport Offset for Y coordinates. An IEEE float. |

Setup Engine Viewport Y Offset

**SE\_VPORT\_ZSCALE - RW - 32 bits - [MMReg:0x1DA8] [MMReg:0x20A8]**

| Field Name   | Bits | Default | Description   |
|--------------|------|---------|---|
| VPORT_ZSCALE | 31:0 | none    | Viewport Scale Factor for Z coordinates. An IEEE float. |

Setup Engine Viewport Z Scale Factor





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**SE\_TCL\_VECTOR\_DATA\_REG - RW - 32 bits - [MMReg:0x2204]**

| Field Name    | Bits | Default | Description                            |
|---------------|------|---------|--|
| DATA_REGISTER | 31:0 | none    | 32-bit data to write to Vector Memory. |

No description available for this register.

**SE\_TCL\_SCALAR\_INDY\_REG - RW - 32 bits - [MMReg:0x2208]**

| Field Name   | Bits  | Default | Description   |
|--------------|-------|---------|---|
| DWORD_OFFSET | 6:0   | none    | Dword offset to begin writing.                          |
| DWORD_STRIDE | 22:16 | none    | Dword stride to increment each new data register write. |

No description available for this register.

**SE\_TCL\_SCALAR\_DATA\_REG - RW - 32 bits - [MMReg:0x220C]**

| Field Name    | Bits | Default | Description                            |
|---------------|------|---------|--|
| DATA_REGISTER | 31:0 | none    | 32-bit data to write to Vector Memory. |

No description available for this register.

45. TCL**SE\_TCL\_MATERIAL\_EMISSIVE\_RED - RW - 32 bits - [MMReg:0x2210]**

| Field Name            | Bits | Default | Description                  |
|-----------------------|------|---------|------------------------------|
| MATERIAL_EMISSIVE_RED | 31:0 | none    | Material Emissive Color Red. |

No description available for this register.

**SE\_TCL\_MATERIAL\_EMISSIVE\_GREEN - RW - 32 bits - [MMReg:0x2214]**

| Field Name              | Bits | Default | Description                    |
|-------------------------|------|---------|--------------------------------|
| MATERIAL_EMISSIVE_GREEN | 31:0 | none    | Material Emissive Color Green. |

No description available for this register.

**SE\_TCL\_MATERIAL\_EMISSIVE\_BLUE - RW - 32 bits - [MMReg:0x2218]**

| Field Name             | Bits | Default | Description                   |
|------------------------|------|---------|-------------------------------|
| MATERIAL_EMISSIVE_BLUE | 31:0 | none    | Material Emissive Color Blue. |

No description available for this register.

**SE\_TCL\_MATERIAL\_EMISSIVE\_ALPHA - RW - 32 bits - [MMReg:0x221C]**

| Field Name              | Bits | Default | Description                    |
|-------------------------|------|---------|--------------------------------|
| MATERIAL_EMISSIVE_ALPHA | 31:0 | none    | Material Emissive Color Alpha. |

No description available for this register.

**SE\_TCL\_MATERIAL\_AMBIENT\_RED - RW - 32 bits - [MMReg:0x2220]**

| Field Name           | Bits | Default | Description                 |
|----------------------|------|---------|-----------------------------|
| MATERIAL_AMBIENT_RED | 31:0 | none    | Material Ambient Color Red. |

No description available for this register.

**SE\_TCL\_MATERIAL\_AMBIENT\_GREEN - RW - 32 bits - [MMReg:0x2224]**

| Field Name             | Bits | Default | Description                   |
|------------------------|------|---------|-------------------------------|
| MATERIAL_AMBIENT_GREEN | 31:0 | none    | Material Ambient Color Green. |

No description available for this register.

**SE\_TCL\_MATERIAL\_AMBIENT\_BLUE - RW - 32 bits - [MMReg:0x2228]**

| Field Name            | Bits | Default | Description                  |
|-----------------------|------|---------|------------------------------|
| MATERIAL_AMBIENT_BLUE | 31:0 | none    | Material Ambient Color Blue. |

No description available for this register.

**SE\_TCL\_MATERIAL\_AMBIENT\_ALPHA - RW - 32 bits - [MMReg:0x222C]**

| Field Name             | Bits | Default | Description                   |
|------------------------|------|---------|-------------------------------|
| MATERIAL_AMBIENT_ALPHA | 31:0 | none    | Material Ambient Color Alpha. |

No description available for this register.

**SE\_TCL\_MATERIAL\_DIFFUSE\_RED - RW - 32 bits - [MMReg:0x2230]**

| Field Name           | Bits | Default | Description                 |
|----------------------|------|---------|-----------------------------|
| MATERIAL_DIFFUSE_RED | 31:0 | none    | Material Diffuse Color Red. |

No description available for this register.

**SE\_TCL\_MATERIAL\_DIFFUSE\_GREEN - RW - 32 bits - [MMReg:0x2234]**

| Field Name             | Bits | Default | Description                   |
|------------------------|------|---------|-------------------------------|
| MATERIAL_DIFFUSE_GREEN | 31:0 | none    | Material Diffuse Color Green. |

No description available for this register.

**SE\_TCL\_MATERIAL\_DIFFUSE\_BLUE - RW - 32 bits - [MMReg:0x2238]**

| Field Name            | Bits | Default | Description                  |
|-----------------------|------|---------|------------------------------|
| MATERIAL_DIFFUSE_BLUE | 31:0 | none    | Material Diffuse Color Blue. |

No description available for this register.

**SE\_TCL\_MATERIAL\_DIFFUSE\_ALPHA - RW - 32 bits - [MMReg:0x223C]**

| Field Name             | Bits | Default | Description                   |
|------------------------|------|---------|-------------------------------|
| MATERIAL_DIFFUSE_ALPHA | 31:0 | none    | Material Diffuse Color Alpha. |

No description available for this register.

**SE\_TCL\_MATERIAL\_SPECULAR\_RED - RW - 32 bits - [MMReg:0x2240]**

| Field Name            | Bits | Default | Description                  |
|-----------------------|------|---------|------------------------------|
| MATERIAL_SPECULAR_RED | 31:0 | none    | Material Specular Color Red. |

No description available for this register.

**SE\_TCL\_MATERIAL\_SPECULAR\_GREEN - RW - 32 bits - [MMReg:0x2244]**

| Field Name              | Bits | Default | Description                    |
|-------------------------|------|---------|--------------------------------|
| MATERIAL_SPECULAR_GREEN | 31:0 | none    | Material Specular Color Green. |

No description available for this register.

**SE\_TCL\_MATERIAL\_SPECULAR\_BLUE - RW - 32 bits - [MMReg:0x2248]**

| Field Name             | Bits | Default | Description                   |
|------------------------|------|---------|-------------------------------|
| MATERIAL_SPECULAR_BLUE | 31:0 | none    | Material Specular Color Blue. |

No description available for this register.

**SE\_TCL\_MATERIAL\_SPECULAR\_ALPHA - RW - 32 bits - [MMReg:0x224C]**

| Field Name              | Bits | Default | Description                    |
|-------------------------|------|---------|--------------------------------|
| MATERIAL_SPECULAR_ALPHA | 31:0 | none    | Material Specular Color Alpha. |

No description available for this register.

**SE\_TCL\_SHININESS - RW - 32 bits - [MMReg:0x2250]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**SE\_TCL\_SHININESS - RW - 32 bits - [MMReg:0x2250]**

| Field Name       | Bits | Default | Description   |
|------------------|------|---------|---|
| SE_TCL_SHININESS | 31:0 | none    | Specular Shininess<br>NOTE: This register maps to the same memory as the indexed register pair (SE_TCL_SCALAR_INDXX_REG and SE_TCL_SCALAR_DATA_REG) when the index register equals 60 |

No description available for this register.

**SE\_TCL\_OUTPUT\_VTX\_FMT - RW - 32 bits - [MMReg:0x2254]**

| Field Name          | Bits | Default | Description   |
|---------------------|------|---------|---|
| VTX_W0_PRESENT      | 0    | 0x0     | Primary vertex W value is present (1 float).  |
| VTX_FPCOLOR_PRESENT | 1    | 0x0     |   |
| VTX_FPALPHA_PRESENT | 2    | 0x0     | Floating-point Alpha is Present (1 float).  |
| VTX_PKCOLOR_PRESENT | 3    | 0x0     |   |
| VTX_FPSPEC_PRESENT  | 4    | 0x0     | Floating-point Specular Color is Present (3 floats).  |
| VTX_FPFOG_PRESENT   | 5    | 0x0     | Floating-point Fog Color is Present (1 float).  |
| VTX_PKSPEC_PRESENT  | 6    | 0x0     | Packed (8,8,8) RGBF Specular is Present.<br>This is mutually exclusive with FPSPEC_PRESENT and FPF0G_PRESENT. |
| VTX_ST0_PRESENT     | 7    | 0x0     | Texture 0 S, T values are present (2 floats).   |
| VTX_ST1_PRESENT     | 8    | 0x0     | Texture 1 S, T values are present (2 floats).   |
| VTX_Q1_PRESENT      | 9    | 0x0     | Texture 1 Q value is present (1 float).   |
| VTX_ST2_PRESENT     | 10   | 0x0     | Texture 2 S, T values are present (2 floats).   |
| VTX_Q2_PRESENT      | 11   | 0x0     | Texture 2 Q value is present (1 float).   |
| VTX_ST3_PRESENT     | 12   | 0x0     | Texture 3 S, T values are present (2 floats).   |
| VTX_Q3_PRESENT      | 13   | 0x0     | Texture 3 Q value is present (1 float).   |
| VTX_Q0_PRESENT      | 14   | 0x0     | Texture 0 Q value is present (1 float).   |
| VTX_Z_PRESENT       | 31   | 0x0     |   |

No description available for this register.

**SE\_TCL\_OUTPUT\_VTX\_SEL - RW - 32 bits - [MMReg:0x2258]**

| Field Name              | Bits | Default | Description   |
|-------------------------|------|---------|---|
| VTX_XYZW_SELECT         | 0    | 0x0     | Select the computed XYZW values (0 means output the input data).                      |
| VTX_PKDIFFUSE_SELECT    | 1    | 0x0     | Select the computed diffuse color/alpha value (0 means output the input data).        |
| VTX_PKSPEC_SELECT       | 2    | 0x0     | Select the computed specular color/fog value (0 means output the input data).         |
| FORCE_NAN_IF_CCOLOR_NAN | 3    | 0x0     | If set, instructs TCL to send NAN on output if NAN detected prior to Flt->Fix.        |
| FORCE_INORDER_PROC      | 4    | 0x0     | If set, forces fixed order vertex output for lighting (@ slight performance penalty). |



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**SE\_TCL\_OUTPUT\_VTX\_SEL - RW - 32 bits - [MMReg:0x2258]**

| Field Name      | Bits  | Default | Description   |
|-----------------|-------|---------|---|
| RSVD_1BIT_NUM0  | 5     | 0x0     | Reserved 1-Bit Field.   |
| RSVD_3BIT_NUM0  | 8:6   | 0x0     | Reserved 3-Bit Field.   |
| RSVD_3BIT_NUM1  | 11:9  | 0x0     | Reserved 3-Bit Field.   |
| RSVD_4BIT_NUM0  | 15:12 | 0x0     | Reserved 4-Bit Field.   |
| VTX_TEX0_SELECT | 19:16 | 0x0     | Select the computed S, T, Q values.<br>0 => Input Texture 0<br>1 => Input Texture 1<br>2 => Input Texture 2<br>3 => Input Texture 3<br>4 => Input Texture 4 (Not currently supported.)<br>5 => Input Texture 5 (Not currently supported.)<br>6 => Input Texture 6 (Not currently supported.)<br>7 => Input Texture 7 (Not currently supported.)<br>8 => Computed Texture 0 (ONLY VALID FOR VTX_TEX0_SELECT.)<br>9 => Computed Texture 1 (ONLY VALID FOR VTX_TEX1_SELECT.)<br>10 => Computed Texture 2 (ONLY VALID FOR VTX_TEX2_SELECT.)<br>11 => Computed Texture 3 (ONLY VALID FOR VTX_TEX3_SELECT.)<br>12 => Computed Texture 4 (Not currently supported.)<br>13 => Computed Texture 5 (Not currently supported.) |
| VTX_TEX1_SELECT | 23:20 | 0x0     | Select the computed S, T, Q values.<br>0 => Input Texture 0<br>1 => Input Texture 1<br>2 => Input Texture 2<br>3 => Input Texture 3<br>4 => Input Texture 4 (Not currently supported.)<br>5 => Input Texture 5 (Not currently supported.)<br>6 => Input Texture 6 (Not currently supported.)<br>7 => Input Texture 7 (Not currently supported.)<br>8 => Computed Texture 0 (ONLY VALID FOR VTX_TEX0_SELECT.)<br>9 => Computed Texture 1 (ONLY VALID FOR VTX_TEX1_SELECT.)<br>10 => Computed Texture 2 (ONLY VALID FOR VTX_TEX2_SELECT.)<br>11 => Computed Texture 3 (ONLY VALID FOR VTX_TEX3_SELECT.)<br>12 => Computed Texture 4 (Not currently supported.)<br>13 => Computed Texture 5 (Not currently supported.) |

**SE\_TCL\_OUTPUT\_VTX\_SEL - RW - 32 bits - [MMReg:0x2258]**

| Field Name      | Bits  | Default | Description   |
|-----------------|-------|---------|---|
| VTX_TEX2_SELECT | 27:24 | 0x0     | Select the computed S, T, Q values.<br>0 => Input Texture 0<br>1 => Input Texture 1<br>2 => Input Texture 2<br>3 => Input Texture 3<br>4 => Input Texture 4 (Not currently supported.)<br>5 => Input Texture 5 (Not currently supported.)<br>6 => Input Texture 6 (Not currently supported.)<br>7 => Input Texture 7 (Not currently supported.)<br>8 => Computed Texture 0 (ONLY VALID FOR VTX_TEX0_SELECT.)<br>9 => Computed Texture 1 (ONLY VALID FOR VTX_TEX1_SELECT.)<br>10 => Computed Texture 2 (ONLY VALID FOR VTX_TEX2_SELECT.)<br>11 => Computed Texture 3 (ONLY VALID FOR VTX_TEX3_SELECT.)<br>12 => Computed Texture 4 (Not currently supported.)<br>13 => Computed Texture 5 (Not currently supported.) |
| VTX_TEX3_SELECT | 31:28 | 0x0     | Select the computed S, T, Q values.<br>0 => Input Texture 0<br>1 => Input Texture 1<br>2 => Input Texture 2<br>3 => Input Texture 3<br>4 => Input Texture 4 (Not currently supported.)<br>5 => Input Texture 5 (Not currently supported.)<br>6 => Input Texture 6 (Not currently supported.)<br>7 => Input Texture 7 (Not currently supported.)<br>8 => Computed Texture 0 (ONLY VALID FOR VTX_TEX0_SELECT.)<br>9 => Computed Texture 1 (ONLY VALID FOR VTX_TEX1_SELECT.)<br>10 => Computed Texture 2 (ONLY VALID FOR VTX_TEX2_SELECT.)<br>11 => Computed Texture 3 (ONLY VALID FOR VTX_TEX3_SELECT.)<br>12 => Computed Texture 4 (Not currently supported.)<br>13 => Computed Texture 5 (Not currently supported.) |

No description available for this register.

**SE\_TCL\_MATRIX\_SELECT\_0 - RW - 32 bits - [MMReg:0x225C]**

| Field Name             | Bits  | Default | Description  |
|------------------------|-------|---------|--|
| MODELVIEW_MTX_0_SEL    | 3:0   | 0x0     | Matrix Select for ModelView Matrix 0.                  |
| MODELVIEW_MTX_1_SEL    | 7:4   | 0x0     | Matrix Select for ModelView Matrix 1.                  |
| MODELVIEW_MTX_2_SEL    | 11:8  | 0x0     | Matrix Select for ModelView Matrix 2.                  |
| MODELVIEW_MTX_3_SEL    | 15:12 | 0x0     | Matrix Select for ModelView Matrix 3.                  |
| IT_MODELVIEW_MTX_0_SEL | 19:16 | 0x0     | Matrix Select for Inverse Tranpose ModelView Matrix 0. |
| IT_MODELVIEW_MTX_1_SEL | 23:20 | 0x0     | Matrix Select for Inverse Tranpose ModelView Matrix 1. |
| IT_MODELVIEW_MTX_2_SEL | 27:24 | 0x0     | Matrix Select for Inverse Tranpose ModelView Matrix 2. |
| IT_MODELVIEW_MTX_3_SEL | 31:28 | 0x0     | Matrix Select for Inverse Tranpose ModelView Matrix 3. |

No description available for this register.

**SE\_TCL\_MATRIX\_SELECT\_1 - RW - 32 bits - [MMReg:0x2260]**

| Field Name           | Bits  | Default | Description                                   |
|----------------------|-------|---------|---|
| MODEL2CLIP_MTX_0_SEL | 3:0   | 0x0     | Matrix Select for Model To Clip Matrix 0.     |
| MODEL2CLIP_MTX_1_SEL | 7:4   | 0x0     | Matrix Select for Model To Clip Matrix 1.     |
| MODEL2CLIP_MTX_2_SEL | 11:8  | 0x0     | Matrix Select for Model To Clip Matrix 2.     |
| MODEL2CLIP_MTX_3_SEL | 15:12 | 0x0     | Matrix Select for Model To Clip Matrix 3.     |
| TEX_XFORM_MTX_0_SEL  | 19:16 | 0x0     | Matrix Select for Texture Transform Matrix 0. |
| TEX_XFORM_MTX_1_SEL  | 23:20 | 0x0     | Matrix Select for Texture Transform Matrix 1. |
| TEX_XFORM_MTX_2_SEL  | 27:24 | 0x0     | Matrix Select for Texture Transform Matrix 2. |
| TEX_XFORM_MTX_3_SEL  | 31:28 | 0x0     | Matrix Select for Texture Transform Matrix 3. |

No description available for this register.

**SE\_TCL\_UCP\_VERT\_BLEND\_CTL - RW - 32 bits - [MMReg:0x2264]**

| Field Name               | Bits  | Default | Description  |
|--------------------------|-------|---------|--|
| UCP_IN_CLIP_SPACE        | 0     | 0x0     | Perform User Clip Plane Processing in Clip Coordinates.  |
| UCP_IN_MODEL_SPACE       | 1     | 0x0     | Perform User Clip Plane Processing in Model (Object) Coordinates.                                      |
| UCP_ENA_0                | 2     | 0x0     | Enable User Clip Plane 0.  |
| UCP_ENA_1                | 3     | 0x0     | Enable User Clip Plane 1.  |
| UCP_ENA_2                | 4     | 0x0     | Enable User Clip Plane 2.  |
| UCP_ENA_3                | 5     | 0x0     | Enable User Clip Plane 3.  |
| UCP_ENA_4                | 6     | 0x0     | Enable User Clip Plane 4.  |
| UCP_ENA_5                | 7     | 0x0     | Enable User Clip Plane 5.  |
| FOG_MODE                 | 9:8   | 0x0     | Vertex Fog Mode (0=DISABLE, 1=EXP, 2=EXPSQ, 3=LINEAR)  |
| RNG_BASED_FOG            | 10    | 0x0     | If set, use range (length of eye vector) for fog computations, otherwise use depth (eye z value).      |
| TWO_SIDED_LIGHTING_ENA   | 11    | 0x0     | If set, performs 2-sided lighting determination. Culling must be enabled to activate 2-sided lighting. |
| BLEND_OP_CNT             | 14:12 | 0x0     | Number of Blend Ops to Perform (Only used if USE_ST_BLEND_OP_CNT set).                                 |
| USE_ST_BLEND_OP_CNT      | 15    | 0x0     |  |
| POSITION_BLEND_OPERATION | 16    | 0x0     | Vertex Position Operation Selection (0=Disable, 1=Blend).  |
| NORMAL_BLEND_OPERATION   | 17    | 0x0     | Normal Blending Operation Selection (0=Disable, 1=Blend).  |
| VERTEX_BLEND_SOURCE_0    | 18    | 0x0     | Input Vertex Select for Blending Operation (0=Primary Vtx, 1=Secondary Vtx).                           |
| VERTEX_BLEND_SOURCE_1    | 19    | 0x0     | Input Vertex Select for Blending Operation (0=Primary Vtx, 1=Secondary Vtx).                           |

**SE\_TCL\_UCP\_VERT\_BLEND\_CTL - RW - 32 bits - [MMReg:0x2264]**

| Field Name              | Bits  | Default | Description   |
|-------------------------|-------|---------|---|
| VERTEX_BLEND_SOURCE_2   | 20    | 0x0     | Input Vertex Select for Blending Operation (0=Primary Vtx, 1=Secondary Vtx).  |
| VERTEX_BLEND_SOURCE_3   | 21    | 0x0     | Input Vertex Select for Blending Operation (0=Primary Vtx, 1=Secondary Vtx).  |
| BLEND_WEIGHT_MINUS_ONE  | 22    | 0x0     | 0=#Blend Weights in Input Vtx=Number of Vertex/Matrix in Computation<br>1=#Blend Weights in Input Vtx=Number of Vertex/Matrix in Computation - 1 (where the remaining Blend Weight is (1-Sum of Provided Blend Weights))  |
| VERT_BLEND_USE_PROJ_MTX | 23    | 0x0     | Performance Optimization. If Set, when needing eye_coord verts/normals, the blend eye coord vert will be rotated through the projection matrix instead of blended through the model2clip matrix. This could cause cracks. |
| VERT_BLEND_2_OPTIMIZE   | 24    | 0x0     | Performance Optimization. If Set, when only using 2 blend weights, an optimized path is used which could cause cracks if there are .2 blend weights with some being 0.0 This could cause cracks.                          |
| CULL_EQ_0_ENA           | 25    | 0x0     | Cull If Cross-Product is Equal to 0.0 Only used if CULL_FF_ENA or CULL_BF_ENA is set.   |
| CULL_METHOD             | 27:26 | 0x0     | 0: Cull Always 1: Cull Only Front of Near Plane 2: Cull O   |
| CULLING_FF_DIR          | 28    | 0x0     | Defines Front Face Dir 0=CW, 1=CCW  |
| CULL_FF_ENA             | 29    | 0x0     | Cull Front Facing Primitives (TRI,2VTX LINE, 3VTX POINT)  |
| CULL_BF_ENA             | 30    | 0x0     | Cull Back Facing Primitives (TRI,2VTX LINE, 3VTX POINT)   |
| FORCE_W_TO_ONE          | 31    | 0x0     | When set, the incoming W0 (and W1 for vert blending) are over-ridden with 1.0   |

No description available for this register.

**SE\_TCL\_TEXTURE\_PROC\_CTL - RW - 32 bits - [MMReg:0x2268]**

| Field Name        | Bits | Default | Description   |
|-------------------|------|---------|---|
| TEX_CS_PROC_ENA_0 | 0    | 0x0     | Set if either coordinate generation or texture transform is required for texture 0. |
| TEX_CS_PROC_ENA_1 | 1    | 0x0     | Set if either coordinate generation or texture transform is required for texture 1. |
| TEX_CS_PROC_ENA_2 | 2    | 0x0     | Set if either coordinate generation or texture transform is required for texture 2. |
| TEX_CS_PROC_ENA_3 | 3    | 0x0     | Set if either coordinate generation or texture transform is required for texture 3. |
| TEX_XFORM_ENA_0   | 4    | 0x0     | Enable Texture Transform Matrix for texture 0.                                      |
| TEX_XFORM_ENA_1   | 5    | 0x0     | Enable Texture Transform Matrix for texture 1.                                      |
| TEX_XFORM_ENA_2   | 6    | 0x0     | Enable Texture Transform Matrix for texture 2.                                      |
| TEX_XFORM_ENA_3   | 7    | 0x0     | Enable Texture Transform Matrix for texture 3.                                      |



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**SE\_TCL\_TEXTURE\_PROC\_CTL - RW - 32 bits - [MMReg:0x2268]**

| Field Name        | Bits  | Default | Description   |
|-------------------|-------|---------|---|
| RSVD_2BIT_NUM3    | 9:8   | 0x0     | Reserved 2-Bit Field  |
| RSVD_2BIT_NUM4    | 11:10 | 0x0     | Reserved 2-Bit Field  |
| RSVD_2BIT_NUM5    | 13:12 | 0x0     | Reserved 2-Bit Field  |
| RSVD_2BIT_NUM6    | 15:14 | 0x0     | Reserved 2-Bit Field  |
| TEX_CS_PROC_SRC_0 | 19:16 | 0x0     | Input Texture (or Texture Coordinate Generation) Selection<br>0 => Input Texture Coordinate Set 0<br>1 => Input Texture Coordinate Set 1<br>2 => Input Texture Coordinate 2<br>3 => Input Texture Coordinate Set 3<br>4 => Vertex Position in Object Coordinates<br>5 => Vertex Position in Eye Coordinates<br>6 => Vertex Normal in Eye Coordinates (This vector is the same as what is used by Lighting.) (Normalized if renorm or rescale is enabled.)<br>7 => Reflection Vector in Eye Coordinates<br>8 => Vertex Position in Eye Coordinates Normalized (This vector is used for Local Viewer specular computations. Probably will never be used by TCG, but here it is anyway.) |
| TEX_CS_PROC_SRC_1 | 23:20 | 0x0     | Input Texture (or Texture Coordinate Generation) Selection<br>0 => Input Texture Coordinate Set 0<br>1 => Input Texture Coordinate Set 1<br>2 => Input Texture Coordinate 2<br>3 => Input Texture Coordinate Set 3<br>4 => Vertex Position in Object Coordinates<br>5 => Vertex Position in Eye Coordinates<br>6 => Vertex Normal in Eye Coordinates (This vector is the same as what is used by Lighting.) (Normalized if renorm or rescale is enabled.)<br>7 => Reflection Vector in Eye Coordinates<br>8 => Vertex Position in Eye Coordinates Normalized (This vector is used for Local Viewer specular computations. Probably will never be used by TCG, but here it is anyway.) |
| TEX_CS_PROC_SRC_2 | 27:24 | 0x0     | Input Texture (or Texture Coordinate Generation) Selection<br>0 => Input Texture Coordinate Set 0<br>1 => Input Texture Coordinate Set 1<br>2 => Input Texture Coordinate 2<br>3 => Input Texture Coordinate Set 3<br>4 => Vertex Position in Object Coordinates<br>5 => Vertex Position in Eye Coordinates<br>6 => Vertex Normal in Eye Coordinates (This vector is the same as what is used by Lighting.) (Normalized if renorm or rescale is enabled.)<br>7 => Reflection Vector in Eye Coordinates<br>8 => Vertex Position in Eye Coordinates Normalized (This vector is used for Local Viewer specular computations. Probably will never be used by TCG, but here it is anyway.) |

**SE\_TCL\_TEXTURE\_PROC\_CTL - RW - 32 bits - [MMReg:0x2268]**

| Field Name        | Bits  | Default | Description   |
|-------------------|-------|---------|---|
| TEX_CS_PROC_SRC_3 | 31:28 | 0x0     | Input Texture (or Texture Coordinate Generation) Selection<br>0 => Input Texture Coordinate Set 0<br>1 => Input Texture Coordinate Set 1<br>2 => Input Texture Coordinate Set 2<br>3 => Input Texture Coordinate Set 3<br>4 => Vertex Position in Object Coordinates<br>5 => Vertex Position in Eye Coordinates<br>6 => Vertex Normal in Eye Coordinates (This vector is the same as what is used by Lighting.) (Normalized if renorm or rescale is enabled.)<br>7 => Reflection Vector in Eye Coordinates<br>8 => Vertex Position in Eye Coordinates Normalized (This vector is used for Local Viewer specular computations. Probably will never be used by TCG, but here it is anyway.) |

No description available for this register.

**SE\_TCL\_LIGHT\_MODEL\_CTL - RW - 32 bits - [MMReg:0x226C]**

| Field Name               | Bits | Default | Description   |
|--------------------------|------|---------|---|
| LIGHTING_ENA             | 0    | 0x0     | Enables light processing. Must be set for any light processing to occur.  |
| LIGHTING_IN_MODEL        | 1    | 0x0     | Enables light processing in model. This is a performance optimization path. If the ModelView matrix is length and angle-reserving, it is possible to perform lighting computations in model (object) coordinates. This flag, currently, should only be enabled if all of the lights are infinte viewer/infinite light lights. |
| LOCAL_VIEWER             | 2    | 0x0     | Selects local viewer processing for specular computation as opposed to infinte viewer.  |
| NORMALIZE_NORMAL         | 3    | 0x0     | If either the input vertex normals are not normalized, or the ModelView Matrix changes the lenght of the normals, this flag should be set. If forces the renormalization of the vertex normal after the InvTranspose MV rotation.   |
| RESCALE_NORMAL           | 4    | 0x0     | If the input vertex normals are normalized, but the MV matrix changes the length of the normals, the renormalization (rescale) factor can be computed once from the matrix. This rescale value is in ??????????.  |
| SPECULAR_ENA             | 5    | 0x0     | Enable specular lighting computations. If any of the 8 lights that are enabled desire specular computations, this bit needs to be set.  |
| DIFFUSE_SPECULAR_COMBINE | 6    | 0x0     | If set, the lighting diffuse and specular values are combined and output in the diffuse field. If clear, the two color values are output independently.   |
| ALPHA_LIGHTING           | 7    | 0x0     | Perform lighting computations son the alpha channel.  |
| LOC_LIGHT_W_SCALE_SUB    | 8    | 0x0     | If set, the local lighting vertex->light vector is computed using the w terms using the OpenGL cross-multiply method. If clear, the w value of the light and the vertex are ignored for computing the vertex->light vector.   |
| NO_NORMAL_DO_AMB_ONLY    | 9    | 0x0     | If set and no normal in the vertex, TCL only calculates ambient per light.  |

**SE\_TCL\_LIGHT\_MODEL\_CTL - RW - 32 bits - [MMReg:0x226C]**

| Field Name        | Bits  | Default | Description  |
|-------------------|-------|---------|--|
| RSVD_LT_1BIT_NUM0 | 10    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT_1BIT_NUM1 | 11    | 0x0     | Reserved 1-Bit Field   |
| XFORM_OUT_LIGHT   | 12    | 0x0     | XFORM_OUT_LIGHT and CLIP_DBL_BUF_ENA work together as follows:<br>CLIP_DBL_BUF_ENA==0 XFORM_OUT_LIGHT==(don't care) -> Clipper is responsible for starting post clip<br>CLIP_DBL_BUF_ENA==1 XFORM_OUT_LIGHT==0 -> Input Controller is responsible for starting post clip<br>CLIP_DBL_BUF_ENA==1 XFORM_OUT_LIGHT==1 -> Transform Controllers are responsible for starting post clip |
| CLIP_DBL_BUF_ENA  | 13    | 0x0     | Decouples the vertex processing from clip processing. (See description of XFORM_OUT_LIGHT)   |
| CLIP_DISABLE      | 14    | 0x0     | Disables clip code generation and clipping process for TCL.  |
| WAIT_ON_CLIP_DIS  | 15    | 0x0     | Allows post-clip processing to be performed prior (indiscriminate of) clipping / culling testing.  |
| EMISSIVE_SOURCE   | 17:16 | 0x0     | Input Selection for Emissive Value.  |
| AMBIENT_SOURCE    | 19:18 | 0x0     | Input Selection for Ambient Value.   |
| DIFFUSE_SOURCE    | 21:20 | 0x0     | Input Selection for Diffuse Value.   |
| SPECULAR_SOURCE   | 23:22 | 0x0     | Input Selection for Specular Value.  |
| RSVD_LT_2BIT_NUM1 | 25:24 | 0x0     | Reserved 2-bit Field   |
| RSVD_LT_3BIT_NUM0 | 28:26 | 0x0     | Reserved 2-bit Field   |
| RSVD_LT_3BIT_NUM1 | 31:29 | 0x0     | Reserved 3-bit Field   |

No description available for this register.

**SE\_TCL\_PER\_LIGHT\_CTL\_0 - RW - 32 bits - [MMReg:0x2270]**

| Field Name             | Bits | Default | Description  |
|------------------------|------|---------|--|
| LIGHT_ENA_0            | 0    | 0x0     | Enables light.   |
| AMBIENT_ENA_0          | 1    | 0x0     | Enables ambient computations for light.  |
| SPECULAR_ENA_0         | 2    | 0x0     | Enables specular computations for light.   |
| LOCAL_LIGHT_0          | 3    | 0x0     | Specifies a local light instead of an infinite light.  |
| SPOT_ENA_0             | 4    | 0x0     | Enables spotlight attenuation processing for light.  |
| SPOT_DUAL_CONE_0       | 5    | 0x0     | Specifies dual-cone (inner/outer) spot calculations (Direct X) instead of cutoff angle spot calculations (OpenGL).             |
| RNG_ATT_ENA_0          | 6    | 0x0     | Enables range attenuation processing for the light.  |
| RNG_ATT_CONSTANT_ENA_0 | 7    | 0x0     | Enables using a constant value for the range attenuation instead of computing the value. The RNG_ATT_ENA bit must also be set. |
| RSVD_LT0_1BIT_NUM0     | 8    | 0x0     | Reserved 1-Bit Field   |

**SE\_TCL\_PER\_LIGHT\_CTL\_0 - RW - 32 bits - [MMReg:0x2270]**

| Field Name             | Bits  | Default | Description  |
|------------------------|-------|---------|--|
| RSVD_LT0_1BIT_NUM1     | 9     | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT0_1BIT_NUM2     | 10    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT0_1BIT_NUM3     | 11    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT0_2BIT_NUM0     | 13:12 | 0x0     | Reserved 2-Bit Field   |
| RSVD_LT0_2BIT_NUM1     | 15:14 | 0x0     | Reserved 2-Bit Field   |
| LIGHT_ENA_1            | 16    | 0x0     | Enables light.   |
| AMBIENT_ENA_1          | 17    | 0x0     | Enables ambient computations for light.  |
| SPECULAR_ENA_1         | 18    | 0x0     | Enables specular computations for light.   |
| LOCAL_LIGHT_1          | 19    | 0x0     | Specifies a local light instead of an infinite light.  |
| SPOT_ENA_1             | 20    | 0x0     | Enables spotlight attenuation processing for light.  |
| SPOT_DUAL_CONE_1       | 21    | 0x0     | Specifies dual-cone (inner/outer) spot calculations (Direct X) instead of cutoff angle spot calculations (OpenGL).             |
| RNG_ATT_ENA_1          | 22    | 0x0     | Enables range attenuation processing for the light.  |
| RNG_ATT_CONSTANT_ENA_1 | 23    | 0x0     | Enables using a constant value for the range attenuation instead of computing the value. The RNG_ATT_ENA bit must also be set. |
| RSVD_LT1_1BIT_NUM0     | 24    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT1_1BIT_NUM1     | 25    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT1_1BIT_NUM2     | 26    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT1_1BIT_NUM3     | 27    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT1_2BIT_NUM0     | 29:28 | 0x0     | Reserved 2-Bit Field   |
| RSVD_LT1_2BIT_NUM1     | 31:30 | 0x0     | Reserved 2-Bit Field   |

No description available for this register.

**SE\_TCL\_PER\_LIGHT\_CTL\_1 - RW - 32 bits - [MMReg:0x2274]**

| Field Name       | Bits | Default | Description  |
|------------------|------|---------|--|
| LIGHT_ENA_2      | 0    | 0x0     | Enables light.   |
| AMBIENT_ENA_2    | 1    | 0x0     | Enables ambient computations for light.  |
| SPECULAR_ENA_2   | 2    | 0x0     | Enables specular computations for light.   |
| LOCAL_LIGHT_2    | 3    | 0x0     | Specifies a local light instead of an infinite light.  |
| SPOT_ENA_2       | 4    | 0x0     | Enables spotlight attenuation processing for light.  |
| SPOT_DUAL_CONE_2 | 5    | 0x0     | Specifies dual-cone (inner/outer) spot calculations (Direct X) instead of cutoff angle spot calculations (OpenGL). |
| RNG_ATT_ENA_2    | 6    | 0x0     | Enables range attenuation processing for the light.  |

**SE\_TCL\_PER\_LIGHT\_CTL\_1 - RW - 32 bits - [MMReg:0x2274]**

| Field Name             | Bits  | Default | Description  |
|------------------------|-------|---------|--|
| RNG_ATT_CONSTANT_ENA_2 | 7     | 0x0     | Enables using a constant value for the range attenuation instead of computing the value. The RNG_ATT_ENA bit must also be set. |
| RSVD_LT2_1BIT_NUM0     | 8     | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT2_1BIT_NUM1     | 9     | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT2_1BIT_NUM2     | 10    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT2_1BIT_NUM3     | 11    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT2_2BIT_NUM0     | 13:12 | 0x0     | Reserved 2-Bit Field   |
| RSVD_LT2_2BIT_NUM1     | 15:14 | 0x0     | Reserved 2-Bit Field   |
| LIGHT_ENA_3            | 16    | 0x0     | Enables light.   |
| AMBIENT_ENA_3          | 17    | 0x0     | Enables ambient computations for light.  |
| SPECULAR_ENA_3         | 18    | 0x0     | Enables specular computations for light.   |
| LOCAL_LIGHT_3          | 19    | 0x0     | Specifies a local light instead of an infinite light.  |
| SPOT_ENA_3             | 20    | 0x0     | Enables spotlight attenuation processing for light.  |
| SPOT_DUAL_CONE_3       | 21    | 0x0     | Specifies dual-cone (inner/outer) spot calculations (Direct X) instead of cutoff angle spot calculations (OpenGL).             |
| RNG_ATT_ENA_3          | 22    | 0x0     | Enables range attenuation processing for the light.  |
| RNG_ATT_CONSTANT_ENA_3 | 23    | 0x0     | Enables using a constant value for the range attenuation instead of computing the value. The RNG_ATT_ENA bit must also be set. |
| RSVD_LT3_1BIT_NUM0     | 24    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT3_1BIT_NUM1     | 25    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT3_1BIT_NUM2     | 26    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT3_1BIT_NUM3     | 27    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT3_2BIT_NUM0     | 29:28 | 0x0     | Reserved 2-Bit Field   |
| RSVD_LT3_2BIT_NUM1     | 31:30 | 0x0     | Reserved 2-Bit Field   |

No description available for this register.

**SE\_TCL\_PER\_LIGHT\_CTL\_2 - RW - 32 bits - [MMReg:0x2278]**

| Field Name     | Bits | Default | Description   |
|----------------|------|---------|---|
| LIGHT_ENA_4    | 0    | 0x0     | Enables light.  |
| AMBIENT_ENA_4  | 1    | 0x0     | Enables ambient computations for light.               |
| SPECULAR_ENA_4 | 2    | 0x0     | Enables specular computations for light.              |
| LOCAL_LIGHT_4  | 3    | 0x0     | Specifies a local light instead of an infinite light. |
| SPOT_ENA_4     | 4    | 0x0     | Enables spotlight attenuation processing for light.   |

**SE\_TCL\_PER\_LIGHT\_CTL\_2 - RW - 32 bits - [MMReg:0x2278]**

| Field Name             | Bits  | Default | Description  |
|------------------------|-------|---------|--|
| SPOT_DUAL_CONE_4       | 5     | 0x0     | Specifies dual-cone (inner/outer) spot calculations (Direct X) instead of cutoff angle spot calculations (OpenGL).             |
| RNG_ATT_ENA_4          | 6     | 0x0     | Enables range attenuation processing for the light.  |
| RNG_ATT_CONSTANT_ENA_4 | 7     | 0x0     | Enables using a constant value for the range attenuation instead of computing the value. The RNG_ATT_ENA bit must also be set. |
| RSVD_LT4_1BIT_NUM0     | 8     | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT4_1BIT_NUM1     | 9     | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT4_1BIT_NUM2     | 10    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT4_1BIT_NUM3     | 11    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT4_2BIT_NUM0     | 13:12 | 0x0     | Reserved 2-Bit Field   |
| RSVD_LT4_2BIT_NUM1     | 15:14 | 0x0     | Reserved 2-Bit Field   |
| LIGHT_ENA_5            | 16    | 0x0     | Enables light.   |
| AMBIENT_ENA_5          | 17    | 0x0     | Enables ambient computations for light.  |
| SPECULAR_ENA_5         | 18    | 0x0     | Enables specular computations for light.   |
| LOCAL_LIGHT_5          | 19    | 0x0     | Specifies a local light instead of an infinite light.  |
| SPOT_ENA_5             | 20    | 0x0     | Enables spotlight attenuation processing for light.  |
| SPOT_DUAL_CONE_5       | 21    | 0x0     | Specifies dual-cone (inner/outer) spot calculations (Direct X) instead of cutoff angle spot calculations (OpenGL).             |
| RNG_ATT_ENA_5          | 22    | 0x0     | Enables range attenuation processing for the light.  |
| RNG_ATT_CONSTANT_ENA_5 | 23    | 0x0     | Enables using a constant value for the range attenuation instead of computing the value. The RNG_ATT_ENA bit must also be set. |
| RSVD_LT5_1BIT_NUM0     | 24    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT5_1BIT_NUM1     | 25    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT5_1BIT_NUM2     | 26    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT5_1BIT_NUM3     | 27    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT5_2BIT_NUM0     | 29:28 | 0x0     | Reserved 2-Bit Field   |
| RSVD_LT5_2BIT_NUM1     | 31:30 | 0x0     | Reserved 2-Bit Field   |

No description available for this register.

**SE\_TCL\_PER\_LIGHT\_CTL\_3 - RW - 32 bits - [MMReg:0x227C]**

| Field Name     | Bits | Default | Description                              |
|----------------|------|---------|--|
| LIGHT_ENA_6    | 0    | 0x0     | Enables light.                           |
| AMBIENT_ENA_6  | 1    | 0x0     | Enables ambient computations for light.  |
| SPECULAR_ENA_6 | 2    | 0x0     | Enables specular computations for light. |

**SE\_TCL\_PER\_LIGHT\_CTL\_3 - RW - 32 bits - [MMReg:0x227C]**

| Field Name             | Bits  | Default | Description  |
|------------------------|-------|---------|--|
| LOCAL_LIGHT_6          | 3     | 0x0     | Specifies a local light instead of an infinite light.  |
| SPOT_ENA_6             | 4     | 0x0     | Enables spotlight attenuation processing for light.  |
| SPOT_DUAL_CONE_6       | 5     | 0x0     | Specifies dual-cone (inner/outer) spot calculations (Direct X) instead of cutoff angle spot calculations (OpenGL).             |
| RNG_ATT_ENA_6          | 6     | 0x0     | Enables range attenuation processing for the light.  |
| RNG_ATT_CONSTANT_ENA_6 | 7     | 0x0     | Enables using a constant value for the range attenuation instead of computing the value. The RNG_ATT_ENA bit must also be set. |
| RSVD_LT6_1BIT_NUM0     | 8     | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT6_1BIT_NUM1     | 9     | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT6_1BIT_NUM2     | 10    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT6_1BIT_NUM3     | 11    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT6_2BIT_NUM0     | 13:12 | 0x0     | Reserved 2-Bit Field   |
| RSVD_LT6_2BIT_NUM1     | 15:14 | 0x0     | Reserved 2-Bit Field   |
| LIGHT_ENA_7            | 16    | 0x0     | Enables light.   |
| AMBIENT_ENA_7          | 17    | 0x0     | Enables ambient computations for light.  |
| SPECULAR_ENA_7         | 18    | 0x0     | Enables specular computations for light.   |
| LOCAL_LIGHT_7          | 19    | 0x0     | Specifies a local light instead of an infinite light.  |
| SPOT_ENA_7             | 20    | 0x0     | Enables spotlight attenuation processing for light.  |
| SPOT_DUAL_CONE_7       | 21    | 0x0     | Specifies dual-cone (inner/outer) spot calculations (Direct X) instead of cutoff angle spot calculations (OpenGL).             |
| RNG_ATT_ENA_7          | 22    | 0x0     | Enables range attenuation processing for the light.  |
| RNG_ATT_CONSTANT_ENA_7 | 23    | 0x0     | Enables using a constant value for the range attenuation instead of computing the value. The RNG_ATT_ENA bit must also be set. |
| RSVD_LT7_1BIT_NUM0     | 24    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT7_1BIT_NUM1     | 25    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT7_1BIT_NUM2     | 26    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT7_1BIT_NUM3     | 27    | 0x0     | Reserved 1-Bit Field   |
| RSVD_LT7_2BIT_NUM0     | 29:28 | 0x0     | Reserved 2-Bit Field   |
| RSVD_LT7_2BIT_NUM1     | 31:30 | 0x0     | Reserved 2-Bit Field   |

No description available for this register.

46. Pixel Pipe

| PP_CNTL - RW - 32 bits - [MMReg:0x1C38] [MMReg:0x2C38] |      |         |   |
|--|------|---------|---|
| Field Name   | Bits | Default | Description   |
| STIPPLE_ENABLE   | 0    | 0x0     | Disable Stipple function: Enable Stipple function Enable for the 32x32 stipple function, also known as polygon stipple.<br>0=Disable<br>1=Enable  |
| SCISSOR_ENABLE   | 1    | 0x0     | Aux scissor planes not enabled. Ignore scissor enable bits in RE_MISC.: Aux scissor plane enabled Global enable for the four auxiliary scissor planes.<br>0=Disable<br>1=Enable   |
| PATTERN_ENABLE   | 2    | 0x0     | Disable patterned lines: Enable patterned lines Enable for patterned lines, also known as line stipple. When this bit is a 1, the hardware automatically goes into single pixel mode for lines, independent of the dual pixel enable bit.<br>0=Disable<br>1=Enable  |
| SHADOW_ENABLE  | 3    | 0x0     | Disable shadow ID compare: Enable shadow ID compare. In the second pass the Shadow ID register is compared to the unexpanded secondary texels. If the compare fails the secondary texel is set to 0. If the compare passes the color is set to white (0xff). The mask for the compare is inferred from the secondary texture format. If it is the first pass then the Shadow ID value is substituted<br>0=Disable<br>1=Enable |
| TEX_0_ENABLE   | 4    | 0x0     | 0=Disable<br>1=Enable   |
| TEX_1_ENABLE   | 5    | 0x0     | 0=Disable<br>1=Enable   |
| TEX_2_ENABLE   | 6    | 0x0     | 0=Disable<br>1=Enable   |
| TEX_3_ENABLE   | 7    | 0x0     | Must be 0 in Rage 6<br>0=Disable<br>1=Enable  |
| TEX_BLEND_0_ENABLE                                     | 12   | 0x0     | NOTE: Bit 0 of this field is hardwired to ZERO.<br>Disable texture blender 0: Enable texture blender 0 This bit will force the blender to replicate it's inputs on to the inputs of the next stage (blender 1). The output of the stage will be diffuse color.<br>0=Disable<br>1=Enable   |
| TEX_BLEND_1_ENABLE                                     | 13   | 0x0     | Disable texture blender 1: Enable texture blender 1 This bit will force the blender to replicate it's inputs on to the inputs of the next stage (blender 2). The output of the stage will be the same as blender 0 output.<br>0=Disable<br>1=Enable   |



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**PP\_CNTL - RW - 32 bits - [MMReg:0x1C38] [MMReg:0x2C38]**

| Field Name         | Bits  | Default | Description  |
|--------------------|-------|---------|--|
| TEX_BLEND_2_ENABLE | 14    | 0x0     | Disable texture blender 2: Enable texture blender 2 The output of this stage the output of blender 1.<br>0=Disable<br>1=Enable   |
| TEX_BLEND_3_ENABLE | 15    | 0x0     | Must be 0 in Rage 6<br>0=Disable<br>1=Enable<br><br>NOTE: Bit 0 of this field is hardwired to ZERO.  |
| PLANAR_YUV_ENABLE  | 20    | 0x0     | Not doing planar YUV. Planar YUV is enabled. For planar YUV, pipe 0 will be the Y map, pipe 1 will be the U map, and pipe 2 will be the V map. Each map should be programmed to Y8 format in the TXFORMAT field.<br>0=Disable<br>1=Enable  |
| SPECULAR_ENABLE    | 21    | 0x0     | Specular Add is disabled: Specular Add is enabled<br>0=Disable<br>1=Enable   |
| FOG_ENABLE         | 22    | 0x0     | Fog is Disabled: Fog is Enabled<br>0=Disable<br>1=Enable   |
| ALPHA_TEST_ENABLE  | 23    | 0x0     | Disable alpha test: Enable alpha test.<br>0=Disable<br>1=Enable  |
| ANTI_ALIAS_CTL     | 25:24 | 0x0     | 000: No anti-aliasing 001 : Line Anti-aliasing, for lines the source alpha will be modulated by the coverage prior to the SRC/DEST alpha blender 010 : Poly Anti-Aliasing, for triangles the source alpha will be modulated by the coverage prio to the SRC/DEST alpha blender. 011 : Line and Poly Anti-aliasing. For both lines and triangles, the source alpha will be modulated by the coverage prior to SRC/DEST blending. 100 : Obuffer anti-aliasing. 1xx : RESERVED<br>0=No AA<br>1=Line AA<br>2=Poly AA<br>3=Line and Poly AA |
| BUMP_MAP_ENABLE    | 26    | 0x0     | 0=Disable<br>1=Enable  |
| BUMPED_MAP         | 28:27 | 0x0     | 0=T0<br>1=T1<br>2=T2<br>3=RESERVED   |
| TEX_3D_ENABLE_0    | 29    | 0x0     | 0=Disable<br>1=Enable  |
| TEX_3D_ENABLE_1    | 30    | 0x0     | Must be 0 in Rage 6<br>0=Disable<br>1=Enable<br><br>NOTE: Bit 0 of this field is hardwired to ZERO.  |

No description available for this register.

**PP\_TXFILTER\_0 - RW - 32 bits - [MMReg:0x1C54] [MMReg:0x2C54]**



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| Field Name      | Bits  | Default | Description   |
|-----------------|-------|---------|---|
| MAG_FILTER      | 0     | 0x0     | Nearest: Linear<br>0=Nearest<br>1=Linear  |
| MIN_FILTER      | 4:1   | 0x0     |   |
| MAX_ANIS        | 7:5   | 0x0     | 000 : Max 1 to 1 001 : Max 2 to 1 010 : Max 4 to 1 011 : Max 8 to 1 100 : Max 16 to 1 (TXFILTER_0 only)   |
| LOD_BIAS        | 15:8  | 0x0     | Mip-Map LOD bias measured in mip levels. It's a signed 2's complement value w/ range -1.0 <= Bias < 1.0   |
| MAX_MIP_LEVEL   | 19:16 | 0x0     | Maximum number of Mip-Map levels  |
| YUV_TO_RGB      | 20    | 0x0     | Do NOT convert YUV textures to RGB: Convert YUV textures to RGB This bit is RESERVED in TX_FILTER_1 and TX_FILTER_2.<br>0=Disable YUV to RGB<br>1=Enable YUV to RGB   |
| YUV_TEMPERATURE | 21    | 0x0     | YUV to RGB conversion temperature (RESERVED in TXFILTER_1,2): R@650 K, GB@9300 K: RGB@9300 K<br>0=Cool<br>1=Hot   |
| WRAPEN_S        | 22    | 0x0     | Disable cylindrical wrap: Enable cylindrical wrap<br>0=Disable cylindrical wrap<br>1=Enable cylindrical wrap  |
| CLAMP_S         | 25:23 | 0x0     | 1200 Wrap 1 : Mirror 10 : Clamp to last texel 11 : Clamp to border color Non-power of two textures will always clamp.<br>0=Wrap<br>1=Mirror<br>2=Clamp Last<br>3=Mirror Clamp Last<br>4=reserved<br>5=reserved<br>6=Clamp Border<br>7=Mirror Clamp Border |
| WRAPEN_T        | 26    | 0x0     | Disable cylindrical wrap: Enable cylindrical wrap<br>0=Disable cylindrical wrap<br>1=Enable cylindrical wrap  |
| CLAMP_T         | 29:27 | 0x0     | Wrap 01 : Mirror 10 : Clamp to last texel 11 : Clamp to border color Non-power of two textures will always clamp.<br>0=Wrap<br>1=Mirror<br>2=Clamp Last<br>3=Mirror Clamp Last<br>4=reserved<br>5=reserved<br>6=Clamp Border<br>7=Mirror Clamp Border     |
| BORDER_MODE     | 31    | 0x0     | OpenGL border mode: D3D border mode.<br>0=OpenGL<br>1=D3D   |

[ R/W ] Filter and Wrap State for Map 0

**PP\_TXFILTER\_1 - RW - 32 bits - [MMReg:0x1C6C] [MMReg:0x2C6C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



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**PP\_TXFILTER\_1 - RW - 32 bits - [MMReg:0x1C6C] [MMReg:0x2C6C]**

| Field Name    | Bits  | Default | Description  |
|---------------|-------|---------|--|
| MAG_FILTER    | 0     | 0x0     | Nearest: Linear<br>0=Nearest<br>1=Linear   |
| MIN_FILTER    | 4:1   | 0x0     | 0000 : Nearest 0001 : Linear 0010 : Nearest Mip-Map<br>Nearest 0011 : Nearest Mip-Map Linear 010X :<br>RESERVED 0110 : Linear Mip-Map Nearest 0111 : Linear<br>Mip-Map Linear 1000 : Anisotropy Nearest (TXFILTER_0<br>only) 1001 : Anisotropy Linear (TXFILTER_0 only) 1010 :<br>Anisotropy Nearest Mip-Map Nearest (TXFILTER_0 only)<br>1011 : Anisotropy Nearest Mip-Map Linear (TXFILTER_0<br>only) 11XX : RESERVED<br>0=Nearest<br>1=Linear<br>2=Nearest_MIP_Nearest<br>3=Nearest_MIP_Linear<br>4=RESERVED<br>5=RESERVED<br>6=Linear_MIP_Nearest<br>7=Linear_MIP_Linear<br>8=Anisotropy_Nearest<br>9=Anisotropy_Linear<br>10=Anisotropy_Nearest_MIP_Nearest<br>11=Anisotropy_Nearest_MIP_Linear<br>12=RESERVED<br>13=RESERVED<br>14=RESERVED<br>15=RESERVED |
| LOD_BIAS      | 15:8  | 0x0     | Mip-Map LOD bias measured in mip levels. It's a signed<br>2's complement value w/ range -1.0 <= Bias < 1.0   |
| MAX_MIP_LEVEL | 19:16 | 0x0     | Maximum number of Mip-Map levels   |
| WRAPEN_S      | 22    | 0x0     | Disable cylindrical wrap: Enable cylindrical wrap<br>0=Disable cylindrical wrap<br>1=Enable cylindrical wrap   |
| CLAMP_S       | 25:23 | 0x0     | 00 : Wrap 01 : Mirror 10 : Clamp to last texel 11 : Clamp to<br>border color Non-power of two textures will always clamp.<br>0=Wrap<br>1=Mirror<br>2=Clamp Last<br>3=Mirror Clamp Last<br>4=reserved<br>5=reserved<br>6=Clamp Border<br>7=Mirror Clamp Border  |
| WRAPEN_T      | 26    | 0x0     | 0 : Disable cylindrical wrap 1 : Enable cylindrical wrap<br>0=Disable cylindrical wrap<br>1=Enable cylindrical wrap  |
| CLAMP_T       | 29:27 | 0x0     | 00 : Wrap 01 : Mirror 10 : Clamp to last texel 11 : Clamp to<br>border color Non-power of two textures will always clamp.<br>0=Wrap<br>1=Mirror<br>2=Clamp Last<br>3=Mirror Clamp Last<br>4=reserved<br>5=reserved<br>6=Clamp Border<br>7=Mirror Clamp Border  |



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**PP\_TXFILTER\_1 - RW - 32 bits - [MMReg:0x1C6C] [MMReg:0x2C6C]**

| Field Name  | Bits | Default | Description   |
|-------------|------|---------|---|
| BORDER_MODE | 31   | 0x0     | 0 : OpenGL border mode. 1 : D3D border mode.<br>0=OpenGL<br>1=D3D |

[ R/W ] Filter and Wrap State for Map 1

**PP\_TXFILTER\_2 - RW - 32 bits - [MMReg:0x1C84] [MMReg:0x2C84]**

| Field Name    | Bits  | Default | Description  |
|---------------|-------|---------|--|
| MAG_FILTER    | 0     | 0x0     | 0 : Nearest 1 : Linear<br>0=Nearest<br>1=Linear  |
| MIN_FILTER    | 4:1   | 0x0     | 0000 : Nearest 0001 : Linear 0010 : Nearest Mip-Map<br>Nearest 0011 : Nearest Mip-Map Linear 010X :<br>RESERVED 0110 : Linear Mip-Map Nearest 0111 : Linear<br>Mip-Map Linear 1000 : Anisotropy Nearest (TXFILTER_0<br>only) 1001 : Anisotropy Linear (TXFILTER_0 only) 1010 :<br>Anisotropy Nearest Mip-Map Nearest (TXFILTER_0 only)<br>1011 : Anisotropy Nearest Mip-Map Linear (TXFILTER_0<br>only) 11XX : RESERVED<br>0=Nearest<br>1=Linear<br>2=Nearest_MIP_Nearest<br>3=Nearest_MIP_Linear<br>4=RESERVED<br>5=RESERVED<br>6=Linear_MIP_Nearest<br>7=Linear_MIP_Linear<br>8=Anisotropy_Nearest<br>9=Anisotropy_Linear<br>10=Anisotropy_Nearest_MIP_Nearest<br>11=Anisotropy_Nearest_MIP_Linear<br>12=RESERVED<br>13=RESERVED<br>14=RESERVED<br>15=RESERVED |
| LOD_BIAS      | 15:8  | 0x0     | Mip-Map LOD bias measured in mip levels. It's a signed<br>2's complement value w/ range -1.0 <= Bias < 1.0   |
| MAX_MIP_LEVEL | 19:16 | 0x0     | Maximum number of Mip-Map levels   |
| WRAPEN_S      | 22    | 0x0     | 0 : Disable cylindrical wrap 1 : Enable cylindrical wrap<br>0=Disable cylindrical wrap<br>1=Enable cylindrical wrap  |
| CLAMP_S       | 25:23 | 0x0     | 00 : Wrap 01 : Mirror 10 : Clamp to last texel 11 : Clamp to<br>border color Non-power of two textures will always clamp.<br>0=Wrap<br>1=Mirror<br>2=Clamp Last<br>3=Mirror Clamp Last<br>4=Clamp Border<br>5=Mirror Clamp Border  |
| WRAPEN_T      | 26    | 0x0     | 0 : Disable cylindrical wrap 1 : Enable cylindrical wrap<br>0=Disable cylindrical wrap<br>1=Enable cylindrical wrap  |

**PP\_TXFILTER\_2 - RW - 32 bits - [MMReg:0x1C84] [MMReg:0x2C84]**

| Field Name  | Bits  | Default | Description  |
|-------------|-------|---------|--|
| CLAMP_T     | 29:27 | 0x0     | 00 : Wrap 01 : Mirror 10 : Clamp to last texel 11 : Clamp to border color Non-power of two textures will always clamp.<br>0=Wrap<br>1=Mirror<br>2=Clamp Last<br>3=Mirror Clamp Last<br>4=reserved<br>5=reserved<br>6=Clamp Border<br>7=Mirror Clamp Border |
| BORDER_MODE | 31    | 0x0     | 0 : OpenGL border mode. 1 : D3D border mode.<br>0=OpenGL<br>1=D3D  |

[ R/W ] Filter and Wrap State for Map 2

**PP\_TXFORMAT\_0 - RW - 32 bits - [MMReg:0x1C58] [MMReg:0x2C58]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| TXFORMAT   | 4:0  | 0x0     | Specifies texel format of the texture map. 00000 : 8 bpp I (greyscale intensity duplicated on all channels, Green is stored) 00001 : 16bpp AI (greyscale intensity w/ alpha) 00010 : 8 bpp RGB 332 00011 : 16 bpp, ARGB (1555) 00100 : 16 bpp RGB (565) 00101 : 16 bpp ARGB (4444) 00110 : 32 bpp ARGB (8888) 00111 : RESERVED 01000 : 8bpp Y8 luminance 01001 : AYUV 444 (8888) 01010 : YUV 422 packed (VYUY) 01011 : YUV 422 packed (YVYU) 01100 : Color Cell Compression NO alpha or 1-bit alpha 01101 : RESERVED 01110 : Color Cell Compression explicit alpha 01111 : Color Cell Compression compressed alpha 10000 : 16 bpp shadow map 10001 : 32 bpp shadow map<br>0=8bpp I<br>1=16bpp AI (8:8)<br>2=8bpp RGB (3:3:2)<br>3=16bpp ARGB (1:5:5:5)<br>4=16bpp RGB (5:6:5)<br>5=16bpp ARGB (4:4:4:4)<br>6=32bpp ARGB (8:8:8:8)<br>7=32bpp RGBA (8:8:8:8)<br>8=8bpp Y<br>9=AYUV 444 (8:8:8:8)<br>10=YUV 422 (V:Y0:U:Y1) (8:8:8:8)<br>11=YUV 422 (Y0:V:Y1:U) (8:8:8:8)<br>12=Color Cell Compression, NO alpha or 1-bit alpha<br>13=RESERVED<br>14=Color Cell Compression, explicit alpha<br>15=Color Cell Compression, compressed alpha<br>16=16bpp Shadow Map<br>17=32bpp Shadow Map<br>18=du8:dv8<br>19=du5:dv5:l6<br>20=A:du8:dv8:l8<br>21=RESERVED<br>22=RESERVED<br>23=RESERVED<br>24=RESERVED<br>25=RESERVED<br>26=RESERVED<br>27=RESERVED<br>28=RESERVED<br>29=RESERVED<br>30=RESERVED |



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**PP\_TXFORMAT\_0 - RW - 32 bits - [MMReg:0x1C58] [MMReg:0x2C58]**

| Field Name        | Bits  | Default | Description   |
|-------------------|-------|---------|---|
|                   |       |         | 31=RESERVED   |
| APPLE_YUV         | 5     | 0x0     | 0 : Not Apple YUV Mode 1 : Apple YUV Mode (hardware inverts the top bit in U and V)<br>0=NOT Apple YUV Mode<br>1=Apple YUV Mode   |
| ALPHA_ENABLE      | 6     | 0x0     | 0 : No alpha in the map. Assume alpha is 0xff. Formats that do not have alpha (ex. RGB565) will assume alpha is 0xff independent of this bit. 1 : Alpha is in the map<br>0=No Alpha in the Map<br>1=Alpha in the Map  |
| NON_POWER2        | 7     | 0x0     | 0 : The texture resolution is a power of 2. TXWIDTH and TXHEIGHT are used for wrap detection and monolithic mipmap address calculation. TXWIDTH is also used to calculate the map pitch. 1 : This texture resolution is not a power of 2. If this bit is set then the setup engine will pre-multiply the parametric texture coordinates by (TEX_USIZE+1) and (TEX_VSIZE+1). The pipe will automatically clamp to TEX_USIZE and TEX_VSIZE. If the MIN_FILTER is not set to use mip-maps then TXPITCH is used for memory address calculation, otherwise TXWIDTH and TXHEIGHT will be used for monolithic mipmap address calculation. Use of non-power of 2 mipmapping REQUIRES that each map be padded out to the next power of 2 resolution and TXWIDTH and TXHEIGHT to be set to the padded dimensions.<br>0=Texture Resolution is a power of 2<br>1=Texture resolution is not a power of 2 |
| TXWIDTH           | 11:8  | 0x0     | Width of the base map in texels. (Face 0 (-rx) for cubic maps) 0000 : 1 0001 : 2 0010 : 4 0011 : 8 0100 : 16 0101 : 32 0110 : 64 0111 : 128 1000 : 256 1001 : 512 1010 : 1024 1011 : 2048   |
| TXHEIGHT          | 15:12 | 0x0     | Height of the base map in texels. (Face 0 (-rx) for cubic maps) 0000 : 1 0001 : 2 0010 : 4 0011 : 8 0100 : 16 0101 : 32 0110 : 64 0111 : 128 1000 : 256 1001 : 512 1010 : 1024 1011 : 2048  |
| FACE_WIDTH_5      | 19:16 | 0x0     | LOG2 of the width of cube face 5 (-ry) (used for cubic env. Mapping)  |
| FACE_HEIGHT_5     | 23:20 | 0x0     | LOG2 of the height of cube face 5 (-ry) (used for cubic env. Mapping)   |
| ST_ROUTE          | 25:24 | 0x0     | 00 : Use S0,T0 (RESERVED in PP_TXFORMAT_0) 01 : Use S1,T1 (RESERVED in PP_TXFORMAT_0) 10 : Use S2,T2 (RESERVED in PP_TXFORMAT_0,1) 11 : RESERVED ENDIAN_SWAP 27: 26 00 - No Swap 01 - 16bit Swap 10 - 32bit Swap 11 - Half-dword swap<br>0=Use S0, T0, Q0<br>1=Use S1, T1, Q1<br>2=Use S2, T2, Q2<br>3=Use S3, T3, Q3   |
| ALPHA_MASK_ENABLE | 28    | 0x0     | 0=Disable Alpha Mask<br>1=Enable Alpha Mask   |
| CHROMA_KEY_ENABLE | 29    | 0x0     | 0=Disable Chroma Key<br>1=Enable Chroma Key   |



**PP\_TXFORMAT\_0 - RW - 32 bits - [MMReg:0x1C58] [MMReg:0x2C58]**

| Field Name         | Bits | Default | Description   |
|--------------------|------|---------|---|
| CUBIC_MAP_ENABLE   | 30   | 0x0     | 0=Disable cubic environment mapping<br>1=Enable cubic environment mapping   |
| PERSPECTIVE_ENABLE | 31   | 0x0     | 0 : Disable perspective correction 1 : Enable perspective correction<br>0=Persepctive correction disabled<br>1=Persepctive correction enabled |

[ R/W] Texture Format for Maps 0

**PP\_TXFORMAT\_1 - RW - 32 bits - [MMReg:0x1C70] [MMReg:0x2C70]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| TXFORMAT   | 4:0  | 0x0     | Specifies texel format of the texture map. 00000 : 8 bpp I (greyscale intensity duplicated on all channels, Green is stored) 00001 : 16bpp AI (greyscale intensity w/ alpha) 00010 : 8 bpp RGB 332 00011 : 16 bpp, ARGB (1555) 00100 : 16 bpp RGB (565) 00101 : 16 bpp ARGB (4444) 00110 : 32 bpp ARGB (8888) 00111 : RESERVED 01000 : 8bpp Y8 luminance 01001 : AYUV 444 (8888) 01010 : YUV 422 packed (VYUY) 01011 : YUV 422 packed (YVYU) 01100 : Color Cell Compression NO alpha or 1-bit alpha 01101 : RESERVED 01110 : Color Cell Compression explicit alpha 01111 : Color Cell Compression compressed alpha 10000 : 16 bpp shadow map 10001 : 32 bpp shadow map<br>0=8bpp I<br>1=16bpp AI (8:8)<br>2=8bpp RGB (3:3:2)<br>3=16bpp ARGB (1:5:5:5)<br>4=16bpp RGB (5:6:5)<br>5=16bpp ARGB (4:4:4:4)<br>6=32bpp ARGB (8:8:8:8)<br>7=32bpp RGBA (8:8:8:8)<br>8=8bpp Y<br>9=AYUV 444 (8:8:8:8)<br>10=YUV 422 (V:Y0:U:Y1) (8:8:8:8)<br>11=YUV 422 (Y0:V:Y1:U) (8:8:8:8)<br>12=Color Cell Compression, NO alpha or 1-bit alpha<br>13=RESERVED<br>14=Color Cell Compression, explicit alpha<br>15=Color Cell Compression, compressed alpha<br>16=16bpp Shadow Map<br>17=32bpp Shadow Map<br>18=du8:dv8<br>19=du5:dv5:l6<br>20=A:du8:dv8:l8<br>21=RESERVED<br>22=RESERVED<br>23=RESERVED<br>24=RESERVED<br>25=RESERVED<br>26=RESERVED<br>27=RESERVED<br>28=RESERVED<br>29=RESERVED<br>30=RESERVED<br>31=RESERVED |
| APPLE_YUV  | 5    | 0x0     | 0 : Not Apple YUV Mode 1 : Apple YUV Mode (hardware inverts the top bit in U and V)<br>0=NOT Apple YUV Mode<br>1=Apple YUV Mode   |

**PP\_TXFORMAT\_1 - RW - 32 bits - [MMReg:0x1C70] [MMReg:0x2C70]**

| Field Name         | Bits  | Default | Description   |
|--------------------|-------|---------|---|
| ALPHA_ENABLE       | 6     | 0x0     | 0 : No alpha in the map. Assume alpha is 0xff. Formats that do not have alpha (ex. RGB565) will assume alpha is 0xff independent of this bit. 1 : Alpha is in the map<br>0=No Alpha in the Map<br>1=Alpha in the Map  |
| NON_POWER2         | 7     | 0x0     | 0 : The texture resolution is a power of 2. TXWIDTH and TXHEIGHT are used for wrap detection and monolithic mipmap address calculation. TXWIDTH is also used to calculate the map pitch. 1 : This texture resolution is not a power of 2. If this bit is set then the setup engine will pre-multiply the parametric texture coordinates by (TEX_USIZE+1) and (TEX_VSIZE+1). The pipe will automatically clamp to TEX_USIZE and TEX_VSIZE. If the MIN_FILTER is not set to use mip-maps then TXPITCH is used for memory address calculation, otherwise TXWIDTH and TXHEIGHT will be used for monolithic mipmap address calculation. Use of non-power of 2 mipmapping REQUIRES that each map be padded out to the next power of 2 resolution and TXWIDTH and TXHEIGHT to be set to the padded dimensions.<br>0=Texture Resolution is a power of 2<br>1=Texture resolution is not a power of 2 |
| TXWIDTH            | 11:8  | 0x0     | Width of the base map in texels. (Face 0 (-rx) for cubic maps) 0000 : 1 0001 : 2 0010 : 4 0011 : 8 0100 : 16 0101 : 32 0110 : 64 0111 : 128 1000 : 256 1001 : 512 1010 : 1024 1011 : 2048   |
| TXHEIGHT           | 15:12 | 0x0     | Height of the base map in texels. (Face 0 (-rx) for cubic maps) 0000 : 1 0001 : 2 0010 : 4 0011 : 8 0100 : 16 0101 : 32 0110 : 64 0111 : 128 1000 : 256 1001 : 512 1010 : 1024 1011 : 2048  |
| FACE_WIDTH_5       | 19:16 | 0x0     | LOG2 of the width of cube face 5 (-ry) (used for cubic env. Mapping)  |
| FACE_HEIGHT_5      | 23:20 | 0x0     | LOG2 of the height of cube face 5 (-ry) (used for cubic env. Mapping)   |
| ST_ROUTE           | 25:24 | 0x0     | 00 : Use S0,T0 (RESERVED in PP_TXFORMAT_0) 01 : Use S1,T1 (RESERVED in PP_TXFORMAT_0) 10 : Use S2,T2 (RESERVED in PP_TXFORMAT_0,1) 11 : RESERVED ENDIAN_SWAP 27: 26 00 - No Swap 01 - 16bit Swap 10 - 32bit Swap 11 - Half-dword swap<br>0=Use S0, T0, Q0<br>1=Use S1, T1, Q1<br>2=Use S2, T2, Q2<br>3=Use S3, T3, Q3   |
| ALPHA_MASK_ENABLE  | 28    | 0x0     | 0=Disable Alpha Mask<br>1=Enable Alpha Mask   |
| CHROMA_KEY_ENABLE  | 29    | 0x0     | 0=Disable Chroma Key<br>1=Enable Chroma Key   |
| CUBIC_MAP_ENABLE   | 30    | 0x0     | 0=Disable cubic environment mapping<br>1=Enable cubic environment mapping   |
| PERSPECTIVE_ENABLE | 31    | 0x0     | 0 : Disable perspective correction 1 : Enable perspective correction<br>0=Persepctive correction disabled<br>1=Persepctive correction enabled   |



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**PP\_TXFORMAT\_1 - RW - 32 bits - [MMReg:0x1C70] [MMReg:0x2C70]****Field Name****Bits****Default****Description**

[R/W] Texture Format for Maps 1

**PP\_TXFORMAT\_2 - RW - 32 bits - [MMReg:0x1C88] [MMReg:0x2C88]****Field Name****Bits****Default****Description**

TXFORMAT

4:0

0x0

Specifies texel format of the texture map. 00000 : 8 bpp I (greyscale intensity duplicated on all channels, Green is stored) 00001 : 16bpp AI (greyscale intensity w/ alpha) 00010 : 8 bpp RGB 332 00011 : 16 bpp, ARGB (1555) 00100 : 16 bpp RGB (565) 00101 : 16 bpp ARGB (4444) 00110 : 32 bpp ARGB (8888) 00111 : RESERVED 01000 : 8bpp Y8 luminance 01001 : AYUV 444 (8888) 01010 : YUV 422 packed (VYUY) 01011 : YUV 422 packed (YVYU) 01100 : Color Cell Compression NO alpha or 1-bit alpha 01101 : RESERVED 01110 : Color Cell Compression explicit alpha 01111 : Color Cell Compression compressed alpha 10000 : 16 bpp shadow map 10001 : 32 bpp shadow map

0=8bpp I  
1=16bpp AI (8:8)  
2=8bpp RGB (3:3:2)  
3=16bpp ARGB (1:5:5:5)  
4=16bpp RGB (5:6:5)  
5=16bpp ARGB (4:4:4:4)  
6=32bpp ARGB (8:8:8:8)  
7=32bpp RGBA (8:8:8:8)  
8=8bpp Y  
9=AYUV 444 (8:8:8:8)  
10=YUV 422 (V:Y0:U:Y1) (8:8:8:8)  
11=YUV 422 (Y0:V:Y1:U) (8:8:8:8)  
12=Color Cell Compression, NO alpha or 1-bit alpha  
13=RESERVED  
14=Color Cell Compression, explicit alpha  
15=Color Cell Compression, compressed alpha  
16=16bpp Shadow Map  
17=32bpp Shadow Map  
18=du8:dv8  
19=du5:dv5:l6  
20=A:du8:dv8:l8  
21=RESERVED  
22=RESERVED  
23=RESERVED  
24=RESERVED  
25=RESERVED  
26=RESERVED  
27=RESERVED  
28=RESERVED  
29=RESERVED  
30=RESERVED  
31=RESERVED

APPLE\_YUV

5

0x0

0 : Not Apple YUV Mode 1 : Apple YUV Mode (hardware inverts the top bit in U and V)  
0=NOT Apple YUV Mode  
1=Apple YUV Mode

ALPHA\_ENABLE

6

0x0

0 : No alpha in the map. Assume alpha is 0xff. Formats that do not have alpha (ex. RGB565) will assume alpha is 0xff independent of this bit. 1 : Alpha is in the map  
0=No Alpha in the Map  
1=Alpha in the Map



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**PP\_TXFORMAT\_2 - RW - 32 bits - [MMReg:0x1C88] [MMReg:0x2C88]**

| Field Name         | Bits  | Default | Description   |
|--------------------|-------|---------|---|
| NON_POWER2         | 7     | 0x0     | 0 : The texture resolution is a power of 2. TXWIDTH and TXHEIGHT are used for wrap detection and monolithic mipmap address calculation. TXWIDTH is also used to calculate the map pitch. 1 : This texture resolution is not a power of 2. If this bit is set then the setup engine will pre-multiply the parametric texture coordinates by (TEX_USIZE+1) and (TEX_VSIZE+1). The pipe will automatically clamp to TEX_USIZE and TEX_VSIZE. If the MIN_FILTER is not set to use mip-maps then TXPITCH is used for memory address calculation, otherwise TXWIDTH and TXHEIGHT will be used for monolithic mipmap address calculation. Use of non-power of 2 mipmapping REQUIRES that each map be padded out to the next power of 2 resolution and TXWIDTH and TXHEIGHT to be set to the padded dimensions.<br>0=Texture Resolution is a power of 2<br>1=Texture resolution is not a power of 2 |
| TXWIDTH            | 11:8  | 0x0     | Width of the base map in texels. (Face 0 (-rx) for cubic maps) 0000 : 1 0001 : 2 0010 : 4 0011 : 8 0100 : 16 0101 : 32 0110 : 64 0111 : 128 1000 : 256 1001 : 512 1010 : 1024 1011 : 2048   |
| TXHEIGHT           | 15:12 | 0x0     | Height of the base map in texels. (Face 0 (-rx) for cubic maps) 0000 : 1 0001 : 2 0010 : 4 0011 : 8 0100 : 16 0101 : 32 0110 : 64 0111 : 128 1000 : 256 1001 : 512 1010 : 1024 1011 : 2048  |
| FACE_WIDTH_5       | 19:16 | 0x0     | LOG2 of the width of cube face 5 (-ry) (used for cubic env. Mapping)  |
| FACE_HEIGHT_5      | 23:20 | 0x0     | LOG2 of the height of cube face 5 (-ry) (used for cubic env. Mapping)   |
| ST_ROUTE           | 25:24 | 0x0     | 00 : Use S0,T0 (RESERVED in PP_TXFORMAT_0) 01 : Use S1,T1 (RESERVED in PP_TXFORMAT_0) 10 : Use S2,T2 (RESERVED in PP_TXFORMAT_0,1) 11 : RESERVED ENDIAN_SWAP 27: 26 00 - No Swap 01 - 16bit Swap 10 - 32bit Swap 11 - Half-dword swap<br>0=Use S0, T0, Q0<br>1=Use S1, T1, Q1<br>2=Use S2, T2, Q2<br>3=Use S3, T3, Q3   |
| ALPHA_MASK_ENABLE  | 28    | 0x0     | 0=Disable Alpha Mask<br>1=Enable Alpha Mask   |
| CHROMA_KEY_ENABLE  | 29    | 0x0     | 0=Disable Chroma Key<br>1=Enable Chroma Key   |
| CUBIC_MAP_ENABLE   | 30    | 0x0     | 0=Disable cubic environment mapping<br>1=Enable cubic environment mapping   |
| PERSPECTIVE_ENABLE | 31    | 0x0     | 0 : Disable perspective correction 1 : Enable perspective correction<br>0=Perspective correction disabled<br>1=Perspective correction enabled   |

[ R/W ] Texture Format for Maps 2

**PP\_TXOFFSET\_0 - RW - 32 bits - [MMReg:0x1C5C] [MMReg:0x2C5C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**PP\_TXOFFSET\_0 - RW - 32 bits - [MMReg:0x1C5C] [MMReg:0x2C5C]**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| ENDIAN_SWAP | 1:0  | 0x0     | 0=No Swap<br>1=Byte Swap<br>2=Word Swap<br>3=Half-dword swap |
| MACRO_TILE  | 2    | 0x0     | 0=Linear<br>1=Tiled  |
| MICRO_TILE  | 4:3  | 0x0     | 0=Linear<br>1=X2<br>2=Optimized<br>3=RESERVED                |
| TXOFFSET    | 31:5 | 0x0     | 32-byte aligned pointer to largest texture map               |

[ R/W ] Texture Map Offsets for Maps 0

**PP\_TXOFFSET\_1 - RW - 32 bits - [MMReg:0x1C74] [MMReg:0x2C74]**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| ENDIAN_SWAP | 1:0  | 0x0     | 0=No Swap<br>1=Byte Swap<br>2=Word Swap<br>3=Half-dword swap |
| MACRO_TILE  | 2    | 0x0     | 0=Linear<br>1=Tiled  |
| MICRO_TILE  | 4:3  | 0x0     | 0=Linear<br>1=X2<br>2=Optimized<br>3=RESERVED                |
| TXOFFSET    | 31:5 | 0x0     | 32-byte aligned pointer to largest texture map               |

[ R/W ] Texture Map Offsets for Maps 1

**PP\_TXOFFSET\_2 - RW - 32 bits - [MMReg:0x1C8C] [MMReg:0x2C8C]**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| ENDIAN_SWAP | 1:0  | 0x0     | 0=No Swap<br>1=Byte Swap<br>2=Word Swap<br>3=Half-dword swap |
| MACRO_TILE  | 2    | 0x0     | 0=Linear<br>1=Tiled  |
| MICRO_TILE  | 4:3  | 0x0     | 0=Linear<br>1=X2<br>2=Optimized<br>3=RESERVED                |
| TXOFFSET    | 31:5 | 0x0     | 32-byte aligned pointer to largest texture map               |

[ R/W ] Texture Map Offsets for Maps 2

**PP\_TEX\_SIZE\_0 - RW - 32 bits - [MMReg:0x1D04] [MMReg:0x2D04]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**PP\_TEX\_SIZE\_0 - RW - 32 bits - [MMReg:0x1D04] [MMReg:0x2D04]**

| Field Name | Bits  | Default | Description   |
|------------|-------|---------|---|
| TEX_USIZE  | 10:0  | 0x0     | Maximum U of the texture. (0 - 2047). Used for non-power of two textures. |
| TEX_VSIZE  | 26:16 | 0x0     | Maximum V of the texture. (0 - 2047). Used for non-power of two textures. |

[ R/W ] Texture Map Size 0 (for non-power of 2)

**PP\_TEX\_SIZE\_1 - RW - 32 bits - [MMReg:0x1D0C] [MMReg:0x2D0C]**

| Field Name | Bits  | Default | Description   |
|------------|-------|---------|---|
| TEX_USIZE  | 10:0  | 0x0     | Maximum U of the texture. (0 - 2047). Used for non-power of two textures. |
| TEX_VSIZE  | 26:16 | 0x0     | Maximum V of the texture. (0 - 2047). Used for non-power of two textures. |

[ R/W ] Texture Map Size 1 (for non-power of 2)

**PP\_TEX\_SIZE\_2 - RW - 32 bits - [MMReg:0x1D14] [MMReg:0x2D14]**

| Field Name | Bits  | Default | Description   |
|------------|-------|---------|---|
| TEX_USIZE  | 10:0  | 0x0     | Maximum U of the texture. (0 - 2047). Used for non-power of two textures. |
| TEX_VSIZE  | 26:16 | 0x0     | Maximum V of the texture. (0 - 2047). Used for non-power of two textures. |

[ R/W ] Texture Map Size 2 (for non-power of 2)

**PP\_TXPITCH\_0 - RW - 32 bits - [MMReg:0x1D08] [MMReg:0x2D08]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| TXPITCH    | 13:5 | 0x0     | 32-byte aligned stride of texture map.<br>PP_CUBIC_FACES_0 [ R/W ] Texture Map Cubic Map Face Dimensions |

[ R/W ] Texture Map pitches for Map 0 (for non-power of 2)

**PP\_TXPITCH\_1 - RW - 32 bits - [MMReg:0x1D10] [MMReg:0x2D10]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| TXPITCH    | 13:5 | 0x0     | 32-byte aligned stride of texture map.<br>PP_CUBIC_FACES_0 [ R/W ] Texture Map Cubic Map Face Dimensions |

[ R/W ] Texture Map pitches for Map 1 (for non-power of 2)

**PP\_TXPITCH\_2 - RW - 32 bits - [MMReg:0x1D18] [MMReg:0x2D18]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| TXPITCH    | 13:5 | 0x0     | 32-byte aligned stride of texture map.<br>PP_CUBIC_FACES_0 [ R/W ] Texture Map Cubic Map Face Dimensions |

[ R/W ] Texture Map pitches for Map 2 (for non-power of 2)

**PP\_CUBIC\_FACES\_0 - RW - 32 bits - [MMReg:0x1D24] [MMReg:0x2D24]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**PP\_CUBIC\_FACES\_0 - RW - 32 bits - [MMReg:0x1D24] [MMReg:0x2D24]**

| Field Name    | Bits  | Default | Description                             |
|---------------|-------|---------|---|
| FACE_WIDTH_1  | 3:0   | 0x0     | LOG2 of the width of cube face 1 (rz)   |
| FACE_HEIGHT_1 | 7:4   | 0x0     | LOG2 of the hieght of cube face 1 (rz)  |
| FACE_WIDTH_2  | 11:8  | 0x0     | LOG2 of the width of cube face 2 (rx)   |
| FACE_HEIGHT_2 | 15:12 | 0x0     | LOG2 of the hieght of cube face 2 (rx)  |
| FACE_WIDTH_3  | 19:16 | 0x0     | LOG2 of the width of cube face 3 (-rz)  |
| FACE_HEIGHT_3 | 23:20 | 0x0     | LOG2 of the hieght of cube face 3 (-rz) |
| FACE_WIDTH_4  | 27:24 | 0x0     | LOG2 of the width of cube face 4 (ry)   |
| FACE_HEIGHT_4 | 31:28 | 0x0     | LOG2 of the hieght of cube face 4 (ry)  |

No description available for this register.

**PP\_CUBIC\_FACES\_1 - RW - 32 bits - [MMReg:0x1D28] [MMReg:0x2D28]**

| Field Name    | Bits  | Default | Description                             |
|---------------|-------|---------|---|
| FACE_WIDTH_1  | 3:0   | 0x0     | LOG2 of the width of cube face 1 (rz)   |
| FACE_HEIGHT_1 | 7:4   | 0x0     | LOG2 of the hieght of cube face 1 (rz)  |
| FACE_WIDTH_2  | 11:8  | 0x0     | LOG2 of the width of cube face 2 (rx)   |
| FACE_HEIGHT_2 | 15:12 | 0x0     | LOG2 of the hieght of cube face 2 (rx)  |
| FACE_WIDTH_3  | 19:16 | 0x0     | LOG2 of the width of cube face 3 (-rz)  |
| FACE_HEIGHT_3 | 23:20 | 0x0     | LOG2 of the hieght of cube face 3 (-rz) |
| FACE_WIDTH_4  | 27:24 | 0x0     | LOG2 of the width of cube face 4 (ry)   |
| FACE_HEIGHT_4 | 31:28 | 0x0     | LOG2 of the hieght of cube face 4 (ry)  |

[ R/W ] Texture Map Cubic Map Face Dimensions

**PP\_CUBIC\_FACES\_2 - RW - 32 bits - [MMReg:0x1D2C] [MMReg:0x2D2C]**

| Field Name    | Bits  | Default | Description                             |
|---------------|-------|---------|---|
| FACE_WIDTH_1  | 3:0   | 0x0     | LOG2 of the width of cube face 1 (rz)   |
| FACE_HEIGHT_1 | 7:4   | 0x0     | LOG2 of the hieght of cube face 1 (rz)  |
| FACE_WIDTH_2  | 11:8  | 0x0     | LOG2 of the width of cube face 2 (rx)   |
| FACE_HEIGHT_2 | 15:12 | 0x0     | LOG2 of the hieght of cube face 2 (rx)  |
| FACE_WIDTH_3  | 19:16 | 0x0     | LOG2 of the width of cube face 3 (-rz)  |
| FACE_HEIGHT_3 | 23:20 | 0x0     | LOG2 of the hieght of cube face 3 (-rz) |
| FACE_WIDTH_4  | 27:24 | 0x0     | LOG2 of the width of cube face 4 (ry)   |
| FACE_HEIGHT_4 | 31:28 | 0x0     | LOG2 of the hieght of cube face 4 (ry)  |

[ R/W ] Texture Map Cubic Map Face Dimensions

**PP\_CUBIC\_OFFSET\_T0\_0 - RW - 32 bits - [MMReg:0x1DD0] [MMReg:0x2DD0]**



| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T0\_1 - RW - 32 bits - [MMReg:0x1DD4] [MMReg:0x2DD4]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T0\_2 - RW - 32 bits - [MMReg:0x1DD8] [MMReg:0x2DD8]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T0\_3 - RW - 32 bits - [MMReg:0x1DDC] [MMReg:0x2DDC]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T0\_4 - RW - 32 bits - [MMReg:0x1DE0] [MMReg:0x2DE0]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T1\_0 - RW - 32 bits - [MMReg:0x1E00] [MMReg:0x2E00]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T1\_1 - RW - 32 bits - [MMReg:0x1E04] [MMReg:0x2E04]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T1\_2 - RW - 32 bits - [MMReg:0x1E08] [MMReg:0x2E08]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T1\_3 - RW - 32 bits - [MMReg:0x1E0C] [MMReg:0x2E0C]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T1\_4 - RW - 32 bits - [MMReg:0x1E10] [MMReg:0x2E10]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T2\_0 - RW - 32 bits - [MMReg:0x1E14] [MMReg:0x2E14]**



| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T2\_1 - RW - 32 bits - [MMReg:0x1E18] [MMReg:0x2E18]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T2\_2 - RW - 32 bits - [MMReg:0x1E1C] [MMReg:0x2E1C]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T2\_3 - RW - 32 bits - [MMReg:0x1E20] [MMReg:0x2E20]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T2\_4 - RW - 32 bits - [MMReg:0x1E24] [MMReg:0x2E24]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T3\_0 - RW - 32 bits - [MMReg:0x2E28]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T3\_1 - RW - 32 bits - [MMReg:0x2E2C]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T3\_2 - RW - 32 bits - [MMReg:0x2E30]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T3\_3 - RW - 32 bits - [MMReg:0x2E34]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_CUBIC\_OFFSET\_T3\_4 - RW - 32 bits - [MMReg:0x2E38]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| FACE_OFFSET | 31:5 | none    |             |

No description available for this register.

**PP\_SHADOW\_ID - RW - 32 bits - [MMReg:0x1D34] [MMReg:0x2D34]**



| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| SHADOW_ID  | 23:0 | 0x0     | Shadow ID   |

No description available for this register.

#### PP\_CHROMA\_COLOR - RW - 32 bits - [MMReg:0x1D38] [MMReg:0x2D38]

| Field Name   | Bits | Default | Description                   |
|--------------|------|---------|-------------------------------|
| CHROMA_COLOR | 31:0 | none    | Color used for chroma keying. |

[ R/W ] Chroma Key Color

#### PP\_CHROMA\_MASK - RW - 32 bits - [MMReg:0x1D3C] [MMReg:0x2D3C]

| Field Name  | Bits | Default | Description                      |
|-------------|------|---------|----------------------------------|
| CHROMA_MASK | 31:0 | none    | Mask used in chroma key compare. |

[ R/W ] Chroma Key Mask

#### PP\_BORDER\_COLOR\_0 - RW - 32 bits - [MMReg:0x1D40] [MMReg:0x2D40]

| Field Name | Bits | Default | Description                     |
|------------|------|---------|---------------------------------|
| BORD_COLOR | 31:0 | none    | Texture border color ARGB 8888. |

[ R/W ] Texture Border Colors for Map 0

#### PP\_BORDER\_COLOR\_1 - RW - 32 bits - [MMReg:0x1D44] [MMReg:0x2D44]

| Field Name | Bits | Default | Description                     |
|------------|------|---------|---------------------------------|
| BORD_COLOR | 31:0 | none    | Texture border color ARGB 8888. |

[ R/W ] Texture Border Colors for Map 1

#### PP\_BORDER\_COLOR\_2 - RW - 32 bits - [MMReg:0x1D48] [MMReg:0x2D48]

| Field Name | Bits | Default | Description                     |
|------------|------|---------|---------------------------------|
| BORD_COLOR | 31:0 | none    | Texture border color ARGB 8888. |

[ R/W ] Texture Border Colors for Map 2

#### PP\_MISC - RW - 32 bits - [MMReg:0x1C14] [MMReg:0x2C14]

| Field Name    | Bits | Default | Description   |
|---------------|------|---------|---|
| REF_ALPHA     | 7:0  | none    | Reference Alpha used in alpha test  |
| ALPHA_TEST_OP | 10:8 | 0x0     | 000 : Alpha test never passes<br>001 : Src Alpha < Ref Alpha<br>010 : Src Alpha <= Ref Alpha<br>011 : Src Alpha == Ref Alpha<br>100 : Src Alpha >= Ref Alpha<br>101 : Src Alpha > Ref Alpha<br>110 : Src Alpha != Ref Alpha<br>111 : Alpha test always passes<br>0=Always Fail<br>1=Src Alpha < Ref Alpha<br>2=Src Alpha <= Ref Alpha<br>3=Src Alpha == Ref Alpha<br>4=Src Alpha >= Ref Alpha<br>5=Src Alpha > Ref Alpha<br>6=Src Alpha != Ref Alpha<br>7=Always Pass |



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**PP\_MISC - RW - 32 bits - [MMReg:0x1C14] [MMReg:0x2C14]**

| Field Name      | Bits  | Default | Description  |
|-----------------|-------|---------|--|
| CHROMA_FUNC     | 17:16 | 0x0     | 00 : False (Chroma Key function always fails, cull all pixels) 01 : True (Chroma Key function always passes, don't cull any pixels) 10 : if Texel != Chroma Color cull the pixel 11 : if Texel == Chroma Color cull the pixel Texture borders always pass the test.<br>0=Cull All Pixels<br>1=Cull No Pixels<br>2=Cull if NOT Equal<br>3=Cull if Equal   |
| CHROMA_KEY_MODE | 18    | 0x0     | 0 : If the nearest texel in a bilinear sample matches the chroma key then the pixel is culled. If texels other than the nearest of a bilinear sample match the chroma key then we substitute that sample's color with the nearest color. 1 : For any sample that matches the chroma color. The color of the sample is set to 0. The pixel is not culled. In both modes the alpha channel is set to 0 for any texel that matches the chroma color.<br>0=Nearest<br>1=Zero |
| SHADOW_AUTO_INC | 20    | 0x0     | 0 : Do NOT auto-increment the shadow id per primitive 1 : Increment the shadow ID per primitive<br>0=Do NOT auto increment the shadow ID<br>1=Auto increment the shadow ID   |
| SHADOW_FUNC     | 21    | 0x0     | 0 : Pass if Shadow ID matches texel. 1 : Pass if Shadow ID doesn't match texel.<br>0=Pass if shadow id matches secondary texel<br>1=Pass if id doesn't match secondary texel   |
| SHADOW_PASS     | 22    | 0x0     | 0 : Pass 1 of the shadow algorithm 1 : Pass 2 of the shadow algorithm<br>0=Pass 1 of the shadow algorithm<br>1=Pass 2 of the shadow algorithm  |
| RIGHT_HAND_CUBE | 24    | 0x0     | This bit only needs to be hit when one of the texture pipes is doing cubic environment mapping. 0 : The six faces of the cube for cubic environment mapping are organized per spurious DX7 documentation. (Left hand coordinate system) 1 : The six faces of the cube for cubic environment mapping are organized per Foley and Van Dam and likely OpenGL. (Right hand coordinate system)<br>0=D3D<br>1=OpenGL   |

No description available for this register.

**PP\_TXCBLEND\_0 - RW - 32 bits - [MMReg:0x1C60] [MMReg:0x2C60]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



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**PP\_TXCBLEND\_0 - RW - 32 bits - [MMReg:0x1C60] [MMReg:0x2C60]**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| COLOR_ARG_A | 4:0  | 0x0     | 0000 : Zero (0.0) 0001 : RESERVED 0010 : Current Color (This defaults to diffuse Color on unit 3) 0011 : Current Alpha (Defaults to diffuse Alpha on unit 3) 0100 : Diffuse Color 0101 : Diffuse Alpha 0110 : Specular Color 0111 : Specular Alpha (Fog) 1000 : Tfactor Color 1001 : Tfactor Alpha 1010 : Texel 0 Color 1011 : Texel 0 Alpha 1100 : Texel 1 Color 1101 : Texel 1 Alpha 1110 : Texel 2 Color 1111 : Texel 2 Alpha<br>0=Zero<br>1=RESERVED<br>2=Current Color<br>3=Current Alpha<br>4=Diffuse Color<br>5=Diffuse Alpha<br>6=Specular Color<br>7=Specular Alpha<br>8=TFACTOR Color<br>9=TFACTOR Alpha<br>10=T0 Color<br>11=T0 Alpha<br>12=T1 Color<br>13=T1 Alpha<br>14=T2 Color<br>15=T2 Alpha<br>16=T3 Color<br>17=T3 Alpha |
| COLOR_ARG_B | 9:5  | 0x0     | Same decode as Color Argument A<br>0=Zero<br>1=RESERVED<br>2=Current Color<br>3=Current Alpha<br>4=Diffuse Color<br>5=Diffuse Alpha<br>6=Specular Color<br>7=Specular Alpha<br>8=TFACTOR Color<br>9=TFACTOR Alpha<br>10=T0 Color<br>11=T0 Alpha<br>12=T1 Color<br>13=T1 Alpha<br>14=T2 Color<br>15=T2 Alpha<br>16=T3 Color<br>17=T3 Alpha  |



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**PP\_TXCBLEND\_0 - RW - 32 bits - [MMReg:0x1C60] [MMReg:0x2C60]**

| Field Name  | Bits  | Default | Description   |
|-------------|-------|---------|---|
| COLOR_ARG_C | 14:10 | 0x2     | Same decode as Color Argument A<br>0=Zero<br>1=RESERVED<br>2=Current Color<br>3=Current Alpha<br>4=Diffuse Color<br>5=Diffuse Alpha<br>6=Specular Color<br>7=Specular Alpha<br>8=TFACOR Color<br>9=TFACOR Alpha<br>10=T0 Color<br>11=T0 Alpha<br>12=T1 Color<br>13=T1 Alpha<br>14=T2 Color<br>15=T2 Alpha<br>16=T3 Color<br>17=T3 Alpha |
| COMP_ARG_A  | 15    | 0x0     | 0: Do NOT complement argument A 1: Complement argument A, (1.0 - A)<br>0=Do NOT Complement Argument A<br>1=Complement Argument A  |
| COMP_ARG_B  | 16    | 0x0     | 0: Do NOT complement argument B 1: Complement argument B, (1.0 - B)<br>0=Do NOT Complement Argument B<br>1=Complement Argument B  |
| COMP_ARG_C  | 17    | 0x0     | 0: Do NOT complement argument C 1: Complement argument C, (1.0 - C)<br>0=Do NOT Complement Argument C<br>1=Complement Argument C  |
| BLEND_CTL   | 20:18 | 0x0     | 000: ADD (A * B + C) 001: SUBTRACT (A * B - C) 010: ADDSIGNED (A * B + C - 0.5) 011: BLEND ((1 - C) * A + C * B) 1xx: RESERVED<br>0=ADD<br>1=SUBTRACT<br>2=ADDSIGNED<br>3=BLEND<br>4=DOT3<br>5=RESERVED<br>6=RESERVED<br>7=RESERVED   |
| SCALE_TX    | 22:21 | 0x0     | 00: 1x, do not scale the output of the adder 01: 2x, scale by 2 (used for ADDSIGNED2X and MODULATE2X) 10: 4x, scale by 4 (used for MODULATE4x) 11: RESERVED<br>0=Scale 1X<br>1=Scale 2X<br>2=Scale 4x<br>3=RESERVED   |
| CLAMP_TX    | 23    | 0x1     | 0: Do not clamp output values 1: Clamp output values. Method of clamping is dependent on blender control bits<br>0=Do NOT Clamp<br>1=Clamp  |

**PP\_TXCBLEND\_0 - RW - 32 bits - [MMReg:0x1C60] [MMReg:0x2C60]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| T0_EQ_TCUR | 24   | 0x0     | 0: Pass Texel 0 input of this stage to Texel 0 input of next stage 1: Replicate the output of this stage on to the Texel 0 input of the next stage (AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T0 in to T0 in of next stage<br>1=Copy output to T0 in of next stage |
| T1_EQ_TCUR | 25   | 0x0     | 0: Pass Texel 1 input of this stage to Texel 1 input of next stage 1: Replicate the output of this stage on to the Texel 1 input of the next stage (AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T1 in to T1 in of next stage<br>1=Copy output to T1 in of next stage |
| T2_EQ_TCUR | 26   | 0x0     | 0: Pass Texel 2 input of this stage to Texel 2 input of next stage 1: Replicate the output of this stage on to the Texel 2 input of the next stage (AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T2 in to T2 in of next stage<br>1=Copy output to T2 in of next stage |
| T3_EQ_TCUR | 27   | 0x0     | 0=Pass T3 in to T3 in of next stage<br>1=Copy output to T3 in of next stage   |

[ R/W ] Control for Color Texture Blender 0

**PP\_TXCBLEND\_1 - RW - 32 bits - [MMReg:0x1C78] [MMReg:0x2C78]**

| Field Name  | Bits | Default | Description   |
|-------------|------|---------|---|
| COLOR_ARG_A | 4:0  | 0x0     | 0000: Zero (0.0): RESERVED 0010: Current Color (This defaults to diffuse Color on unit 3) 0011: Current Alpha (Defaults to diffuse Alpha on unit 3) 0100: Diffuse Color 0101: Diffuse Alpha 0110: Specular Color 0111: Specular Alpha (Fog) 1000: Tfactor Color 1001: Tfactor Alpha 1010: Texel 0 Color 1011: Texel 0 Alpha 1100: Texel 1 Color 1101: Texel 1 Alpha 1110: Texel 2 Color 1111: Texel 2 Alpha<br>0=Zero<br>1=RESERVED<br>2=Current Color<br>3=Current Alpha<br>4=Diffuse Color<br>5=Diffuse Alpha<br>6=Specular Color<br>7=Specular Alpha<br>8=TFACTOR Color<br>9=TFACTOR Alpha<br>10=T0 Color<br>11=T0 Alpha<br>12=T1 Color<br>13=T1 Alpha<br>14=T2 Color<br>15=T2 Alpha<br>16=T3 Color<br>17=T3 Alpha |

**PP\_TXCBLEND\_1 - RW - 32 bits - [MMReg:0x1C78] [MMReg:0x2C78]**

| Field Name  | Bits  | Default | Description   |
|-------------|-------|---------|---|
| COLOR_ARG_B | 9:5   | 0x0     | Same decode as Color Argument A<br>0=Zero<br>1=RESERVED<br>2=Current Color<br>3=Current Alpha<br>4=Diffuse Color<br>5=Diffuse Alpha<br>6=Specular Color<br>7=Specular Alpha<br>8=TFACTOR Color<br>9=TFACTOR Alpha<br>10=T0 Color<br>11=T0 Alpha<br>12=T1 Color<br>13=T1 Alpha<br>14=T2 Color<br>15=T2 Alpha<br>16=T3 Color<br>17=T3 Alpha |
| COLOR_ARG_C | 14:10 | 0x2     | Same decode as Color Argument A<br>0=Zero<br>1=RESERVED<br>2=Current Color<br>3=Current Alpha<br>4=Diffuse Color<br>5=Diffuse Alpha<br>6=Specular Color<br>7=Specular Alpha<br>8=TFACTOR Color<br>9=TFACTOR Alpha<br>10=T0 Color<br>11=T0 Alpha<br>12=T1 Color<br>13=T1 Alpha<br>14=T2 Color<br>15=T2 Alpha<br>16=T3 Color<br>17=T3 Alpha |
| COMP_ARG_A  | 15    | 0x0     | 0: Do NOT complement argument A 1: Complement argument A, (1.0 - A)<br>0=Do NOT Complement Argument A<br>1=Complement Argument A  |
| COMP_ARG_B  | 16    | 0x0     | 0: Do NOT complement argument B 1: Complement argument B, (1.0 - B)<br>0=Do NOT Complement Argument B<br>1=Complement Argument B  |
| COMP_ARG_C  | 17    | 0x0     | 0: Do NOT complement argument C 1: Complement argument C, (1.0 - C)<br>0=Do NOT Complement Argument C<br>1=Complement Argument C  |



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**PP\_TXCBLEND\_1 - RW - 32 bits - [MMReg:0x1C78] [MMReg:0x2C78]**

| Field Name | Bits  | Default | Description  |
|------------|-------|---------|--|
| BLEND_CTL  | 20:18 | 0x0     | 000: ADD (A * B + C) 001: SUBTRACT (A * B - C) 010: ADDSIGNED (A * B + C - 0.5) 011: BLEND ((1 - C) * A + C * B) 1xx: RESERVED<br>0=ADD<br>1=SUBTRACT<br>2=ADDSIGNED<br>3=BLEND<br>4=DOT3<br>5=RESERVED<br>6=RESERVED<br>7=RESERVED                          |
| SCALE_TX   | 22:21 | 0x0     | 00: 1x, do not scale the output of the adder 01: 2x, scale by 2 (used for ADDSIGNED2X and MODULATE2X) 10: 4x, scale by 4 (used for MODULATE4x) 11: RESERVED<br>0=Scale 1X<br>1=Scale 2X<br>2=Scale 4x<br>3=RESERVED  |
| CLAMP_TX   | 23    | 0x1     | 0: Do not clamp output values 1: Clamp output values. Method of clamping is dependent on blender control bits<br>0=Do NOT Clamp<br>1=Clamp   |
| T0_EQ_TCUR | 24    | 0x0     | 0: Pass Texel 0 input of this stage to Texel 0 input of next stage: Replicate the output of this stage on to the Texel 0 input of the next stage(AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T0 in to T0 in of next stage<br>1=Copy output to T0 in of next stage   |
| T1_EQ_TCUR | 25    | 0x0     | 0: Pass Texel 1 input of this stage to Texel 1 input of next stage 1: Replicate the output of this stage on to the Texel 1 input of the next stage(AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T1 in to T1 in of next stage<br>1=Copy output to T1 in of next stage |
| T2_EQ_TCUR | 26    | 0x0     | 0: Pass Texel 2 input of this stage to Texel 2 input of next stage 1: Replicate the output of this stage on to the Texel 2 input of the next stage(AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T2 in to T2 in of next stage<br>1=Copy output to T2 in of next stage |
| T3_EQ_TCUR | 27    | 0x0     | 0=Pass T3 in to T3 in of next stage<br>1=Copy output to T3 in of next stage  |

[ R/W ] Control for Color Texture Blender 1

**PP\_TXCBLEND\_2 - RW - 32 bits - [MMReg:0x1C90] [MMReg:0x2C90]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



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**PP\_TXCBLEND\_2 - RW - 32 bits - [MMReg:0x1C90] [MMReg:0x2C90]**

| Field Name  | Bits | Default | Description   |
|-------------|------|---------|---|
| COLOR_ARG_A | 4:0  | 0x0     | 0000: Zero (0.0) 0001 : RESERVED 0010 : Current Color (This defaults to diffuse Color on unit 3) 0011 : Current Alpha (Defaults to diffuse Alpha on unit 3) 0100 : Diffuse Color 0101 : Diffuse Alpha 0110 : Specular Color 0111 : Specular Alpha (Fog) 1000 : Tfactor Color 1001 : Tfactor Alpha 1010 : Texel 0 Color 1011 : Texel 0 Alpha 1100 : Texel 1 Color 1101 : Texel 1 Alpha 1110 : Texel 2 Color 1111 : Texel 2 Alpha<br>0=Zero<br>1=RESERVED<br>2=Current Color<br>3=Current Alpha<br>4=Diffuse Color<br>5=Diffuse Alpha<br>6=Specular Color<br>7=Specular Alpha<br>8=TFACTOR Color<br>9=TFACTOR Alpha<br>10=T0 Color<br>11=T0 Alpha<br>12=T1 Color<br>13=T1 Alpha<br>14=T2 Color<br>15=T2 Alpha<br>16=T3 Color<br>17=T3 Alpha |
| COLOR_ARG_B | 9:5  | 0x0     | Same decode as Color Argument A<br>0=Zero<br>1=RESERVED<br>2=Current Color<br>3=Current Alpha<br>4=Diffuse Color<br>5=Diffuse Alpha<br>6=Specular Color<br>7=Specular Alpha<br>8=TFACTOR Color<br>9=TFACTOR Alpha<br>10=T0 Color<br>11=T0 Alpha<br>12=T1 Color<br>13=T1 Alpha<br>14=T2 Color<br>15=T2 Alpha<br>16=T3 Color<br>17=T3 Alpha   |

**PP\_TXCBLEND\_2 - RW - 32 bits - [MMReg:0x1C90] [MMReg:0x2C90]**

| Field Name  | Bits  | Default | Description   |
|-------------|-------|---------|---|
| COLOR_ARG_C | 14:10 | 0x2     | Same decode as Color Argument A<br>0=Zero<br>1=RESERVED<br>2=Current Color<br>3=Current Alpha<br>4=Diffuse Color<br>5=Diffuse Alpha<br>6=Specular Color<br>7=Specular Alpha<br>8=TFACTOR Color<br>9=TFACTOR Alpha<br>10=T0 Color<br>11=T0 Alpha<br>12=T1 Color<br>13=T1 Alpha<br>14=T2 Color<br>15=T2 Alpha<br>16=T3 Color<br>17=T3 Alpha |
| COMP_ARG_A  | 15    | 0x0     | 0: Do NOT complement argument A 1 : Complement argument A, (1.0 - A)<br>0=Do NOT Complement Argument A<br>1=Complement Argument A   |
| COMP_ARG_B  | 16    | 0x0     | 0: Do NOT complement argument B 1 : Complement argument B, (1.0 - B)<br>0=Do NOT Complement Argument B<br>1=Complement Argument B   |
| COMP_ARG_C  | 17    | 0x0     | 0: Do NOT complement argument C 1 : Complement argument C, (1.0 - C)<br>0=Do NOT Complement Argument C<br>1=Complement Argument C   |
| BLEND_CTL   | 20:18 | 0x0     | 000: ADD (A * B + C) 001 : SUBTRACT (A * B - C) 010 : ADDSIGNED (A * B + C - 0.5) 011 : BLEND ((1 - C) * A + C * B) 1xx : RESERVED<br>0=ADD<br>1=SUBTRACT<br>2=ADDSIGNED<br>3=BLEND<br>4=DOT3<br>5=RESERVED<br>6=RESERVED<br>7=RESERVED   |
| SCALE_TX    | 22:21 | 0x0     | 00: 1x, do not scale the output of the adder 01 : 2x, scale by 2 (used for ADDSIGNED2X and MODULATE2X) 10 : 4x, scale by 4 (used for MODULATE4x) 11 : RESERVED<br>0=Scale 1X<br>1=Scale 2X<br>2=Scale 4x<br>3=RESERVED  |
| CLAMP_TX    | 23    | 0x1     | 0: Do not clamp output values. 1 : Clamp output values. Method of clamping is dependent on blender control bits<br>0=Do NOT Clamp<br>1=Clamp  |



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**PP\_TXCBLEND\_2 - RW - 32 bits - [MMReg:0x1C90] [MMReg:0x2C90]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| T0_EQ_TCUR | 24   | 0x0     | 0: Pass Texel 0 input of this stage to Texel 0 input of next stage 1 : Replicate the output of this stage on to the Texel 0 input of the next stage (AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T0 in to T0 in of next stage<br>1=Copy output to T0 in of next stage |
| T1_EQ_TCUR | 25   | 0x0     | 0: Pass Texel 1 input of this stage to Texel 1 input of next stage 1 : Replicate the output of this stage on to the Texel 1 input of the next stage (AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T1 in to T1 in of next stage<br>1=Copy output to T1 in of next stage |
| T2_EQ_TCUR | 26   | 0x0     | 0: Pass Texel 2 input of this stage to Texel 2 input of next stage 1 : Replicate the output of this stage on to the Texel 2 input of the next stage (AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T2 in to T2 in of next stage<br>1=Copy output to T2 in of next stage |
| T3_EQ_TCUR | 27   | 0x0     | 0=Pass T3 in to T3 in of next stage<br>1=Copy output to T3 in of next stage  |

[ R/W ] Control for Color Texture Blender 2

**PP\_TXABLEND\_0 - RW - 32 bits - [MMReg:0x1C64] [MMReg:0x2C64]**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| ALPHA_ARG_A | 3:0  | 0x0     | 000: Zero (0.0): Current Alpha (Defaults to diffuse alpha on stage 0)010: Diffuse Alpha 011: Specular Alpha (Fog) 100: Tfactor Alpha 101: Texel 0 Alpha 110: Texel 1 Alpha 111: Texel 2 Alpha<br>0=Zero<br>1=Current Alpha<br>2=Diffuse Alpha<br>3=Specular Alpha<br>4=TFACTOR Alpha<br>5=T0 Alpha<br>6=T1 Alpha<br>7=T2 Alpha<br>8=T3 Alpha |
| ALPHA_ARG_B | 7:4  | 0x0     | Same decode as Alpha Argument A<br>0=Zero<br>1=Current Alpha<br>2=Diffuse Alpha<br>3=Specular Alpha<br>4=TFACTOR Alpha<br>5=T0 Alpha<br>6=T1 Alpha<br>7=T2 Alpha<br>8=T3 Alpha   |

**PP\_TXABLEND\_0 - RW - 32 bits - [MMReg:0x1C64] [MMReg:0x2C64]**

| Field Name  | Bits  | Default | Description   |
|-------------|-------|---------|---|
| ALPHA_ARG_C | 11:8  | 0x1     | Same decode as Alpha Argument A<br>0=Zero<br>1=Current Alpha<br>2=Diffuse Alpha<br>3=Specular Alpha<br>4=TFACITOR Alpha<br>5=T0 Alpha<br>6=T1 Alpha<br>7=T2 Alpha<br>8=T3 Alpha   |
| DOT_ALPHA   | 12    | 0x0     | 0: If Color Op is DOT then replicate DOT product in alpha<br>1: Don't replicate DOT product result in alpha.<br>0=Replicate DOTPROD to Alpha<br>1=Do NOT replicate DOTPROD to Alpha   |
| COMP_ARG_A  | 15    | 0x0     | 0: Do NOT complement argument A 1: Complement argument A, (1.0 - A)<br>0=Do NOT Complement Argument A<br>1=Complement Argument A  |
| COMP_ARG_B  | 16    | 0x0     | 0: Do NOT complement argument B 1: Complement argument B, (1.0 - B)<br>0=Do NOT Complement Argument B<br>1=Complement Argument B  |
| COMP_ARG_C  | 17    | 0x0     | 0: Do NOT complement argument C 1: Complement argument C, (1.0 - C)<br>0=Do NOT Complement Argument C<br>1=Complement Argument C  |
| BLEND_CTL   | 20:18 | 0x0     | 000: ADD (A * B + C); SUBTRACT (A * B - C) 010: ADDSIGNED (A * B + C - 0.5) 011: BLEND ((1 - C) * A + C * B) 1xx: RESERVED<br>0=ADD<br>1=SUBTRACT<br>2=ADDSIGNED<br>3=BLEND   |
| SCALE_TX    | 22:21 | 0x0     | 00: 1x, do not scale the output of the adder: 2x, scale by 2 (used for ADDSIGNED2X and MODULATE2X) 10: 4x, scale by 4 (used for MODULATE4x) 11: RESERVED<br>0=Scale 1X<br>1=Scale 2X<br>2=Scale 4x<br>3=RESERVED  |
| CLAMP_TX    | 23    | 0x1     | 0: Do not clamp output values 1: Clamp output values. Method of clamping is dependent on blender control bits<br>0=Do NOT Clamp<br>1=Clamp  |
| T0_EQ_TCUR  | 24    | 0x0     | 0: Pass Texel 0 input of this stage to Texel 0 input of next stage 1: Replicate the output of this stage on to the Texel 0 input of the next stage(AND w/TEX_BLEND_n_ENABLE)<br>0=Pass T0 in to T0 in of next stage<br>1=Copy output to T0 in of next stage |
| T1_EQ_TCUR  | 25    | 0x0     | 0: Pass Texel 1 input of this stage to Texel 1 input of next stage 1: Replicate the output of this stage on to the Texel 1 input of the next stage(AND w/TEX_BLEND_n_ENABLE)<br>0=Pass T1 in to T1 in of next stage<br>1=Copy output to T1 in of next stage |

**PP\_TXABLEND\_0 - RW - 32 bits - [MMReg:0x1C64] [MMReg:0x2C64]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| T2_EQ_TCUR | 26   | 0x0     | 0: Pass Texel 2 input of this stage to Texel 2 input of next stage 1: Replicate the output of this stage on to the Texel 2 input of the next stage (AND w/TEX_BLEND_n_ENABLE)<br>0=Pass T2 in to T2 in of next stage<br>1=Copy output to T2 in of next stage |
| T3_EQ_TCUR | 27   | 0x0     | 0=Pass T3 in to T3 in of next stage<br>1=Copy output to T3 in of next stage  |

[ R/W ] Control for Alpha Texture Blender 0

**PP\_TXABLEND\_1 - RW - 32 bits - [MMReg:0x1C7C] [MMReg:0x2C7C]**

| Field Name  | Bits | Default | Description   |
|-------------|------|---------|---|
| ALPHA_ARG_A | 3:0  | 0x0     | 000: Zero (0.0) 001: Current Alpha (Defaults to diffuse alpha on stage 0) 010: Diffuse Alpha 011: Specular Alpha (Fog) 100: Tfactor Alpha 101: Texel 0 Alpha 110: Texel 1 Alpha 111: Texel 2 Alpha<br>0=Zero<br>1=Current Alpha<br>2=Diffuse Alpha<br>3=Specular Alpha<br>4=TFACTOR Alpha<br>5=T0 Alpha<br>6=T1 Alpha<br>7=T2 Alpha<br>8=T3 Alpha |
| ALPHA_ARG_B | 7:4  | 0x0     | Same decode as Alpha Argument A<br>0=Zero<br>1=Current Alpha<br>2=Diffuse Alpha<br>3=Specular Alpha<br>4=TFACTOR Alpha<br>5=T0 Alpha<br>6=T1 Alpha<br>7=T2 Alpha<br>8=T3 Alpha  |
| ALPHA_ARG_C | 11:8 | 0x1     | Same decode as Alpha Argument A<br>0=Zero<br>1=Current Alpha<br>2=Diffuse Alpha<br>3=Specular Alpha<br>4=TFACTOR Alpha<br>5=T0 Alpha<br>6=T1 Alpha<br>7=T2 Alpha<br>8=T3 Alpha  |
| DOT_ALPHA   | 12   | 0x0     | 0: If Color Op is DOT then replicate DOT product in alpha<br>1: Don't replicate DOT product result in alpha.<br>0=Replicate DOTPROD to Alpha<br>1=Do NOT replicate DOTPROD to Alpha   |
| COMP_ARG_A  | 15   | 0x0     | 0: Do NOT complement argument A 1: Complement argument A, (1.0 - A)<br>0=Do NOT Complement Argument A<br>1=Complement Argument A  |



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**PP\_TXABLEND\_1 - RW - 32 bits - [MMReg:0x1C7C] [MMReg:0x2C7C]**

| Field Name | Bits  | Default | Description   |
|------------|-------|---------|---|
| COMP_ARG_B | 16    | 0x0     | 0: Do NOT complement argument B 1: Complement argument B, (1.0 - B)<br>0=Do NOT Complement Argument B<br>1=Complement Argument B  |
| COMP_ARG_C | 17    | 0x0     | 0: Do NOT complement argument C 1: Complement argument C, (1.0 - C)<br>0=Do NOT Complement Argument C<br>1=Complement Argument C  |
| BLEND_CTL  | 20:18 | 0x0     | 000: ADD (A * B + C) 001: SUBTRACT (A * B - C) 010: ADDSIGNED (A * B + C - 0.5) 011: BLEND ((1 - C) * A + C * B) 1xx: RESERVED<br>0=ADD<br>1=SUBTRACT<br>2=ADDSIGNED<br>3=BLEND   |
| SCALE_TX   | 22:21 | 0x0     | 00:1x, do not scale the output of the adder 01: 2x, scale by 2 (used for ADDSIGNED2X and MODULATE2X) 10: 4x, scale by 4 (used for MODULATE4x) 11: RESERVED<br>0=Scale 1X<br>1=Scale 2X<br>2=Scale 4x<br>3=RESERVED  |
| CLAMP_TX   | 23    | 0x1     | 0: Do not clamp output values 1: Clamp output values. Method of clamping is dependent on blender control bits<br>0=Do NOT Clamp<br>1=Clamp  |
| T0_EQ_TCUR | 24    | 0x0     | 0: Pass Texel 0 input of this stage to Texel 0 input of next stage 1: Replicate the output of this stage on to the Texel 0 input of the next stage (AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T0 in to T0 in of next stage<br>1=Copy output to T0 in of next stage |
| T1_EQ_TCUR | 25    | 0x0     | 0: Pass Texel 1 input of this stage to Texel 1 input of next stage 1: Replicate the output of this stage on to the Texel 1 input of the next stage (AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T1 in to T1 in of next stage<br>1=Copy output to T1 in of next stage |
| T2_EQ_TCUR | 26    | 0x0     | 0: Pass Texel 2 input of this stage to Texel 2 input of next stage 1: Replicate the output of this stage on to the Texel 2 input of the next stage (AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T2 in to T2 in of next stage<br>1=Copy output to T2 in of next stage |
| T3_EQ_TCUR | 27    | 0x0     | 0=Pass T3 in to T3 in of next stage<br>1=Copy output to T3 in of next stage   |

[ R/W ] Control for Alpha Texture Blender 1

**PP\_TXABLEND\_2 - RW - 32 bits - [MMReg:0x1C94] [MMReg:0x2C94]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



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**PP\_TXABLEND\_2 - RW - 32 bits - [MMReg:0x1C94] [MMReg:0x2C94]**

| Field Name  | Bits  | Default | Description   |
|-------------|-------|---------|---|
| ALPHA_ARG_A | 3:0   | 0x0     | 000: Zero (0.0) 001: Current Alpha (Defaults to diffuse alpha on stage 0) 010: Diffuse Alpha 011: Specular Alpha (Fog) 100: Tfactor Alpha 101: Texel 0 Alpha 110: Texel 1 Alpha 111: Texel 2 Alpha<br>0=Zero<br>1=Current Alpha<br>2=Diffuse Alpha<br>3=Specular Alpha<br>4=TFACTOR Alpha<br>5=T0 Alpha<br>6=T1 Alpha<br>7=T2 Alpha<br>8=T3 Alpha |
| ALPHA_ARG_B | 7:4   | 0x0     | Same decode as Alpha Argument A<br>0=Zero<br>1=Current Alpha<br>2=Diffuse Alpha<br>3=Specular Alpha<br>4=TFACTOR Alpha<br>5=T0 Alpha<br>6=T1 Alpha<br>7=T2 Alpha<br>8=T3 Alpha  |
| ALPHA_ARG_C | 11:8  | 0x1     | Same decode as Alpha Argument A<br>0=Zero<br>1=Current Alpha<br>2=Diffuse Alpha<br>3=Specular Alpha<br>4=TFACTOR Alpha<br>5=T0 Alpha<br>6=T1 Alpha<br>7=T2 Alpha<br>8=T3 Alpha  |
| DOT_ALPHA   | 12    | 0x0     | 0: If Color Op is DOT then replicate DOT product in alpha<br>1: Don't replicate DOT product result in alpha.<br>0=Replicate DOTPROD to Alpha<br>1=Do NOT replicate DOTPROD to Alpha   |
| COMP_ARG_A  | 15    | 0x0     | 0: Do NOT complement argument A 1: Complement argument A, (1.0 - A)<br>0=Do NOT Complement Argument A<br>1=Complement Argument A  |
| COMP_ARG_B  | 16    | 0x0     | 0: Do NOT complement argument B 1: Complement argument B, (1.0 - B)<br>0=Do NOT Complement Argument B<br>1=Complement Argument B  |
| COMP_ARG_C  | 17    | 0x0     | 0: Do NOT complement argument C 1: Complement argument C, (1.0 - C)<br>0=Do NOT Complement Argument C<br>1=Complement Argument C  |
| BLEND_CTL   | 20:18 | 0x0     | 000: ADD (A * B + C) 001: SUBTRACT (A * B - C) 010: ADDSIGNED (A * B + C - 0.5) 011: BLEND ((1 - C) * A + C * B) 1xx: RESERVED<br>0=ADD<br>1=SUBTRACT<br>2=ADDSIGNED<br>3=BLEND   |

**PP\_TXABLEND\_2 - RW - 32 bits - [MMReg:0x1C94] [MMReg:0x2C94]**

| Field Name | Bits  | Default | Description   |
|------------|-------|---------|---|
| SCALE_TX   | 22:21 | 0x0     | 00: 1x, do not scale the output of the adder 01: 2x, scale by 2 (used for ADDSIGNED2X and MODULATE2X) 10: 4x, scale by 4 (used for MODULATE4x) 11: RESERVED<br>0=Scale 1X<br>1=Scale 2X<br>2=Scale 4x<br>3=RESERVED   |
| CLAMP_TX   | 23    | 0x1     | 0: Do not clamp output values 1: Clamp output values. Method of clamping is dependent on blender control bits<br>0=Do NOT Clamp<br>1=Clamp  |
| T0_EQ_TCUR | 24    | 0x0     | 0: Pass Texel 0 input of this stage to Texel 0 input of next stage 1: Replicate the output of this stage on to the Texel 0 input of the next stage (AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T0 in to T0 in of next stage<br>1=Copy output to T0 in of next stage |
| T1_EQ_TCUR | 25    | 0x0     | 0: Pass Texel 1 input of this stage to Texel 1 input of next stage 1: Replicate the output of this stage on to the Texel 1 input of the next stage (AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T1 in to T1 in of next stage<br>1=Copy output to T1 in of next stage |
| T2_EQ_TCUR | 26    | 0x0     | 0: Pass Texel 2 input of this stage to Texel 2 input of next stage 1: Replicate the output of this stage on to the Texel 2 input of the next stage (AND w/ TEX_BLEND_n_ENABLE)<br>0=Pass T2 in to T2 in of next stage<br>1=Copy output to T2 in of next stage |
| T3_EQ_TCUR | 27    | 0x0     | 0=Pass T3 in to T3 in of next stage<br>1=Copy output to T3 in of next stage   |

[ R/W ] Control for Alpha Texture Blender 2

**PP\_TFACTOR\_0 - RW - 32 bits - [MMReg:0x1C68] [MMReg:0x2C68]**

| Field Name | Bits | Default | Description                         |
|------------|------|---------|-------------------------------------|
| TFACTOR    | 31:0 | none    | Tfactor color in ARGB (8888) format |

[ R/W ] Texture Scale Factor

**PP\_TFACTOR\_1 - RW - 32 bits - [MMReg:0x1C80] [MMReg:0x2C80]**

| Field Name | Bits | Default | Description                         |
|------------|------|---------|-------------------------------------|
| TFACTOR    | 31:0 | none    | Tfactor color in ARGB (8888) format |

[ R/W ] Texture Scale Factor

**PP\_TFACTOR\_2 - RW - 32 bits - [MMReg:0x1C98] [MMReg:0x2C98]**

| Field Name | Bits | Default | Description                         |
|------------|------|---------|-------------------------------------|
| TFACTOR    | 31:0 | none    | Tfactor color in ARGB (8888) format |

[ R/W ] Texture Scale Factor

**PP\_ROT\_MATRIX\_0 - RW - 32 bits - [MMReg:0x1D58] [MMReg:0x2D58]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| M00_MAN    | 10:0 | none    |             |

**PP\_ROT\_MATRIX\_0 - RW - 32 bits - [MMReg:0x1D58] [MMReg:0x2D58]**

| Field Name | Bits  | Default | Description |
|------------|-------|---------|-------------|
| M10_MAN    | 26:16 | none    |             |
| Mx0_EXPO   | 30:27 | none    |             |

No description available for this register.

**PP\_ROT\_MATRIX\_1 - RW - 32 bits - [MMReg:0x1D5C] [MMReg:0x2D5C]**

| Field Name | Bits  | Default | Description |
|------------|-------|---------|-------------|
| M01_MAN    | 10:0  | none    |             |
| M11_MAN    | 26:16 | none    |             |
| Mx1_EXPO   | 30:27 | none    |             |

No description available for this register.

**PP\_LUM\_MATRIX - RW - 32 bits - [MMReg:0x1D00] [MMReg:0x2D00]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| LSCALE     | 7:0  | none    |             |
| LOFFSET    | 15:8 | none    |             |

No description available for this register.

**PP\_FOG\_COLOR - RW - 32 bits - [MMReg:0x1C18] [MMReg:0x2C18]**

| Field Name    | Bits  | Default | Description  |
|---------------|-------|---------|--|
| FOG_COLOR     | 23:0  | none    | Fog color in RGB (888) format  |
| FOG_TABLE     | 24    | 0x0     | Use vertex fog 1: Use table fog<br>0=Use Vertex Fog<br>1=Use Fog Table   |
| FOG_INDEX_SEL | 26:25 | 0x0     | 0x:Use depth to index table fog 10: Use Diffuse Alpha to index fog table 11: Use Specular Alpha to index fog table<br>0=Use Depth<br>1=RESERVED<br>2=Use Diffuse Alpha<br>3=Use Specular Alpha |

[ R/W ] Fog Color used in the Fog blend unit

**47. Raster Engine****RE\_STIPPLE\_ADDR - RW - 32 bits - [MMReg:0x1CC8] [MMReg:0x26C8]**

| Field Name   | Bits | Default | Description   |
|--------------|------|---------|---|
| STIPPLE_ADDR | 4:0  | 0x0     | 5-bit index into the 32 x 32 RAM. It is self incrementing with every access to RE_STIPPLE_DATA. |

No description available for this register.

**RE\_STIPPLE\_DATA - RW - 32 bits - [MMReg:0x1CCC] [MMReg:0x26CC]**

| Field Name   | Bits | Default | Description                                     |
|--------------|------|---------|---|
| STIPPLE_DATA | 31:0 | none    | Row of stipple data indexed by RE_STIPPLE_ADDR. |

[ R/W] (MM: X\_XX)

**RE\_MISC - RW - 32 bits - [MMReg:0x1CC4] [MMReg:0x26C4]**

| Field Name        | Bits | Default | Description   |
|-------------------|------|---------|---|
| STIPPLE_X_OFFSET  | 4:0  | 0x0     | X offset to apply to X index of stipple RAM   |
| STIPPLE_Y_OFFSET  | 12:8 | 0x0     | Y offset to apply to Y index of stipple RAM   |
| STIPPLE_BIT_ORDER | 16   | 0x0     | 0 : Little Bit Order (x= 0 on the right of stipple data) 1 : Big Bit Order (x = 0 on the left of stipple data)<br>0=Little Bit Order<br>1=Big Bit Order |

No description available for this register.

**RE\_SOLID\_COLOR - RW - 32 bits - [MMReg:0x1C1C] [MMReg:0x261C]**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| SOLID_COLOR | 31:0 | none    | 32-bit color used for solid shading. Organized as 8: 8: 8: 8 ARGB. |

[ R/W] (MM: X\_XX)

**RE\_WIDTH\_HEIGHT - RW - 32 bits - [MMReg:0x1C44] [MMReg:0x2644]**

| Field Name | Bits  | Default | Description                       |
|------------|-------|---------|-----------------------------------|
| WIDTH      | 10:0  | 0x0     | Width-1 of primary scissor plane  |
| HEIGHT     | 26:16 | 0x0     | Height-1 of primary scissor plane |

[ R/W] (MM: X\_XX)

**RE\_TOP\_LEFT - RW - 32 bits - [MMReg:0x26C0]**

| Field Name | Bits  | Default | Description |
|------------|-------|---------|-------------|
| X_LEFT     | 10:0  | none    |             |
| Y_TOP      | 26:16 | none    |             |

No description available for this register.

**RE\_LINE\_PATTERN - RW - 32 bits - [MMReg:0x1CD0] [MMReg:0x26D0]**

| Field Name   | Bits | Default | Description                         |
|--------------|------|---------|-------------------------------------|
| LINE_PATTERN | 15:0 | none    | 0 : Don't Draw Pixel 1 : Draw Pixel |



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**RE\_LINE\_PATTERN - RW - 32 bits - [MMReg:0x1CD0] [MMReg:0x26D0]**

| Field Name        | Bits  | Default | Description   |
|-------------------|-------|---------|---|
| REPEAT_COUNT      | 23:16 | none    | 16 Pattern Repeat Count 0x00 : 256x 0x01 : 1x 0x02 : 2x : 0xFF : 255x   |
| PATTERN_START     | 27:24 | none    | Indicates starting state of pattern pointer 0x0 : Points to pattern bit 0 0x1 : Points to pattern bit 1 : 0xF : Points to pattern bit 15                                    |
| PATTERN_BIT_ORDER | 28    | 0x0     | 0 : Little Bit Order (Pointer = 0 is on the right of the pattern)<br>1 : Big Bit Order (Pointer = 0 is on the left of the pattern)<br>0=Little Bit Order<br>1=Big Bit Order |
| AUTO_RESET_ENABLE | 29    | 0x0     | 0 : Do not reset the counter and pointer at EndOfLinePattern 1 : Automatically reset the counter and pointer at EndOfLinePattern<br>0=disable<br>1=enable                   |

[ R/W] (MM: X\_XX)

**RE\_LINE\_STATE - RW - 32 bits - [MMReg:0x1CD4] [MMReg:0x26D4]**

| Field Name    | Bits | Default | Description   |
|---------------|------|---------|---|
| CURRENT_PTR   | 3:0  | none    | Indicates current state of pattern pointer (can be set w/ a register write) 0x0 : Points to pattern bit 0 0x1 : Points to pattern bit 1 : 0xF : Points to pattern bit 15 At the end of a line this value will reset to Pattern Start if EndOfPacket is set by the setup engine and AUTO_RESET_ENABLE is on. |
| CURRENT_COUNT | 15:8 | none    | Current state of the repeat counter (can be set w/ a register write). At the end of a line this value will reset to 1 if EndOfLinePattern is set by the setup engine and AUTO_RESET_ENABLE is on.   |

[ R/W] (MM: X\_XX)

**48. Miscellaneous Detailed Register Reference****F1\_VENDOR\_ID - R - 16 bits - [MMReg:0xF80] [pciConfig:0x100]**

| Field Name   | Bits | Default | Description |
|--------------|------|---------|-------------|
| F1_VENDOR_ID | 15:0 | 0x1002  |             |

No description available for this register.

**F1\_DEVICE\_ID - R - 16 bits - [MMReg:0xF82] [pciConfig:0x102]**

| Field Name   | Bits | Default | Description |
|--------------|------|---------|-------------|
| F1_DEVICE_ID | 15:0 | 0x5157  |             |

No description available for this register.

**F1\_COMMAND - RW - 16 bits - [MMReg:0xF84]:R [pciConfig:0x104]**

| Field Name         | Bits | Default | Description           |
|--------------------|------|---------|-----------------------|
| F1_IO_ACCESS_EN    | 0    | 0x0     | 0=Disable<br>1=Enable |
| F1_MEM_ACCESS_EN   | 1    | 0x0     | 0=Disable<br>1=Enable |
| F1_BUS_MASTER_EN   | 2    | 0x0     | 0=Disable<br>1=Enable |
| F1_AD_STEPPING (R) | 7    | 0x1     | 0=Disable<br>1=Enable |
| F1_FAST_B2B_EN     | 9    | 0x0     | 0=Disable<br>1=Enable |

No description available for this register.

**F1\_STATUS - R - 16 bits - [MMReg:0xF86]:R [pciConfig:0x106]**

| Field Name               | Bits | Default | Description           |
|--------------------------|------|---------|-----------------------|
| F1_CAP_LIST              | 4    | 0x1     |                       |
| F1_PCI_66_EN             | 5    | 0x1     |                       |
| F1_UDF_EN                | 6    | 0x0     | 0=Disable<br>1=Enable |
| F1_FAST_BACK_CAPABLE     | 7    | 0x1     |                       |
| F1_DEVSEL_TIMING         | 10:9 | 0x1     |                       |
| F1_SIGNAL_TARGET_ABORT   | 11   | 0x0     |                       |
| F1_RECEIVED_TARGET_ABORT | 12   | 0x0     |                       |
| F1_RECEIVED_MASTER_ABORT | 13   | 0x0     |                       |
| F1_PARITY_ERROR_DETECTED | 15   | 0x0     |                       |

No description available for this register.

**F1\_REVISION\_ID - R - 8 bits - [MMReg:0xF88] [pciConfig:0x108]**

| Field Name      | Bits | Default | Description |
|-----------------|------|---------|-------------|
| F1_MINOR_REV_ID | 3:0  | 0x0     |             |
| F1_MAJOR_REV_ID | 7:4  | 0x0     |             |

No description available for this register.

**F1\_REGPROG\_INF - R - 8 bits - [MMReg:0xF89] [pciConfig:0x109]**

| Field Name            | Bits | Default | Description |
|-----------------------|------|---------|-------------|
| F1_REG_LEVEL_PROG_INF | 7:0  | 0x0     |             |

**F1\_REGPROG\_INF - R - 8 bits - [MMReg:0xF89] [pciConfig:0x109]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

No description available for this register.

**F1\_SUB\_CLASS - R - 8 bits - [MMReg:0xF8A] [pciConfig:0x10A]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                  |   |     |   |
|------------------|---|-----|---|
| F1_SUB_CLASS_INF | 7 | 0x0 | 0=00 - VGA device<br>1=80 - extended graphics |
|------------------|---|-----|---|

No description available for this register.

**F1\_BASE\_CODE - R - 8 bits - [MMReg:0xF8B] [pciConfig:0x10B]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                    |     |     |  |
|--------------------|-----|-----|--|
| F1_BASE_CLASS_CODE | 7:0 | 0x3 |  |
|--------------------|-----|-----|--|

No description available for this register.

**F1\_CACHE\_LINE - RW - 8 bits - [MMReg:0xF8C]:R [pciConfig:0x10C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                    |     |     |  |
|--------------------|-----|-----|--|
| F1_CACHE_LINE_SIZE | 7:0 | 0x0 |  |
|--------------------|-----|-----|--|

No description available for this register.

**F1\_LATENCY - RW - 8 bits - [MMReg:0xF8D]:R [pciConfig:0x10D]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                  |     |     |  |
|------------------|-----|-----|--|
| F1_LATENCY_TIMER | 7:0 | 0x0 |  |
|------------------|-----|-----|--|

No description available for this register.

**F1\_HEADER - R - 8 bits - [MMReg:0xF8E] [pciConfig:0x10E]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                |     |     |   |
|----------------|-----|-----|---|
| F1_HEADER_TYPE | 6:0 | 0x0 |   |
| F1_DEVICE_TYPE | 7   | 0x0 | 0=Single-Function Device<br>1=Multi-Function Device |

No description available for this register.

**F1\_BIST - R - 8 bits - [MMReg:0xF8F] [pciConfig:0x10F]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|              |     |     |  |
|--------------|-----|-----|--|
| F1_BIST_COMP | 3:0 | 0x0 |  |
|--------------|-----|-----|--|

|              |   |     |  |
|--------------|---|-----|--|
| F1_BIST_STRT | 6 | 0x0 |  |
|--------------|---|-----|--|

|             |   |     |  |
|-------------|---|-----|--|
| F1_BIST_CAP | 7 | 0x0 |  |
|-------------|---|-----|--|

No description available for this register.

**F1\_MEM\_BASE - RW - 32 bits - [MMReg:0xF90]:R [pciConfig:0x110]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|                    |   |     |  |
|--------------------|---|-----|--|
| F1_PREFETCH_EN (R) | 3 | 0x1 |  |
|--------------------|---|-----|--|

|             |       |     |  |
|-------------|-------|-----|--|
| F1_MEM_BASE | 31:25 | 0x0 |  |
|-------------|-------|-----|--|

No description available for this register.

**F1\_REG\_BASE - RW - 32 bits - [MMReg:0xF94]:R [pciConfig:0x114]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

|             |       |     |  |
|-------------|-------|-----|--|
| F1_REG_BASE | 31:16 | 0x0 |  |
|-------------|-------|-----|--|

No description available for this register.

**F1\_ADAPTER\_ID - R - 32 bits - [MMReg:0xFAC] [pciConfig:0x12C]**

| Field Name  | Bits  | Default | Description |
|---|-------|---------|-------------|
| F1_SUBSYSTEM_VENDOR_ID                                  | 15:0  | 0x0     |             |
| <i>(mirror of<br/>ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)</i> |       |         |             |
| F1_SUBSYSTEM_ID   | 31:16 | 0x0     |             |

No description available for this register.

**F1\_CAPABILITIES\_PTR - R - 32 bits - [MMReg:0xFB4] [pciConfig:0x134]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| F1_CAP_PTR | 7:0  | 0x50    |             |

No description available for this register.

**F1\_INTERRUPT\_LINE - RW - 8 bits - [MMReg:0xFBC]:R [pciConfig:0x13C]**

| Field Name        | Bits | Default | Description |
|-------------------|------|---------|-------------|
| F1_INTERRUPT_LINE | 7:0  | 0xff    |             |

No description available for this register.

**F1\_INTERRUPT\_PIN - R - 8 bits - [MMReg:0xFBD] [pciConfig:0x13D]**

| Field Name       | Bits | Default | Description |
|------------------|------|---------|-------------|
| F1_INTERRUPT_PIN | 0    | 0x0     |             |

No description available for this register.

**F1\_MIN\_GRANT - R - 8 bits - [MMReg:0xFBE] [pciConfig:0x13E]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| F1_MIN_GNT | 7:0  | 0x8     |             |

No description available for this register.

**F1\_MAX\_LATENCY - R - 8 bits - [MMReg:0xFBF] [pciConfig:0x13F]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| F1_MAX_LAT | 7:0  | 0x0     |             |

No description available for this register.

**F1\_PMI\_CAP\_ID - R - 8 bits - [MMReg:0xFD0] [pciConfig:0x150]**

| Field Name    | Bits | Default | Description   |
|---------------|------|---------|---|
| F1_PMI_CAP_ID | 7:0  | 0x1     | 1=PCI Bus Power Management Interface (PMI) register section |

No description available for this register.

**F1\_PMI\_NXT\_CAP\_PTR - R - 8 bits - [MMReg:0xFD1] [pciConfig:0x151]**

| Field Name         | Bits | Default | Description |
|--------------------|------|---------|-------------|
| F1_PMI_NXT_CAP_PTR | 7:0  | 0x0     |             |

No description available for this register.

**F1\_PMI\_PMC\_REG - R - 16 bits - [MMReg:0xFD2] [pciConfig:0x152]**

| Field Name               | Bits | Default | Description                                    |
|--------------------------|------|---------|--|
| F1_PMI_VERSION           | 2:0  | 0x2     | 2=Compliant with PMI Specification version 1.1 |
| F1_PMI_PME_CLOCK         | 3    | 0x0     |  |
| F1_PMI_DEV_SPECIFIC_INIT | 5    | 0x0     |  |

**F1\_PMI\_PMC\_REG - R - 16 bits - [MMReg:0xFD2] [pciConfig:0x152]**

| Field Name         | Bits  | Default | Description |
|--------------------|-------|---------|-------------|
| F1_PMI_D1_SUPPORT  | 9     | 0x1     |             |
| F1_PMI_D2_SUPPORT  | 10    | 0x1     |             |
| F1_PMI_PME_SUPPORT | 15:11 | 0x0     |             |

No description available for this register.

**F1\_PM\_STATUS - RW - 16 bits - [MMReg:0xFD4]:R [pciConfig:0x154]**

| Field Name             | Bits  | Default | Description |
|------------------------|-------|---------|-------------|
| F1_PMI_POWER_STATE     | 1:0   | 0x0     |             |
| F1_PMI_PME_EN (R)      | 8     | 0x0     |             |
| F1_PMI_DATA_SELECT (R) | 12:9  | 0x0     |             |
| F1_PMI_DATA_SCALE (R)  | 14:13 | 0x0     |             |
| F1_PMI_PME_STATUS (R)  | 15    | 0x0     |             |

No description available for this register.

**F1\_PMI\_DATA - R - 8 bits - [MMReg:0xFD7] [pciConfig:0x157]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| F1_PMI_DATA | 7:0  | 0x0     |             |

No description available for this register.

**F1\_AGP\_CAP\_ID - R - 32 bits - [MMReg:0xFD8] [pciConfig:0x158]**

| Field Name   | Bits  | Default | Description |
|--------------|-------|---------|-------------|
| F1_CAP_ID    | 7:0   | 0x2     |             |
| F1_NEXT_PTR  | 15:8  | 0x50    |             |
| F1_AGP_MINOR | 19:16 | 0x0     |             |
| F1_AGP_MAJOR | 23:20 | 0x2     |             |

No description available for this register.

**F1\_AGP\_STATUS - R - 32 bits - [MMReg:0xFDC] [pciConfig:0x15C]**

| Field Name | Bits  | Default | Description |
|------------|-------|---------|-------------|
| F1_RATE1X  | 0     | 0x1     |             |
| F1_RATE2X  | 1     | 0x1     |             |
| F1_RATE4X  | 2     | 0x1     |             |
| F1_SBA     | 9     | 0x1     |             |
| F1_RQ      | 31:24 | 0x2f    |             |

No description available for this register.

**F1\_AGP\_COMMAND - RW - 32 bits - [MMReg:0xFE0]:R [pciConfig:0x160]**

| Field Name    | Bits  | Default | Description           |
|---------------|-------|---------|-----------------------|
| F1_DATA_RATE  | 2:0   | 0x0     |                       |
| F1_AGP_EN     | 8     | 0x0     | 0=disable<br>1=enable |
| F1_SBA_EN (R) | 9     | 0x1     | 0=Disable<br>1=Enable |
| F1_RQ_DEPTH   | 31:24 | 0x0     |                       |

No description available for this register.

**MEM\_TIMING\_CNTL - RW - 32 bits - [MMReg:0x144]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|



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**MEM\_TIMING\_CNTL - RW - 32 bits - [MMReg:0x144]**

| Field Name | Bits  | Default | Description  |
|------------|-------|---------|--|
| MEM_TRCD   | 2:0   | 0x0     | 0=1 clock<br>1=2 clocks<br>2=3 clocks<br>3=4 clocks<br>4=5 clocks<br>5=6 clocks<br>6=7 clocks<br>7=8 clocks  |
| MEM_TRCDW  | 6:4   | 0x0     | 0=1 clock<br>1=2 clocks<br>2=3 clocks<br>3=4 clocks<br>4=5 clocks<br>5=6 clocks<br>6=7 clocks<br>7=8 clocks  |
| MEM_TRP    | 10:8  | 0x0     | 0=1 clock<br>1=2 clocks<br>2=3 clocks<br>3=4 clocks<br>4=5 clocks<br>5=6 clocks<br>6=7 clocks<br>7=8 clocks  |
| MEM_TRAS   | 15:12 | 0x0     | 0=4 clocks<br>1=5 clocks<br>2=6 clocks<br>3=7 clocks<br>4=8 clocks<br>5=9 clocks<br>6=10 clocks<br>7=11 clocks<br>8=12 clocks<br>9=13 clocks<br>10=14 clocks<br>11=15 clocks<br>12=16 clocks<br>13=17 clocks<br>14=18 clocks<br>15=19 clocks |
| MEM_TRRD   | 17:16 | 0x0     | 0=1 clock<br>1=2 clocks<br>2=3 clocks<br>3=4 clocks  |
| MEM_TR2W   | 19:18 | 0x0     | 0=CL+1 clock<br>1=CL+2 clocks<br>2=CL+3 clocks<br>3=CL+4 clocks  |
| MEM_TWR    | 22:20 | 0x0     | 0=1 clock<br>1=2 clocks<br>2=3 clocks<br>3=4 clocks<br>4=5 clocks<br>5=6 clocks<br>6=7 clocks<br>7=8 clocks  |

**MEM\_TIMING\_CNTL - RW - 32 bits - [MMReg:0x144]**

| Field Name         | Bits  | Default | Description   |
|--------------------|-------|---------|---|
| MEM_TW2R           | 26:24 | 0x0     | 0=1 clock<br>1=2 clocks<br>2=3 clocks<br>3=4 clocks<br>4=5 clocks<br>5=6 clocks<br>6=7 clocks<br>7=8 clocks |
| MEM_TW2R_SAME_BANK | 27    | 0x0     | 0=Use TW2R Rule<br>1=Use TWR Rule   |
| MEM_TR2R           | 29:28 | 0x0     | 0=1 clock<br>1=2 clocks<br>2=3 clocks<br>3=4 clocks   |

No description available for this register.

**MEM\_REFRESH\_CNTL - RW - 32 bits - [MMReg:0x178]**

| Field Name        | Bits  | Default | Description  |
|-------------------|-------|---------|--|
| MEM_REFRESH_RATE  | 7:0   | 0x0     |  |
| MEM_REFRESH_DIS   | 8     | 0x0     | 0=Not Disabled<br>1=Disabled   |
| MEM_DYNAMIC_CKE   | 9     | 0x0     | 0=Disable<br>1=Enable  |
| MEM_TRFC          | 15:12 | 0x0     | 0=8 clocks<br>1=9 clocks<br>2=10 clocks<br>3=11 clocks<br>4=12 clocks<br>5=13 clocks<br>6=14 clocks<br>7=15 clocks<br>8=16 clocks<br>9=17 clocks<br>10=18 clocks<br>11=19 clocks<br>12=20 clocks<br>13=21 clocks<br>14=22 clocks<br>15=23 clocks |
| MEM_CLKA0_ENABLE  | 16    | 0x1     | 0=Not Enabled<br>1=Enabled   |
| MEM_CLKA0b_ENABLE | 17    | 0x1     | 0=Not Enabled<br>1=Enabled   |
| MEM_CLKA1_ENABLE  | 18    | 0x1     | 0=Not Enabled<br>1=Enabled   |
| MEM_CLKA1b_ENABLE | 19    | 0x1     | 0=Not Enabled<br>1=Enabled   |
| MEM_CLKAFB_ENABLE | 20    | 0x0     | 0=Not Enabled<br>1=Enabled   |
| DLL_FB_SLCT_CKA   | 23:22 | 0x0     |  |

**MEM\_REFRESH\_CNTL - RW - 32 bits - [MMReg:0x178]**

| Field Name        | Bits  | Default | Description                |
|-------------------|-------|---------|----------------------------|
| MEM_CLKB0_ENABLE  | 24    | 0x1     | 0=Not Enabled<br>1=Enabled |
| MEM_CLKB0b_ENABLE | 25    | 0x1     | 0=Not Enabled<br>1=Enabled |
| MEM_CLKB1_ENABLE  | 26    | 0x1     | 0=Not Enabled<br>1=Enabled |
| MEM_CLKB1b_ENABLE | 27    | 0x1     | 0=Not Enabled<br>1=Enabled |
| MEM_CLKBFB_ENABLE | 28    | 0x0     | 0=Not Enabled<br>1=Enabled |
| DLL_FB_SLCT_CKB   | 31:30 | 0x0     |                            |

No description available for this register.

**AGP\_BASE - RW - 32 bits - [MMReg:0x170]**

| Field Name    | Bits | Default | Description  |
|---------------|------|---------|--|
| AGP_BASE_ADDR | 31:0 | 0x0     | NOTE: Bits 0:21 of this field are hardwired to ZERO. |

No description available for this register.

**MEM\_READ\_CNTL - RW - 32 bits - [MMReg:0x17C]**

| Field Name           | Bits | Default | Description   |
|----------------------|------|---------|---|
| MEM_RBS_POSITION_A   | 2:0  | 0x0     | 0=CL + 0 clocks<br>1=CL + 0.5 clocks<br>2=CL + 1 clocks<br>3=CL + 1.5 clocks<br>4=CL + 2 clocks<br>5=CL + 2.5 clocks<br>6=CL + 3 clocks<br>7=CL + 3.5 clocks                                    |
| MEM_STR_SEL_A        | 3    | 0x1     | 0=Directly from QS pin<br>1=From DLL input  |
| MEM_ERST_POSITION_A  | 6:4  | 0x0     | 0=CL - 2 clocks<br>1=CL - 1.5 clocks<br>2=CL - 1 clocks<br>3=CL - 0.5 clocks<br>4=CL + 0 clocks<br>5=CL + 0.5 clocks<br>6=Always on after first idle or refresh<br>7=Reset when idle or refresh |
| MEM_ERST_EXTEND_A    | 7    | 0x0     | 0=Do not extend ERST<br>1=Extend ERST 1 clock   |
| MEM_QSREC_POSITION_A | 10:8 | 0x0     | 0=CL - 2 clocks<br>1=CL - 1.5 clocks<br>2=CL - 1 clocks<br>3=CL - 0.5 clocks<br>4=CL + 0 clocks<br>5=CL + 0.5 clocks<br>7=Always Enabled  |
| MEM_QSREC_EXTEND_A   | 11   | 0x0     | 0=Do not extend QSREC<br>1=Extend QSREC 1 clock   |

**MEM\_READ\_CNTL - RW - 32 bits - [MMReg:0x17C]**

| Field Name           | Bits  | Default | Description   |
|----------------------|-------|---------|---|
| MEM_ERST_SYNC_A      | 12    | 0x0     | 0=MCLK controlled ERST<br>1=HCLK synchronized ERST  |
| MEM_QSREC_SYNC_A     | 13    | 0x0     | 0=MCLK controlled QSREC<br>1=HCLK synchronized QSREC  |
| MEM_READ_STR_FALL_A  | 14    | 0x0     | 0=Use strobe rising edge for SDR read<br>1=Use strobe falling edge for SDR read   |
| MEM_RBS_POSITION_B   | 18:16 | 0x0     | 0=CL + 0 clocks<br>1=CL + 0.5 clocks<br>2=CL + 1 clocks<br>3=CL + 1.5 clocks<br>4=CL + 2 clocks<br>5=CL + 2.5 clocks<br>6=CL + 3 clocks<br>7=CL + 3.5 clocks                                    |
| MEM_STR_SEL_B        | 19    | 0x1     | 0=Directly from QS pin<br>1=From DLL input  |
| MEM_ERST_POSITION_B  | 22:20 | 0x0     | 0=CL - 2 clocks<br>1=CL - 1.5 clocks<br>2=CL - 1 clocks<br>3=CL - 0.5 clocks<br>4=CL + 0 clocks<br>5=CL + 0.5 clocks<br>6=Always on after first idle or refresh<br>7=Reset when idle or refresh |
| MEM_ERST_EXTEND_B    | 23    | 0x0     | 0=Do not extend ERST<br>1=Extend ERST 1 clock   |
| MEM_QSREC_POSITION_B | 26:24 | 0x0     | 0=CL - 2 clocks<br>1=CL - 1.5 clocks<br>2=CL - 1 clocks<br>3=CL - 0.5 clocks<br>4=CL + 0 clocks<br>5=CL + 0.5 clocks<br>7=Always Enabled  |
| MEM_QSREC_EXTEND_B   | 27    | 0x0     | 0=Do not extend QSREC<br>1=Extend QSREC 1 clock   |
| MEM_ERST_SYNC_B      | 28    | 0x0     | 0=MCLK controlled ERST<br>1=HCLK synchronized ERST  |
| MEM_QSREC_SYNC_B     | 29    | 0x0     | 0=MCLK controlled QSREC<br>1=HCLK synchronized QSREC  |
| MEM_READ_STR_FALL_B  | 30    | 0x0     | 0=Use strobe rising edge for SDR read<br>1=Use strobe falling edge for SDR read   |

No description available for this register.

**MC\_STATUS - R - 32 bits - [MMReg:0x150]**

| Field Name        | Bits | Default | Description                        |
|-------------------|------|---------|------------------------------------|
| MEM_PWRUP_COMPL_A | 0    | 0x0     | 0=SDRAM Init in Process<br>1=Ready |

**MC\_STATUS - R - 32 bits - [MMReg:0x150]**

| Field Name            | Bits  | Default | Description                        |
|-----------------------|-------|---------|------------------------------------|
| MEM_PWRUP_COMPL_B     | 1     | 0x0     | 0=SDRAM Init in Process<br>1=Ready |
| MC_IDLE               | 2     | 0x0     | 0=Not Idle<br>1=Idle               |
| IMP_N_VALUE_R_BACK    | 6:3   | 0x0     |                                    |
| IMP_P_VALUE_R_BACK    | 10:7  | 0x0     |                                    |
| TEST_OUT_R_BACK       | 11    | 0x0     |                                    |
| DUMMY_OUT_R_BACK      | 12    | 0x0     |                                    |
| IMP_N_VALUE_A_R_BACK  | 16:13 | 0x0     |                                    |
| IMP_P_VALUE_A_R_BACK  | 20:17 | 0x0     |                                    |
| IMP_N_VALUE_CK_R_BACK | 24:21 | 0x0     |                                    |
| IMP_P_VALUE_CK_R_BACK | 28:25 | 0x0     |                                    |

No description available for this register.

**MC\_CHP\_IO\_OE\_CNTL - RW - 32 bits - [MMReg:0x18C]**

| Field Name         | Bits  | Default | Description  |
|--------------------|-------|---------|--|
| DQ_OE_POSITION_A   | 1:0   | 0x0     | 0=WL - 1 clocks<br>1=WL - 0.5 clocks<br>2=WL + 0 clocks<br>3=WL + 0.5 clocks                     |
| QS_OE_POSITION_A   | 3:2   | 0x0     | 0=WL - 1 clocks<br>1=WL - 0.5 clocks<br>2=WL + 0 clocks<br>3=WL + 0.5 clocks                     |
| DQ_OE_EXTEND_A     | 4     | 0x0     | 0=0 clocks<br>1=1 clock  |
| QS_OE_EXTEND_A     | 5     | 0x0     | 0=0 clocks<br>1=1 clock  |
| DQ_OE_ADVANCE_A    | 6     | 0x0     | 0=DQ OE as specified<br>1=DQ OE 1 clock earlier for WL 1 clock and more                          |
| QS_OE_ADVANCE_A    | 7     | 0x0     | 0=QS OE as specified<br>1=QS OE 1 clock earlier for WL 1 clock and more                          |
| DQS_DRIVER_SLCT_A0 | 8     | 0x0     | 0=Not On QS0_7<br>1=On QS0_7   |
| DQS_DRIVER_SLCT_A1 | 9     | 0x0     | 0=Not On QS1_6<br>1=On QS1_6   |
| DQS_DRIVER_SLCT_A2 | 10    | 0x0     | 0=Not On QS2_5<br>1=On QS2_5   |
| DQS_DRIVER_SLCT_A3 | 11    | 0x0     | 0=Not On QS3_4<br>1=On QS3_4   |
| MEM_SDR_STROBE_A   | 13:12 | 0x0     | 0=SDR no strobe<br>1=SDR free running strobe<br>2=SDR read strobe<br>3=SDR read and write strobe |
| DQ_OE_POSITION_B   | 17:16 | 0x0     | 0=WL - 1 clocks<br>1=WL - 0.5 clocks<br>2=WL + 0 clocks<br>3=WL + 0.5 clocks                     |

**MC\_CHP\_IO\_OE\_CNTL - RW - 32 bits - [MMReg:0x18C]**

| Field Name          | Bits  | Default | Description  |
|---------------------|-------|---------|--|
| QS_OE_POSITION_B    | 19:18 | 0x0     | 0=WL - 1 clocks<br>1=WL - 0.5 clocks<br>2=WL + 0 clocks<br>3=WL + 0.5 clocks                     |
| DQ_OE_EXTEND_B      | 20    | 0x0     | 0=0 clocks<br>1=1 clock  |
| QS_OE_EXTEND_B      | 21    | 0x0     | 0=0 clocks<br>1=1 clock  |
| DQ_OE_ADVANCE_B     | 22    | 0x0     | 0=DQ OE as specified<br>1=DQ OE 1 clock earlier for WL 1 clock and more                          |
| QS_OE_ADVANCE_B     | 23    | 0x0     | 0=QS OE as specified<br>1=QS OE 1 clock earlier for WL 1 clock and more                          |
| DQS_DRIVER_SLCT_B0  | 24    | 0x0     | 0=Not On QS0_7<br>1=On QS0_7   |
| DQS_DRIVER_SLCT_B1  | 25    | 0x0     | 0=Not On QS1_6<br>1=On QS1_6   |
| DQS_DRIVER_SLCT_B2  | 26    | 0x0     | 0=Not On QS2_5<br>1=On QS2_5   |
| DQS_DRIVER_SLCT_B3  | 27    | 0x0     | 0=Not On QS3_4<br>1=On QS3_4   |
| MEM_SDR_STROBE_B    | 29:28 | 0x0     | 0=SDR no strobe<br>1=SDR free running strobe<br>2=SDR read strobe<br>3=SDR read and write strobe |
| MEM_PM_SDRAM_TRI_EN | 30    | 0x0     | 0=Not Allowed<br>1=Allowed   |
| MEM_IO_TRISTATE     | 31    | 0x0     | 0=Normal<br>1=Tristate   |

No description available for this register.

**AGP\_BASE\_2 - RW - 32 bits - [MMReg:0x15C]**

| Field Name      | Bits | Default | Description |
|-----------------|------|---------|-------------|
| AGP_BASE_ADDR_2 | 3:0  | 0x0     |             |

No description available for this register.

**MC\_IND\_INDEX - RW - 32 bits - [MMReg:0x1F8]**

| Field Name   | Bits | Default | Description   |
|--------------|------|---------|---|
| MC_IND_ADDR  | 4:0  | 0x0     |   |
| MC_IND_WR_EN | 8    | 0x0     | 0=Disable write capability (read only)<br>1=Enable write capability |

No description available for this register.

**MC\_IND\_DATA - RW - 32 bits - [MMReg:0x1FC]**

| Field Name  | Bits | Default | Description |
|-------------|------|---------|-------------|
| MC_IND_DATA | 31:0 | 0x0     |             |

No description available for this register.

**MC\_IMP\_CNTL - RW - 32 bits - MCIND:0xA**

| Field Name                 | Bits  | Default | Description |
|----------------------------|-------|---------|-------------|
| MEM_IO_UPDATE_RATE         | 4:0   | 0x16    |             |
| MEM_IO_SAMPLE_DELAY        | 9:5   | 0x6     |             |
| MEM_IO_INC_THRESHOLD       | 14:10 | 0x18    |             |
| MEM_IO_DEC_THRESHOLD       | 19:15 | 0x8     |             |
| MEM_IO_MANUAL_OVERRIDE_CK  | 20    | 0x1     |             |
| MEM_IO_MANUAL_OVERRIDE_A   | 21    | 0x1     |             |
| MEM_IO_MANUAL_OVERRIDE_DQM | 22    | 0x1     |             |
| MEM_IO_MANUAL_OVERRIDE_DQS | 23    | 0x1     |             |
| MEM_IO_SLEWN               | 24    | 0x0     |             |
| MEM_IO_SLEWP               | 25    | 0x0     |             |

No description available for this register.

**MC\_CHP\_IO\_CNTL\_A0 - RW - 32 bits - MCIND:0xB**

| Field Name | Bits  | Default | Description |
|------------|-------|---------|-------------|
| MEM_N_CKA  | 3:0   | 0xf     |             |
| MEM_N_AA   | 7:4   | 0xf     |             |
| MEM_N_DQMA | 11:8  | 0x0     |             |
| MEM_N_DQSA | 15:12 | 0x0     |             |
| MEM_P_CKA  | 19:16 | 0xf     |             |
| MEM_P_AA   | 23:20 | 0xf     |             |
| MEM_P_DQMA | 27:24 | 0x0     |             |
| MEM_P_DQSA | 31:28 | 0x0     |             |

No description available for this register.

**MC\_CHP\_IO\_CNTL\_A1 - RW - 32 bits - MCIND:0xC**

| Field Name      | Bits | Default | Description                |
|-----------------|------|---------|----------------------------|
| MEM_SLEWN_CKA   | 0    | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_SLEWN_AA    | 1    | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_SLEWN_DQMA  | 2    | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_SLEWN_DQSA  | 3    | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_SLEWP_CKA   | 4    | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_SLEWP_AA    | 5    | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_SLEWP_DQMA  | 6    | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_SLEWP_DQSA  | 7    | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_PREAMP_AA   | 8    | 0x0     | 0=Not Enabled<br>1=Enabled |
| MEM_PREAMP_DQMA | 9    | 0x0     | 0=Not Enabled<br>1=Enabled |



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**MC\_CHP\_IO\_CNTL\_A1 - RW - 32 bits - MCIND:0xC**

| Field Name       | Bits  | Default | Description  |
|------------------|-------|---------|--|
| MEM_PREAMP_DQSA  | 10    | 0x0     | 0=Not Enabled<br>1=Enabled   |
| MEM_IO_MODEA     | 13:12 | 0x0     | 0=LVTTL Interface<br>1=SSTL Interface<br>2=NDR Interface   |
| MEM_REC_CKA      | 15:14 | 0x0     | 0=Schmitt Trigger<br>1=Differential Receiver<br>2=NDR Receiver   |
| MEM_REC_AA       | 17:16 | 0x0     | 0=Schmitt Trigger<br>1=Differential Receiver<br>2=NDR Receiver   |
| MEM_REC_DQMA     | 19:18 | 0x0     | 0=Schmitt Trigger<br>1=Differential Receiver<br>2=NDR Receiver   |
| MEM_REC_DQSA     | 21:20 | 0x0     | 0=Schmitt Trigger<br>1=Differential Receiver<br>2=NDR Receiver   |
| MEM_SYNC_PHASEA  | 22    | 0x0     | 0=Nominal, theoretically correct<br>1=What if theory is not correct???   |
| MEM_SYNC_CENTERA | 23    | 0x0     | 0=Sync 2 YCLK hold margin<br>1=Sync 1 YCLK setup/hold margin   |
| MEM_SYNC_ENA     | 25:24 | 0x1     | 0=MCLK/YCLK Sync Disabled<br>1=MCLK/YCLK Sync Manual<br>2=MCLK/YCLK Sync Automatic during refresh<br>3=RFU   |
| MEM_CLK_SELA     | 27:26 | 0x0     | 0=Memory clock from DLL, through or bypass<br>1=Memory clock from YCLK/2 rise<br>2=Memory clock from YCLK/2 fall, 1/4 clock delay<br>3=Memory clock in test mode |
| MEM_CLK_INVA     | 28    | 0x0     | 0=Memory clock from YCLK/2, nominal<br>1=Memory clock from YCLK/2, inverted, 1/2 clock delay   |
| MEM_DATA_ENIMP_A | 30    | 0x0     | 0=Disable data/mask impedance controller<br>1=Enable data/mask impedance controller  |
| MEM_CNTL_ENIMP_A | 31    | 0x0     | 0=Disable cntl/addr impedance controller<br>1=Enable cntl/addr impedance controller  |

No description available for this register.

**MC\_CHP\_IO\_CNTL\_B0 - RW - 32 bits - MCIND:0xD**

| Field Name | Bits  | Default | Description |
|------------|-------|---------|-------------|
| MEM_N_CKB  | 3:0   | 0xf     |             |
| MEM_N_AB   | 7:4   | 0xf     |             |
| MEM_N_DQMB | 11:8  | 0x0     |             |
| MEM_N_DQSB | 15:12 | 0x0     |             |
| MEM_P_CKB  | 19:16 | 0xf     |             |
| MEM_P_AB   | 23:20 | 0xf     |             |
| MEM_P_DQMB | 27:24 | 0x0     |             |
| MEM_P_DQSB | 31:28 | 0x0     |             |

No description available for this register.



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**MC\_CHP\_IO\_CNTL\_B1 - RW - 32 bits - MCIND:0xE**

| Field Name       | Bits  | Default | Description  |
|------------------|-------|---------|--|
| MEM_SLEWN_CKB    | 0     | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_SLEWN_AB     | 1     | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_SLEWN_DQMB   | 2     | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_SLEWN_DQSB   | 3     | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_SLEWP_CKB    | 4     | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_SLEWP_AB     | 5     | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_SLEWP_DQMB   | 6     | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_SLEWP_DQSB   | 7     | 0x0     | 0=Low Slew<br>1=High Slew  |
| MEM_PREAMP_AB    | 8     | 0x0     | 0=Not Enabled<br>1=Enabled   |
| MEM_PREAMP_DQMB  | 9     | 0x0     | 0=Not Enabled<br>1=Enabled   |
| MEM_PREAMP_DQSB  | 10    | 0x0     | 0=Not Enabled<br>1=Enabled   |
| MEM_IO_MODEB     | 13:12 | 0x0     | 0=LVTTTL Interface<br>1=SSTL Interface<br>2=NDR Interface              |
| MEM_REC_CKB      | 15:14 | 0x0     | 0=Schmitt Trigger<br>1=Differential Receiver<br>2=NDR Receiver         |
| MEM_REC_AB       | 17:16 | 0x0     | 0=Schmitt Trigger<br>1=Differential Receiver<br>2=NDR Receiver         |
| MEM_REC_DQMB     | 19:18 | 0x0     | 0=Schmitt Trigger<br>1=Differential Receiver<br>2=NDR Receiver         |
| MEM_REC_DQSB     | 21:20 | 0x0     | 0=Schmitt Trigger<br>1=Differential Receiver<br>2=NDR Receiver         |
| MEM_SYNC_PHASEB  | 22    | 0x0     | 0=Nominal, theoretically correct<br>1=What if theory is not correct??? |
| MEM_SYNC_CENTERB | 23    | 0x0     | 0=Sync 2 YCLK hold margin<br>1=Sync 1 YCLK setup/hold margin           |

**MC\_CHP\_IO\_CNTL\_B1 - RW - 32 bits - MCIND:0xE**

| Field Name       | Bits  | Default | Description  |
|------------------|-------|---------|--|
| MEM_SYNC_ENB     | 25:24 | 0x1     | 0=MCLK/YCLK Sync Disabled<br>1=MCLK/YCLK Sync Manual<br>2=MCLK/YCLK Sync Automatic during refresh<br>3=RFU   |
| MEM_CLK_SELB     | 27:26 | 0x0     | 0=Memory clock from DLL, through or bypass<br>1=Memory clock from YCLK/2 rise<br>2=Memory clock from YCLK/2 fall, 1/4 clock delay<br>3=Memory clock in test mode |
| MEM_CLK_INVB     | 28    | 0x0     | 0=Memory clock from YCLK/2, nominal<br>1=Memory clock from YCLK/2, inverted, 1/2 clock delay   |
| MEM_DATA_ENIMP_B | 30    | 0x0     | 0=Disable data/mask impedance controller<br>1=Enable data/mask impedance controller  |
| MEM_CNTL_ENIMP_B | 31    | 0x0     | 0=Disable cntl/addr impedance controller<br>1=Enable cntl/addr impedance controller  |

No description available for this register.

**MC\_IMP\_CNTL\_0 - RW - 32 bits - MCIND:0xF**

| Field Name     | Bits  | Default | Description |
|----------------|-------|---------|-------------|
| MEM_STEP_N_A   | 1:0   | 0x1     |             |
| MEM_STEP_N_CK  | 4:3   | 0x1     |             |
| MEM_STEP_N_DQS | 7:6   | 0x1     |             |
| MEM_STEP_P_A   | 10:9  | 0x1     |             |
| MEM_STEP_P_CK  | 13:12 | 0x1     |             |
| MEM_STEP_P_DQS | 16:15 | 0x1     |             |

No description available for this register.

**TC\_MISMATCH\_1 - R - 32 bits - MCIND:0x10**

| Field Name    | Bits | Default | Description |
|---------------|------|---------|-------------|
| TC_MISMATCH_1 | 31:0 | 0x0     |             |

No description available for this register.

**TC\_MISMATCH\_2 - R - 32 bits - MCIND:0x11**

| Field Name    | Bits | Default | Description |
|---------------|------|---------|-------------|
| TC_MISMATCH_2 | 31:0 | 0x0     |             |

No description available for this register.

**MC\_BIST\_CTRL - RW - 32 bits - MCIND:0x12**

| Field Name   | Bits | Default | Description |
|--------------|------|---------|-------------|
| MC_BIST_CTRL | 31:0 | 0x0     |             |

No description available for this register.

**REG\_COLLAR\_WRITE - RW - 32 bits - MCIND:0x13**

| Field Name       | Bits | Default | Description |
|------------------|------|---------|-------------|
| REG_COLLAR_WRITE | 31:0 | 0x0     |             |

No description available for this register.

**REG\_COLLAR\_READ - RW - 32 bits - MCIND:0x14**

| Field Name      | Bits | Default | Description |
|-----------------|------|---------|-------------|
| REG_COLLAR_READ | 31:0 | 0x0     |             |

**REG\_COLLAR\_READ - RW - 32 bits - MCIND:0x14****Field Name****Bits****Default****Description**

No description available for this register.

**DST\_OFFSET - RW - 32 bits - [MMReg:0x1404]****Field Name****Bits****Default****Description**

DST\_OFFSET

31:0

0x0

Destination Offset in Units of 1KB, 0 to (4GB-1KB). When a write to this register occurs, bits 9: 0 of destination offset will be set to 0.

NOTE: Bits 0:3 of this field are hardwired to ZERO.

Destination Offset in Units of 1KB, 0 to (4GB-1KB). When a write to this register occurs, bits 9: 0 of destination offset will be set to 0.

**DST\_PITCH - RW - 32 bits - [MMReg:0x1408]****Field Name****Bits****Default****Description**

DST\_PITCH

13:0

0x0

Pitch in units of 64 bytes, 0 to 16320 bytes across. DST\_TILE 31: 30 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) 2: microtiled 3: tiled and microtiled Write bits 31: 30 to E2\_DST\_TILE, 29: 22 to E2\_DST\_PITCH and 21: 0 to E2\_DST\_OFFSET

NOTE: Bits 0:3 of this field are hardwired to ZERO.

Pitch in units of 64 bytes, 0 to 16320 bytes across. DST\_TILE 31: 30 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) 2: microtiled 3: tiled and microtiled Write bits 31: 30 to E2\_DST\_TILE, 29: 22 to E2\_DST\_PITCH and 21: 0 to E2\_DST\_OFFSET

**DST\_TILE - RW - 32 bits - [MMReg:0x1700]****Field Name****Bits****Default****Description**

DST\_TILE

1:0

none

0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) 2: microtiled 3: tiled and microtiled Write 9: 0 to E2\_DST\_TILE DST\_PITCH\_OFFSET[ W/R]

**DST\_PITCH\_OFFSET - W - 32 bits - [MMReg:0x142C]****Field Name****Bits****Default****Description**

DST\_OFFSET

21:0

none

Destination Offset in Units of 1KB, 0 to (4GB-1KB). When a write to this register occurs, bits 9: 0 of destination offset will be set to 0.

*(mirror bits 10:31 of DST\_OFFSET:DST\_OFFSET)*

DST\_PITCH

29:22

none

Pitch in units of 64 bytes, 0 to 16320 bytes across. DST\_TILE 31: 30 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) 2: microtiled 3: tiled and microtiled Write bits 31: 30 to E2\_DST\_TILE, 29: 22 to E2\_DST\_PITCH and 21: 0 to E2\_DST\_OFFSET

*(mirror bits 6:13 of DST\_PITCH:DST\_PITCH)*

DST\_TILE

31:30

none

0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) 2: microtiled 3: tiled and microtiled Write 9: 0 to E2\_DST\_TILE DST\_PITCH\_OFFSET[ W/R]

*(mirror of DST\_TILE:DST\_TILE)*

No description available for this register.

**DST\_X - RW - 32 bits - [MMReg:0x141C]****Field Name****Bits****Default****Description**

DST\_X

13:0

none

Destination X

Destination X

**DST\_Y - RW - 32 bits - [MMReg:0x1420]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---------------|
| DST_Y      | 13:0 | none    | Destination Y |

Destination Y

**DST\_X\_Y - W - 32 bits - [MMReg:0x1594]**

| Field Name                     | Bits  | Default | Description   |
|--------------------------------|-------|---------|---------------|
| DST_Y                          | 13:0  | none    | Destination Y |
| <i>(mirror of DST_Y:DST_Y)</i> |       |         |               |
| DST_X                          | 29:16 | none    | Destination X |
| <i>(mirror of DST_X:DST_X)</i> |       |         |               |

No description available for this register.

**DST\_Y\_X - W - 32 bits - [MMReg:0x1438]**

| Field Name                     | Bits  | Default | Description   |
|--------------------------------|-------|---------|---------------|
| DST_X                          | 13:0  | none    | Destination X |
| <i>(mirror of DST_X:DST_X)</i> |       |         |               |
| DST_Y                          | 29:16 | none    | Destination Y |
| <i>(mirror of DST_Y:DST_Y)</i> |       |         |               |

No description available for this register.

**DST\_WIDTH - RW - 32 bits - [MMReg:0x140C]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| DST_WIDTH  | 13:0 | none    | Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete |

Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2\_DST\_X, Write 31: 16 to E2\_DST\_WIDTH, then signal blit\_start. E2\_DST\_Y = E2\_DEST\_Y (+/-) E2\_DST\_HEIGHT as function of direction after blit is complete

**DST\_HEIGHT - RW - 32 bits - [MMReg:0x1410]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| DST_HEIGHT | 13:0 | none    | Destination Height Write 15: 0 to E2_DST_Y, Write 31: 16 to E2_DST_HEIGHT |

Destination Height Write 15: 0 to E2\_DST\_Y, Write 31: 16 to E2\_DST\_HEIGHT

**DST\_WIDTH\_HEIGHT - W - 32 bits - [MMReg:0x1598]**

| Field Name                               | Bits  | Default | Description   |
|--|-------|---------|---|
| DST_HEIGHT                               | 13:0  | none    | Destination Height Write 15: 0 to E2_DST_Y, Write 31: 16 to E2_DST_HEIGHT   |
| <i>(mirror of DST_HEIGHT:DST_HEIGHT)</i> |       |         |   |
| DST_WIDTH                                | 29:16 | none    | Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete |
| <i>(mirror of DST_WIDTH:DST_WIDTH)</i>   |       |         |   |

Destination Width and Height

**DST\_HEIGHT\_WIDTH - W - 32 bits - [MMReg:0x143C]**

| Field Name   | Bits  | Default | Description   |
|--|-------|---------|---|
| DST_WIDTH<br><i>(mirror of DST_WIDTH:DST_WIDTH)</i>    | 13:0  | none    | Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete |
| DST_HEIGHT<br><i>(mirror of DST_HEIGHT:DST_HEIGHT)</i> | 29:16 | none    | Destination Height Write 15: 0 to E2_DST_Y, Write 31: 16 to E2_DST_HEIGHT   |

[ W ] Destination Height and Width

**DST\_HEIGHT\_WIDTH\_8 - W - 32 bits - [MMReg:0x158C]**

| Field Name  | Bits  | Default | Description   |
|---|-------|---------|---|
| DST_WIDTH<br><i>(mirror bits 0:7 of DST_WIDTH:DST_WIDTH)</i>    | 23:16 | none    | Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete |
| DST_HEIGHT<br><i>(mirror bits 0:7 of DST_HEIGHT:DST_HEIGHT)</i> | 31:24 | none    | Destination Height Write 15: 0 to E2_DST_Y, Write 31: 16 to E2_DST_HEIGHT   |

[ W ] (Reserved) 15: 0 DST\_WIDTH 23: 16 Destination width: range 0 to 256 (ZERO extent)

**DST\_HEIGHT\_Y - W - 32 bits - [MMReg:0x15A0]**

| Field Name   | Bits  | Default | Description   |
|--|-------|---------|---|
| DST_Y<br><i>(mirror of DST_Y:DST_Y)</i>                | 13:0  | none    | Destination Y   |
| DST_HEIGHT<br><i>(mirror of DST_HEIGHT:DST_HEIGHT)</i> | 29:16 | none    | Destination Height Write 15: 0 to E2_DST_Y, Write 31: 16 to E2_DST_HEIGHT |

No description available for this register.

**DST\_WIDTH\_X - W - 32 bits - [MMReg:0x1588]**

| Field Name  | Bits  | Default | Description   |
|---|-------|---------|---|
| DST_X<br><i>(mirror of DST_X:DST_X)</i>             | 13:0  | none    | Destination X   |
| DST_WIDTH<br><i>(mirror of DST_WIDTH:DST_WIDTH)</i> | 29:16 | none    | Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete |

[ W ] Destination X and Width coordinate

**DST\_WIDTH\_X\_INCY - W - 32 bits - [MMReg:0x159C]**

| Field Name                              | Bits | Default | Description   |
|---|------|---------|---------------|
| DST_X<br><i>(mirror of DST_X:DST_X)</i> | 13:0 | none    | Destination X |

**DST\_WIDTH\_X\_INCY - W - 32 bits - [MMReg:0x159C]**

| Field Name  | Bits  | Default | Description   |
|---|-------|---------|---|
| DST_WIDTH<br><i>(mirror of DST_WIDTH:DST_WIDTH)</i> | 29:16 | none    | Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete |

[ W ] Destination Width and X coordinate

**DST\_LINE\_START - RW - 32 bits - [MMReg:0x1600]**

| Field Name  | Bits  | Default | Description  |
|-------------|-------|---------|--|
| DST_START_X | 13:0  | none    | Start X  |
| DST_START_Y | 29:16 | none    | Start Y Write 13: 0 to E2_LINE_START_X; Write 29: 16 to E2_LINE_START_Y; Write 0 to E2_LINE_PATCOUNT |

No description available for this register.

**DST\_LINE\_END - RW - 32 bits - [MMReg:0x1604]**

| Field Name | Bits  | Default | Description  |
|------------|-------|---------|--|
| DST_END_X  | 13:0  | none    | End X  |
| DST_END_Y  | 29:16 | none    | End Y Write 15: 0 to E2_LINE_END_X; Write 31: 16 to E2_LINE_END_Y; signal line_start; then copy E2_LINE_END_X into E2_LINE_START_X and E2_LINE_END_Y into E2_LINE_START_Y. |

No description available for this register.

**DST\_LINE\_PATCOUNT - RW - 32 bits - [MMReg:0x1608]**

| Field Name    | Bits | Default | Description   |
|---------------|------|---------|---|
| LINE_PATCOUNT | 4:0  | none    | Line pattern counter Write 4: 0 to E2_LINE_PATCOUNT. When DST_LINE_START register is written into the line pattern counter is reset to 0. If a non-zero starting value is desired, this register must be written in after writing to DST_LINE_START register. BRUSH_Y_X [ W/R] (MM: 5_1D) |
| BRES_CNTL     | 15:8 | none    |   |

No description available for this register.

**DP\_DST\_ENDIAN - W - 32 bits - [MMReg:0x15D0]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| DST_ENDIAN | 1:0  | none    | 0=no swap<br>1=16 bit swap<br>2=32 bit swap<br>3=half dword swap |

00 = No swap (the default after reset, for all the endian converters) 01 = 16bit swap: 0xAABBCCDD becomes 0xBBAADDCC  
10 = 32bit swap: 0xAABBCCDD becomes 0xDDCCBBAA 11 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB  
Write to E2\_DP\_DST\_ENDIAN

**BRUSH\_Y\_X - RW - 32 bits - [MMReg:0x1474]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| BRUSH_X    | 2:0  | none    | and BRUSH_Y to E2_BAGU_X and E2_BAGU_Y<br>BRUSH_DATA [ 63: 0] [ R/W] (MM: 5_20 - 5_5F) |

**BRUSH\_Y\_X - RW - 32 bits - [MMReg:0x1474]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_Y    | 10:8 | none    |             |

No description available for this register.

**BRUSH\_DATA0 - W - 32 bits - [MMReg:0x1480]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA1 - W - 32 bits - [MMReg:0x1484]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA2 - W - 32 bits - [MMReg:0x1488]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA3 - W - 32 bits - [MMReg:0x148C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA4 - W - 32 bits - [MMReg:0x1490]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA5 - W - 32 bits - [MMReg:0x1494]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA6 - W - 32 bits - [MMReg:0x1498]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA7 - W - 32 bits - [MMReg:0x149C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA8 - W - 32 bits - [MMReg:0x14A0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA9 - W - 32 bits - [MMReg:0x14A4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA10 - W - 32 bits - [MMReg:0x14A8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA11 - W - 32 bits - [MMReg:0x14AC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA12 - W - 32 bits - [MMReg:0x14B0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA13 - W - 32 bits - [MMReg:0x14B4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA14 - W - 32 bits - [MMReg:0x14B8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA15 - W - 32 bits - [MMReg:0x14BC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA16 - W - 32 bits - [MMReg:0x14C0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA17 - W - 32 bits - [MMReg:0x14C4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA18 - W - 32 bits - [MMReg:0x14C8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA19 - W - 32 bits - [MMReg:0x14CC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA20 - W - 32 bits - [MMReg:0x14D0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA21 - W - 32 bits - [MMReg:0x14D4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA22 - W - 32 bits - [MMReg:0x14D8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA23 - W - 32 bits - [MMReg:0x14DC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA24 - W - 32 bits - [MMReg:0x14E0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA25 - W - 32 bits - [MMReg:0x14E4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA26 - W - 32 bits - [MMReg:0x14E8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA27 - W - 32 bits - [MMReg:0x14EC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA28 - W - 32 bits - [MMReg:0x14F0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA29 - W - 32 bits - [MMReg:0x14F4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA30 - W - 32 bits - [MMReg:0x14F8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA31 - W - 32 bits - [MMReg:0x14FC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA32 - W - 32 bits - [MMReg:0x1500]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA33 - W - 32 bits - [MMReg:0x1504]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA34 - W - 32 bits - [MMReg:0x1508]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA35 - W - 32 bits - [MMReg:0x150C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA36 - W - 32 bits - [MMReg:0x1510]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA37 - W - 32 bits - [MMReg:0x1514]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA38 - W - 32 bits - [MMReg:0x1518]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA39 - W - 32 bits - [MMReg:0x151C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA40 - W - 32 bits - [MMReg:0x1520]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA41 - W - 32 bits - [MMReg:0x1524]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA42 - W - 32 bits - [MMReg:0x1528]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA43 - W - 32 bits - [MMReg:0x152C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA44 - W - 32 bits - [MMReg:0x1530]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA45 - W - 32 bits - [MMReg:0x1534]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA46 - W - 32 bits - [MMReg:0x1538]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA47 - W - 32 bits - [MMReg:0x153C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA48 - W - 32 bits - [MMReg:0x1540]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA49 - W - 32 bits - [MMReg:0x1544]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA50 - W - 32 bits - [MMReg:0x1548]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA51 - W - 32 bits - [MMReg:0x154C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA52 - W - 32 bits - [MMReg:0x1550]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA53 - W - 32 bits - [MMReg:0x1554]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA54 - W - 32 bits - [MMReg:0x1558]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA55 - W - 32 bits - [MMReg:0x155C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA56 - W - 32 bits - [MMReg:0x1560]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA57 - W - 32 bits - [MMReg:0x1564]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA58 - W - 32 bits - [MMReg:0x1568]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA59 - W - 32 bits - [MMReg:0x156C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA60 - W - 32 bits - [MMReg:0x1570]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA61 - W - 32 bits - [MMReg:0x1574]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA62 - W - 32 bits - [MMReg:0x1578]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**BRUSH\_DATA63 - W - 32 bits - [MMReg:0x157C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| BRUSH_DATA | 31:0 | none    |             |

No description available for this register.

**DP\_BRUSH\_FRGD\_CLR - RW - 32 bits - [MMReg:0x147C]**

| Field Name        | Bits | Default | Description   |
|-------------------|------|---------|---|
| DP_BRUSH_FRGD_CLR | 31:0 | none    | Foreground color. Write to RB2D_BRUSHDATA[ 2] DP_BRUSH_BKGD_CLR [ R/W] (MM: 5_1E) |

No description available for this register.

**DP\_BRUSH\_BKGD\_CLR - RW - 32 bits - [MMReg:0x1478]**

| Field Name        | Bits | Default | Description   |
|-------------------|------|---------|---|
| DP_BRUSH_BKGD_CLR | 31:0 | none    | Background color Write to RB2D_BRUSHDATA[ 3] SRC_OFFSET[ W/R] Source Offset |

Background color Write to RB2D\_BRUSHDATA[ 3] SRC\_OFFSET[ W/R] Source Offset

**SRC\_OFFSET - RW - 32 bits - [MMReg:0x15AC]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| SRC_OFFSET | 31:0 | 0x0     | Source Offset in Units of 1KB, 0 to (4GB-1KB). When a write to this register occurs, bits 9: 0 of source offset will be set to 0.<br><br>NOTE: Bits 0:3 of this field are hardwired to ZERO. |

Source Offset in Units of 1KB, 0 to (4GB-1KB). When a write to this register occurs, bits 9: 0 of source offset will be set to 0.

**SRC\_PITCH - RW - 32 bits - [MMReg:0x15B0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**SRC\_PITCH - RW - 32 bits - [MMReg:0x15B0]**

| Field Name | Bits | Default | Description   |
|------------|------|---------|---|
| SRC_PITCH  | 13:0 | 0x0     | Pitch in units of 64 bytes, 0 to 16320 bytes across. SRC_TILE 30 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) Write bit 30 to E2_SRC_TILE, 29: 22 to E2_SRC_PITCH and 21: 0 to E2_SRC_OFFSET<br><br>NOTE: Bits 0:3 of this field are hardwired to ZERO. |

Pitch in units of 64 bytes, 0 to 16320 bytes across. SRC\_TILE 30 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) Write bit 30 to E2\_SRC\_TILE, 29: 22 to E2\_SRC\_PITCH and 21: 0 to E2\_SRC\_OFFSET

**SRC\_TILE - RW - 32 bits - [MMReg:0x1704]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| SRC_TILE   | 0    | none    | 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) Write 0 to E2_SRC_TILE SRC_PITCH_OFFSET[ W/R] |

0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) Write 0 to E2\_SRC\_TILE SRC\_PITCH\_OFFSET[ W/R]

**SRC\_PITCH\_OFFSET - W - 32 bits - [MMReg:0x1428]**

| Field Name  | Bits  | Default | Description  |
|---|-------|---------|--|
| SRC_OFFSET<br><i>(mirror bits 10:31 of SRC_OFFSET:SRC_OFFSET)</i> | 21:0  | none    | Source Offset in Units of 1KB, 0 to (4GB-1KB). When a write to this register occurs, bits 9: 0 of source offset will be set to 0.  |
| SRC_PITCH<br><i>(mirror bits 6:13 of SRC_PITCH:SRC_PITCH)</i>     | 29:22 | none    | Pitch in units of 64 bytes, 0 to 16320 bytes across. SRC_TILE 30 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) Write bit 30 to E2_SRC_TILE, 29: 22 to E2_SRC_PITCH and 21: 0 to E2_SRC_OFFSET |
| SRC_TILE<br><i>(mirror of SRC_TILE:SRC_TILE)</i>                  | 30    | none    | 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) Write 0 to E2_SRC_TILE SRC_PITCH_OFFSET[ W/R]   |

No description available for this register.

**SRC\_X - RW - 32 bits - [MMReg:0x1414]**

| Field Name | Bits | Default | Description                              |
|------------|------|---------|--|
| SRC_X      | 13:0 | none    | Source X coordinate: range -8192 to 8191 |

Source X coordinate: range -8192 to 8191

**SRC\_Y - RW - 32 bits - [MMReg:0x1418]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| SRC_Y      | 13:0 | none    | Source Y coordinate: range -8192 to 8191 Write 13: 0 to E2_SRC_X, Write 29: 16 to E2_SRC_Y |

Source Y coordinate: range -8192 to 8191 Write 13: 0 to E2\_SRC\_X, Write 29: 16 to E2\_SRC\_Y

**SRC\_X\_Y - W - 32 bits - [MMReg:0x1590]**

| Field Name                              | Bits | Default | Description  |
|---|------|---------|--|
| SRC_Y<br><i>(mirror of SRC_Y:SRC_Y)</i> | 13:0 | none    | Source Y coordinate: range -8192 to 8191 Write 13: 0 to E2_SRC_X, Write 29: 16 to E2_SRC_Y |

**SRC\_X\_Y - W - 32 bits - [MMReg:0x1590]**

| Field Name | Bits  | Default | Description                                    |
|------------|-------|---------|--|
| SRC_X      | 29:16 | none    | 13: 0 Source X coordinate: range -8192 to 8191 |

*(mirror of SRC\_X:SRC\_X)*

(aliased to SRC\_X, SRC\_Y) [ W ] (MM: 5\_64)

**SRC\_Y\_X - W - 32 bits - [MMReg:0x1434]**

| Field Name | Bits  | Default | Description  |
|------------|-------|---------|--|
| SRC_X      | 13:0  | none    | Source X coordinate: range -8192 to 8191   |
| SRC_Y      | 29:16 | none    | Source Y coordinate: range -8192 to 8191 Write 13: 0 to E2_SRC_X, Write 29: 16 to E2_SRC_Y |

*(mirror of SRC\_X:SRC\_X)*

*(mirror of SRC\_Y:SRC\_Y)*

(aliased to SRC\_X, SRC\_Y) [ W ] (MM: 5\_0D)

**SRC\_CLUT\_ADDRESS - RW - 32 bits - [MMReg:0x1780]**

| Field Name       | Bits | Default | Description            |
|------------------|------|---------|------------------------|
| SRC_CLUT_ADDRESS | 7:0  | none    | to E2_SRC_CLUT_ADDRESS |

to E2\_SRC\_CLUT\_ADDRESS

**SRC\_CLUT\_DATA - W - 32 bits - [MMReg:0x1784]**

| Field Name    | Bits | Default | Description     |
|---------------|------|---------|-----------------|
| SRC_CLUT_DATA | 31:0 | none    | CLUT data. Read |

CLUT data. Read

**SRC\_CLUT\_DATA\_RD - R - 32 bits - [MMReg:0x1788]**

| Field Name    | Bits | Default | Description     |
|---------------|------|---------|-----------------|
| SRC_CLUT_DATA | 31:0 | none    | CLUT data. Read |

No description available for this register.

**HOST\_DATA0 - RW - 32 bits - [MMReg:0x17C0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| HOST_DATA  | 31:0 | none    |             |

No description available for this register.

**HOST\_DATA1 - W - 32 bits - [MMReg:0x17C4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| HOST_DATA  | 31:0 | none    |             |

*(mirror of HOST\_DATA0:HOST\_DATA)*

No description available for this register.

**HOST\_DATA2 - W - 32 bits - [MMReg:0x17C8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| HOST_DATA  | 31:0 | none    |             |

*(mirror of HOST\_DATA0:HOST\_DATA)*

No description available for this register.

**HOST\_DATA3 - W - 32 bits - [MMReg:0x17CC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| HOST_DATA  | 31:0 | none    |             |

*(mirror of HOST\_DATA0:HOST\_DATA)*

No description available for this register.

**HOST\_DATA4 - W - 32 bits - [MMReg:0x17D0]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| HOST_DATA  | 31:0 | none    |             |

*(mirror of HOST\_DATA0:HOST\_DATA)*

No description available for this register.

**HOST\_DATA5 - W - 32 bits - [MMReg:0x17D4]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| HOST_DATA  | 31:0 | none    |             |

*(mirror of HOST\_DATA0:HOST\_DATA)*

No description available for this register.

**HOST\_DATA6 - W - 32 bits - [MMReg:0x17D8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| HOST_DATA  | 31:0 | none    |             |

*(mirror of HOST\_DATA0:HOST\_DATA)*

No description available for this register.

**HOST\_DATA7 - W - 32 bits - [MMReg:0x17DC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| HOST_DATA  | 31:0 | none    |             |

*(mirror of HOST\_DATA0:HOST\_DATA)*

No description available for this register.

**HOST\_DATA\_LAST - W - 32 bits - [MMReg:0x17E0]**

| Field Name     | Bits | Default | Description   |
|----------------|------|---------|---|
| HOST_DATA_LAST | 31:0 | none    | Host Data Last. This register is here for R128 compatibility. Write to E2_HOST_DATA |

*(mirror of HOST\_DATA0:HOST\_DATA)*

No description available for this register.

**DP\_SRC\_ENDIAN - W - 32 bits - [MMReg:0x15D4]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| SRC_ENDIAN | 1:0  | none    | 0=no swap<br>1=16 bit swap<br>2=32 bit swap<br>3=half dword swap |

00 = No swap (the default after reset, for all the endian converters) 01 = 16bit swap: 0xAABBCCDD becomes 0xBBAADDCC

10 = 32bit swap: 0xAABBCCDD becomes 0xDDCCBBAA 11 = Half-dword swap: 0xAABBCCDD becomes 0xCCDDAABB

Write to E2\_DP\_SRC\_ENDIAN

**DP\_SRC\_FRGD\_CLR - RW - 32 bits - [MMReg:0x15D8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

**DP\_SRC\_FRGD\_CLR - RW - 32 bits - [MMReg:0x15D8]**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| DP_SRC_FRGD_CLR | 31:0 | none    | Foreground color. When color compare src eq flip is enabled, a '1' in bit location n means enable flipping on bit n. Write to E2_SRC_FRGD_CLR, And write to RB2D_CLRCMP_FLIPE |

No description available for this register.

**DP\_SRC\_BKGD\_CLR - RW - 32 bits - [MMReg:0x15DC]**

| Field Name      | Bits | Default | Description                                |
|-----------------|------|---------|--|
| DP_SRC_BKGD_CLR | 31:0 | none    | Background color. Write to E2_SRC_BKGD_CLR |

Background color. Write to E2\_SRC\_BKGD\_CLR

**SC\_LEFT - RW - 32 bits - [MMReg:0x1640]**

| Field Name | Bits | Default | Description          |
|------------|------|---------|----------------------|
| SC_LEFT    | 13:0 | none    | Range -8192 to 8191. |

Range -8192 to 8191.

**SC\_RIGHT - RW - 32 bits - [MMReg:0x1644]**

| Field Name | Bits | Default | Description          |
|------------|------|---------|----------------------|
| SC_RIGHT   | 13:0 | none    | Range -8192 to 8191. |

Range -8192 to 8191.

**SC\_TOP - RW - 32 bits - [MMReg:0x1648]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| SC_TOP     | 13:0 | none    | Range -8192 to 8191. (Reserved) Write 23: 16 to E2_DST_SCISSOR_TOP, Write 13: 0 to E2_DST_SCISSOR_LEFT |

Range -8192 to 8191. (Reserved) Write 23: 16 to E2\_DST\_SCISSOR\_TOP, Write 13: 0 to E2\_DST\_SCISSOR\_LEFT

**SC\_BOTTOM - RW - 32 bits - [MMReg:0x164C]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| SC_BOTTOM  | 13:0 | none    | Range -8192 to 8191. (Reserved) Write 23: 16 to E2_SRC_SCISSOR_BOTTOM, Write 13: 0 to E2_SRC_SCISSOR_RIGHT |

Range -8192 to 8191. (Reserved) Write 23: 16 to E2\_SRC\_SCISSOR\_BOTTOM, Write 13: 0 to E2\_SRC\_SCISSOR\_RIGHT

**SRC\_SC\_RIGHT - RW - 32 bits - [MMReg:0x1654]**

| Field Name | Bits | Default | Description          |
|------------|------|---------|----------------------|
| SC_RIGHT   | 13:0 | none    | Range -8192 to 8191. |

[ R/W ] (MM: 5\_95)

**SRC\_SC\_BOTTOM - RW - 32 bits - [MMReg:0x165C]**

| Field Name | Bits | Default | Description  |
|------------|------|---------|--|
| SC_BOTTOM  | 13:0 | none    | Range -8192 to 8191. (Reserved) Write 23: 16 to E2_SRC_SCISSOR_BOTTOM, Write 13: 0 to E2_SRC_SCISSOR_RIGHT |

**SRC\_SC\_BOTTOM - RW - 32 bits - [MMReg:0x165C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

[ R/W ] (MM: 5\_97)

**DP\_CNTL - RW - 32 bits - [MMReg:0x16C0]**

| Field Name  | Bits | Default | Description   |
|---|------|---------|---|
| DST_X_DIR<br><br><i>(mirror of<br/>DP_CNTL_XDIR_YDIR_YMAJOR:DST_X_DIR<br/>)</i> | 0    | none    | Destination X0 direction 0 = right to left 1 = left to right<br>Reserved (Must be unused ---. Used by parser to set only xdir/ydir of blits) Write 31 to E2_CNTL_DIRECTION bit 1, Write bit 15 to E2_CNTL_DIRECTION bit 0<br>0=right to left<br>1=left to right   |
| DST_Y_DIR<br><br><i>(mirror of<br/>DP_CNTL_XDIR_YDIR_YMAJOR:DST_Y_DIR<br/>)</i> | 1    | none    | 1 Destination Y direction 0 = bottom to top 1 = top to bottom This bit is written during setup engine initiated operations. Note that this bit is assumed to be '1' for all triangles. This bit is set to '1' by a GUI_MASTER_CNTL write DST_TILE 4: 3 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) 3: tiled and microtiled Write 0: 1 to E2_CNTL_DIRECTION and 4: 3 to E2_DST_TILE<br>0=bottom to top<br>1=top to bottom |
| DST_TILE<br><br><i>(mirror of DST_TILE:DST_TILE)</i>                            | 4:3  | none    |   |

[ R/W ] (MM: 5\_B0)

**DP\_CNTL\_XDIR\_YDIR\_YMAJOR - W - 32 bits - [MMReg:0x16D0]**

| Field Name | Bits | Default | Description                        |
|------------|------|---------|------------------------------------|
| DST_Y_DIR  | 15   | none    | 0=bottom to top<br>1=top to bottom |
| DST_X_DIR  | 31   | none    | 0=right to left<br>1=left to right |

No description available for this register.

**DP\_DATATYPE - RW - 32 bits - [MMReg:0x16C4]**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| DP_DST_DATATYPE | 3:0  | none    | in DP_DATATYPE<br>0=RESERVED<br>1=RESERVED<br>2=8 bpp pseudocolor<br>3=16 bpp aRGB 1555<br>4=16 bpp RGB 565<br>5=RESERVED<br>6=32 aRGB 8888 |

**DP\_DATATYPE - RW - 32 bits - [MMReg:0x16C4]**

| Field Name        | Bits  | Default | Description   |
|-------------------|-------|---------|---|
| DP_BRUSH_DATATYPE | 11:8  | none    | 0=8X8 mono pattern (expanded to frgd, bkgd)<br>1=8X8 mono pattern (expanded to frgd, leave_alone)<br>2=RESERVED<br>3=RESERVED<br>4=RESERVED<br>5=RESERVED<br>6=32X1 mono pattern for lines (expanded to frgd, bkgd)<br>7=32X1 mono pattern for lines (expanded to frgd,leave_alone)<br>8=RESERVED<br>9=RESERVED<br>10=8X8 color (pixel type same as DST)<br>11=RESERVED<br>12=RESERVED<br>13=solid color for blits (use frgd)<br>14=solid color for lines (use frgd)<br>15=solid color for blits (use frgd) |
| DP_SRC_DATATYPE   | 18:16 | none    | 0=mono (expanded to frgd, bkgd)<br>1=mono (expanded to frgd, leave_alone)<br>2=RESERVED<br>3=color (pixel type same as DST)=3<br>4=RESERVED<br>5=8bpp, use clut to translate<br>6=32bpp, use clut to translate<br>7=Obuffer(64 bit in, 32 bit out)  |
| DP_BYTE_PIX_ORDER | 30    | none    | 0=pixel order from MSBit to LSBit<br>1=pixel order from LSBit to MSBit  |

[ R/W] (MM: 5\_B1)

**DP\_MIX - RW - 32 bits - [MMReg:0x16C8]**

| Field Name    | Bits  | Default | Description   |
|---------------|-------|---------|---|
| DP_SRC_SOURCE | 10:8  | none    | 2=loaded from memory (rectangular trajectory)<br>3=loaded thru hostdata (linear trajectory)<br>4=loaded thru hosdata (linear trajectory & byte-aligned) |
| DP_ROP3       | 23:16 | none    | Windows 3.1 ROP3 code. Ternary Raster Operations<br>0=ROP3 function   |

[ R/W] (MM: 5\_B2) (Reserved) 7: 0 DP\_SRC\_SOURCE 10: 8 Src source: 2 = loaded from memory (rectangular trajectory) 3 = loaded thru hostdata (linear trajectory) 4 = loaded thru hostdata (linear trajectory & byte-aligned) Note that during 3D/Scaler Operations (whenever SCALE\_3D\_FCN is non-zero) the DP\_SRC\_SOURCE field is ignored and data is always loaded from the 3D/Scaler pipeline

**DP\_WRITE\_MSK - W - 32 bits - [MMReg:0x16CC]**

| Field Name   | Bits | Default | Description                        |
|--------------|------|---------|------------------------------------|
| DP_WRITE_MSK | 31:0 | none    | Write mask Write to RB2D_WRITEMASK |

Write mask Write to RB2D\_WRITEMASK

**DP\_XOP - W - 32 bits - [MMReg:0x17F8]**

| Field Name | Bits | Default | Description                       |
|------------|------|---------|-----------------------------------|
| XOP_A      | 7:0  | none    | Depends on XOP selected by XOP_OP |
| XOP_B      | 15:8 | none    | Depends on XOP selected by XOP_OP |



**DP\_XOP - W - 32 bits - [MMReg:0x17F8]**

| Field Name | Bits  | Default | Description   |
|------------|-------|---------|---|
| XOP_C      | 23:16 | none    | Depends on XOP selected by XOP_OP   |
| XOP_OP     | 25:24 | none    | Extended operations code, overrides ROP 0 - Normal 1 - D3D/OpenGL blend 2 - Alpha blend (32-bit only) (Reserved) 31: 26 Write to RB2D_XOP |

[ R/W ] (MM: 0x0244)

**CLR\_CMP\_CLR\_SRC - W - 32 bits - [MMReg:0x15C4]**

| Field Name      | Bits | Default | Description   |
|-----------------|------|---------|---|
| CLR_CMP_CLR_SRC | 31:0 | none    | Color comparison color of source Write to RB2D_CLRCMP_CLR_SRC |

Color comparison color of source Write to RB2D\_CLRCMP\_CLR\_SRC

**CLR\_CMP\_CLR\_DST - W - 32 bits - [MMReg:0x15C8]**

| Field Name      | Bits | Default | Description  |
|-----------------|------|---------|--|
| CLR_CMP_CLR_DST | 31:0 | none    | Color comparison color of destination Write to RB2D_CLRCMP_CLR_DST |

Color comparison color of destination Write to RB2D\_CLRCMP\_CLR\_DST

**CLR\_CMP\_CNTL - W - 32 bits - [MMReg:0x15C0]**

| Field Name      | Bits  | Default | Description   |
|-----------------|-------|---------|---|
| CLR_CMP_FCN_SRC | 2:0   | none    | Color comparison function (Mnemonic, action): 0 = False (CMP_FALSE, always draw) 1 = True (CMP_TRUE, never draw) 2-3 = (reserved) 4 = SRC_CLR != CLR_CMP_CLR_SRC (CMP_EQ_COLOR, draw when eq) 5 = SRC_CLR = CLR_CMP_CLR_SRC (CMP_NEQ_COLOR, draw when neq) 6 = (reserved) 7 = SRC_CLR = CLR_CMP_CLR_SRC (CMP_EQ_FLIP, flip using expanded SRC_FRGD_CLR as flip mask when eq) (Reserved) 7: 3 CLR_CMP_FCN_DST 10: 8 Color comparison function (Mnemonic, action): 0 = False (CMP_FALSE, always draw) 1 = True (CMP_TRUE, never draw) 2-3 = (reserved) 4 = DST_CLR != CLR_CMP_CLR_DST (CMP_NEQ_COLOR, draw when eq) 5 = DST_CLR = CLR_CMP_CLR_DST (CMP_EQ_COLOR, draw when neq) 6-7 = (reserved) (Reserved) 23: 11 CLR_CMP_SRC 25: 24 Defines source for color keying: 0 = Destination 1 = Source 2 = Src and Dst 3 = reserved (Reserved) 31: 26 Write to RB2D_CLRCMP_CNTL<br>0=False (always draw)<br>1=True (never draw)<br>4=SRC_CLR !=CLR_CMP_CLR_SRC (draw on eq)<br>5=SRC_CLR = CLR_CMP_CLR_SRC (draw on neq)<br>7=SRC_CLR = CLR_CMP_CLR_SRC (flip on eq) |
| CLR_CMP_FCN_DST | 10:8  | none    | 0=False (always draw)<br>1=True (never draw)<br>4=DST_CLR !=CLR_CMP_CLR_DST (draw on eq)<br>5=DST_CLR = CLR_CMP_CLR_DST (draw on neq)   |
| CLR_CMP_SRC     | 25:24 | none    | 0=Destination<br>1=Source<br>2=Src and Dst  |

[ R/W ] (MM: 5\_70)

**CLR\_CMP\_MSK - W - 32 bits - [MMReg:0x15CC]**

| Field Name  | Bits | Default | Description  |
|-------------|------|---------|--|
| CLR_CMP_MSK | 31:0 | none    | Color comparison color Write to RB2D_CLRCMP_MSK<br>DEFAULT_PITCH_OFFSET[W/R] |

No description available for this register.

**DSTCACHE\_MODE - W - 32 bits - [MMReg:0x1710]**

| Field Name    | Bits | Default | Description |
|---------------|------|---------|-------------|
| DSTCACHE_MODE | 31:0 | none    |             |

No description available for this register.

**DSTCACHE\_CTLSTAT - W - 32 bits - [MMReg:0x1714]**

| Field Name       | Bits | Default | Description |
|------------------|------|---------|-------------|
| DSTCACHE_CTLSTAT | 31:0 | none    |             |

No description available for this register.

**PD2\_DATA - W - 32 bits - [MMReg:0x1718]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| PD2_DATA   | 31:0 | none    |             |

No description available for this register.

**DEFAULT\_PITCH\_OFFSET - RW - 32 bits - [MMReg:0x16E0]**

| Field Name     | Bits  | Default | Description  |
|----------------|-------|---------|--|
| DEFAULT_OFFSET | 21:0  | none    | Default Offset in Units of 1KB, 0 to (4GB-1KB). When a write to this register occurs, bits 9: 0 of default offset will be set to 0.  |
| DEFAULT_PITCH  | 29:22 | none    | Pitch in units of 64 bytes, 0 to 16320 bytes across.<br>DEFAULT_TILE 31: 30 0: linear 1: tiled (tiled imposes additional restrictions on pitch and offset) 2: microtiled(destination only) 3: tiled and microtiled(destination only) Write bits 31: 30 to E2_DEFAULT_TILE, 29: 22 to E2_DEFAULT_PITCH and 21: 0 to E2_DEFAULT_OFFSET |
| DEFAULT_TILE   | 31:30 | none    |  |

No description available for this register.

**DEFAULT\_SC\_BOTTOM\_RIGHT - RW - 32 bits - [MMReg:0x16E8]**

| Field Name        | Bits  | Default | Description  |
|-------------------|-------|---------|--|
| DEFAULT_SC_RIGHT  | 13:0  | none    | Range -8192 to 8191.   |
| DEFAULT_SC_BOTTOM | 29:16 | none    | Range -8192 to 8191. (Reserved) 31: 10 Write 13: 0 to E2_DEFAULT_SCISSOR_RIGHT Write 29: 16 to E2_DEFAULT_SCISSOR_BOTTOM |

[ R/W] (MM: 5\_BA)

**DEFAULT2\_PITCH\_OFFSET - RW - 32 bits - [MMReg:0x16F8]**

| Field Name     | Bits  | Default | Description |
|----------------|-------|---------|-------------|
| DEFAULT_OFFSET | 21:0  | none    |             |
| DEFAULT_PITCH  | 29:22 | none    |             |
| DEFAULT_TILE   | 31:30 | none    |             |

**DEFAULT2\_PITCH\_OFFSET - RW - 32 bits - [MMReg:0x16F8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

No description available for this register.

**DEFAULT2\_SC\_BOTTOM\_RIGHT - RW - 32 bits - [MMReg:0x16DC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

DEFAULT\_SC\_RIGHT

13:0

none

DEFAULT\_SC\_BOTTOM

29:16

none

No description available for this register.

**DP\_GUI\_MASTER\_CNTL - W - 32 bits - [MMReg:0x146C]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
|------------|------|---------|-------------|

GMC\_SRC\_PITCH\_OFFSET\_CNTL

0

none

If 0: use E2\_DEFAULT\_OFFSET for source offset use E2\_DEFAULT\_PITCH for source pitch use E2\_DEFAULT\_TILE for source tiling if 1: use E2\_SRC\_OFFSET for source offset use E2\_SRC\_PITCH for source pitch use E2\_SRC\_TILE for source tiling  
0=(SRC\_OFFSET, SRC\_PITCH) = (DEFAULT\_PITCH\_OFFSET)  
1=Leave Alone

GMC\_DST\_PITCH\_OFFSET\_CNTL

1

none

If 0: use E2\_DEFAULT\_OFFSET for destination offset use E2\_DEFAULT\_PITCH for destination pitch use E2\_DEFAULT\_TILE for destination tiling if 1: use E2\_DST\_OFFSET for destination offset use E2\_DST\_PITCH for destination pitch use E2\_DST\_TILE for destination tiling GMC\_SRC\_CLIPPING If 0: use E2\_DEFAULT\_SCISSOR\_BOTTOM for source scissor bottom use E2\_DEFAULT\_SCISSOR\_RIGHT for source scissor right if 1: use E2\_SRC\_SCISSOR\_BOTTOM for source scissor bottom use E2\_SRC\_SCISSOR\_RIGHT for source scissor right  
0=(DST\_OFFSET, DST\_PITCH) = (DEFAULT\_PITCH\_OFFSET)  
1=Leave Alone

GMC\_SRC\_CLIPPING

2

none

0=(SC\_RIGHT, SC\_BOTTOM) = (DEFAULT\_SC\_BOTTOM\_RIGHT)  
1=no default

GMC\_DST\_CLIPPING

3

none

If 0: use E2\_DEFAULT\_SCISSOR\_BOTTOM for destination scissor bottom use E2\_DEFAULT\_SCISSOR\_RIGHT for destination scissor right use 0 for destination scissor top use 0 for destination scissor left if 1: use E2\_DST\_SCISSOR\_BOTTOM for destination scissor bottom use E2\_DST\_SCISSOR\_RIGHT for destination scissor right use E2\_DST\_SCISSOR\_TOP for destination scissor top use E2\_DST\_SCISSOR\_LEFT for destination scissor left GMC\_BRUSH\_DATATYPE Write to E2\_BAGU\_BRUSHTYPE  
0=(SC\_LEFT, SC\_TOP) = (0,0), (SC\_BOTTOM, SC\_RIGHT) = DEF\_SC\_BOTTOM\_RIGHT  
1=no default

**DP\_GUI\_MASTER\_CNTL - W - 32 bits - [MMReg:0x146C]**

| Field Name   | Bits  | Default | Description   |
|--|-------|---------|---|
| GMC_BRUSH_DATATYPE<br><i>(mirror of DP_DATATYPE:DP_BRUSH_DATATYPE)</i>       | 7:4   | none    | 0=8X8 mono pattern (expanded to frgd, bkgd)<br>1=8X8 mono pattern (expanded to frgd, leave_alone)<br>2=RESERVED<br>3=RESERVED<br>4=RESERVED<br>5=RESERVED<br>6=32X1 mono pattern for lines (expanded to frgd, bkgd)<br>7=32X1 mono pattern for lines (expanded to frgd,leave_alone)<br>8=RESERVED<br>9=RESERVED<br>10=8X8 color (pixel type same as DST)<br>11=RESERVED<br>12=RESERVED<br>13=solid color for blits (use frgd)<br>14=solid color for lines (use frgd)<br>15=solid color for blits (use frgd) |
| GMC_DST_DATATYPE<br><i>(mirror of DP_DATATYPE:DP_DST_DATATYPE)</i>           | 11:8  | none    | 0=RESERVED<br>1=RESERVED<br>2=8 bpp pseudocolor<br>3=16 bpp aRGB 1555<br>4=16 bpp RGB 565<br>5=RESERVED<br>6=32 aRGB 8888   |
| GMC_SRC_DATATYPE<br><i>(mirror bits 0:1 of DP_DATATYPE:DP_SRC_DATATYPE)</i>  | 13:12 | none    | 0=mono (expanded to frgd, bkgd)<br>1=mono (expanded to frgd, leave_alone)<br>2=RESERVED<br>3=color (pixel type same as DST)=3   |
| GMC_BYTE_PIX_ORDER<br><i>(mirror of DP_DATATYPE:DP_BYTE_PIX_ORDER)</i>       | 14    | none    | 0=pixel order from MSBit to LSBit<br>1=pixel order from LSBit to MSBit  |
| GMC_DEFAULT_SEL  | 15    | none    |   |
| GMC_ROP3<br><i>(mirror of DP_MIX:DP_ROP3)</i>                                | 23:16 | none    | 0=ROP3 function   |
| GMC_DP_SRC_SOURCE<br><i>(mirror of DP_MIX:DP_SRC_SOURCE)</i>                 | 26:24 | none    | 2=loaded from memory (rectangular trajectory)<br>3=loaded thru hostadata (linear trajectory)<br>4=loaded thru hosdata (linear trajectory & byte-aligned)  |
| GMC_SRC_DATATYPE2<br><i>(mirror bits 2:2 of DP_DATATYPE:DP_SRC_DATATYPE)</i> | 27    | none    | 0=mono (expanded to frgd, bkgd)<br>1=RESERVED   |
| GMC_CLR_CMP_FCN_DIS  | 28    | none    |   |
| GMC_WR_MSK_DIS   | 30    | none    |   |

[W] (MM: 5\_1B)

**SC\_TOP\_LEFT - W - 32 bits - [MMReg:0x16EC]**

| Field Name                                    | Bits  | Default | Description  |
|---|-------|---------|--|
| SC_LEFT<br><i>(mirror of SC_LEFT:SC_LEFT)</i> | 13:0  | none    | Range -8192 to 8191.   |
| SC_TOP<br><i>(mirror of SC_TOP:SC_TOP)</i>    | 29:16 | none    | Range -8192 to 8191. (Reserved) Write 23: 16 to E2_DST_SCISSOR_TOP, Write 13: 0 to E2_DST_SCISSOR_LEFT |

No description available for this register.

**SC\_BOTTOM\_RIGHT - W - 32 bits - [MMReg:0x16F0]**

| Field Name  | Bits  | Default | Description  |
|---|-------|---------|--|
| SC_RIGHT<br><i>(mirror of SC_RIGHT:SC_RIGHT)</i>    | 13:0  | none    | Range -8192 to 8191.   |
| SC_BOTTOM<br><i>(mirror of SC_BOTTOM:SC_BOTTOM)</i> | 29:16 | none    | Range -8192 to 8191. (Reserved) Write 23: 16 to E2_SRC_SCISSOR_BOTTOM, Write 13: 0 to E2_SRC_SCISSOR_RIGHT |

(aliased to SC\_BOTTOM, SC\_RIGHT) [ W ] (MM: 5\_BC)

**SRC\_SC\_BOTTOM\_RIGHT - W - 32 bits - [MMReg:0x16F4]**

| Field Name  | Bits  | Default | Description  |
|---|-------|---------|--|
| SC_RIGHT<br><i>(mirror of SRC_SC_RIGHT:SC_RIGHT)</i>    | 13:0  | none    | Range -8192 to 8191.   |
| SC_BOTTOM<br><i>(mirror of SRC_SC_BOTTOM:SC_BOTTOM)</i> | 29:16 | none    | Range -8192 to 8191. (Reserved) Write 23: 16 to E2_SRC_SCISSOR_BOTTOM, Write 13: 0 to E2_SRC_SCISSOR_RIGHT |

(aliased to SRC\_SC\_BOTTOM, SRC\_SC\_RIGHT) [ W ] (MM: 5\_BD)

**ROM\_INDEX - RW - 32 bits - [IOReg,MMReg:0xA8]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| ROM_INDEX  | 16:0 | 0x0     |             |

No description available for this register.

**ROM\_DATA - R - 32 bits - [IOReg,MMReg:0xAC]**

| Field Name | Bits | Default | Description |
|------------|------|---------|-------------|
| ROM_DATA   | 7:0  | 0x0     |             |

No description available for this register.

**CAPO Anc BUF01 BLOCK CNT - R - 32 bits - [MMReg:0x974]**

| Field Name              | Bits  | Default | Description |
|-------------------------|-------|---------|-------------|
| CAPO Anc BUF0_BLOCK_CNT | 11:0  | 0x0     |             |
| CAPO Anc BUF1_BLOCK_CNT | 27:16 | 0x0     |             |

No description available for this register.

**CAPO Anc BUF23 BLOCK CNT - R - 32 bits - [MMReg:0x97C]**

| Field Name              | Bits  | Default | Description |
|-------------------------|-------|---------|-------------|
| CAPO Anc BUF2_BLOCK_CNT | 11:0  | 0x0     |             |
| CAPO Anc BUF3_BLOCK_CNT | 27:16 | 0x0     |             |

No description available for this register.

**SPLL\_AUX\_CNTL - RW - 32 bits - CLKIND:0x24**

| Field Name       | Bits | Default | Description                             |
|------------------|------|---------|---|
| SPLL_PDC_C       | 1:0  | 0x1     |   |
| SPLL_CKINVA      | 2    | 0x0     | 0=do not invert OCLK1<br>1=invert OCLK1 |
| SPLL_CKINVC      | 3    | 0x0     | 0=do not invert OCLK3<br>1=invert OCLK3 |
| SPLL_X3_CLK_SKEW | 6:4  | 0x0     |   |
| SPLL_MODEC       | 8:7  | 0x0     |   |

**SPLL\_AUX\_CNTL - RW - 32 bits - CLKIND:0x24**

| Field Name          | Bits | Default | Description   |
|---------------------|------|---------|---|
| TRANSIT_DONE_LENGTH | 12   | 0x1     | 0=create this power man signal, in cg_pm1, only if condition lasts more than one BCLK cycle<br>1=create this signal as per piglet's |

No description available for this register.

**SSPLL\_CNTL - RW - 32 bits - CLKIND:0x30**

| Field Name               | Bits  | Default | Description   |
|--------------------------|-------|---------|---|
| SSPLL_RESET              | 0     | 0x1     | 0=Not Reset SSPLL<br>1=Reset SSPLL                  |
| SSPLL_SLEEP              | 1     | 0x1     | 1=Powerdown SSPLL                                   |
| SSPLL_TST_EN             | 2     | 0x0     |   |
| SSPLL_REFCLK_SEL         | 4     | 0x0     | 0=not flopped<br>1=flopped                          |
| SSPLL_FBCLK_SEL          | 5     | 0x0     | 0=not flopped<br>1=flopped                          |
| SSPLL_TCPOFF             | 6     | 0x0     | 0=normal<br>1=test mode: Hi-Z                       |
| SSPLL_TVCOMAX            | 7     | 0x0     | 0=normal<br>1=test mode: runaway                    |
| SSPLL_PCP                | 10:8  | 0x4     |   |
| SSPLL_PVG                | 13:11 | 0x4     |   |
| SSPLL_PDC                | 15:14 | 0x2     |   |
| SSPLL_ATOMIC_UPDATE_EN   | 16    | 0x0     | 0=Atomic Update Disabled<br>1=Atomic Update Enabled |
| SSPLL_ATOMIC_UPDATE_SYNC | 18    | 0x0     | 0=Update ASAP<br>1=Update in VSYNC                  |

No description available for this register.

**SSPLL\_REF\_DIV - RW - 32 bits - CLKIND:0x31**

| Field Name                | Bits  | Default | Description   |
|---------------------------|-------|---------|---|
| SSPLL_REF_DIV             | 9:0   | 0x0     |   |
| SSPLL_ATOMIC_UPDATE_W (W) | 15    | 0x0     | 0=No Update<br>1=Update   |
| SSPLL_ATOMIC_UPDATE_R (R) | 15    | 0x0     | 0=Update done<br>1=Update Pending   |
| SSPLL_REF_DIV_SRC         | 17:16 | 0x0     | 0=SSPLL_REF = XTALIN<br>1=SSPLL_REF = PLLSCLK/2<br>2=SSPLL_REF = PLLSCLK/4<br>3=SSPLL_REF = Secondary Reference Clock |

No description available for this register.

**SSPLL\_DIV\_0 - RW - 32 bits - CLKIND:0x32**

| Field Name            | Bits  | Default | Description |
|-----------------------|-------|---------|-------------|
| SSPLL_FB_DIV          | 10:0  | 0x0     |             |
| SSPLL_FB_DIV_FRACTION | 14:12 | 0x0     |             |

**SSPLL\_DIV\_0 - RW - 32 bits - CLKIND:0x32**

| Field Name  | Bits  | Default | Description  |
|---|-------|---------|--|
| SSPLL_ATOMIC_UPDATE_W<br><i>(mirror of SSPLL_REF_DIV:SSPLL_ATOMIC_UPDATE_W) (W)</i> | 15    | 0x0     | 0=No Update<br>1=Update  |
| SSPLL_ATOMIC_UPDATE_R<br><i>(mirror of SSPLL_REF_DIV:SSPLL_ATOMIC_UPDATE_R) (R)</i> | 15    | 0x0     | 0=Update done<br>1=Update Pending  |
| SSPLL_POST_DIV  | 18:16 | 0x0     | 0=SS_CLK = SS_CLK_SRC<br>1=SS_CLK = SS_CLK_SRC/2<br>2=SS_CLK = SS_CLK_SRC/4<br>3=SS_CLK = SS_CLK_SRC/8<br>4=SS_CLK = SS_CLK_SRC/3<br>5=reserved<br>6=SS_CLK = SS_CLK_SRC/6<br>7=SS_CLK = SS_CLK_SRC/12 |
| SSPLL_FB_DIV_FRACTION_UPDATE  | 28    | 0x0     |  |

No description available for this register.

**SS\_INT\_CNTL - RW - 32 bits - CLKIND:0x33**

| Field Name               | Bits  | Default | Description  |
|--------------------------|-------|---------|--|
| SS_INT_EN                | 0     | 0x0     | 0=Disable Internal Spread Spectrum<br>1=Enable Internal Spread Spectrum  |
| SS_INT_SEL               | 1     | 0x0     | 0=Use Internal Spread Spectrum on Primary Display<br>1=Use Internal Spread Spectrum on Secondary Display   |
| SS_STEP_SIZE             | 3:2   | 0x0     | 0=Change feedback divider by increments of 0.2<br>1=Change feedback divider by increments of 0.4<br>2=Change feedback divider by increments of 0.6<br>3=Change feedback divider by increments of 1.0 |
| SS_DELAY                 | 6:4   | 0x0     |  |
| SS_DELTA_FRACTION        | 10:8  | 0x0     |  |
| SS_DELTA_INTEGER         | 17:12 | 0x0     |  |
| SS_PLL_DISPLAY_SRC       | 18    | 0x0     | 0=Spread Spectrum Pll to be used as primary display PLL<br>1=Spread Spectrum Pll to be used as second display PLL  |
| SS_PLL_DISPLAY_EN        | 19    | 0x0     | 0=Disable Spread Spectrum Pll to be used as a display PLL<br>1=Enable Spread Spectrum Pll to be used as a display PLL  |
| SS_BUF_GENLOCK_EN        | 20    | 0x0     | 0=Disabled SS_BUF Genlocking<br>1=Enable SS_BUF Genlocking   |
| SS_BUF_GENLOCK_THRESHOLD | 23:21 | 0x1     |  |
| SS_BUF_GENLOCK_DURATION  | 26:24 | 0x0     |  |
| SS_BUF_GENLOCK_HEIGHT    | 29:27 | 0x0     |  |

No description available for this register.

**SS\_TST\_CNTL - RW - 32 bits - CLKIND:0x34**

| Field Name     | Bits | Default | Description |
|----------------|------|---------|-------------|
| SS_TST_CNT (R) | 13:0 | 0x0     |             |

**SS\_TST\_CNTL - RW - 32 bits - CLKIND:0x34**

| Field Name            | Bits  | Default | Description   |
|-----------------------|-------|---------|---|
| SS_TST_CNT_SEL        | 17:16 | 0x0     | 0=Examine upper count<br>1=Examine lower count<br>2=Examine fbdiv range<br>3=Examine post inc/dec fbdiv       |
| SS_TST_GE (R)         | 20    | 0x0     |   |
| SS_TST_LE (R)         | 21    | 0x0     |   |
| SS_TST_DEC (R)        | 22    | 0x0     |   |
| ANALOG_MON_SS         | 23    | 0x0     |   |
| EXP_IMPLEMENTATION_EN | 24    | 0x0     | 0=Default implementation for internal spread spectrum<br>1=Experimental spread spectrum implementation        |
| SS_ANTIGLITCH_EN      | 25    | 0x0     | 0=Disable anti-glitch mux for spread clock to display<br>1=Enable anti-glitch mux for spread clock to display |
| HDP_BUSY_HALF_SCLK    | 26    | 0x0     | 0=Don't include HDP_BUSY as one of the busy conditions<br>1=Include HDP_BUSY as one of the busy conditions    |
| EN_DIV2_HALF_SCLK     | 27    | 0x0     | 0=SCLK is switched thru anti-glitch mux<br>1=Mask out every other SCLK to achieve half speed                  |
| SS_TST_MODE           | 31    | 0x0     | 0=Normal<br>1=Use external clock for spread spectrum controller   |

No description available for this register.

**SCLK\_MORE\_CNTL - RW - 32 bits - CLKIND:0x35**

| Field Name                | Bits | Default | Description   |
|---------------------------|------|---------|---|
| DISPREGS_MAX_DYN_STOP_LAT | 0    | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency |
| MC_GUI_MAX_DYN_STOP_LAT   | 1    | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency |
| MC_HOST_MAX_DYN_STOP_LAT  | 2    | 0x1     | 0=Programmable dynamic stopping latency<br>1=Max dynamic stopping latency |
| FORCE_DISPREGS            | 8    | 0x1     | 0=Dynamic<br>1=ForceOn  |
| FORCE_MC_GUI              | 9    | 0x1     | 0=Dynamic<br>1=ForceOn  |
| FORCE_MC_HOST             | 10   | 0x1     | 0=Dynamic<br>1=ForceOn  |
| STOP_SCLK_EN              | 12   | 0x0     | 0=Disable stopping of SCLK branches<br>1=Enable stopping of SCLK branches |
| STOP_SCLK_A               | 13   | 0x0     | 0=Do not stop SCLK_A except dynamic stopping is enabled<br>1=Stop SCLK_A  |
| STOP_SCLK_B               | 14   | 0x0     | 0=Do not stop SCLK_B except dynamic stopping is enabled<br>1=Stop SCLK_B  |
| STOP_SCLK_C               | 15   | 0x0     | 0=Do not stop SCLK_C except dynamic stopping is enabled<br>1=Stop SCLK_C  |

**SCLK\_MORE\_CNTL - RW - 32 bits - CLKIND:0x35**

| Field Name           | Bits  | Default | Description  |
|----------------------|-------|---------|--|
| HALF_SPEED_SCLK      | 16    | 0x0     | 0=Disable dynamic half speed SCLK<br>1=Enable dynamic half speed SCLK  |
| IO.CG_VOLTAGE_DROP   | 17    | 0x0     | 0=Disable dynamic core voltage drop<br>1=Enable dynamic core voltage drop  |
| TVFB_SOFT_RESET      | 18    | 0x0     | 0=Disable soft reset for TVOUT feedback divider<br>1=Enable soft reset for TVOUT feedback divider  |
| VOLTAGE_DROP_SYNC    | 19    | 0x0     | 0=Disable synchronization of half speed SCLK and core voltage drop<br>1=Enable synchronization   |
| VOLTAGE_DELAY_SEL    | 21:20 | 0x0     | 0=1 clock delay for speeding up SCLK<br>1=2 clock delay for speeding up SCLK<br>2=3 clock delay for speeding up SCLK<br>3=4 clock delay for speeding up SCLK |
| IDLE_DELAY_HALF_SCLK | 22    | 0x0     | 0=Wait for 256 PCICLKs before slowing down SCLK<br>1=Wait for 512 PCICLKs before slowing down SCLK   |
| AGP_BUSY_HALF_SCLK   | 23    | 0x0     | 0=Don't include AGP_BUSY as one of the busy conditions<br>1=Include AGP_BUSY as one of the busy conditions   |
| CG_SPARE_RD_C (R)    | 31:24 | 0x0     |  |

No description available for this register.

**MPLL\_AUX\_CNTL - RW - 32 bits - CLKIND:0x25**

| Field Name          | Bits  | Default | Description                             |
|---------------------|-------|---------|---|
| MPLL_PDC_C          | 1:0   | 0x1     |   |
| MPLL_CKINVA         | 2     | 0x0     | 0=do not invert OCLK1<br>1=invert OCLK1 |
| MPLL_CKINVC         | 3     | 0x0     | 0=do not invert OCLK3<br>1=invert OCLK3 |
| MPLL_X3_CLK_SKEW    | 6:4   | 0x0     |   |
| MPLL_MODEC          | 8:7   | 0x0     |   |
| MPLL_TEST_COUNT (R) | 31:24 | 0x0     |   |

No description available for this register.

**MDLL\_RDCKB - RW - 32 bits - CLKIND:0x11**

| Field Name       | Bits | Default | Description   |
|------------------|------|---------|---|
| MRDCKB0_SLEEP    | 0    | 0x1     | 0=Enabled<br>1=PowerDown                                  |
| MRDCKB0_RESET    | 1    | 0x1     | 0=Enabled<br>1=Reset                                      |
| MRDCKB0_RANGE    | 3:2  | 0x2     |   |
| MRDCKB0_REF_SEL  | 5:4  | 0x0     | 0=MCLK<br>1=QSB0 pad<br>2=delayed HCLK1 feedback          |
| MRDCKB0_FB_SEL   | 7:6  | 0x0     | 0=strobe leaf node<br>1=logic zero<br>2=internal feedback |
| MRDCKB0_REF_SKEW | 10:8 | 0x0     |   |



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**MDLL\_RDCKB - RW - 32 bits - CLKIND:0x11**

| Field Name       | Bits  | Default | Description   |
|------------------|-------|---------|---|
| MRDCKB0_SINSEL   | 11    | 0x0     | 0=read strobe per 32 bits<br>1=read strobe per 8 bits     |
| MRDCKB0_FB_SKEW  | 14:12 | 0x0     |   |
| MRDCKB0_BP_SEL   | 15    | 0x1     | 0=DLL clock<br>1=MCLK                                     |
| MRDCKB1_SLEEP    | 16    | 0x1     | 0=Enabled<br>1=PowerDown                                  |
| MRDCKB1_RESET    | 17    | 0x1     | 0=Enabled<br>1=Reset                                      |
| MRDCKB1_RANGE    | 19:18 | 0x2     |   |
| MRDCKB1_REF_SEL  | 21:20 | 0x0     | 0=MCLK<br>1=QSB4 pad<br>2=delayed HCLK1 feedback          |
| MRDCKB1_FB_SEL   | 23:22 | 0x0     | 0=strobe leaf node<br>1=logic zero<br>2=internal feedback |
| MRDCKB1_REF_SKEW | 26:24 | 0x0     |   |
| MRDCKB1_SINSEL   | 27    | 0x0     | 0=read strobe per 32 bits<br>1=read strobe per 8 bits     |
| MRDCKB1_FB_SKEW  | 30:28 | 0x0     |   |
| MRDCKB1_BP_SEL   | 31    | 0x1     | 0=DLL clock<br>1=MCLK                                     |

No description available for this register.