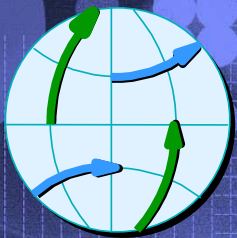


IBM China Design Center

IBM Embedded PowerPC Architecture™



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Agenda

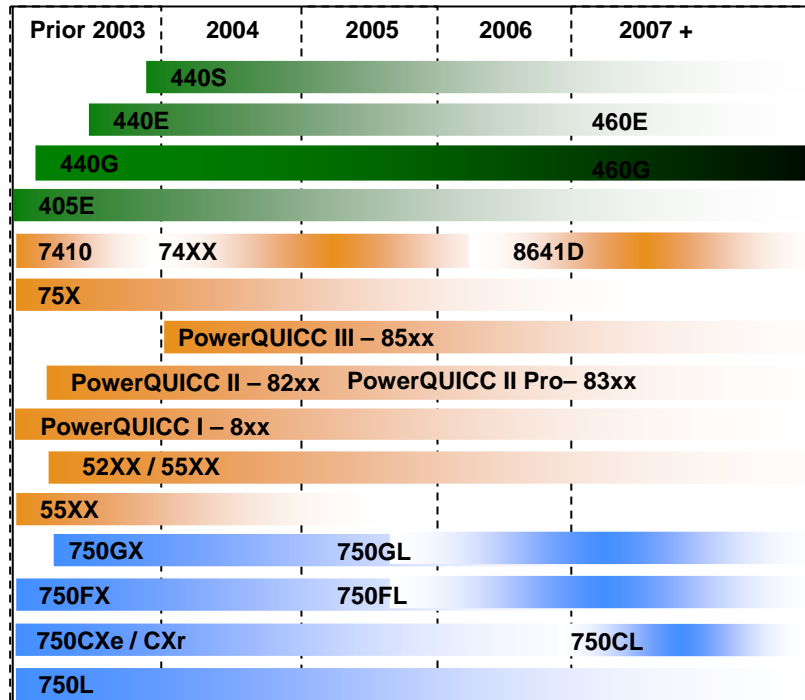
- **PowerPC4xx Family**
- **PowerPC 405 Processor Core**
- **PowerPC 464 Processor Core**
- **PowerPC 476 Processor Core**
- **PowerPC Ecosystem**
- **PowerPC Embedded Environment Architecture**



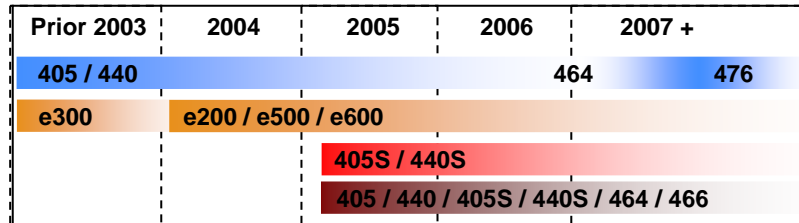
PowerPC Roadmap

■ IBM
 ■ Freescale
 ■ AMCC
 ■ PASEmi
 ■ Synopsys
 ■ HCL
 ■ Xilinx
 ■ Rapport

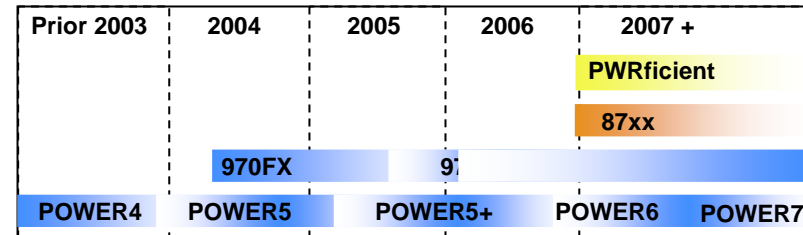
32-bit Processors



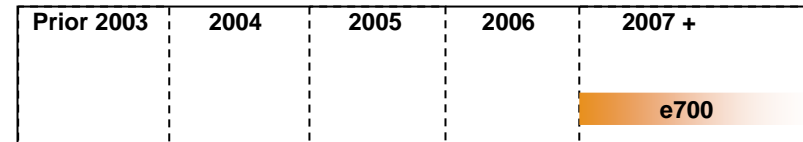
32-bit Cores



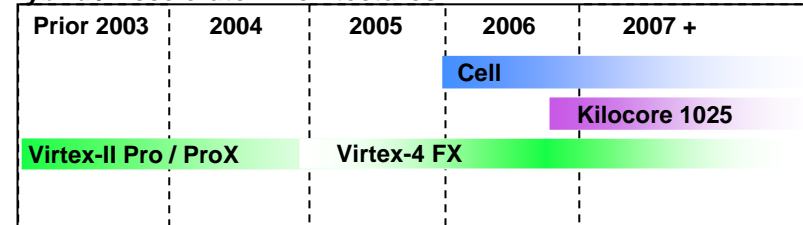
64-bit Processors



64-bit Cores



Hybrid / Accelerator Architectures





IBM PowerPC: Scalable and Flexible

One Architecture – Application binary compatible

**Servers, Workstations, PCs, Gaming Consoles,
Routers, Automotive, Consumer Devices**

POWER™ Server Microprocessors

POWER2™ POWER3™ POWER4™ POWER5™ POWER6™ POWER7™

PowerPC® Embedded Microprocessors

PowerPC 750

PowerPC 970

PowerPC® Licensable Processor Cores and Custom Solutions

PowerPC 405

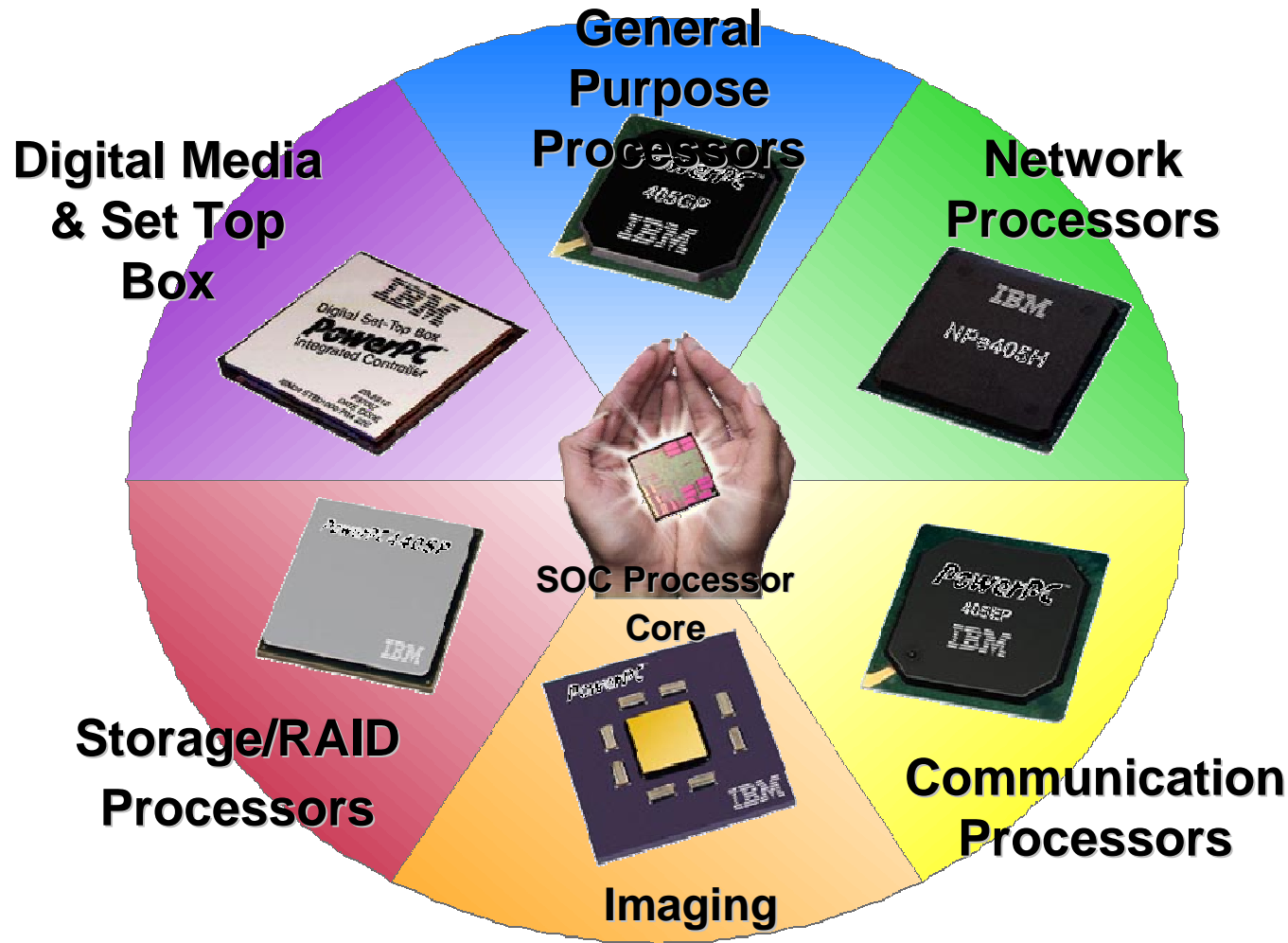
PowerPC 464

PowerPC 476





PowerPC4XX, SoC Embedded Cores



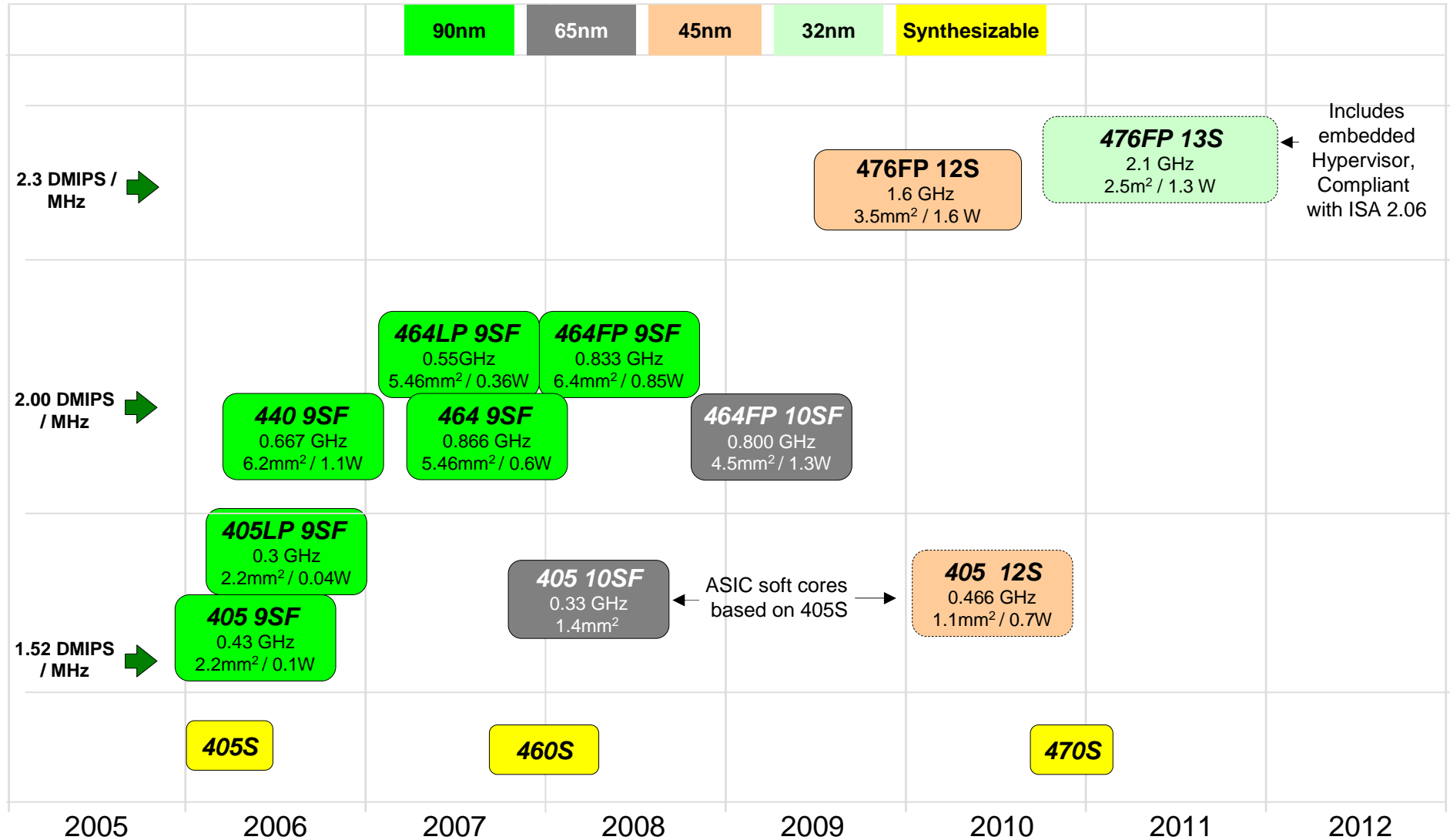


IBM PowerPC 4xx Processor Cores

- **Targeted for low cost , low power and high performance embedded SoC applications**
 - 405 series
 - Entry level
 - 464 series
 - High performance
 - 476 series
 - Very High performance, multiple core
- **IBM itself does not offer standard PPC4xx based SoC products anymore, but we offer the cores to be included in customer chip either to be designed by IBM or 3rd party**
 - High performance Hard cores for IBM, Chartered and Samsung
 - Fully Synthesizable cores for flexibility in fab choice and/or design point
- **IBM's previous 4xx standard PPC4xx based SoC products have been transferred and owned by AMCC**



PowerPC4xx CPU Core Roadmap



** All future dates are estimates only, and subject to change without notice.



PPC405 Processor Core - Overview (1/2)

- **Entry level 32-Bit embedded processor engine**
 - 32-bit single-issue, five-stage pipeline RISC processor
 - Small die size, minimal power high performance --Up to 400MHz&608DMIPS(1.52 DMIPS/MHz) when implemented in IBM's 90-nm copper CMOS technology

- **Target market segments include**
 - Consumer Video Applications – DC, Video games, STB, etc...
 - Portable Products – PDA, handheld GPS receivers, etc...
 - Office Automation Products – printer, fax machines, etc
 - Networking and storage products – disk drive controllers, routes, ATM switches, etc

- **Multiple CCB peripheral /macro core available**

- **Complete tools solutions provided by over 80 3rd-party vendors**

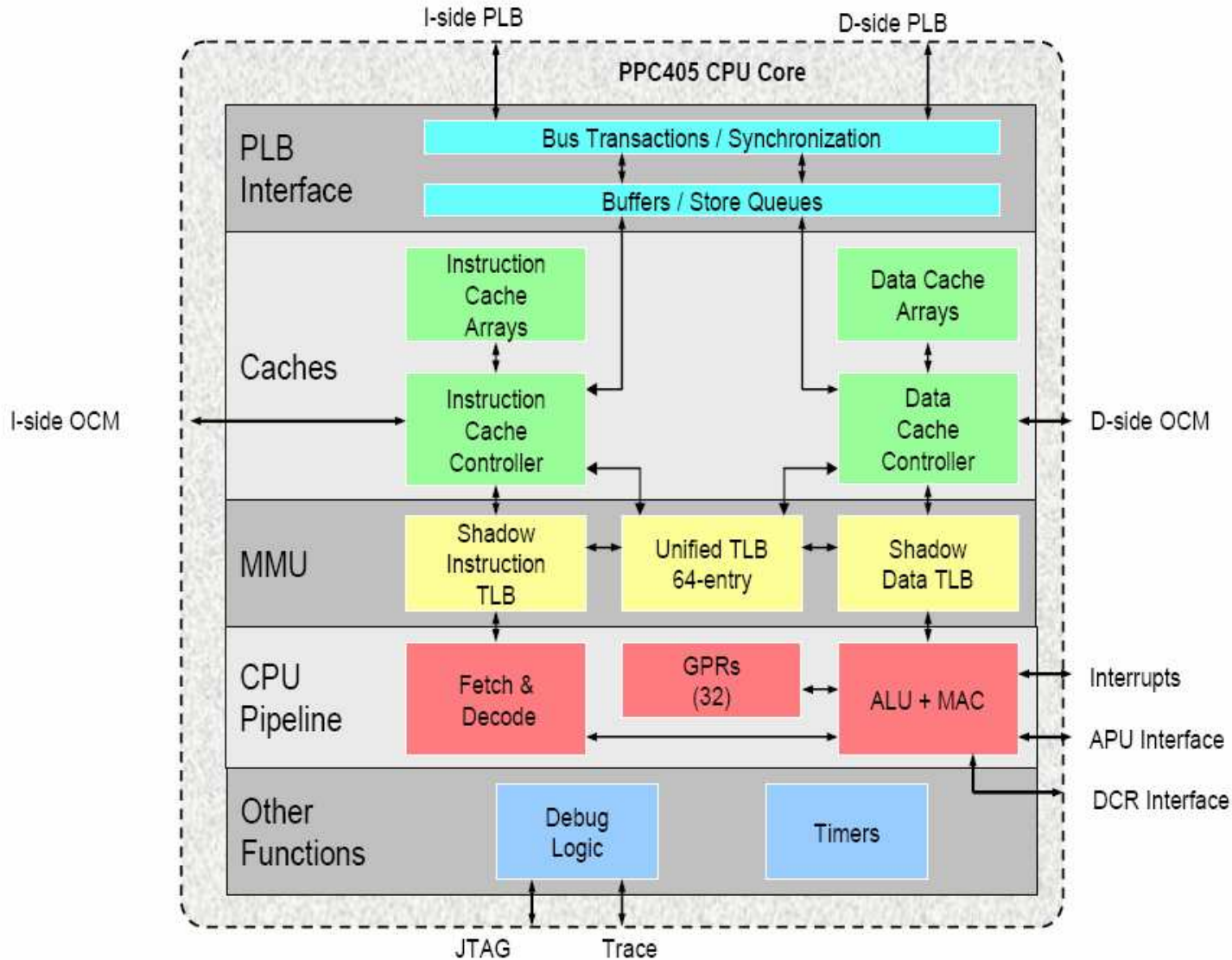


PPC405 Processor Core - Overview (2/2)

PowerPC 405 core parametrics			
Technology	130 nm	90 nm	Fully synthesizable
Fabs supported	IBM, Chartered	IBM, Chartered, Samsung	All
Frequency (worst-case conditions)	366 MHz	400 MHz	250-300 MHz (process dependent)
Performance (estimated)	555 DMIPS	608 DMIPS	380-456 DMIPS
Typical power dissipation (estimated)	0.5 mW/MHz @ 1.5 V 0.3 mW/MHz @ 0.9 V	0.19 mW/MHz @ 1.1 V	0.25-0.6 mW/MHz (process dependent)
Power supply	1.5 V	1.1 V	Process dependent
Temperature range	-40°C to +105°C	-40°C to +105°C	-40°C to +105°C
Die size, CPU + L1	3.8 mm ²	2.0 mm ²	Process dependent



PPC405 Processor Core – Architecture (1/7)





PPC405 Processor Core – Architecture (2/7)

- **PPC405 CPU**

- 5-stage pipeline: fetch, decode, execute, write-back, load write-back stage

Pipeline Stage ----- Instruction Type	Instruction Fetch Buffer	Decode / Dispatch	Execute	Write-Back	Load Write- Back
Integer / Logical	Fetch	Decode / Dispatch	Execute	Write GPR	
Branch	Fetch	Predict / Decode / Dispatch	Execute		
Store	Fetch	Decode / Dispatch	Address Gen	Cache write	
Load	Fetch	Decode / Dispatch	Address Gen	Cache read	Write GPR



PPC405 Processor Core – Architecture (3/7)

- **PPC405 CPU, Fetch and Decode Logic**
 - 3 buffers(PFB0, PFB1 and DCD) contain up to two instructions in the fetch queue
 - Static branch prediction – negative address displacement branches are by default assumed taken. Branches that do not test the condition or count registers are also predicted as taken. Conditional branches are predicted upon default conditions while the default prediction can be overridden by software at assembly or compile time



PPC405 Processor Core – Architecture (4/7)

▪ **PPC405 CPU, Execution Unit**

- Single issue execution unit
- 32*32bit GPR 3 read port and 2 write port reregister file. Data read out in the decode stage and written in the write-back stage
- Load/store operation parallel with ALU operation
- MAC as an APU unit provide one cycle 16bit*16bit MAC operation

▪ **PPC405 CPU, Exception Handling Logic**

- Services 4 kinds of exceptions: error conditions, internal timer facilities, debug events and external interrupts; 19 exceptions
- Critical and non-critical exceptions, each has its own pair of save/restore registers for holding the machine state which allow the core to quickly handle critical interrupts.



PPC405 Processor Core – Architecture (5/7)

▪ **Instruction and Data Cache**

- Consist of PLB master interface, cache arrays and a cache controller
- 2 PLB interfaces
- Separate two-way set-association I-Cache and D-Cache with 8 word(32-byte) cache line
- Factory-configurable Cache size for I-Cache and D-Cache (0KB, 4KB, 8KB, 16KB, 32KB)
- Non-blocking cache array
- LRU replacement policy



PPC405 Processor Core – Architecture (6/7)

▪ MMU

- 8 possible page sizes (1KB to 16MB), improve memory efficiency and minimizes the number of TLB miss.
- Storage attributes: cacheability, write through/write back, allocate write, big/little endian, guarded and user define
- Access control options enable software to control general access for programs in the problem state and control write and execute permissions for all pages
- 64-entry fully-associative unified TLB, a four-entry instruction shadow TLB (ITLB) and an eight-entry data shadow TLB(DTLB)
- Real mode as an alternative to address translation and MMU storage attributes.



PPC405 Processor Core – Architecture (7/7)

▪ **Timer**

- A 64-bit time base and three timers: the Programmable Interval Timer (PIT), the Fixed Interval Timer (FIT), and the watchdog timer

▪ **Debug Logic**

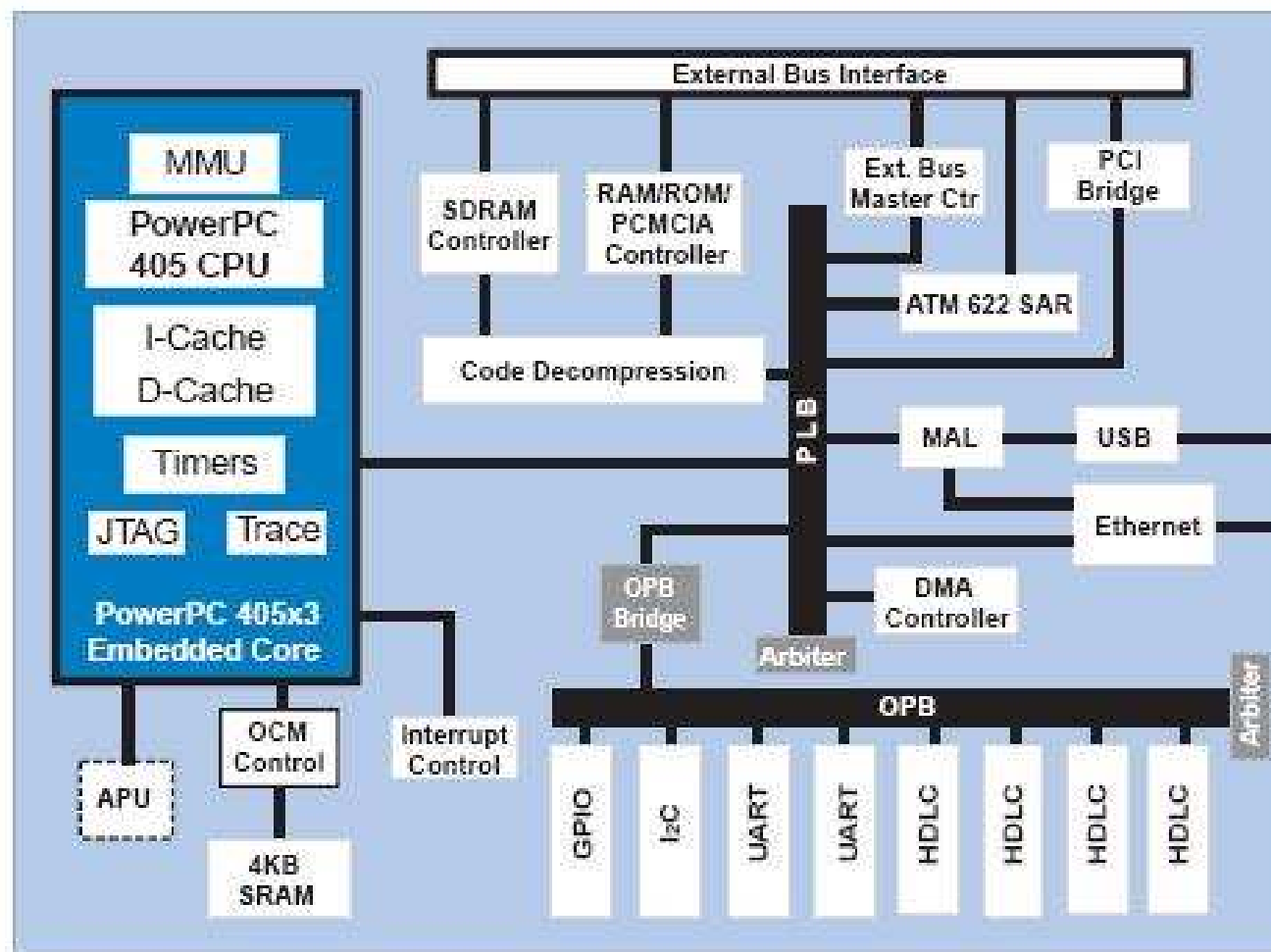
- ROM Monitors, JTAG debuggers and instruction trace tools
- 4 debug mode: internal debug mode, external debug mode, debug wait mode and Real-time trace debug mode

▪ **Core interfaces**

- Processor Local Bus (PLB) interface, DCR Bus interface, OCM interfaces, Auxiliary Processor Unit (APU)/Floating Point Unit (FPU) Interface, External Interrupt Controller (EIC) Interface and Debug interface(JTAG and Trace ports)



PPC405 Processor Core – SoC Example





PPC464 Processor Core - Overview (1/2)

- **High performance embedded PowerPC core**
 - 32-bit out-of-order two-issue seven-stage pipeline RISC superscalar CPU core
 - Optimized for performance leadership and low power system-on-a-chip (SoC) designs -- up to 667MHz & 1334 DMIPS (2.0 DMIPS/MHz) when implemented in IBM's advanced 90-nm copper CMOS technology
- **Target market segments include**
 - Consumer applications including digital cameras, video games, set-top boxes, and internet appliances
 - Office automation products such as laser printers, thin-client systems, and sub-notebooks
 - Storage and networking products such as RAID controllers, routers, ATM switches, cellular base stations, and network cards
- **Multiple CCB peripheral /macro core available**
- **Complete tools solutions provided by over 80 3rd-party vendors**



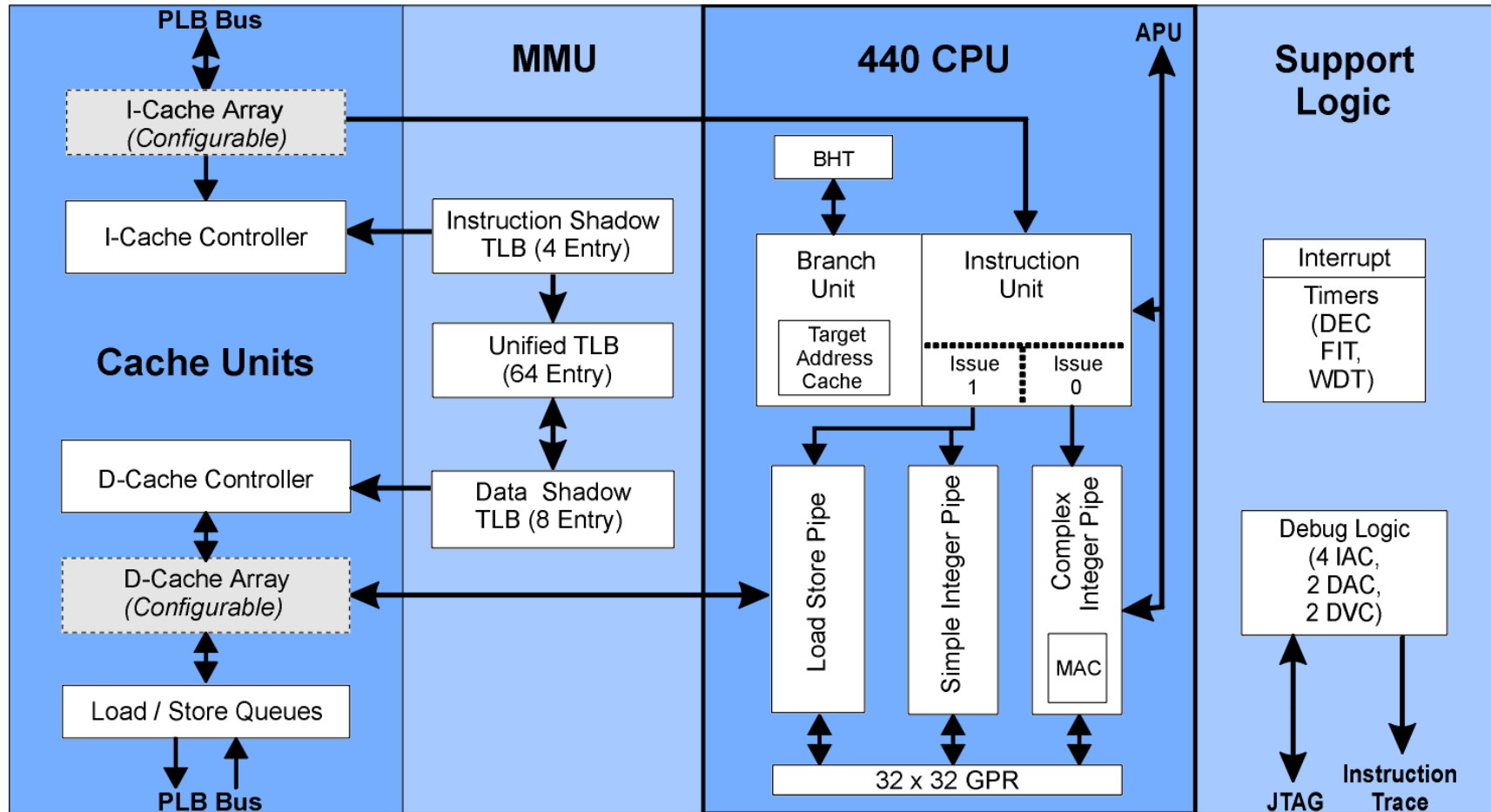
PPC464 Processor Core - Overview (2/2)

PowerPC 440 core parametrics

Technology	130 nm	90 nm	Fully synthesizable
Fabs supported	IBM, Chartered	IBM, Chartered, Samsung	All
Frequency (worst-case conditions)	533 MHz	667 MHz	300-350 MHz (process and library dependent)
Performance (estimated)	1066 DMIPS	1334 DMIPS	600-700 DMIPS
Typical power dissipation (estimated)	1.5 mW/MHz @ 1.4 V	0.76 mW/MHz + 200 mW DC @ 1.1 V	Process dependent
Power supply	1.4 V	1.1 V	Process dependent
Temperature range	-40°C to +105°C	-40°C to +105°C	-40°C to +105°C
Die size, CPU + L1	9.8 mm ²	6.0 mm ²	Process and library dependent



PPC464 Processor Core – Architecture (1/4)





PPC464 Processor Core – Architecture (2/4)

▪ PPC464 CPU

- 2-issue superscalar design
- Out-of-order issue, execution, and completion
- Dynamic branch prediction
- Single-cycle branch latency
- Three execution pipelines
- Single-cycle throughput on 32x32 multiply
- 24 DSP operations (16x16+32->32, MAC with single-cycle throughput)



PPC464 Processor Core – Architecture (3/4)

Stage 1:
Instruction Fetch
(IFTH)

Stage 2:
Predecode
(PDCD)

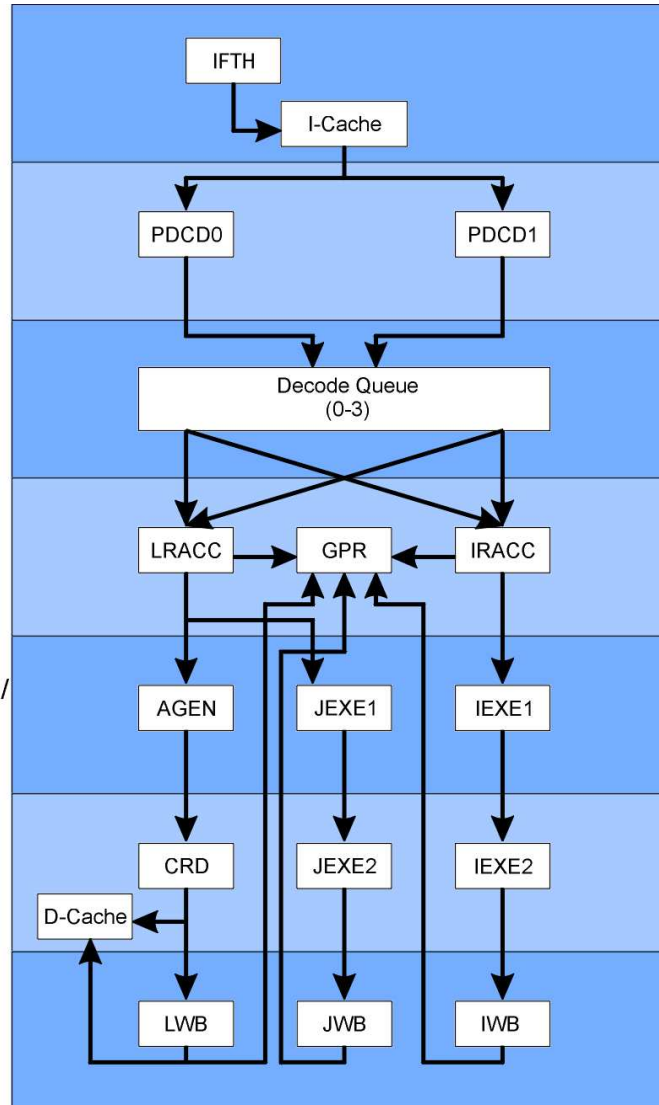
Stage 3:
Decode / Issue
(DISS)

Stage 4:
Register Access
(RACC)

Stage 5:
Address Generation /
Execute 1
(AGEN/EXE1)

Stage 6:
Cache Read /
Execute 2
(CRD/EXE2)

Stage 7:
Writeback
(WB)

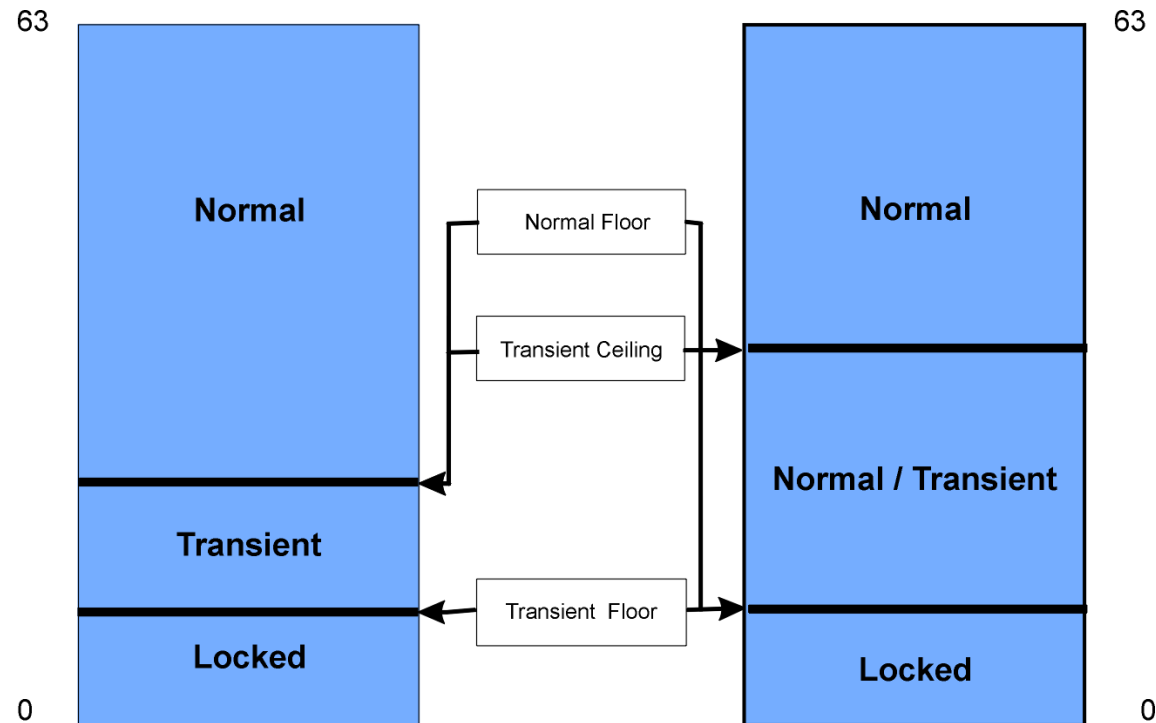




PPC464 Processor Core – Architecture (4/4)

▪ Instruction and Data Cache

- Almost like those of PPC405
- Cache Partitioning
 - The ability to be separated into “normal”, “transient”, and “locked” regions

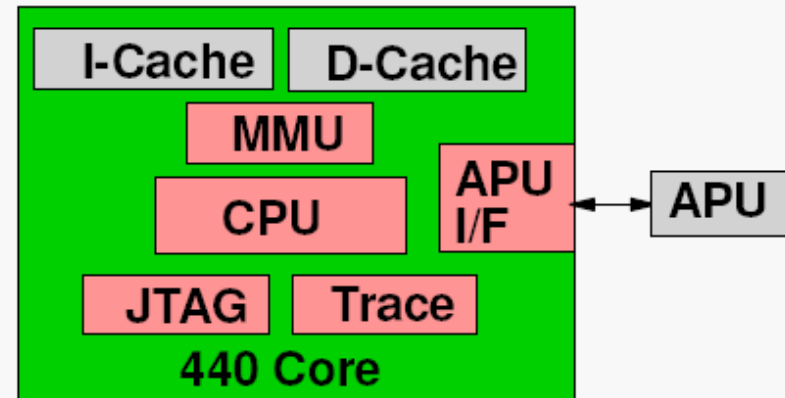




Adding customization (APUs) to the PPC440

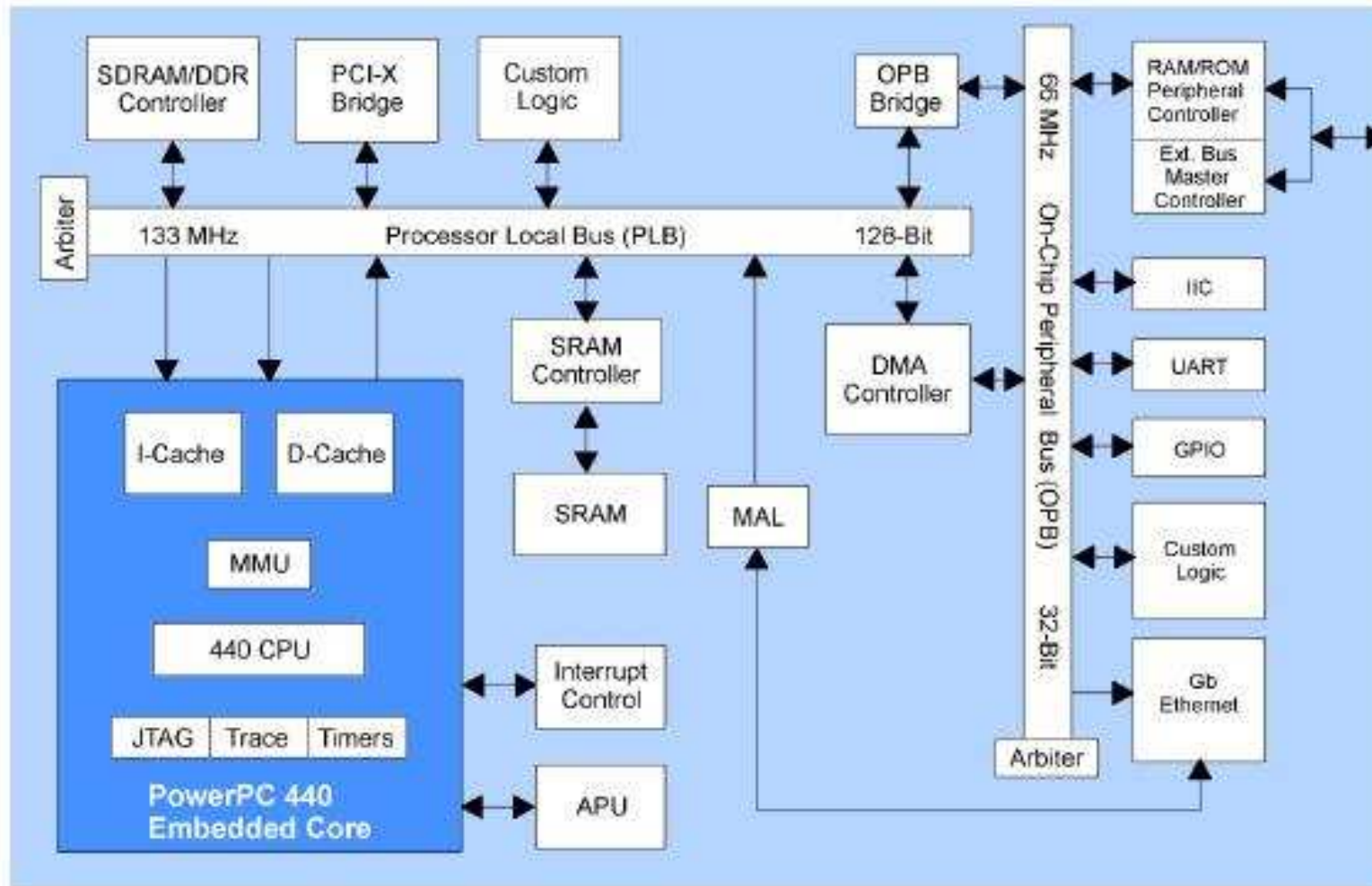
APU interface

- **Allows creation of user-defined instructions on the 440**
 - Tightly coupled with 440 pipeline
 - Provides access to data cache, and condition register
- **Enables CPU-attached coprocessors**
 - Supports independent Register file
 - Instructions executed parallel to CPU
- **APU examples**
 - Simple –instruction acceleration
 - Complex – FPU, SIMD/VMX, DSP





PPC464 Processor Core – SoC Example





PPC405 vs PPC464 Core Characteristics

	PPC405	PPC464
Architecture	32-bit PowerPC Embedded Environment	32-bit PowerPC Embedded Environment
CPU Pipeline	Single issue, 5 stages pipeline	Superscalar, two issue, 7 stages pipeline Out of order dispatch, execution, completion
Internal Configuration	Hardware multiply and divide Enhanced string and multiple-word handling 24 DSP instructions (16 x 16 + 32) 32-bit x 32 general purpose registers Direct processor-local on-chip memory interface	Combined complex integer pipeline Simple integer pipeline Load/Store pipeline 24 DSP instructions (16 x 16 + 32) 32-bit x 32 general purpose registers
Caches - I/D	32KB/32KB, two-way set associative 32-byte line, No blocking Parity added starting with SA-27E	64KB/64KB, 64-way set associative 32-byte line, no blocking Parity added starting with CU-11
Memory Management Unit	64-entry UTLB -- full associativity 4-entry ITLB, 8-entry DTLB 5-cycle miss penalty Variable pages - 1KB to 16MB	64-entry UTLB -- full associativity 4-entry ITLB, 8-entry DTLB 3-cycle miss penalty Variable pages - 1KB to 256MB
Branch Prediction	Static	Dynamic, 4K-entry BHT
On-chip Bus – PLB Interface	32-bit (4GB) physical address 64-bit data bus - PLB3 Supports multiple N:1 and N:2 core:bus ratios Supports on-chip memory via PLB and OCM interfaces	36-bit (64GB) physical address 128-bit data bus - PLB4 Supports multiple N:1, N:2, N:3 core:bus ratios Supports on-chip memory via PLB
Timers	64-bit Time base Decrementer/Programmable interval timer (PIT) Fixed interval timer (FIT) Watchdog timer	64-bit Time base Decrementer/Programmable interval timer (PIT) Fixed interval timer (FIT) Watchdog timer
Debug Support	JTAG and Trace FIFO ports 4 Instruction Address, 2 Data Address, and 2 Data Value breakpoints Real-time non-invasive trace	JTAG and Trace FIFO ports 4 Instruction Address, 2 Data Address, and 2 Data Value breakpoints Real-time non-invasive trace



PPC476 Processor Core - Overview (1/2)

- **High performance embedded PowerPC core**
 - 32-bit out-of-order five-issue nine-stage pipeline RISC superscalar CPU core
 - High performance leadership system-on-a-chip(SoC) designs -- up to 1.6GHz&3680DMIPS(2.3 DMIPS/MHz)when implemented in IBM's advanced 45-nm SOI technology
- **Target market segments include**
 - Consumer applications including Digital TV, imaging
 - I/O ocntroller and service processors
 - Office automation products such printer
 - Storage and networking products such as RAID controllers, routers, ATM switches, cellular basestations, and network cards
 - Network communications including control plane
 - Aerospace and defense applications
 - Highly parallel, high performance coumputing systems



PPC476 Processor Core - Overview (2/2)

➤ Technology

- IBM 45nm CMOS (SOI) – ASIC Cu-45 hard core
- Seven metal-layer core utilization

➤ Specifications

- Dhrystone 2.1: 2.3 DMips/Mhz (* preliminary *)
- CPU clock: 1.6Ghz @ 0.9V, 105C (* preliminary *)
- Power (CPU core): 1.5W – 1.8W (total estimated power) (* preliminary *)
- L2 cache & PLB6 complex clock: 800MHz @ 0.9V, 105C (* preliminary *)
- Size: 3.5mm² (* preliminary *)



PPC476FP Architecture & Implementation

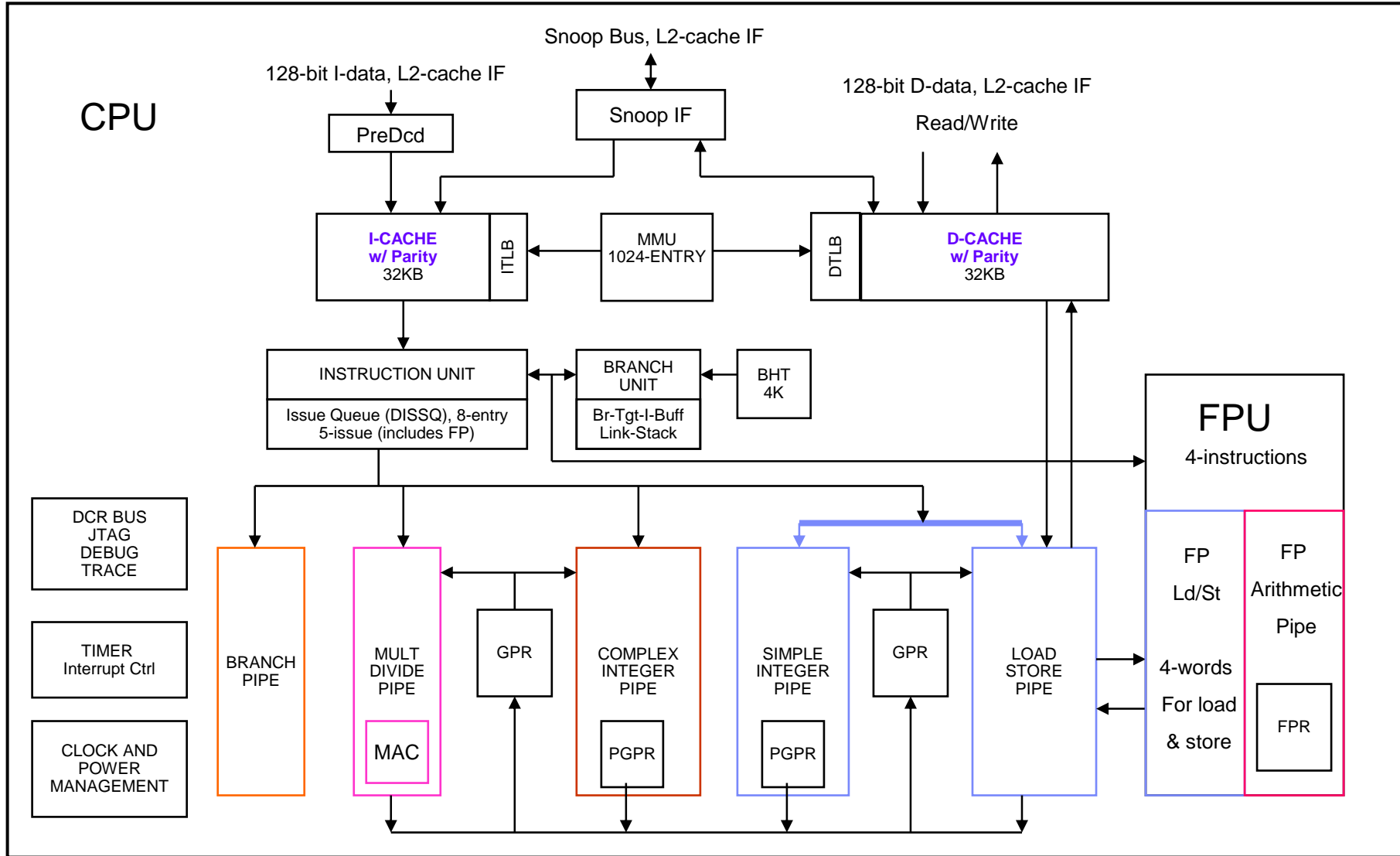
Highlights

High-performance, Out-of-Order, 5-issue / 5-pipeline superscalar RISC CPU

- **PowerPC ISA-V2.05 (Book-3E) 32-bit implementation**
- **DSP MAC instructions support**
- **5-issue and 5-pipelines**
 - Out-of-Order Issue / Execution / Completion
 - 9+ stage pipeline micro-architecture for high-performance
 - Complex Integer Pipeline
 - Floating-point Pipeline
 - Branch Pipeline
 - Load/Store Pipeline
 - Simple Integer Pipeline
- **SMP support with L2 cache & PLB6**
 - Coherency snoop on both I & D cache, and MMU
- **Integrated FPU Coprocessor; support for future VMX integration with asynchronous issue & execution interface**
- **Memory Management Unit**
 - Separate D and I micro-TLBs : 8-entry each
 - 1024-Entry Unified TLB
 - Variable Page Sizes (4KB – 1GB)
 - 42-Bit (4TB) Real Address space
 - 16-bit PID space ; 49-bit virtual address
 - Real Address mode support (with CCR control)
- **Debug Facilities**
 - Hardware Execution Debug Facilities integrated in IEEE 1149.1 JTAG
 - Multiple Instruction and Data Address Breakpoints with a multiple Ranges
 - Data Value Compare
 - Single Step, Branch, Trap and Other Debug Events
 - Real-Time Software Trace Interface



PPC476FP CPU Block Diagram





PPC476 L2 Cache Complex Features

- Single CPU (private) L2 cache configuration
- 256KB, 512KB, 1MB configurations
- 128B cache line
- 4-way set associative
- L2 cache is unified (holds instruction and data)
- L2 cache is inclusive of L1 data cache
- MESI+T+SL+MU Protocol Coherency support
- Write-back (store-in) cache:
- True LRU replacement
- Non-blocking cache
- Single PLB6 master port
- PLB6 snoop interface
- DCR interface for configuration



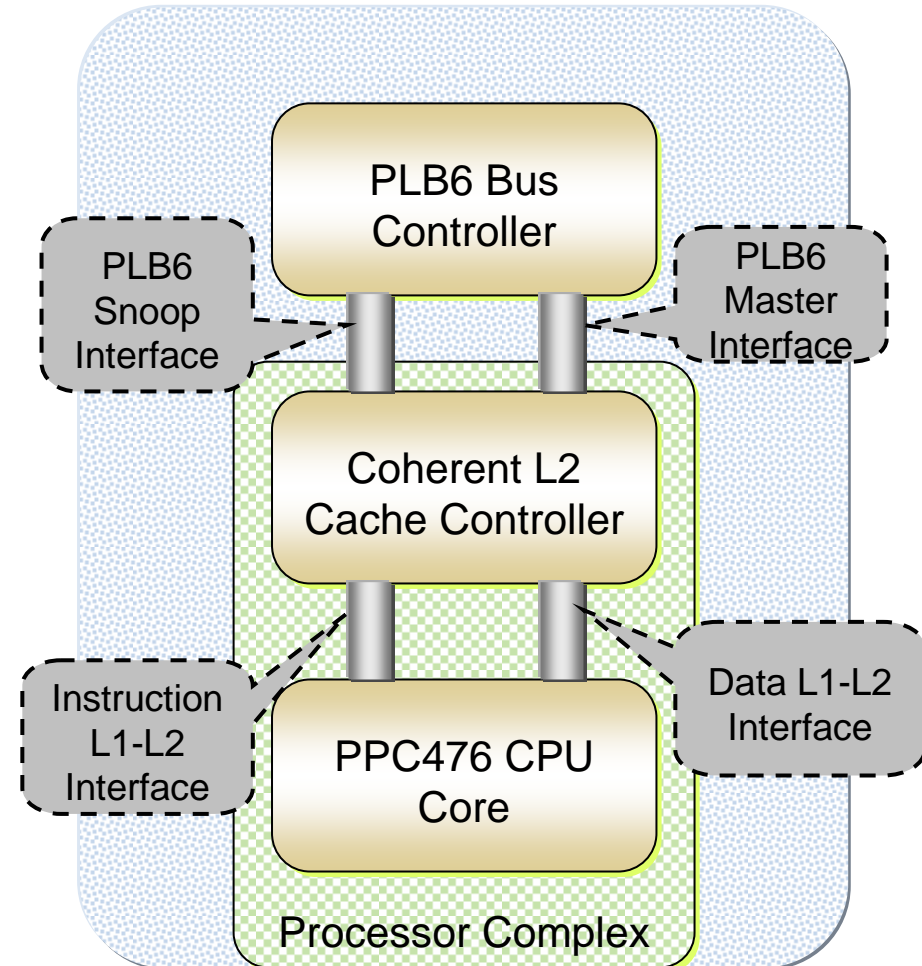
PPC476FP Floating Point Unit

- Two floating point pipelines
 - FP arithmetic
 - FP load / store
- ANSI/IEEE 754-1985 standard and PowerPC ISA V2.05 floating point instructions supported
 - Double precision
 - Single precision
- Six stage pipeline FP arithmetic execution
 - Extended divide stages
 - Extended operation stages for denormal operations



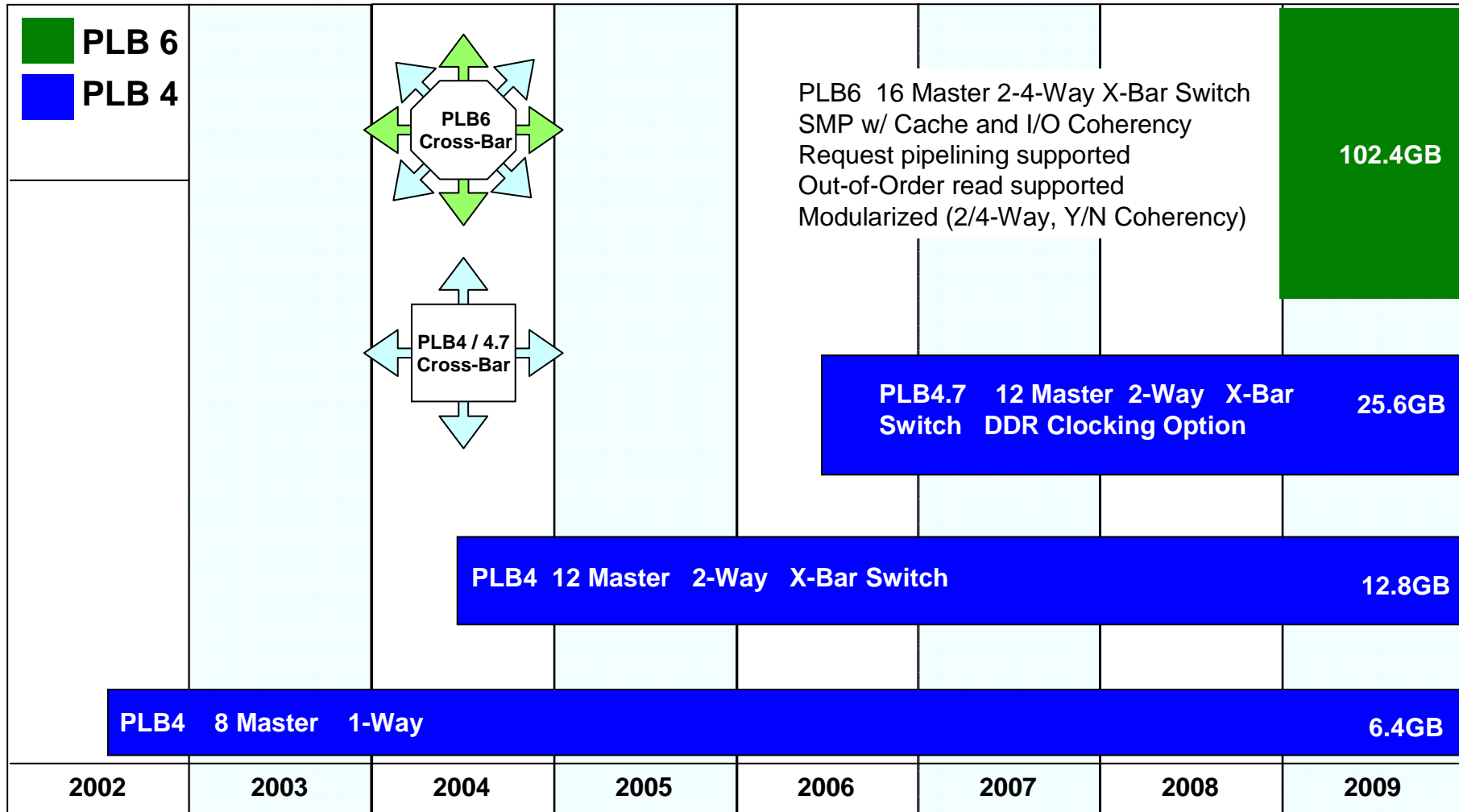
PPC476FP Usage

- High performance CPU core with coherency enabled L1 caches
- Coherent L2 cache complex with PLB6 system bus interface
- Processor local Bus (PLB6) controller supporting coherent multi-core processor complex





Core-Connect IP





PPC476FP/PPC464FP Comparison (1/2)

	PPC464FP	PPC476FP
Architecture	PowerPC Book-E	Power ISA v. 2.05 Book III-E
Performance (DMIPS)	2.0DMIPS / MHz	2.3DMIPS / MHz
Pipeline	2-issue/O-o-O 3-pipes (+ 2 FPU) 7-stage pipeline	5-issue/O-o-O 5-pipes (+ 2 FPU) 9-stage pipeline + pre- decode
APU Interface (FPU, VMX)	Lock step (issue in sync)	O-o-O
Effective Address Real Address	32-bit 36-bit (64GB)	32-bit 42-bit (4TB)
BHT size	512	4K
Link-Stack	none	4-entry
FO4 design	37FO4	26FO4



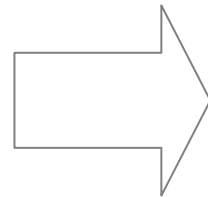
PPC476FP/PPC464FP Comparision (2/2)

	PPC464FP	PPC476FP
MMU page sizes	1KB – 1GB page size	4KB – 1GB page size
MMU entries	64	1024
Cache size	32KB I/D	32KB I/D
Access	1-cycle	2-cycle pipelined
Cache line size	32B	32B
Cache ways	64-way/64-way	4-way/4-way
Speculative I-fetch	no	2-pending
Coherency	no	yes

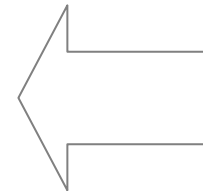


A New Market Disruption in Home Video: Digital TV Moves from a 1-way Static Experience to a 2-way Interactive Experience

Traditional 1-way Content



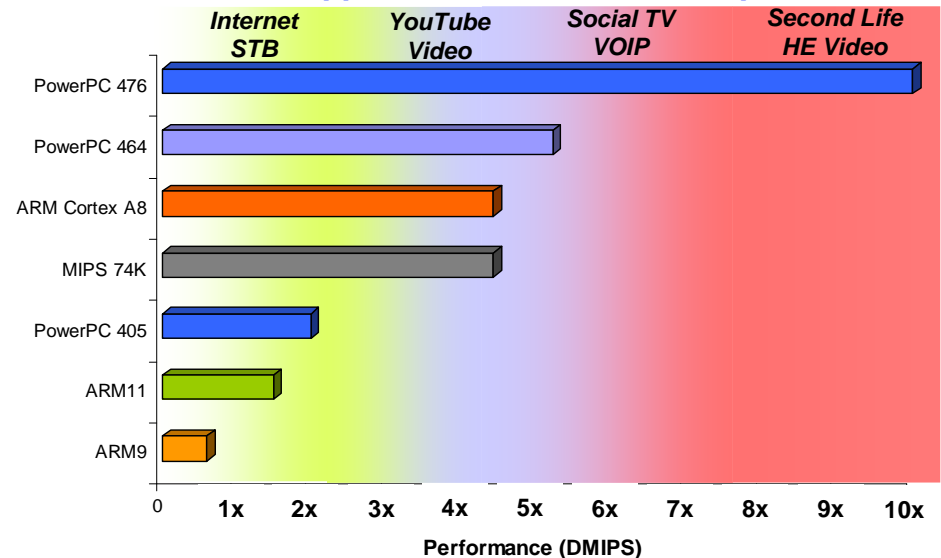
The Internet – 2-way Interactive Experience



All three platforms (DTV, STB and DVD) will enable internet functionality

- **Internet functionality drives dramatic increase in processor performance requirements**
 - Flash video and animation, Java, and Media Players require execution of multiple CODEC standards (WMA, Real Player, Quicktime, etc)
 - Too expensive to implement all standards in hardware
 - >1GHz performance required for software CODEC execution
- **This is what IBM does best**
 - PowerPC – best of breed embedded performance
 - IBM's proven high-performance SoC integration capability

Internet Application Performance Requirements



* Illustration of maximum achievable core performance (DMIPS) based on public statements and/or estimates versus recommended system processor performance for selected applications (estimation based on DMIPS at processor frequency). [Source: IBM Research.](#)



The future of TV is Interactive, with a rich GUI interface

- Today's TV – a “static” experience
- Tomorrows TV
 - Non-traditional sources create a 2-way social interactive experience
 - OEMs are challenged to create this device in a cost-effective manner

TV Display – Where is Churchill Downs?

IP TV and custom base Programming



Real Time Alerts provide Medical and GPS tracking information

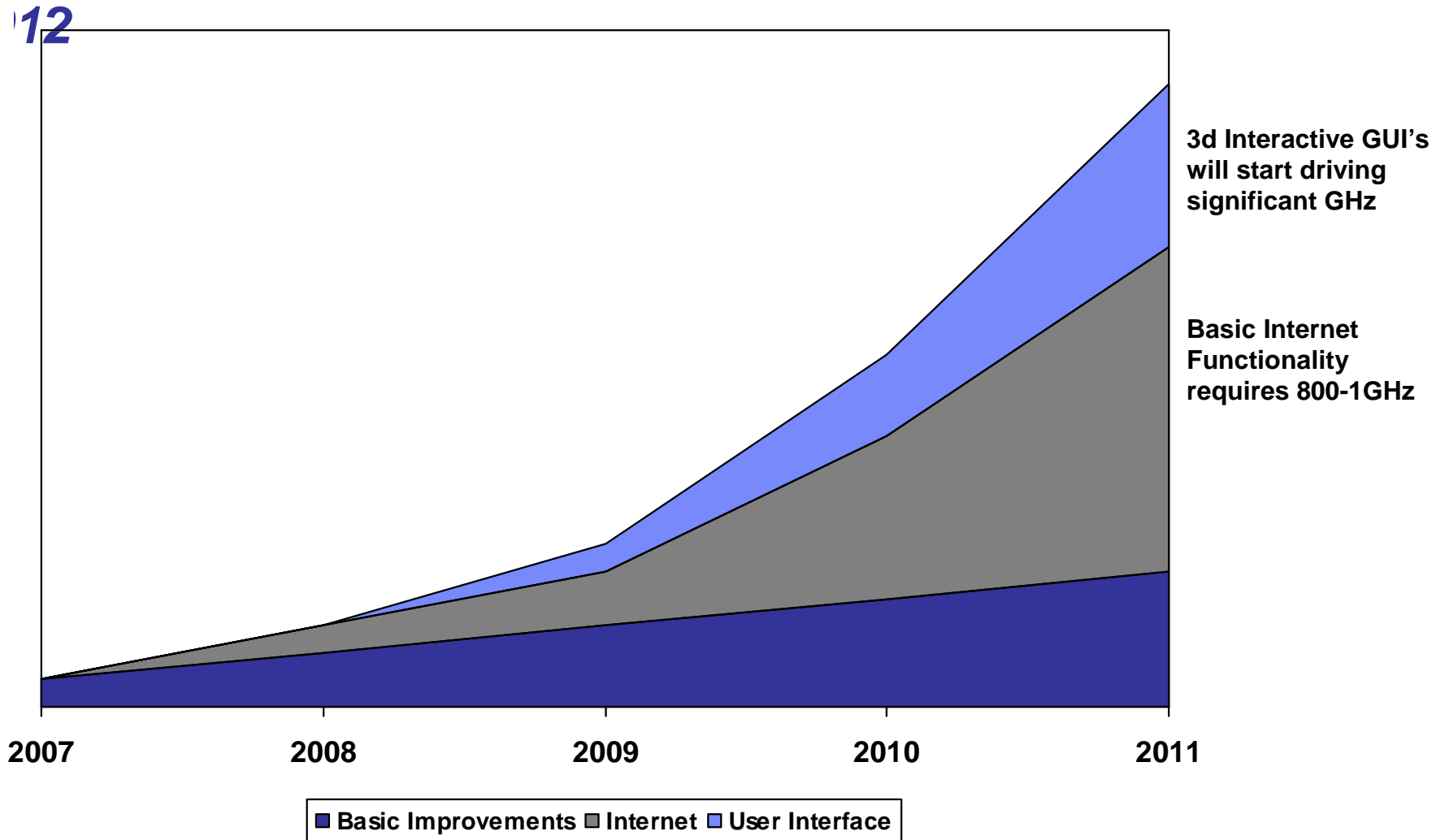
Oh....That's what the racetrack looks like

Time for some fun with Web Based Gaming



Digital Media Processing

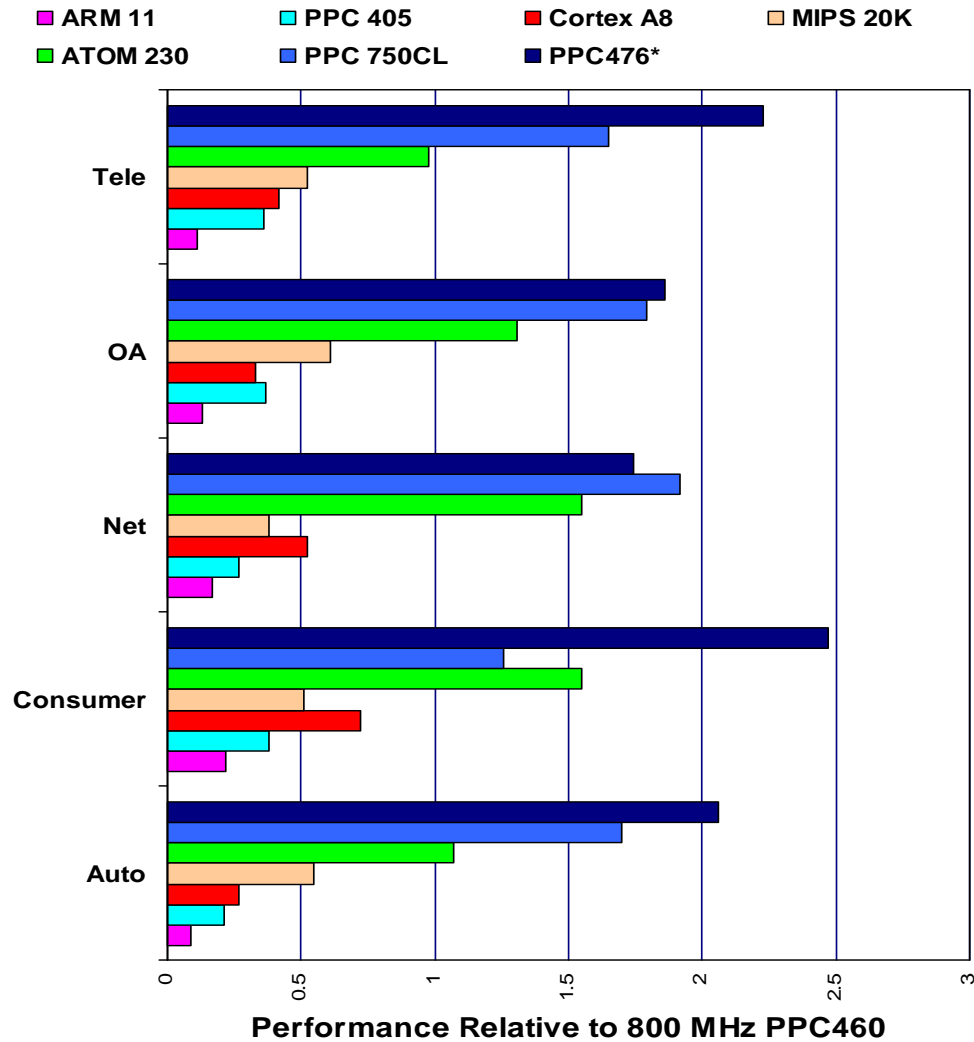
Internet + 3D GUI's will 5x processing requirements by '12






















EEMBC Demonstrates Performance of PowerPC

EEMBC v1 Benchmarks @ Speed





Multi-core Processing Platforms and Applications

Scalable Platform	Application Example
Ultra High-end multi-core	 Service Provider Routers  Network Admission Control  Storage Networks
High-end multi-core	 Metro Carrier Edge Router  IMS Controller  Radio Network Control  Data Center Switching
Mid-range multi-core	 Converged Media Gateway  SSL, IPsec, Firewall  Access Gateway
Low-end multi-core	 Unified Threat Management  VoIP Carrier-Class Media Gateway  Wireless Media Gateway  Base Station
Ultra Low-end multi-core	 Integrated Services Router  Network Attached Storage  Home Media Hub

Source: Freescale



PowerPC Ecosystem



PPC4xx Embedded core – license(1/2)

- **Hard and soft core options**

- hard (fixed layout) macro

- Available in IBM's premium process technologies or fab-optimized versions with the IBM Business Partner fabs(Chartered, Sumsung)

- soft macro

- synthesizable soft core provides the flexibility of fabrication in multiple foundries
 - Also provided in Xilinx FPGA

- <http://www-03.ibm.com/chips/power/powerpc/cores/index.html>



PPC4xx Embedded core – license(2/2)

- **Synopsys DesignWare Star IP**
 - PowerPC 405 Soft Core
 - PowerPC 460 Soft Core
 - http://www.synopsys.com/products/designware/star_ip.html

- **Xilinx Vertex FPGA**
 - Virtex™-II Pro platform FPGA
 - http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex_ii_pro_fpgas/capabilities/powerpc.htm
 - Virtex™-4 FX platform FPGA
 - http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex4/capabilities/powerpc.htm



Simulation/Emulation/EDA Tool Providers

- **No fee, source code license**

- RTL
- SystemC models
- RiscWatch code
- Instruction Set Simulator

- **Enables EDA companies to readily support PowerPC Cores**

- System Level Design
- Emulation models
- Design Flows





SoC IP Providers

SYNOPSYS

- Focus is Industry Standard IP (e.g. Ethernet, USB, GPIO, UART, etc)
- Largest IP provider after ARM
- DesignWare / StarIP distribution network
- Will provide native PLB interface as required by customers

denali

- Focus is memory controllers
- Sells CoreConnect development and verification toolkits

SafeNet

- Leading industry supplier of security IP
- Proven on recent AMCC designs

HCL

- Wide range of latency sensitive IP
- Primarily used for HCL designs



Middleware/Application Providers*



* OS and Middleware business partners of IBM and/or Freescale and/or AMCC and/or PA Semi



OS / IDE / Compiler Suppliers





Debugger Providers





PowerPC Embedded Environment Architecture

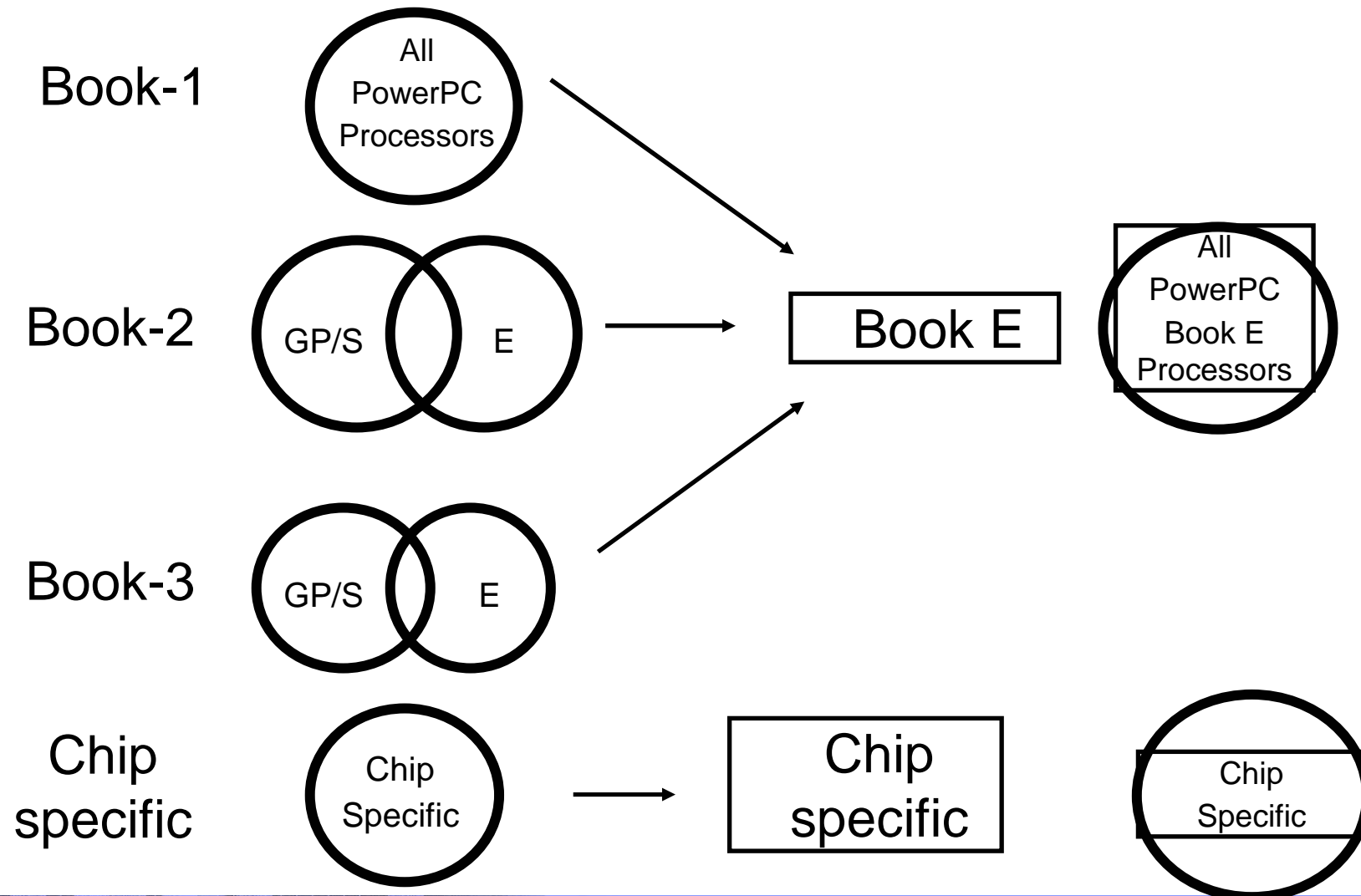


PowerPC Architecture Books

- **Original PowerPC Architecture is a layered architecture that is described in 4 "Books"**
- **Book 1 - User Instruction Set Architecture**
 - Describes the instructions and facilities in ALL PowerPC implementations
 - Compilers normally only use Book 1 facilities
 - Bulk of customer code investment normally in Book 1 code
 - Options
 - 32/64-bit Mode
 - Floating Point via emulation or hardware
- **Book 2 - Virtual Environment Architecture**
 - Processor's relationship to memory
 - Operation of caches
 - How memory-mapped I/O works
 - Atomic Operations
 - User-level timer support
- **Book 3 - Operating Environment Architecture**
 - Facilities required to build an operating system
 - Interrupts
 - Virtual Memory
 - System Call
 - Privileged Facilities
- **"Book 4" - Implementation Specifics**
 - Variations from the other books



PowerPC Embedded Environment Architecture – Book E





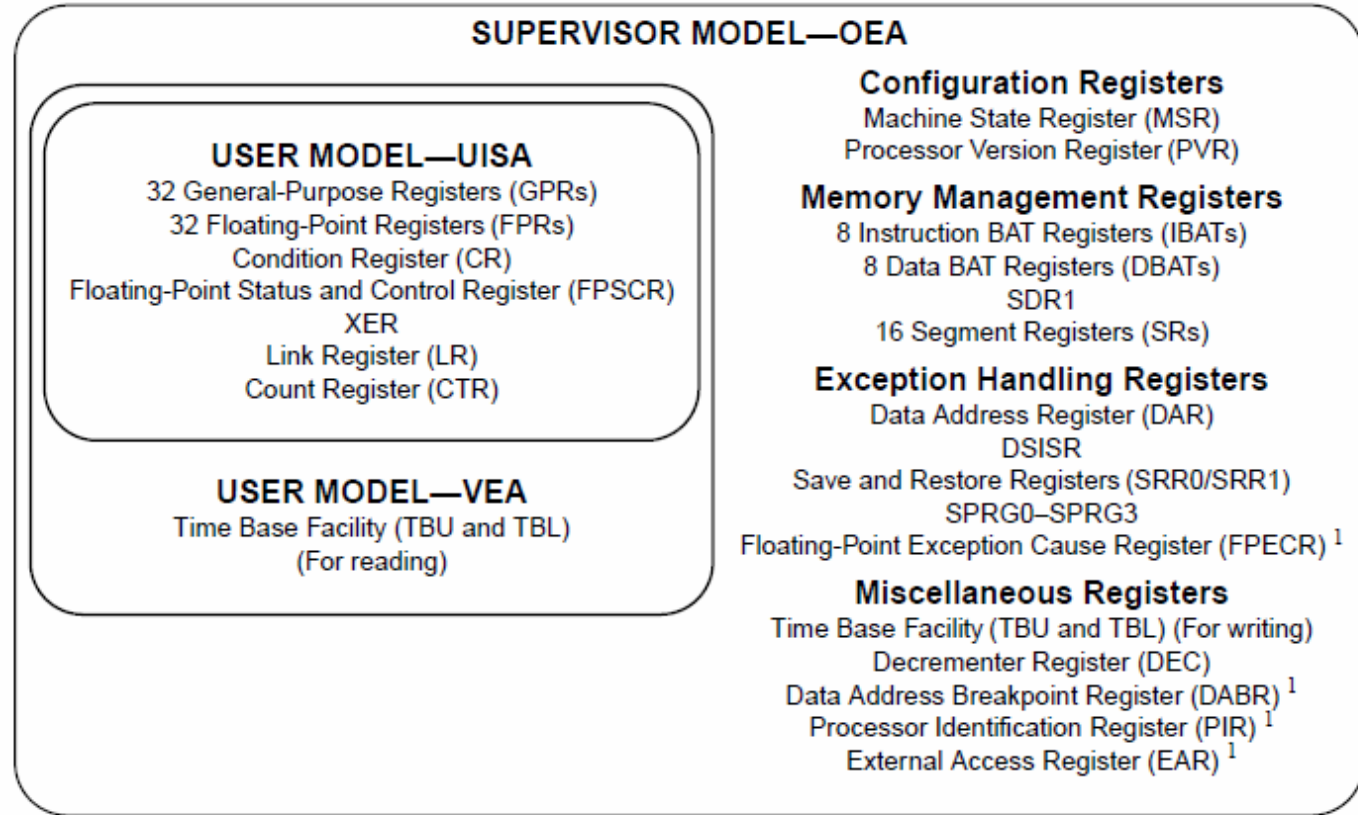
Registers Types

- **General Purpose Registers (GPRs)**
- **Floating Point Registers (FPRs)**
- **Special Purpose Registers (SPRs)**
- **Miscellaneous Registers**
 - Machine State Register (MSR)
 - Condition Register (CR)
- **Altivec Registers (VRs)**
- **Device Control Registers (DCRs)**



Register Access Mode

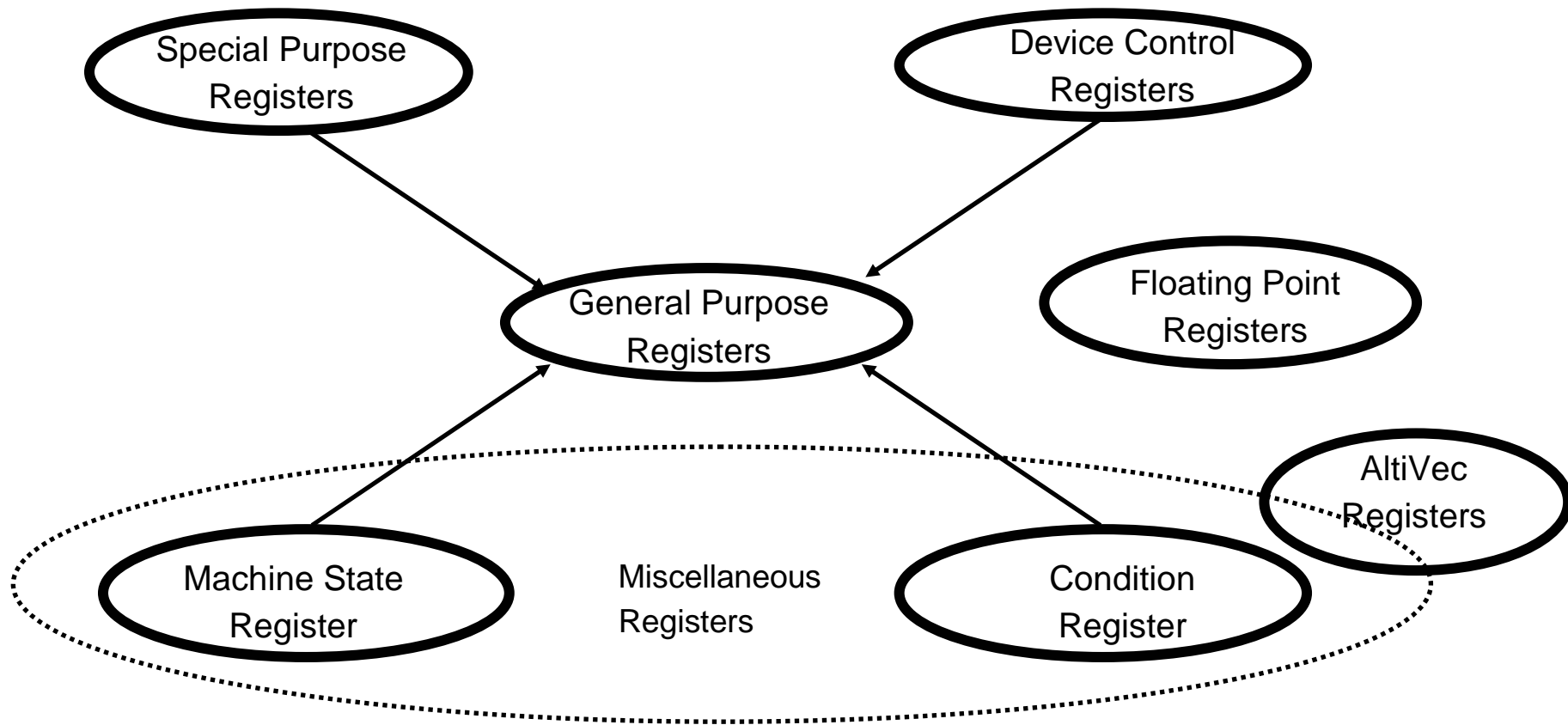
- User Model: GPRs, FPRs, CRs, FPSCR, XER, LR, CTR
- User Model – VEA: TBU & TBL
- Supervisor Model: All user model registers and Conf Regs, MM Regs, EXH Regs, MiscRegs
- Mode Switch: thru MSR



¹ Optional



Register Type



General Purpose Registers are used to move data in and out of other SPRs, DCRs, and Misc. registers



Instruction Categories

Instruction Category	Base Instructions
Data Movement	load, store
Arithmetic	add, subtract, negate, multiply, divide
DSP	Multiply accumulate and other DSP type instructions
Logical	and, or, xor, nand, nor, xnor, sign extension, count leading zeros, andc, orc
Rotate/Shift	rotate, rotate and mask, shift left, shift right
Comparison	compare algebraic, compare logical, compare immediate
Floating-Point	Load, store, move, arithmetic, comparison
Branch	branch, branch conditional, branch to LR, branch to CTR
Condition Logical	crand, crnor, crxnor, crxor, crandc, crorc, crnand, cror, cr move
Cache Control	invalidate, touch, zero, flush, store, dcread, icread
Interrupt Control	write to external interrupt enable bit, move to/from machine state register, return from interrupt, return from critical interrupt
Processor Management	system call, synchronize, eieio, move to/from device control registers, move to/from special purpose registers, mtrcf, mfcr, mtmsr, mfmsr
MMU Control	TLB search, TLB read, TLB write, TLB invalidate all, TLB synchronize



Context Synchronization

- **Context**
 - The environment in which a program executes
 - Privilege, Relocation, etc.
- **Context synchronizing events:**
 - Interrupts (MSR gets re-loaded based on exception type)
 - ISYNC, RFCI, RFI, SC instruction execution
- ***All instructions that precede a context synchronizing event must complete in the context that existed before the context synchronizing operation***
- ***All instructions that follow a context synchronizing event must complete in the context that exists after the context synchronizing operation***
- **Instruction Synchronize (ISYNC)**
 - Provides ordering for all effects of instructions executed by the processor
 - Synchronizes the instruction context, such as memory translation, endianness, cache coherency, etc.
 - Instruction pipeline is flushed and new instructions execute in the new context



Storage Synchronization

- *Enforce In/Order Execution of I/O (EIEIO)*
 - Guarantees loads and stores complete with respect to one another
 - Needed due to weakly ordered storage model
 - Book E has changed this instruction to mbar (Memory Barrier)

- *Synchronize (SYNC)*
 - Guarantees all preceding instructions complete before sync completes
 - Used to guarantee load/store completion
 - Book E has redefined this instruction to msync (Memory Synchronize). It retains the same opcode



Data Type

Byte



Halfword



Word / Single



Doubleword
(64-bit & floating pt)





Addressing Mode

- **Load and store operations have three categories of effective address generation that depend on the operands specified:**

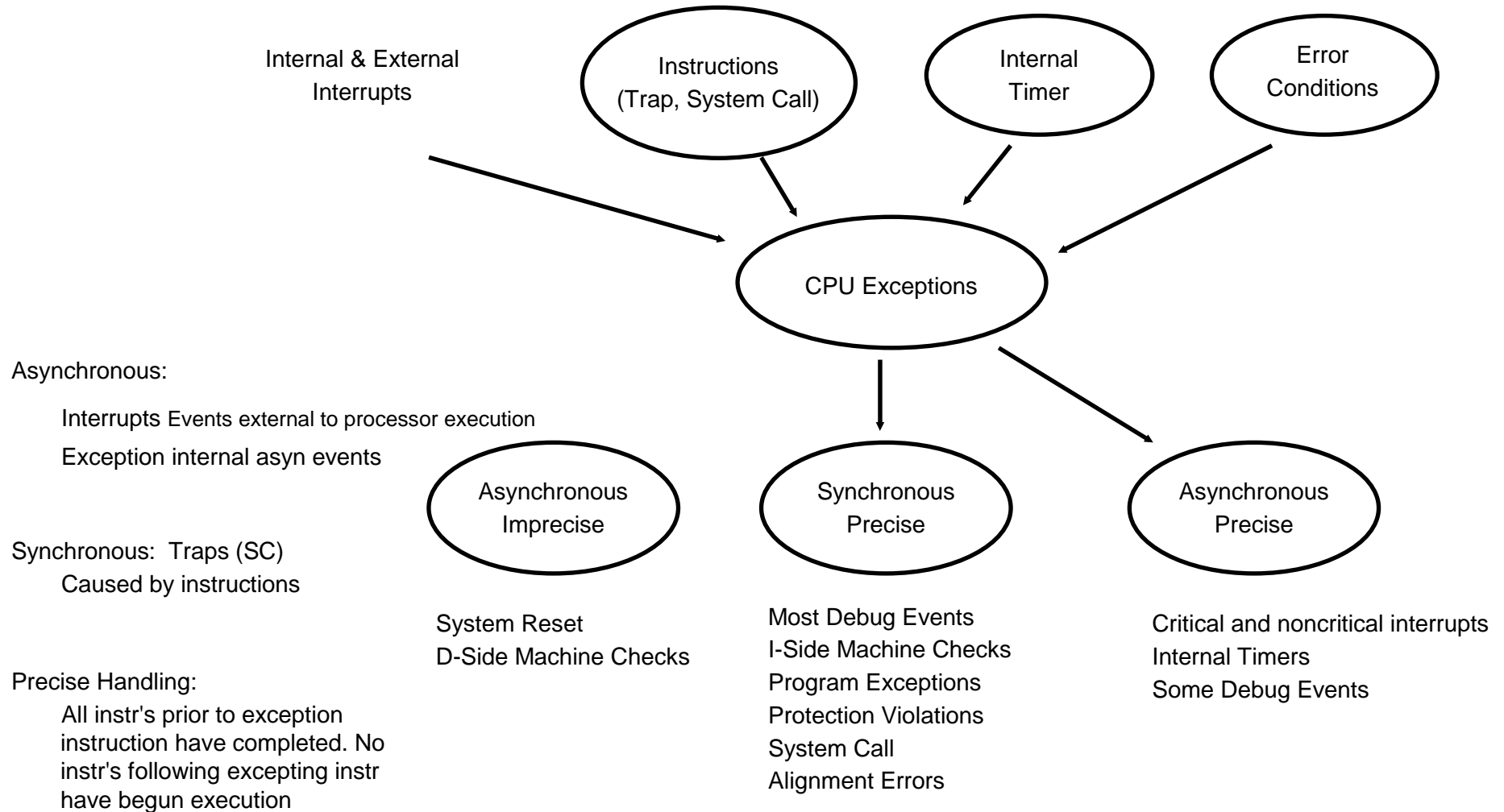
- *Register indirect with immediate index mode* `lwz r0, 4(r1)`
- *Register indirect with index mode (sum of two registers)* `lwzux r0, r1, r2`
- *Register indirect mode* `lwz r0, (r1)`

- **Branch instructions have three categories of effective address generation:**

- *Immediate addressing.* `B 0x20000`
- *Link register indirect* `lis r0, EA@h` `ori r0, EA@l` `mtlr r0` `blr`
- *Count register indirect* `lis r0, EA@h` `ori r0, EA@l` `mtctr r0` `bctr`

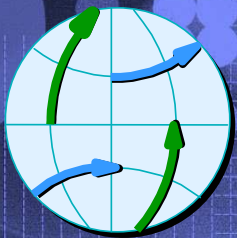


Interrupts, Exceptions, and Traps



IBM China Design Center

Thanks!



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