Power.ORG™

Webinar Series

PowerEN - An "Edge of Network Processor"

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Outline

- Four perspectives on an interconnected world – Client, Data, Infrastructure, Services
- PowerEN Design Philosophy
- Packet Processing Concepts and Terminology
- The PowerEN Processor
  - A Packet Processing Framework
  - Architecture Elements and Values

A Client Perspective

In today's economic environment, clients are telling us they need heightened focus on three essential areas…

- Higher service expectations -
  - Improve efficiencies across the business.
  - Respond to new opportunities quickly.
- Rising cost pressures -
  - Shorten ROI, remove complexities.
  - Add value now.
- New risks and threats -
  - Increase collaboration, but in a protected way.
  - Support anywhere, anytime access.

A Raw Data Perspective

An explosion of data, transactions, and digitally-aware devices strains IT infrastructure and operations.

30 billion

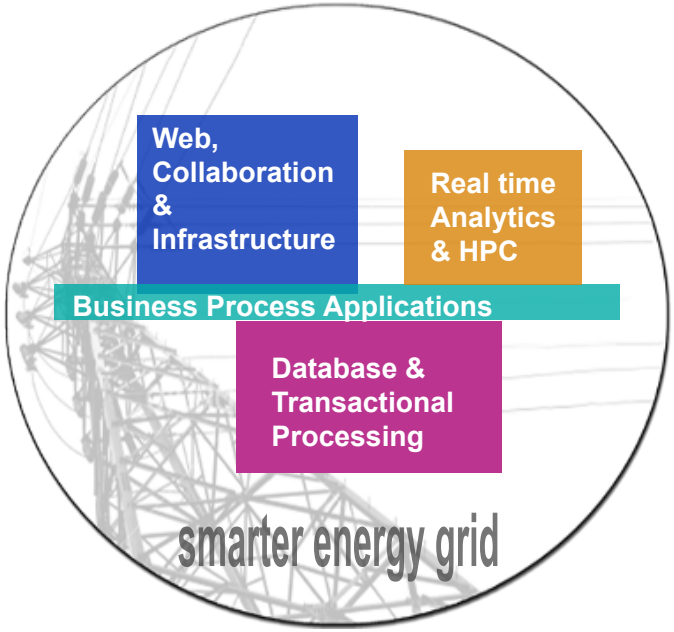
By the end of this year, 30 billion RFID tags will be embedded into our world and across entire ecosystems.

1.5x

Explosion of information driving 54% growth in storage shipments every year.

33%

33% of consumers notified of a security breach will terminate their relationship with the company they perceive as responsible.



85% idle

In distributed computing environments, up to 85% of computing capacity sits idle.

70¢ per $1

70% on average is spent on maintaining current IT infrastructures versus adding new capabilities.

35% prepared

Only 35% of mid-size company IT managers say that they are equipped to deal with a data loss.

10 billion

Mobile Internet devices projected to reach 10 billion world wide by 2015.

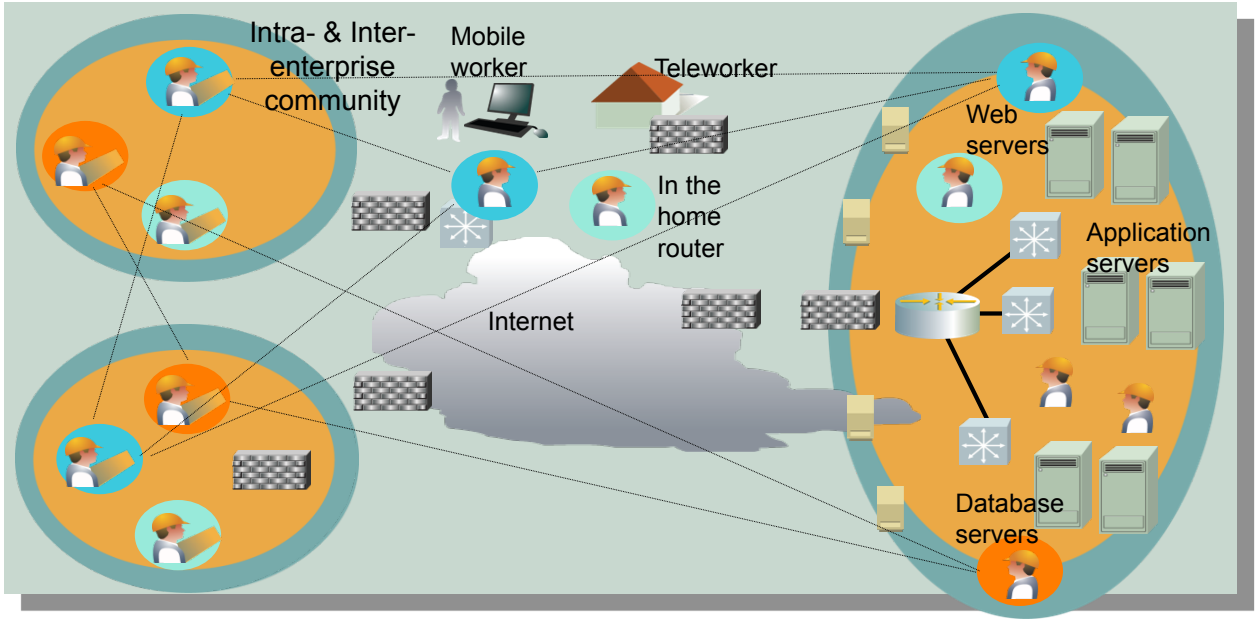
A crisis of complexity

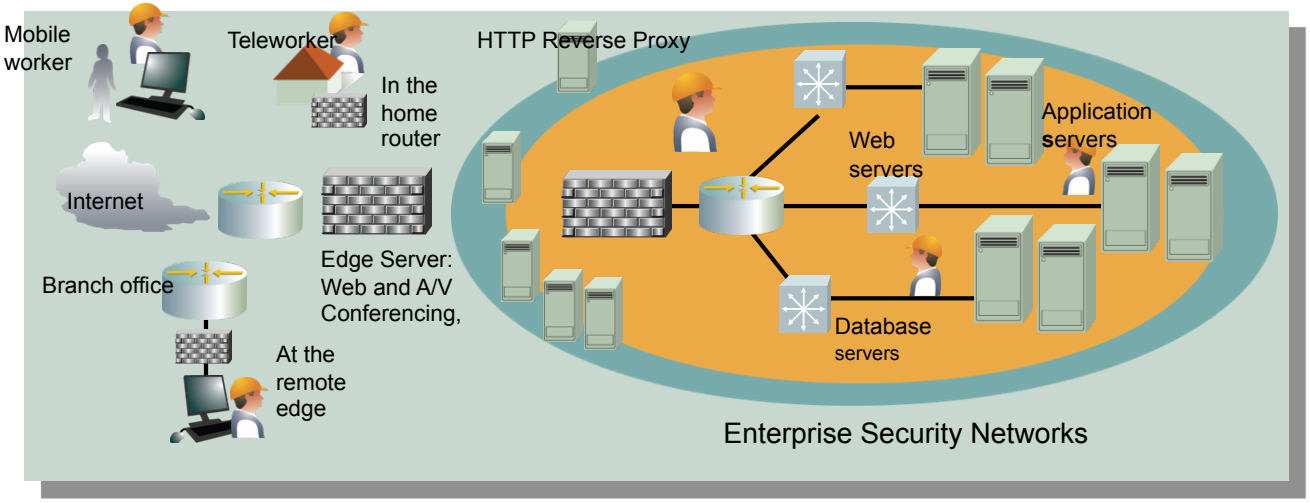
An Infrastructure Perspective

We are witnessing the rapid disappearance of the enterprise security perimeter as the current model of multiple point solutions for security is falling apart.

Drivers for opening up enterprise perimeters:

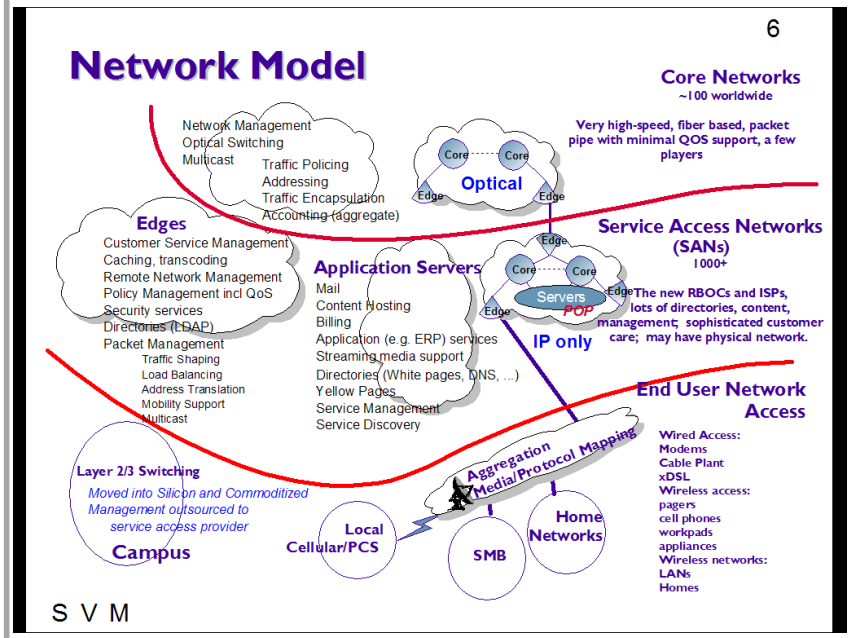
- Outsourcing
- Cross organizational collaborations and partnerships
- Mobile workers
- Ubiquitous access
- Social networks
- Web 2.0
- Cloud Computing, SaaS



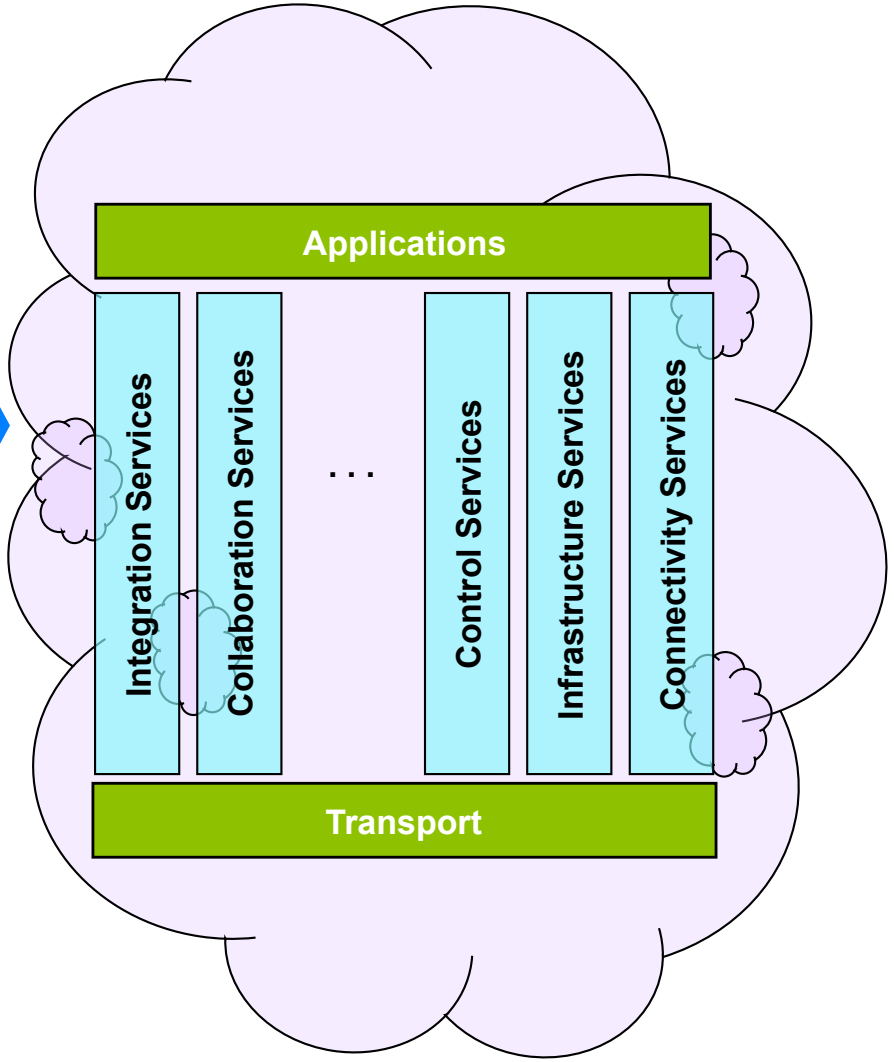


A Services Perspective

"The Network Cloud"



"The Services Cloud"



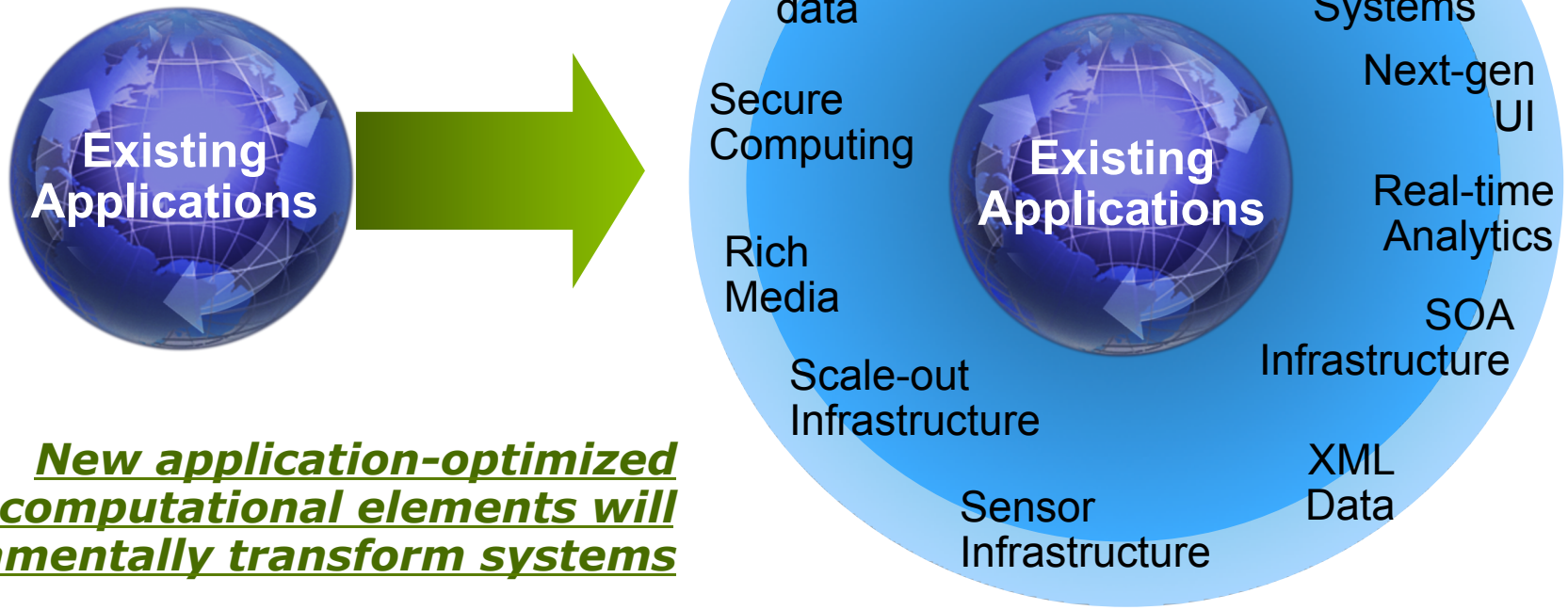
Instead of viewing the network in terms of physical segments, the network is better viewed as a collection of services.

The Transformation of the Cloud

Hybrid Systems and New Applications

Applications are emerging toward Smarter Planet and real-time capabilities

New applications will require substantial improvement in system characteristics



New application-optimized computational elements will fundamentally transform systems

PowerEN Design Philosophy

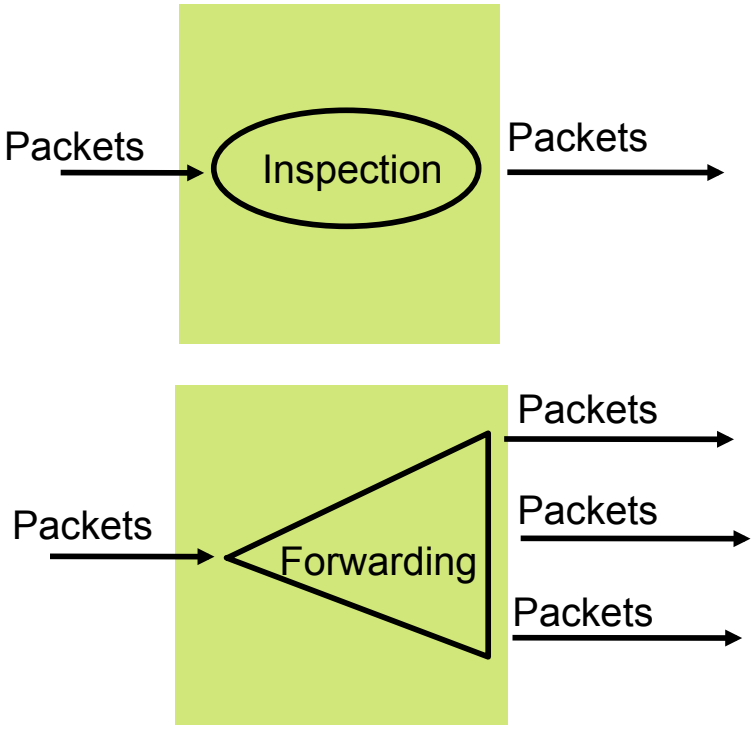
A scalable platform and an SMP programming paradigm were non-negotiable requirements.

Deconstruct the targeted application set and then define appropriate features in the processor architecture with the application set owners.

Focus on balance in the design – memory, IO, general purpose computation, acceleration via special purpose hardware, interconnect, event handling, OS and application programming contexts

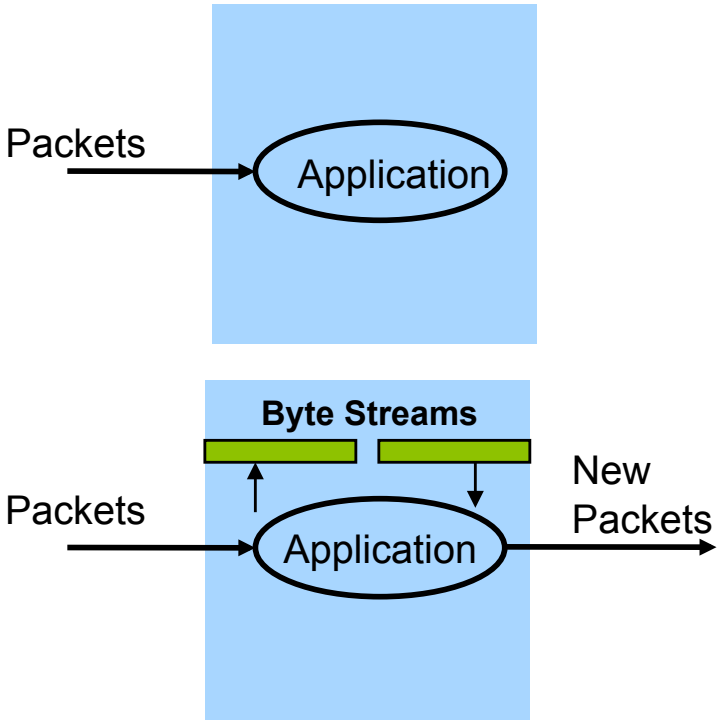
Deconstructing Networking Applications 101

Network Node



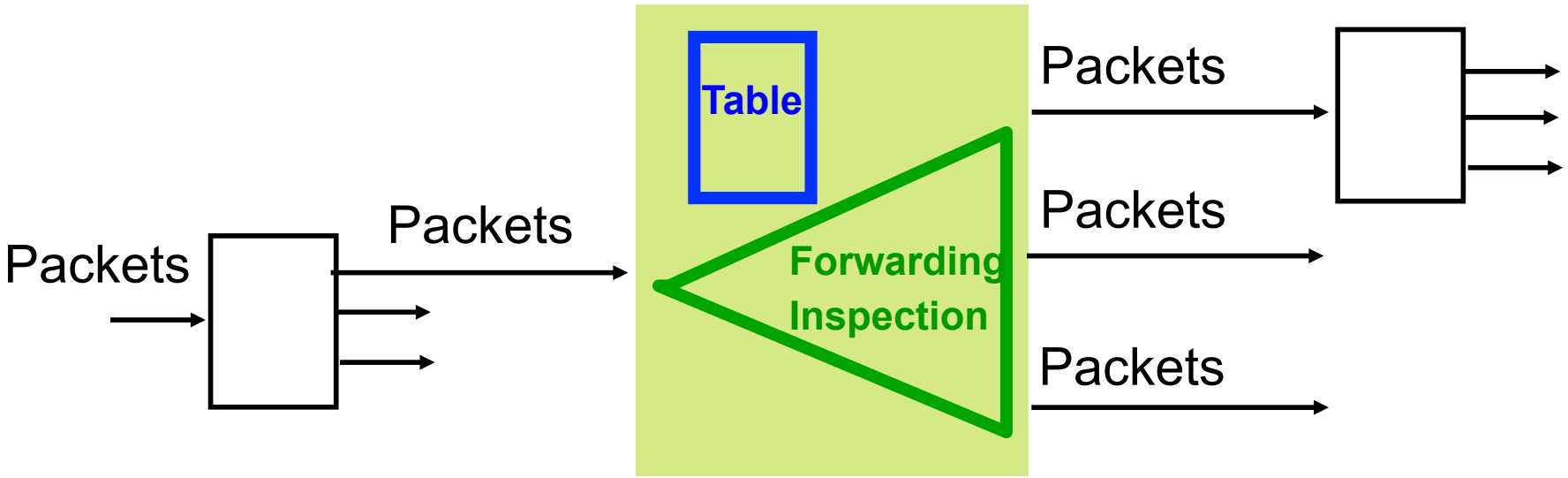
Packets may be modified but protocols are never terminated

End Point



Protocols are always terminated and new packets may be created

Data Domains: Control Plane – Data Plane



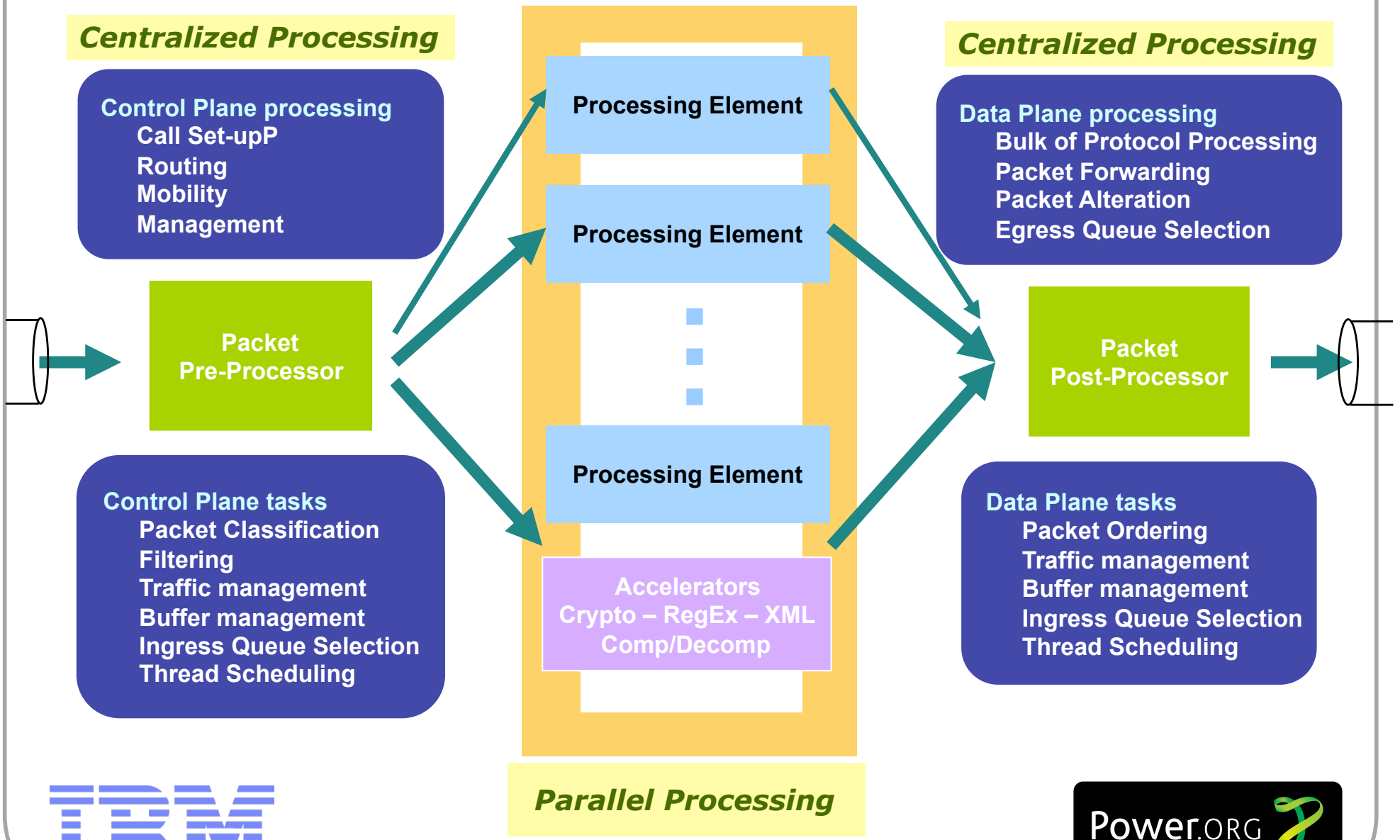
Data Plane: **Packet Forwarding, Deep Packet Inspection …**

Must follow the speed of the media ports: "Forward or Discard"

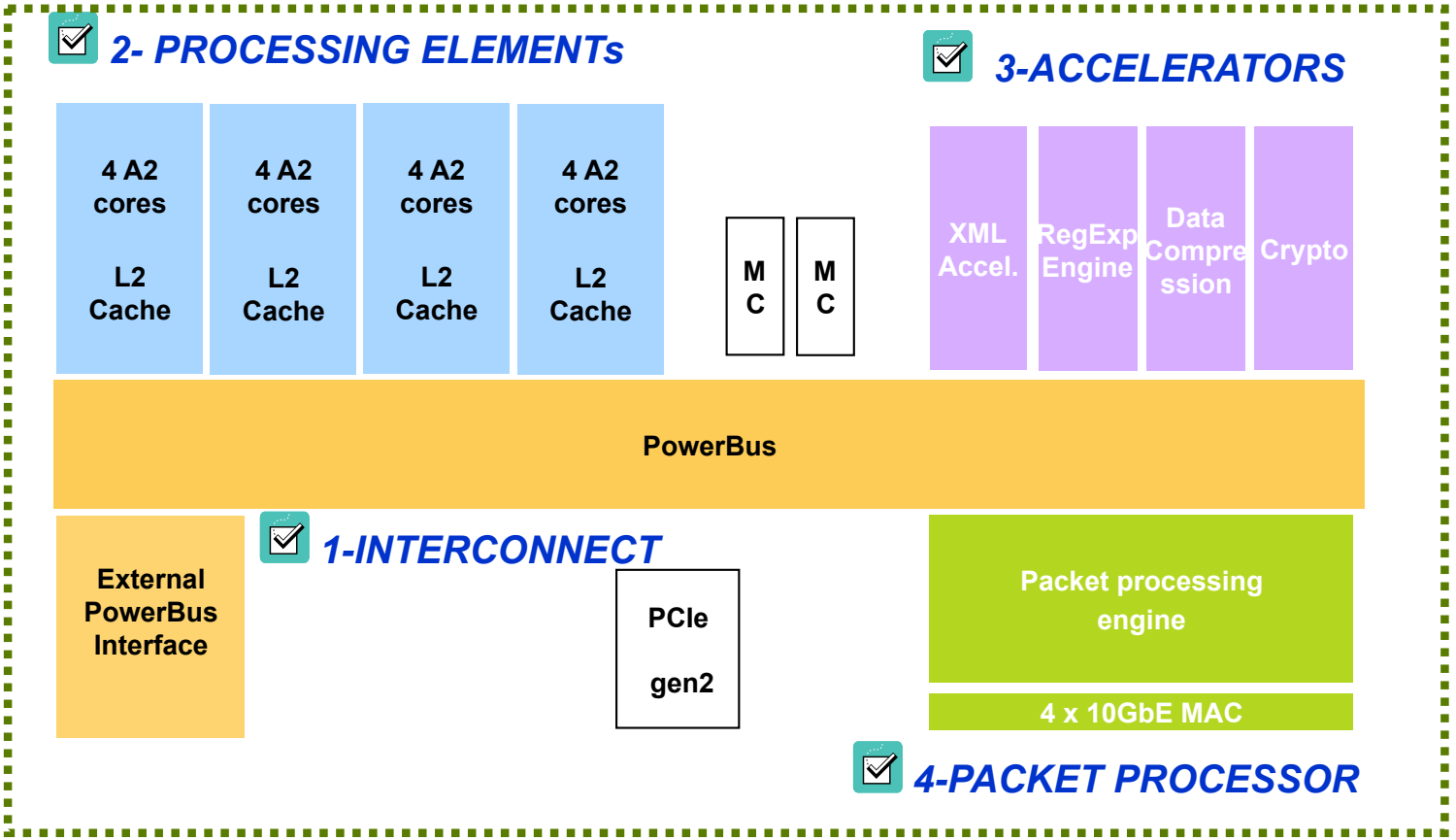
Control Plane: Update the Forwarding tables, the Inspection Rules tables …

Implies End Point functionality

Packet Processing Framework



From Framework to PowerEN Architecture



Power + accelerators integrated into a balanced SoC

PowerEN interconnect architecture

*"All Peers" a*rchitecture

- Accelerators and I/O are *first class citizen*

Proven Power-Bus architecture

- Cache coherency …

64 Byte Cache Line

- Network Application optimized Cache Line size

Forced Cache Injection

- Packets flow in / from Caches in steady state

Key Benefits

- Throughput – Latency
- SW simplification – Simple SMP model
- Scalability – Up to 4 Chip in SMP mode

PowerEN processing element architecture

Balanced Performance/Area - Compute / Throughput

Highlights

- PowerPC 64B architecture
- Enhanced instruction set for Co-processor/I/O interface
  - Initiate Co-Processor , Wait on Loss of reservation
- Multi-Threads
  - Hide Memory/ Coprocessors access latency
- Embedded MMU
- Embedded Hypervisor
- 64 Bytes Cache line

Key Benefits

- Data Plane / Control Plane dynamic load balancing
- Processing / Watt
- Virtualization - Protection

PowerEN accelerators architecture

Common Architecture for all Accelerators (Co-Processors)

Integrated in Power Architecture

- New Initiate Co-Processor Instruction
- New Wait on Loss of Reservation (Thread wake up)
- Application Context communicated to Co-Processor = Access Control

L2 Cache Intervention / Force Inject

Accelerator MMU derived from Processor MMU

- Accelerators operate in Application Adress Space

Key Benefits

- Performance
- Common API (Ease of Use)
- QOS
- Virtualization - Protection

PowerEN packet processor architecture

Offload Media Speed functions that cannot be distributed

- Packet Classification – Distribution
- Packet Ordering
- Traffic Management

Integrated architecture – Synergy with Core / Accelerators

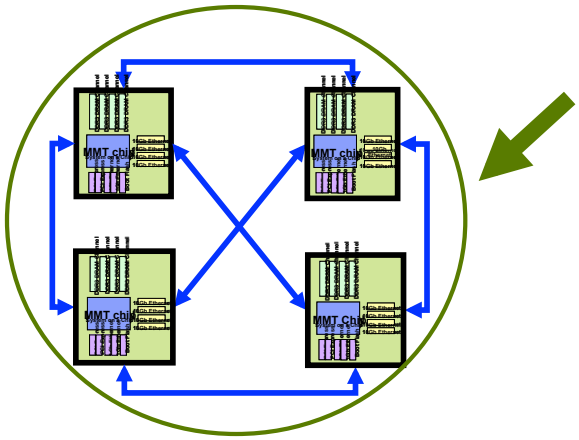
Packet Processor

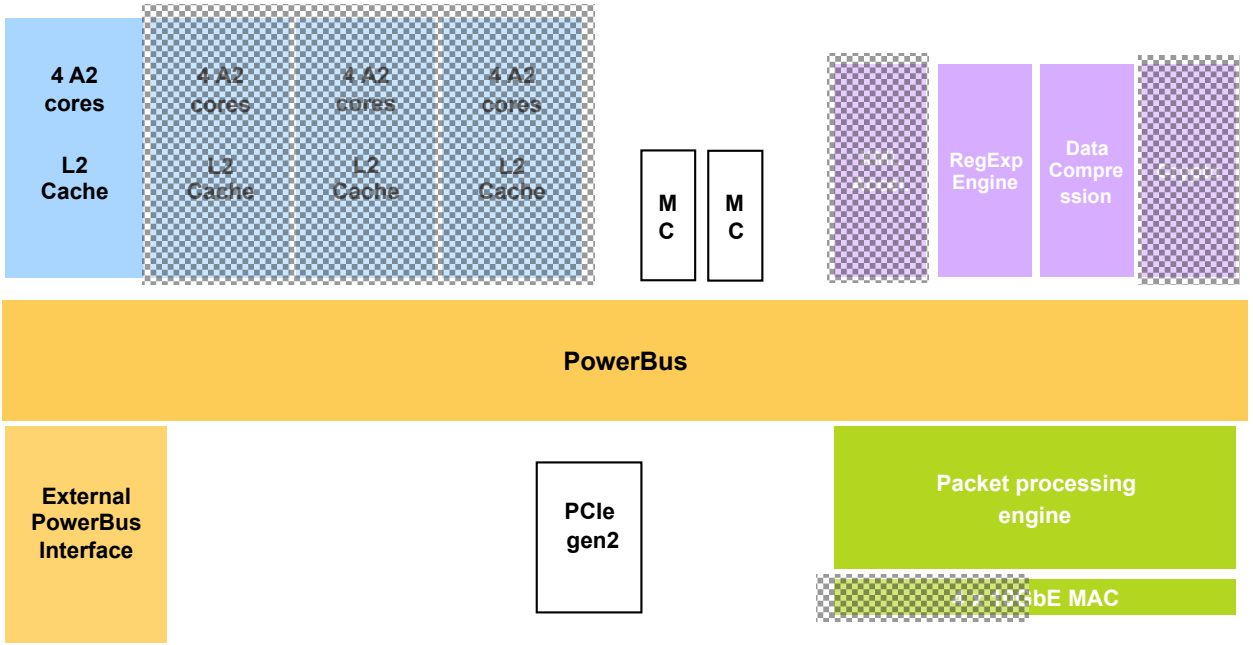
- End Point Mode (Packets to Stream)
- Network Node (Packet Forwarding)
- L2 Cache Intervention / Force Inject
- MMU derived from Processor MMU
  - Operates in Application Address Space

Key Benefits

- Performance
- SW Simplification
- QOS
- Virtualization - Protection

Scalable - UP and DOWN





PowerEN: PowerPC architecture foundation for Edge of Network processing

- *Power instruction set*
- *SMP programming paradigm*

- *Imbedded Hypervisor Support*
- *Address Spaces protection thru MMU*
- *Coprocessor Access Protection*

- *Fully Virtualized Network Interface*
- *Resource allocation and protection per Partition*
- *Fair Media access*
- *Packet processor features*
  - *Packet Classification*
  - *Core/ Thread selection and Scheduling*
  - *Packet Ordering*
  - *Traffic management QOS*
- *Integrated Network Interface*

- *Full set of Accelerators for Processing intensive functions*
- *Generic Accelerators interface architecture*
  - *"All speak the same language"*

- *High Speed Interconnect*
- *64 Bytes Cache Line*
- *Accelerator and Packet Processor Cache Inject*

- *OS Bypass : Accelerators and Packet Processor operate in Application Virtual Space*

Thank you!