DATASHEET
ADDENDUM

Intel 430MX PCIset Timing Specification

272922-001

July, 1996

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect IL 60056-764
or call 1-800-548-4725

82437MX SYSTEM CONTROLLER (MTSC) AND 82438MX DATA PATH UNIT (MTDP) FEATURES

- **Supports the Pentium® Processor at iCOMP® Index 1308/166, 1176/150, 1110/133, 1000/120, 815/100, 735/90, and 610/75 MHz**
- **Integrated Second Level Cache Controller**
  - **— Direct Mapped Organization**
  - **— Write-Back Cache Policy**
  - **— Cacheless, 256 Kbytes, and 512 Kbytes**
  - **— Standard, Burst and Pipelined Burst SRAMs**
  - **— Cache Hit Read/Write Cycle Timings at 3-1-1-1 with Burst or Pipelined Burst SRAMs**
  - **— Back-to-Back Read Cycles at 3-1-1-1-1-1-1-1 with Burst or Pipelined Burst SRAMs**
  - **— Integrated Tag/Valid Status Bits for Cost Savings and Performance**
  - **— Supports 3.3 V SRAMs and Tag Address**
- **Integrated DRAM Controller**
  - **— 64-Bit Data Path to Memory**
  - **— 4-Mbyte to 128-Mbytes Main Memory**
  - **— EDO/Hyper Page Mode DRAM (x-2-2-2 Reads) Provides Superior Cacheless Designs**
  - **— Standard Page Mode DRAMs**
  - **— 4 RAS Lines**
  - **— 4 Qword Deep Buffer for 3-1-1-1 Posted Write Cycles**
  - **— Symmetrical and Asymmetrical DRAMs**
  - **— 3 V or 5 V DRAMs**
- **Fully Synchronous 25/30/33 MHz PCI Bus Interface**
  - **— 100 Mbytes/s Instant Access Enables Native Signal Processing on Pentium Processors**
  - **— Synchronized CPU-to-PCI Interface for High Performance Graphics**
  - **— PCI Bus Arbiter: MPIIX and Three PCI Bus Masters Supported**
  - **— CPU-to-PCI Memory Write Posting with 4 Dword Deep Buffers**
  - **— Converts Back-to-Back Sequential CPU to PCI Memory Writes to PCI Burst Writes**
  - **— PCI-to-DRAM Posting of 12 Dwords**
  - **— PCI-to-DRAM up to 120 Mbytes/s Bandwidth Utilizing Snoop Ahead Feature**
- **NAND Tree for Board-level ATE Testing**
- **208-Pin QFP (MTSC), 100-Pin TQFP (MTDPs)**

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheets published for the Intel 430MX PCIset. Please refer to the standard package datasheets (order numbers 290524 for MTSC and MTDP, and 290525 for MPIIX) for product information and specifications not found in this document.

NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

82371MX PCI I/O IDE XCELERATOR (MPIIX) FEATURES

- **Supports the Pentium® Processor at iCOMP® Index 1308/166, 1176/150, 1110/133, 1000/120, 815/100, 735/90, and 610/75 MHz**
- **Provides a Bridge Between the PCI Bus and Extended I/O Bus**
  - **— PCI Bus; 25–33 MHz**
  - **— Extended I/O Bus; 7.5–8.33 MHz**
- **System Power Management (Intel SMM Support)**
  - **— Programmable System Management Interrupt (SMI)—Hardware/Software Events, EXTSMI#**
  - **— Programmable CPU Clock Control (STPCLK#) with Auto Clock Throttle**
  - **— Peripheral Device Power Management (Local Standby)**
  - **— Suspend State Support (Suspend-to-DRAM and Suspend-to-Disk**
- **Enhanced DMA Functions**
  - **— Two 8237 DMA Controllers**
  - **— Compatible DMA Transfers**
  - **— PC/PCI DMA Expansion for Docking Support**
- **Fast IDE Interface**
  - **— PIO Mode 4 Transfers**
  - **— 2x16-Bit Posted Write Buffer and 1x32-Bit Read Prefetch Buffer**
- **Plug-n-Play Port for Motherboard Devices**
  - **— 3 Steerable DMA Channels**
  - **— 1 Steerable Interrupt Line (Plus 2 Steerable PCI Interrupts)**
  - **— 1 Programmable Chip Select**
- **Functionality of One 82C54 Timer**
  - **— System Timer**
  - **— Refresh Request**
  - **— Speaker Tone Output**
- **Functionality of Two 82C59 Interrupt Controllers**
  - **— 14 Interrupts Supported**
  - **— Independently Programmable for Edge/Level Sensitivity**
- **X-Bus Peripheral Support**
  - **— Chip Select Decode**
  - **— Controls Lower X-Bus Data Byte Transceiver**
- **Non-Maskable Interrupts (NMI) - PCI System Error Reporting**
- **NAND Tree for Board-level ATE Testing**
- **176-Pin TQFP**

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheets published for the Intel 430MX PCIset. Please refer to the standard package datasheets (order numbers 290524 for MTSC and MTDP, and 290525 for MPIIX) for product information and specifications not found in this document.

NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

Intel 430MX PCIset Timing Specification

FIGURES

TABLES

1.0 82437MX (MTSC) and 82438MX (MTDP) SPECIFICATIONS

1.1 Absolute Maximum Ratings

Case Temperature Under Bias .....0°C to +85°C
Storage Temperature ..... -55°C to +150°C
Supply Voltage with respect to ground ..... -0.3 V to V_{DD} + 0.3 V
Supply Voltage with respect to V_{SS} .....-0.3 V to +6.5 V

Maximum Power Dissipation
MTSC: ..... 2.0 W
MTDP: ..... 1.0 W

WARNING*: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

1.2 Thermal Characteristics

The 82437MX MTSC is designed for operation at case temperatures between 0°C and 85°C. The thermal resistances of the 82437MX MTSC QFP package are given in Table 1.

Table 1. 82437MX MTSC Package Thermal Resistance

Parameter	Air Flow 0.0 Meters/Second
θ_{JA}	32°C/W
θ_{JC}	8°C/W

The 82438MX MTDP is designed for operation at case temperatures between 0°C and 85°C. The thermal resistances of the 82438MX MTDP TQFP package are given in Table 2.

Table 2. 82438MX MTDP Package Thermal Resistance

Parameter	Air Flow 0.0 Meters/Second
θ_{JA}	50°C/W
θ_{JC}	13°C/W

1.3 Electrical Characteristics

1.3.1 DC Characteristics

Table 3. MTSC DC Characteristics
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	-0.3	0.8	V	Note 1, V_{DD3}=3.135 V
V_{IH1}	Input High Voltage	2.2	V_{DD3} + 0.3	V	Note 1, V_{DD3}=3.465 V
V_{IL2}	Input Low Voltage	-0.3	0.8	V	Note 2, V_{DD}=4.75 V
V_{IH2}	Input High Voltage	2.2	V_{DD} + 0.3	V	Note 2, V_{DD}=5.25 V
V_{IL3}	Input Low Voltage	0.0	0.2 V_{DDR}	V	Note 3
V_{IH3}	Input High Voltage	0.8 V_{DDR}	V_{DDR} + 0.3	V	Note 3
V_{OL}	Output Low Voltage		0.4	V	Note 4
V_{OH}	Output High Voltage	2.4		V	Note 4
I_{OL1}	Output Low Current		1	mA	
I_{OH1}	Output High Current	-1		mA	
I_{OL2}	Output Low Current		3	mA	Note 5
I_{OH2}	Output High Current	-2		mA	Note 5
I_{OL3}	Output Low Current		6	mA	Note 6
I_{OH3}	Output High Current	-2		mA	Note 6
I_{IL1}	Input Leakage Current		±10	µA	
I_{IL2}	Input Leakage Current		±300	µA	Note 7
I_{DD}	V_{DD} Supply Current		345	mA	Note 8, 5 V Periphery and Core
			7		Note 8, “5 V/3 V well” DRAM
			15		Note 8, 3 V DRAM
			17		Note 8, 3 V Periphery
C_{IN}	Input Capacitance		12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1 MHz

NOTES:

1. V_{IL1} and V_{IH1} apply to the following signals: A[31:3], BE[7:0]#, D/C#, W/R#, M/IO#, HLOCK#, ADS#, HITM#, CACHE#, SMIACT#, TIO[7:0], PLINK[15:0]
2. V_{IL2} and V_{IH2} apply to the following signals: PCIRST#, AD[31:0], C/BE[3:0]#, LOCK#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, REQ[2:0], PCMD[1:0], PCLKIN, HCLKIN
3. V_{IL3} and V_{IH3} apply to the following signals: PWROK, PWRSD, RTCCLK. The voltage reference is to the V_{DDR} “resume well” pin voltage.
4. V_{OL1} and V_{OH1} apply to the following signals: TIO[7:0], TWE#, CADV#/CA4, CADS#/CA3, COE#, CWE[7:0]#, A[31:3], KEN#, AHOLD, BRDY#, NA#, BOFF#, EADS#, PLINK[15:0], PCMD[1:0], MSTB#, MADV#, HOE#, POE#, MOE#, MA[1:0], MA[11:2], CAS[7:0]#, WE#, AD[31:0], CCS#, RAS[3:0]#, GNT[2:0]#, PHLDA, C/BE[3:0]#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, LOCK#
5. I_{OL2} and I_{OH2} apply to the following signals: AD[31:0], C/BE[3:0]#, PAR
6. I_{OL3} and I_{OH3} apply to the following signals: FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, LOCK#, GNT[2:0]#
7. I_{IL2} applies to REQ[3:0]#, PHOLD, CWE#[7:0], CADV#, CADS#.. These signals have internal pullups.
8. This value was determined using worst case instruction mix and at V_{DD} = V_{DDMAX}. See Application Note AP-734, *Intel 430MX PCIset Power Measurement Analysis* (order number 272923-001) for complete power consumption data.

Table 4. MTDP DC Characteristics
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	-0.3	0.8	V	Note 1, V_{DD}=3.135 V
V_{IH1}	Input High Voltage	2.2	V_{DD3} + 0.3	V	Note 1, V_{DD}=3.465 V
V_{IL2}	Input Low Voltage	-0.3	0.8	V	Note 2, V_{DDM}=3.135 V/4.75 V
V_{IH2}	Input High Voltage	2.2	V_{DDM} + 0.3	V	Note 2, V_{DDM}=3.465 V/5.25 V
V_{OL1}	Output Low Voltage		0.4	V	Note 3
V_{OH1}	Output High Voltage	V_{DDM} - 0.5		V	Note 3
I_{OL1}	Output Low Current		1	mA	
I_{OH1}	Output High Current	-1		mA	
I_{IH}	Input Leakage Current		+10	µA	
I_{IL}	Input Leakage Current		-10	µA	
I_{DD}	V_{DD} Supply Current		110 30 90	mA	Note 4, 3 V Host and Plink Note 4, 5 V Core Note 4, MD bus
C_{IN}	Input Capacitance		12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1 MHz

NOTES:

1. V_{IL1} and V_{IH1} apply to the following signals: HD[31:0], MOE#, POE#, HOE#, MADV#, MSTB#, PCMD[1:0], PLINK[7:0]
2. V_{IL2} and V_{IH2} apply to the following signals: MD[31:0], and is dependent on V_{DDM} strapping.
3. V_{OL} and V_{OH} apply to the following signals: MD[31:0], and is dependent on V_{DDM} strapping.
4. This value was determined using worst case instruction mix and at V_{DD} = V_{DDMAX}. See Application Note AP-734, *Intel 430MX PCIset Power Measurement Analysis* (order number 272923-001) for complete power consumption data.

1.3.2 82437MX (MTSC) AC Characteristics

All timings are in nanoseconds (ns), unless otherwise specified.

Table 5. Host Clock Timing
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig.	Notes
t1	HCLKIN Period	15		3	
	HCLKIN Period Stability		±250 ps		
t3	HCLKIN High Time	5.5		3	
t4	HCLKIN Low Time	5.5		3	
t5	HCLKIN Rise Time		1.2	3	
t6	HCLKIN Fall Time		1.2	3	

Table 6. CPU Interface Timing
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig.	Notes
t7	ADS# Setup Time to HCLKIN Rising	5.0		8	
t7	W/R# Setup Time to HCLKIN Rising	6.0		8	
t8	BE[7:0]# Setup Time to HCLKIN Rising	5.0		8	
t10	HITM# Setup Time to HCLKIN Rising	6.0		8	
t11	CACHE# Setup Time to HCLKIN Rising	5.0		8	
t11	M/IO# Setup Time to HCLKIN Rising	6.0		8	
t12	D/C# Setup Time to HCLKIN Rising	5.0		8	
t13	HLOCK#, SMIACT# Setup Time to HCLKIN Rising	5.0		8	
t14	ADS#, HITM#, W/R#, M/IO#, D/C#, HLOCK#, CACHE#, SMIACT#, BE[7:0]# Hold Time from HCLKIN Rising	1.0		8	
t15	A[31:3] Setup Time to HCLKIN Rising	3.0		8	
t16	A[31:3] Hold Time from HCLKIN Rising	1.0		8	
t17	A[31:3] Output Enable From HCLKIN Rising	0.0	13.0		
t18	A[31:3] Valid Delay from HCLKIN Rising	2.0	13.0	7	1
t19	A[31:3] Float Delay from HCLKIN Rising	0.0	13.0	9	
t20	BRDY# Rising Edge Valid Delay from HCLKIN Rising	1.5	8.0	7	1
t21	BRDY# Falling Edge Valid Delay from HCLKIN Rising	1.5	8.5	7	1
t22	NA# Valid Delay from HCLKIN Rising	1.5	8.0	7	1
t23	AHOLD Valid Delay from HCLKIN Rising	1.5	7.0	7	1
t24	BOFF# Valid Delay from HCLKIN Rising	1.5	7.0	7	1
t25	EADS#, INV Valid Delay from HCLKIN Rising	1.5	7.0	7	1
t26	KEN# Valid Delay from HCLKIN Rising	1.5	7.0	7	1

NOTE:
1. 0 pF test load.

Table 7. Second Level Cache Timing
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig.	Notes
Asynchronous and Burst SRAMs					
t27	COE# Valid Delay from HCLKIN Rising	2.0	9.0	7	1
t28	TIO [7:0] Valid Delay from HCLKIN Rising	2.0	9.0	7	1
t28a	TIO[7:0] Flow Thru Delay to BRDY#, NA#, CWE[7:0]#	2.0	10.0	10	
t29	TIO[7:0] Setup time to HCLKIN Rising	2.0		8	
t30	TIO[7:0] Hold time from HCLKIN Rising	2.0		8	
t31	TWE# Valid Delay from HCLKIN Rising	2.0	9.0	7	1
Asynchronous SRAMs Only					
t32	CWE[7:0]# Valid Delay from HCLKIN Rising	3.0	13.0	7	1
t33	CA[4:3]# Valid Delay from HCLKIN Rising	1.5	7.0	7	1
Burst SRAMs Only					
t34	CWE[7:0]# Valid Delay from HCLKIN Rising	2.0	9.5	7	1
t35	CCS# Valid Delay from HCLKIN Rising	1.5	7.0	7	1
t36	CADS# Valid Delay from HCLKIN Rising	1.5	7.0	7	1
t37	CADV# Valid Delay from HCLKIN Rising	1.5	7.0	7	1

NOTE:
1. 0 pF test load.

Table 8. DRAM Interface Timing
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig.	Notes
t39a	WE# Setup to RAS[3:0]# (CBR and Self-Refresh)	13		1, 2	tWRP
t39b	WE# Hold to RAS[3:0]# (CBR and Self-Refresh)	13		1, 2	tWRH
t39c	WE# Valid Delay from HCLKIN Rising	1.5	8.0	7	1
t40a	RAS[3:0]# Pulse Width Low (CBR Refresh)	5		1, 2	HCLKs
t40b	RAS[3:0]# Pulse Width High (Exiting Self- Refresh)	170		1, 2	tRPS
t40c	RAS[3:0]# Pulse Width Low (Entering Self- Refresh)	110 µs		1, 2	tRASS
t41a	CAS[7:0]# Setup to RAS[3:0]# (CBR Refresh)	8		1, 2	tCSR
t41b	CAS[7:0]# Hold to RAS[3:0]# (CBR Refresh)	18		1, 2	tCHR
t42	RAS[3:0]# Valid Delay from HCLKIN Rising	1.5	8.0	7	1
t42a	MOE# Valid Delay from HCLKIN Rising	1.5	8.0	7	
t44	CAS[7:0]# Valid Delay from HCLKIN Rising	1.5	9.0	7	1
t46	MA[11:2] Valid Delay from HCLKIN Rising	2.0	10.0	7	1
t47a	MA[1:0] Valid Delay from HCLKIN Rising	2.0	9.0	7	1
t47b	MA[11:2] Flow Through Delay from HCLKIN Rising	2.0	13.5	10	Lead-off, 0 pF
t47c	MA[1:0] Flow Through Delay from HCLKIN Rising	2.0	13.5	10	Lead-off, 0 pF
t47d	MA[11:2] Valid Delay from HCLKIN Rising for a PCI-to-DRAM Read Cycle	2.0	17.0	7	Lead-off, 0 pF
t47e	MA[11:2] Valid Delay from HCLKIN Rising for a Write Cycle	2.0	19.0	7	Lead-off, 0 pF

NOTE:
1. 0 pF test load.

Table 9. PCI Clock Timing
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig.	Notes
t48	PCLKIN Period	30.0		4	
t49	PCLKIN High Time	12.0		4	
t50	PCLKIN Low Time	12.0		4	
t51	PCLKIN Rise Time		3.0	4	
t52	PCLKIN Fall Time		3.0	4	

Table 10. PCI Interface Timing
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig.	Notes
t53	AD[31:0] Valid Delay from PCLKIN Rising	2	11	7	Min: 0 pF Max: 50 pF
t54	AD[31:0] Setup Time to PCLKIN Rising	7		8	
t55	AD[31:0] Hold Time from PCLKIN	0		8	
t56	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL#, CLKRUN# Valid Delay from PCLKIN Rising	2	11	7	Min: 0 pF Max: 50 pF
t57	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL#, CLKRUN# Output Enable Delay from PCLKIN Rising	2		7	
t58	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL#, CLKRUN# Float Delay from PCLKIN Rising	2	28	9	
t59	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL#, CLKRUN# Setup Time to PCLKIN Rising	7		8	
t60	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL#, CLKRUN# Hold Time from PCLKIN Rising	0		8	
t61	PHLDA# Valid Delay from PCLKIN Rising	2	9	7	Min: 0 pF Max: 50 pF
t65	PHLD# Setup Time to PCLKIN Rising	12		8	
t66	PHLD# Hold Time from PCLKIN Rising	0		8	
t67	GNT[2:0] # Valid Delay from PCLKIN Rising	2	9	7	Min: 0 pF Max: 50 pF
t68	REQ[2:0]# Setup Time to PCLKIN Rising	8		8	
t69	REQ[2:0]# Hold Time from PCLKIN Rising	0		8	
t70	RST# Low Pulse Width	1 ms		11	

Table 11. MTDP Interface Timing
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig.	Notes
t71	HOE# Valid Delay from HCLKIN Rising	1.5	7.0	7	1
t72	MOE# Valid Delay from HCLKIN Rising	1.5	7.0	7	1
t73	POE# Valid Delay from HCLKIN Rising	1.5	7.0	7	1
t74	MSTB# Valid Delay from HCLKIN Rising	1.5	7.0	7	1
t75	MADV# Valid Delay from HCLKIN Rising	1.5	7.0	7	1
t76	PCMD [1:0] Valid Delay from HCLKIN Rising	1.5	7.0	7	1
t77	PLINK[15:0] Valid Delay from HCLKIN Rising	2.0	7.5	7	1
t78	PLINK[15:0] Setup Time to PCLKIN Rising	3.0		8	
t79	PLINK[15:0] Hold Time from PCLKIN Rising	2.5		8	

NOTE:
1. 0 pF test load.

1.3.3 82438MX (MTDP) AC Characteristics

Table 12. Host Clock Timing
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig.	Notes
t80	HCLK Period	15.0		3	
t81	HCLK High Time	5.5		3	
t82	HCLK Low Time	5.5		3	
t83	HCLK Rise Time		1.2	3	
t84	HCLK Fall Time		1.2	3	
t85	HCLK Period Stability		±250 ps		

Table 13. Command Signal Timing
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig.	Notes
t86	MOE# Setup Time to HCLKIN Rising	3		8	
t87	MOE# Hold Time to HCLKIN Rising	1.5		8	
t88	HOE# Setup Time to HCLKIN Rising	3		8	
t89	HOE# Hold Time to HCLKIN Rising	1.5		8	
t90	POE# Setup Time to PCLKIN Rising	3		8	
t91	POE# Hold Time to PCLKIN Rising	1.5		8	
t92	MADV# Setup Time to HCLKIN Rising	5		8	
t93	MADV# Hold Time from HCLKIN Rising	1.5		8	
t94	MSTB# Setup Time to HCLKIN Rising	3		8	
t95	MSTB# Hold TIme to HCLKIN Rising	1.5		8	
t96	PCMD [1:0] Setup Time to HCLKIN Rising	4		8	
t97	PCMD [1:0] Hold Time to HCLKIN Rising	1.5		8	
t98	PLINK [7:0] Setup Time to HCLKIN Rising	3		8	
t99	PLINK [7:0] Hold Time to HCLKIN Rising	2		8	
t100	PLINK [7:0] Output Valid Delay to HCLKIN Rising	2	9	7	1

NOTE:
1. 0 pF test load.

Table 14. Address/Data Timing
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig.	Notes
t101	D[31:0] Valid Delay from HCLKIN Rising	1.4	7.5	7	1
t102	D[31:0] Setup Time to HCLKIN Rising Host Bus	3		8	
t103	D[31:0] Hold Time from HCLK Rising Host Bus	1.5		8	
t104	MD[31:0] Valid Delay from HCLKIN Rising	1.7	11	7	1
t105	MD[31:0] Setup Time to MADV# Falling	3		8	
t106	MD[31:0] Hold Time from MADV# Falling	1		8	

NOTE:
1. 0 pF test load.

1.3.4 Clocking Relationship AC Characteristics

Table 15. Host CLK to PCI CLK Relationship TIMING
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig.	Notes
t107	HCLKIN-MTSC to CLK-CPU Skew		300 ps	5	at 1.5V
t108	HCLKIN-MTSC to PCLKIN-MTSC	1	7	5	at 1.5V
t109	HCLKIN to HCLK-SRAM/MTDP Skew		1	5	at 1.5V

1.3.5 AC Timing Diagrams

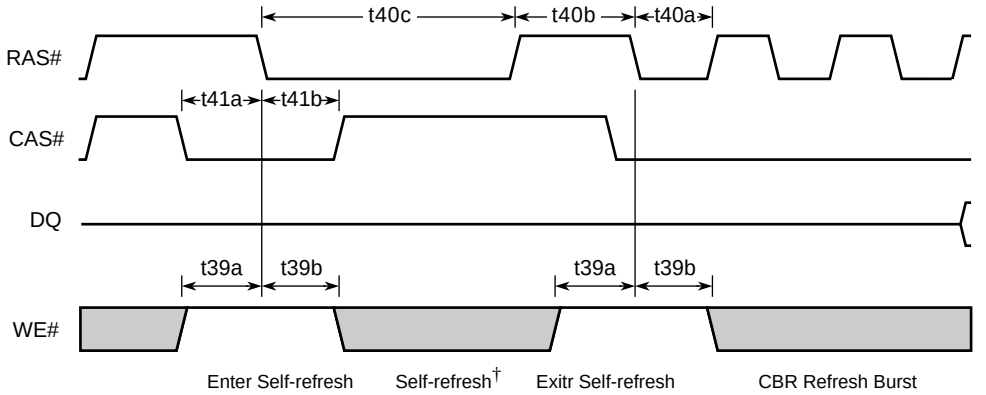

Figure 1. Self Refresh

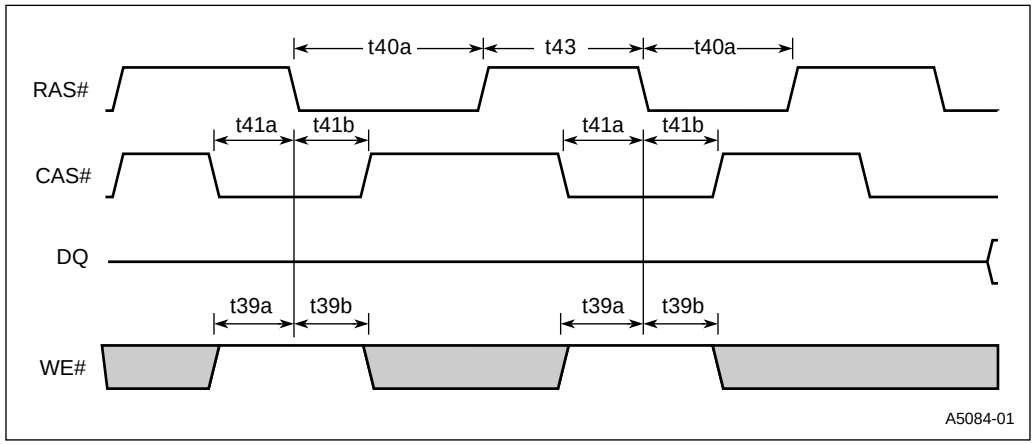

Figure 2. CAS before RAS Refresh

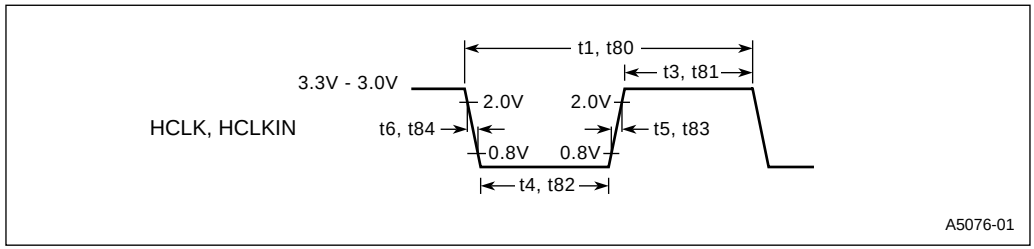

Figure 3. Host Clock Timing

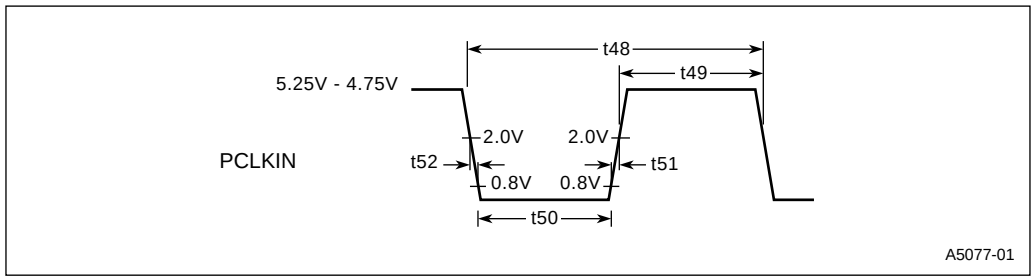

Figure 4. PCI Clock Timing

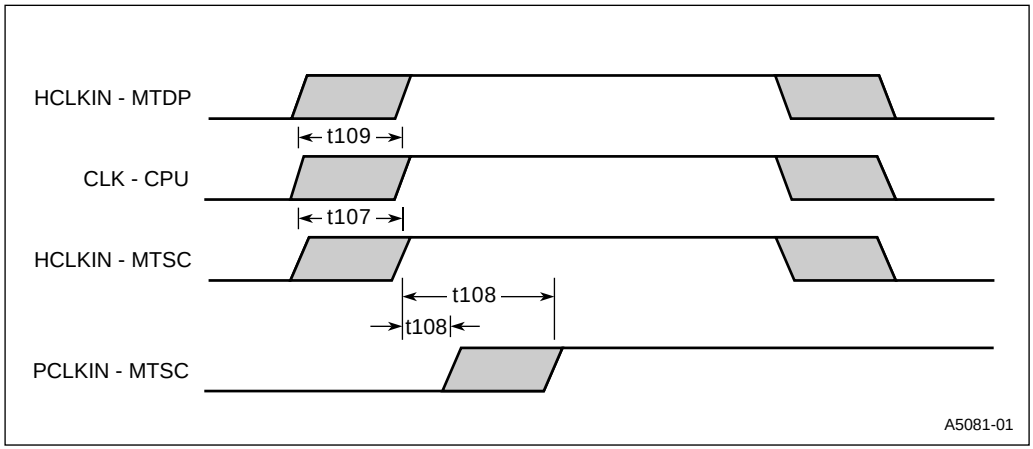

Figure 5. Host CLK to PCI CLK Relationship

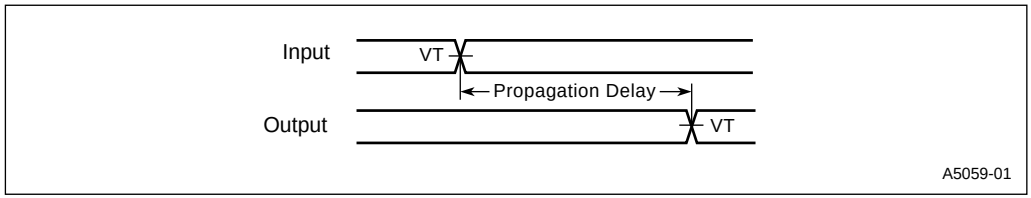

Figure 6. Propagation Delay

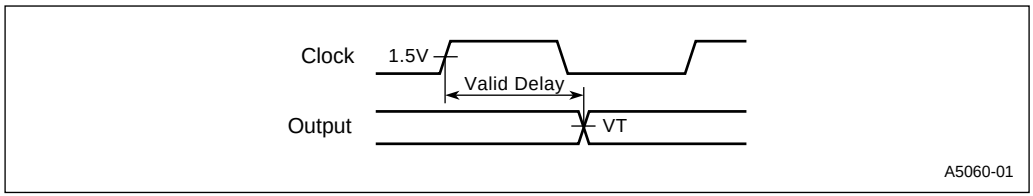

Figure 7. Valid Delay From Rising Clock Edge

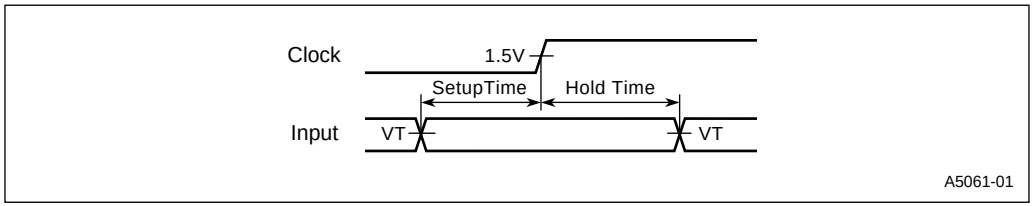

Figure 8. Setup and Hold Times

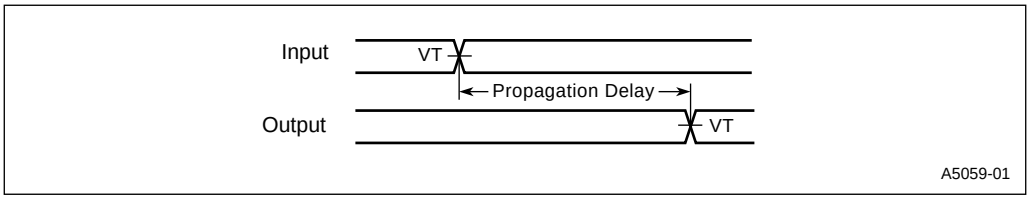

Figure 9. Float Delay

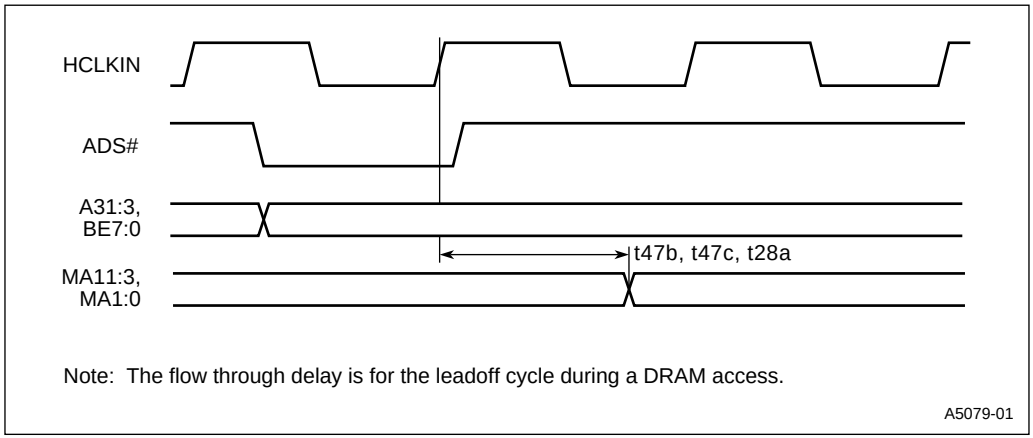

Figure 10. Flow Through Delay

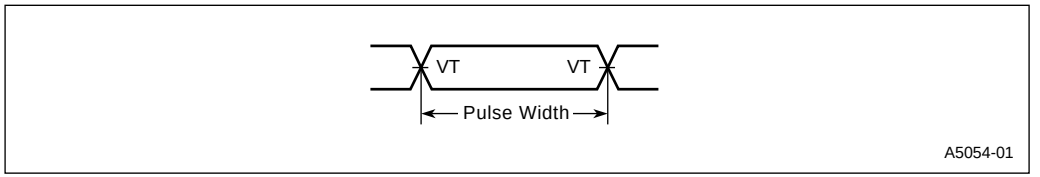

Figure 11. Pulse Width

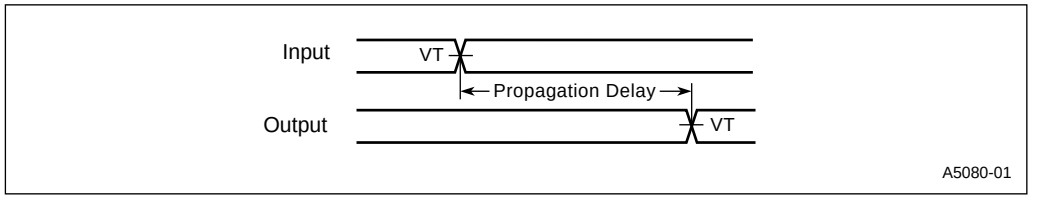

Figure 12. Output Enable Delay

1.4 Timing Relationship Diagrams

1.4.1 Cache Timing Relationships

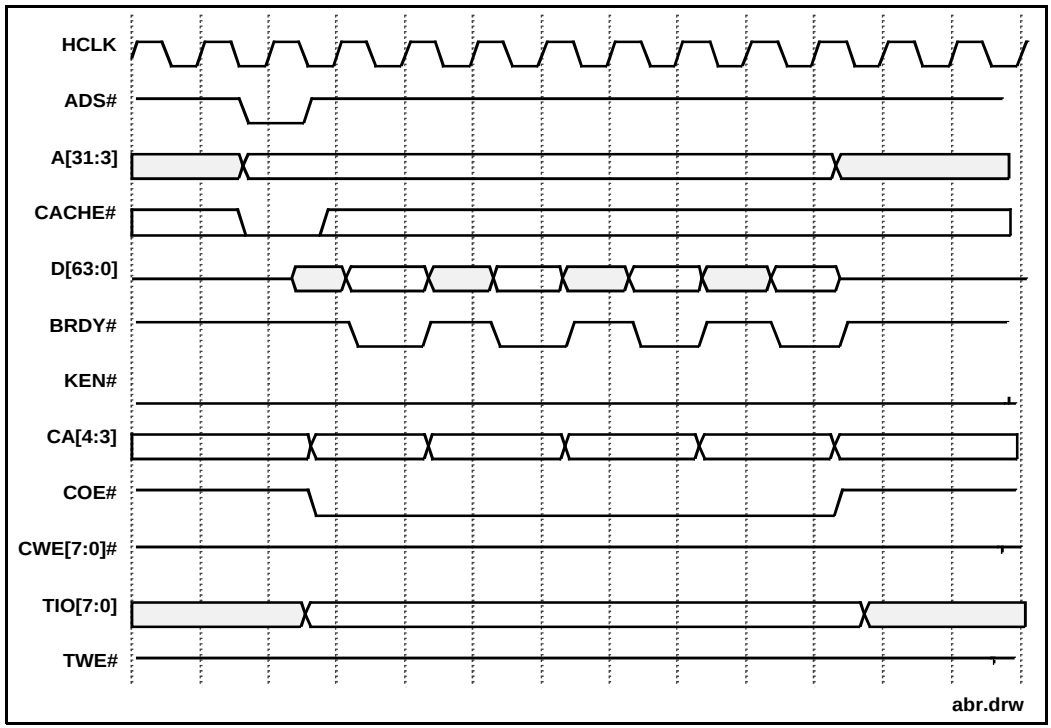

Figure 13. Burst Read (L1 Line Fill), Standard SRAM

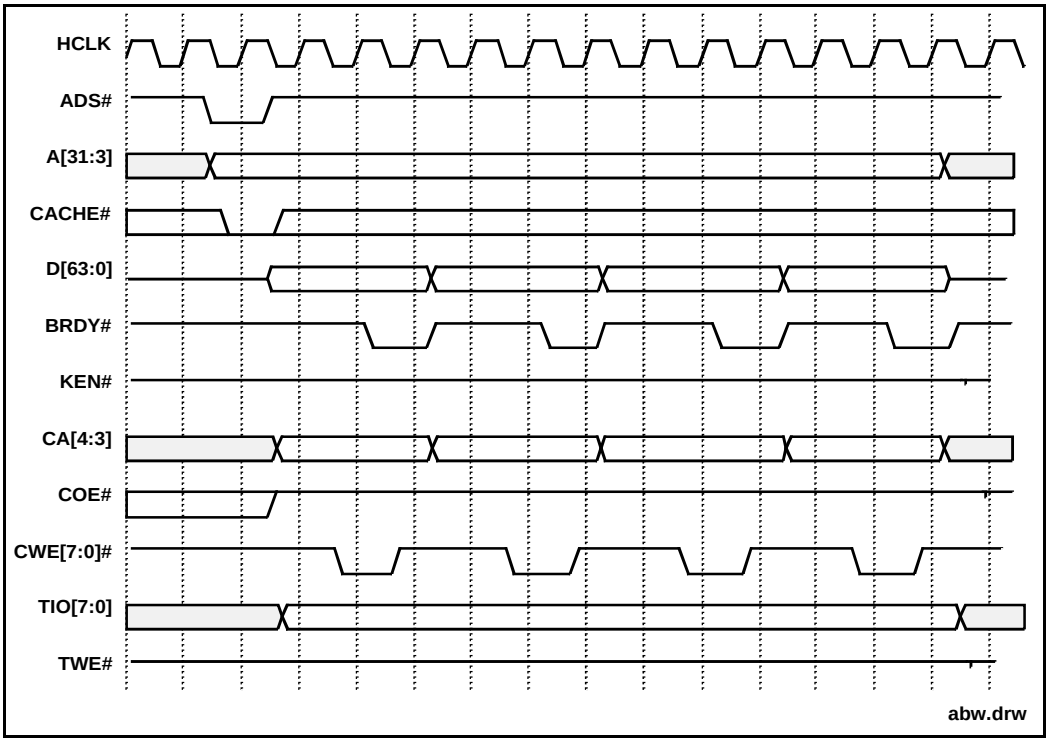

Figure 14. Burst Write (L1 Cache Write-Back), Standard SRAM

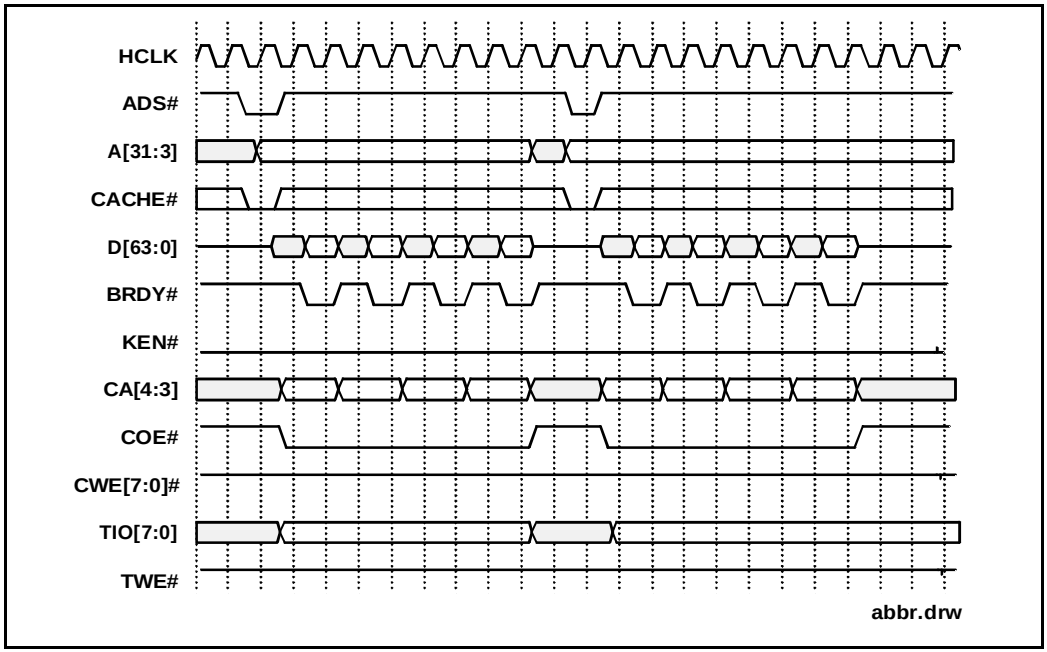

Figure 15. Back to Back Burst Reads (L1 Cache Line Fills), Standard SRAM

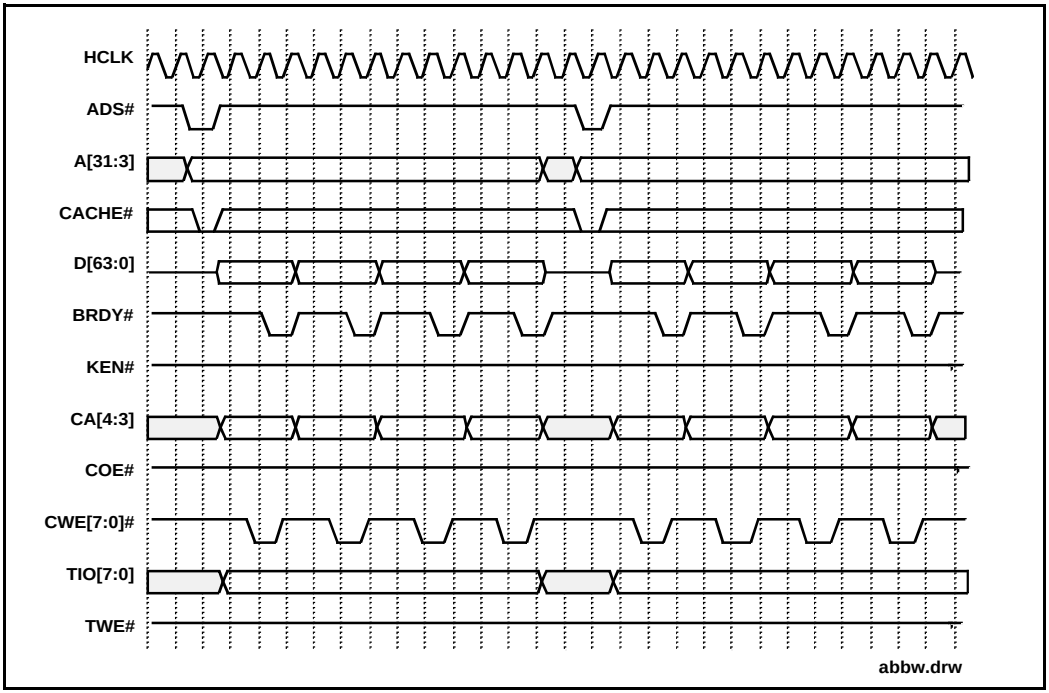

Figure 16. Second Level Cache Read Miss, Write-Back, Line Fill with Pipelined Burst SRAM

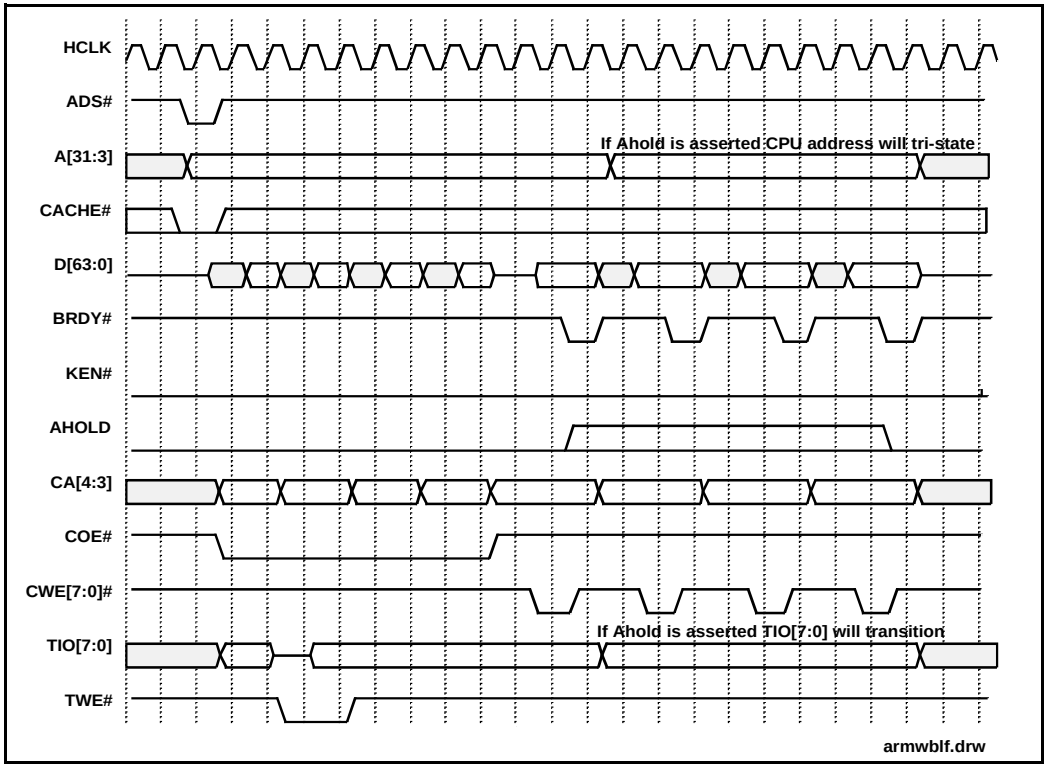

Figure 17. Read Miss, L2 Cache Write-Back, Line Fill, Standard SRAM

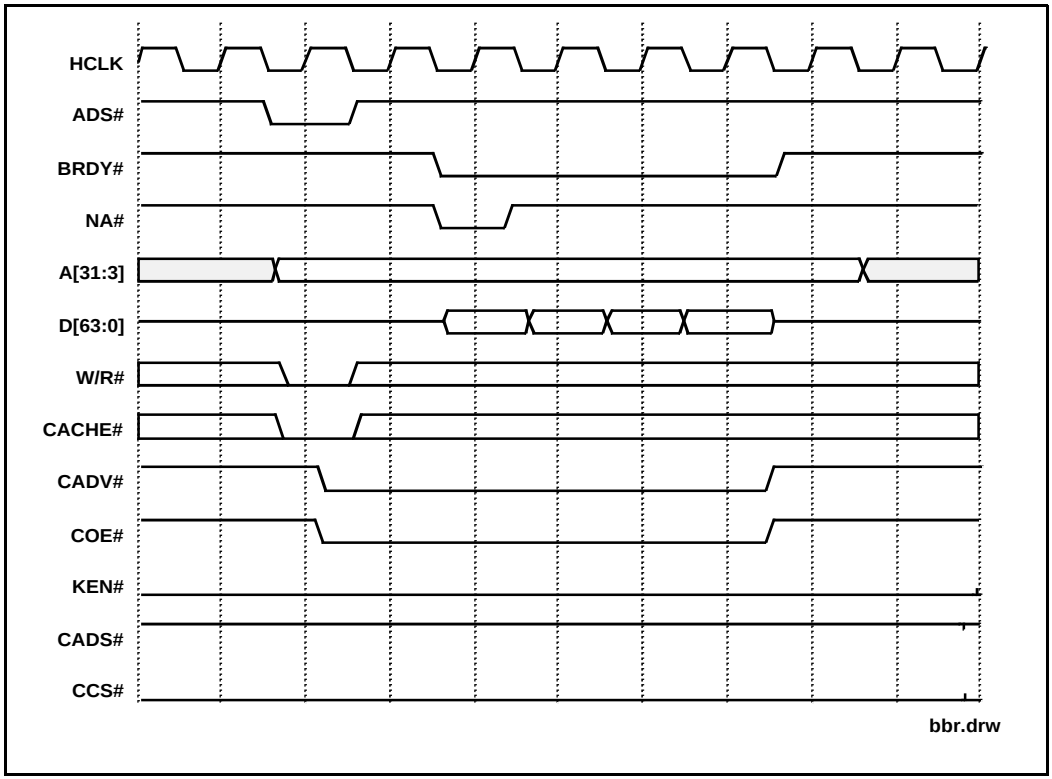

Figure 18. Burst Read, Pipelined Burst SRAM

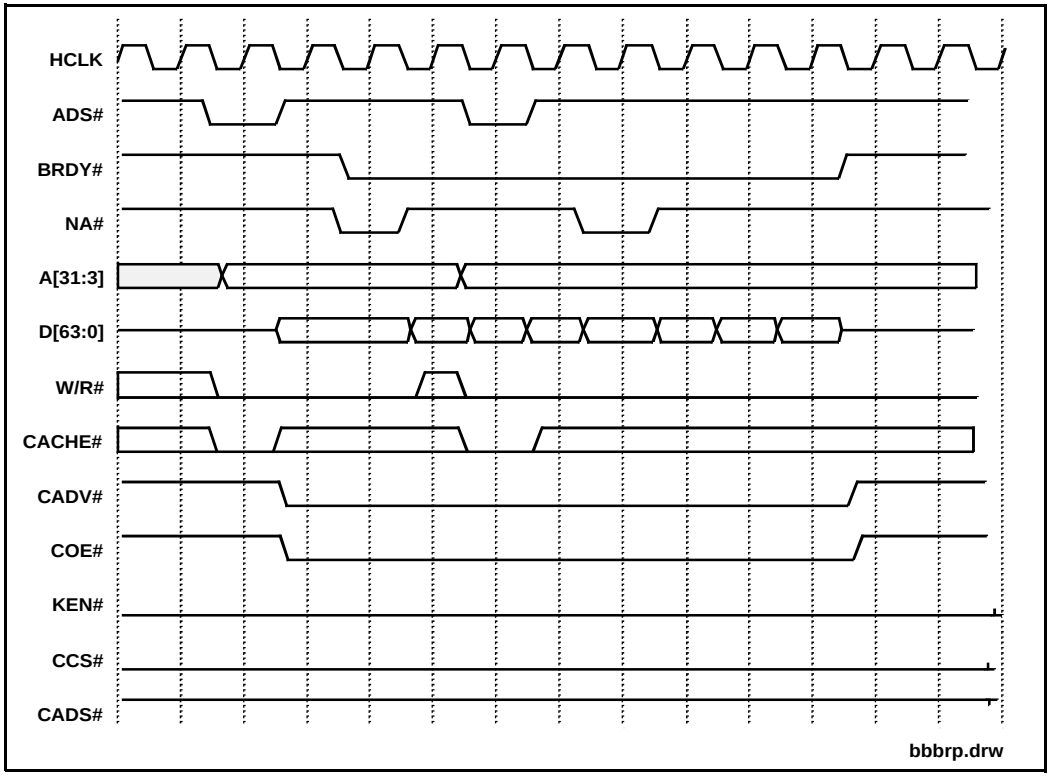

Figure 19. Back-to-Back Reads (L1 Cache Line Fills), Pipelined Burst SRAM

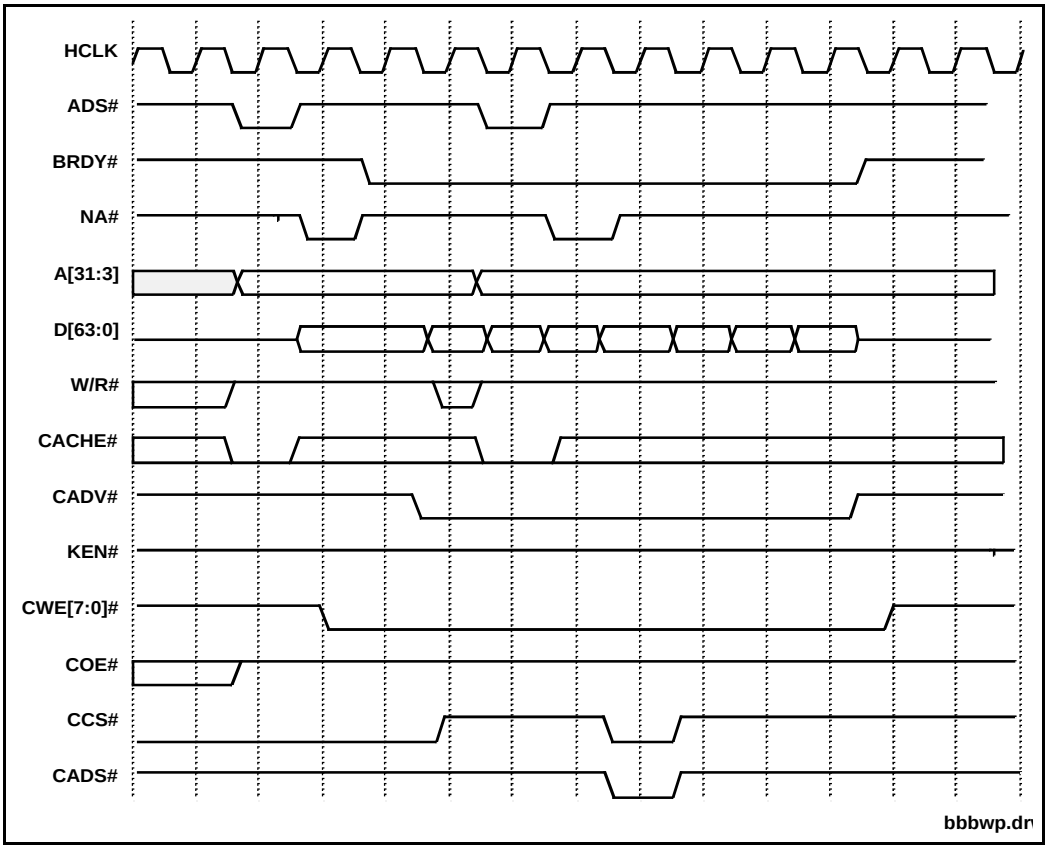

Figure 20. Back-to-Back Writes (L1 Cache Line Fills), Pipelined Burst SRAM

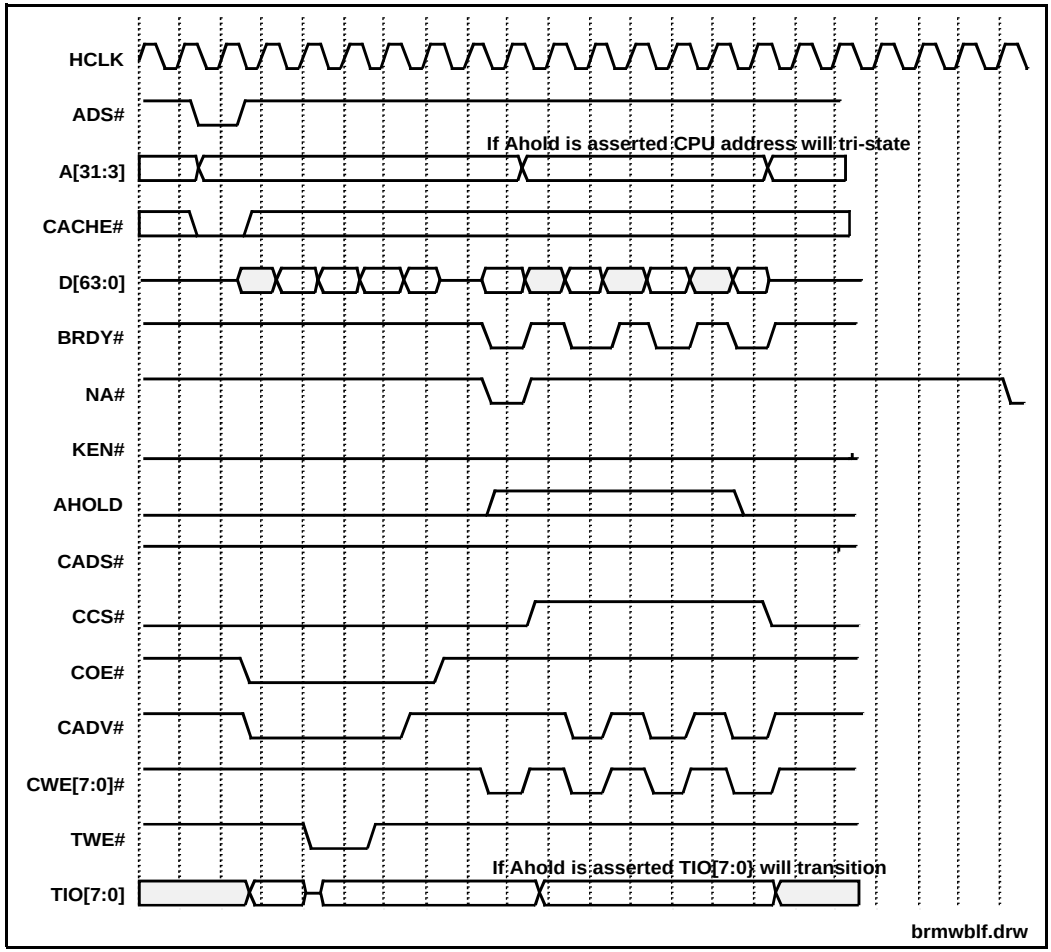

Figure 21. L2 Cache Read Miss, Write-Back, Line Fill, Piplined Burst SRAM

1.4.2 DRAM Timing Relationships

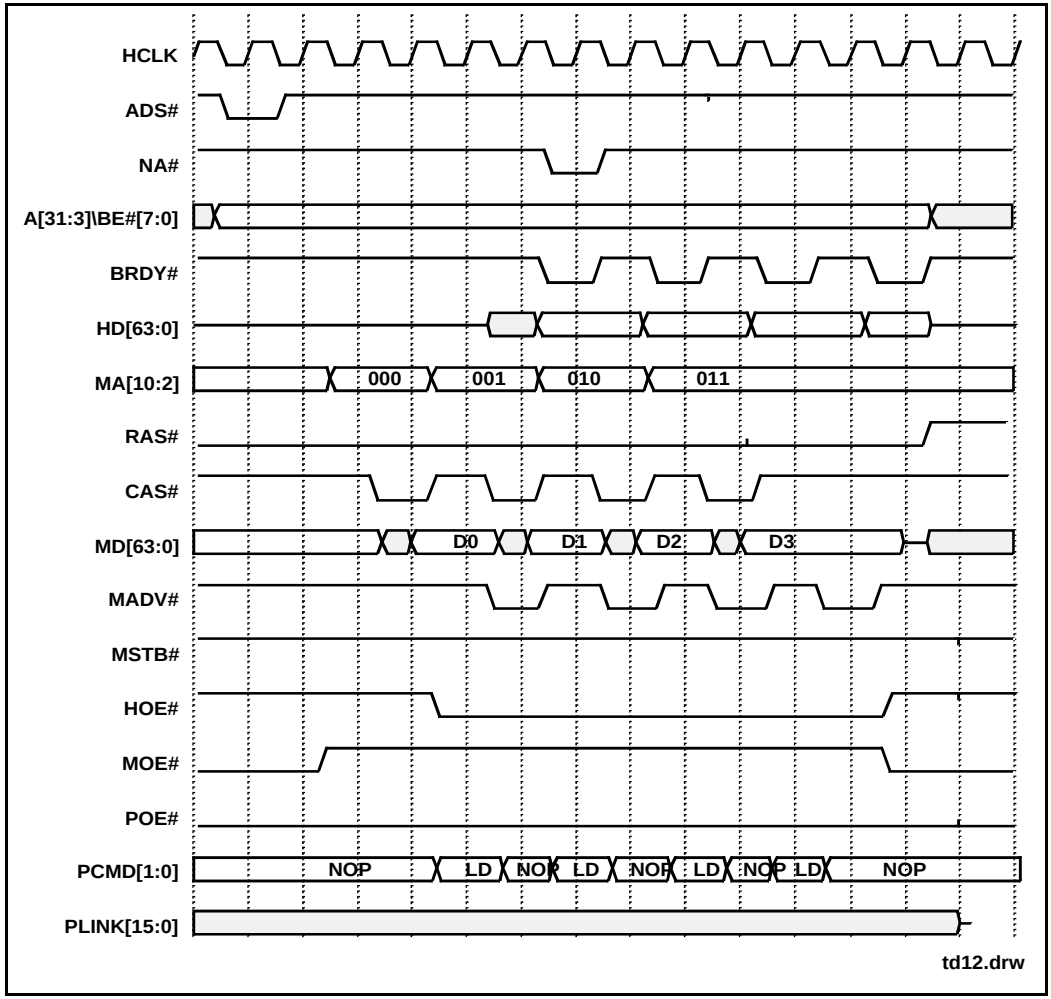

Figure 22. Burst Read Page Hit (EDO)

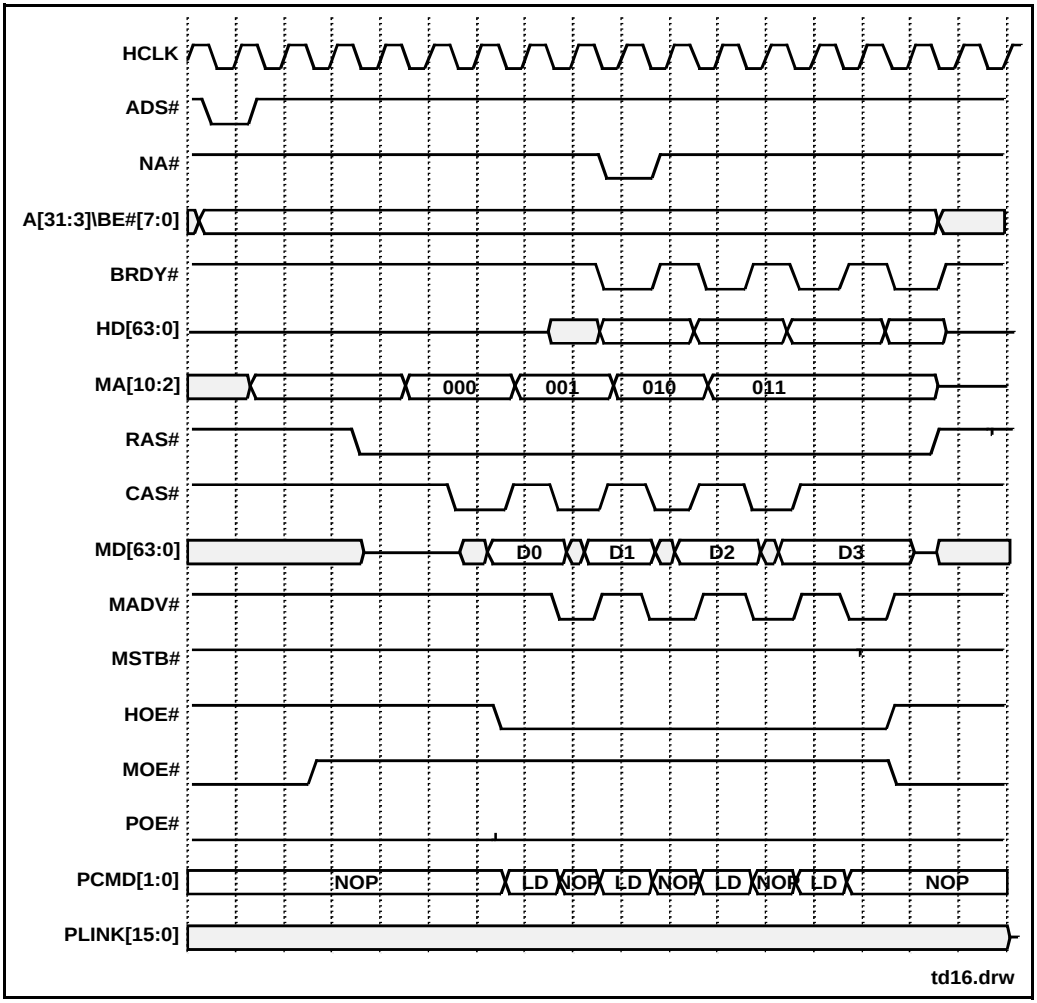

Figure 23. FBurst Read Row Miss (EDO)

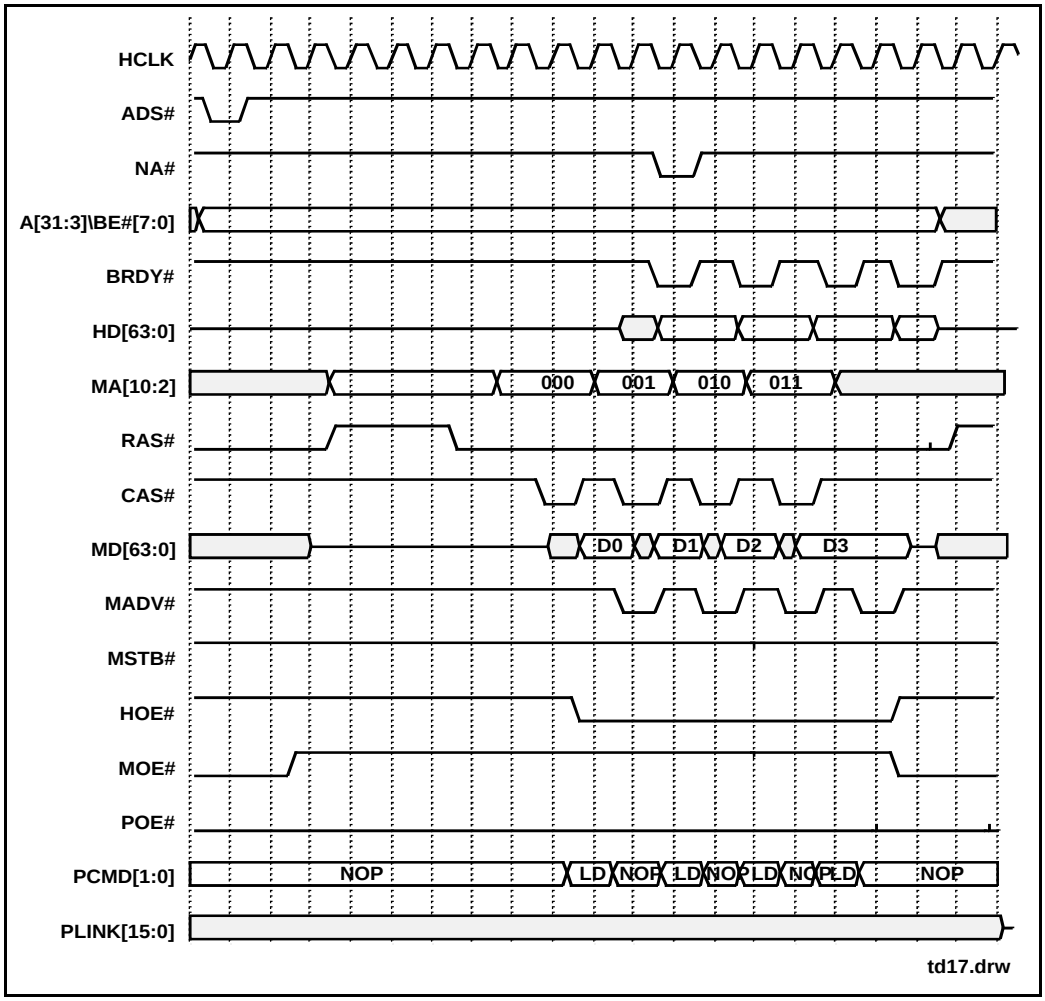

Figure 24. Burst Read Page Miss (EDO)

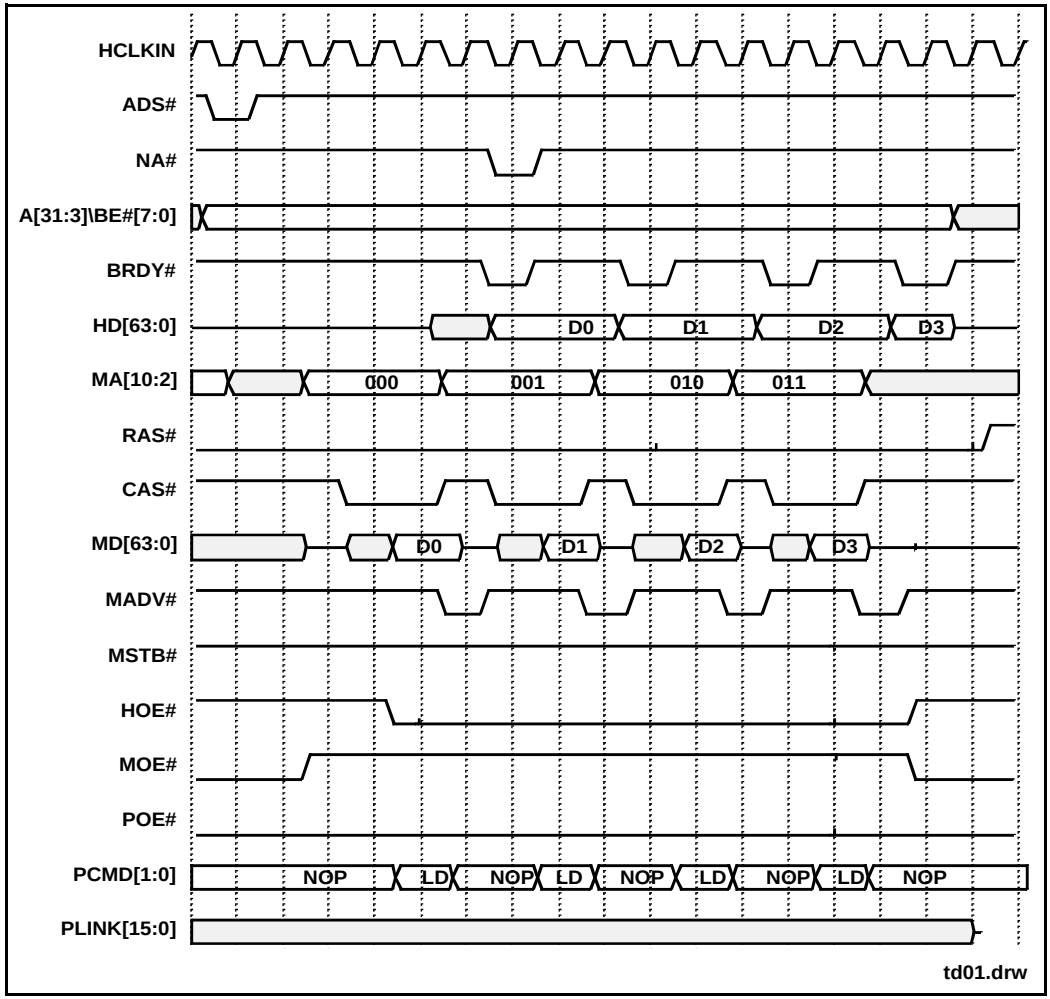

Figure 25. Burst Read Page Hit (Standard Page Mode)

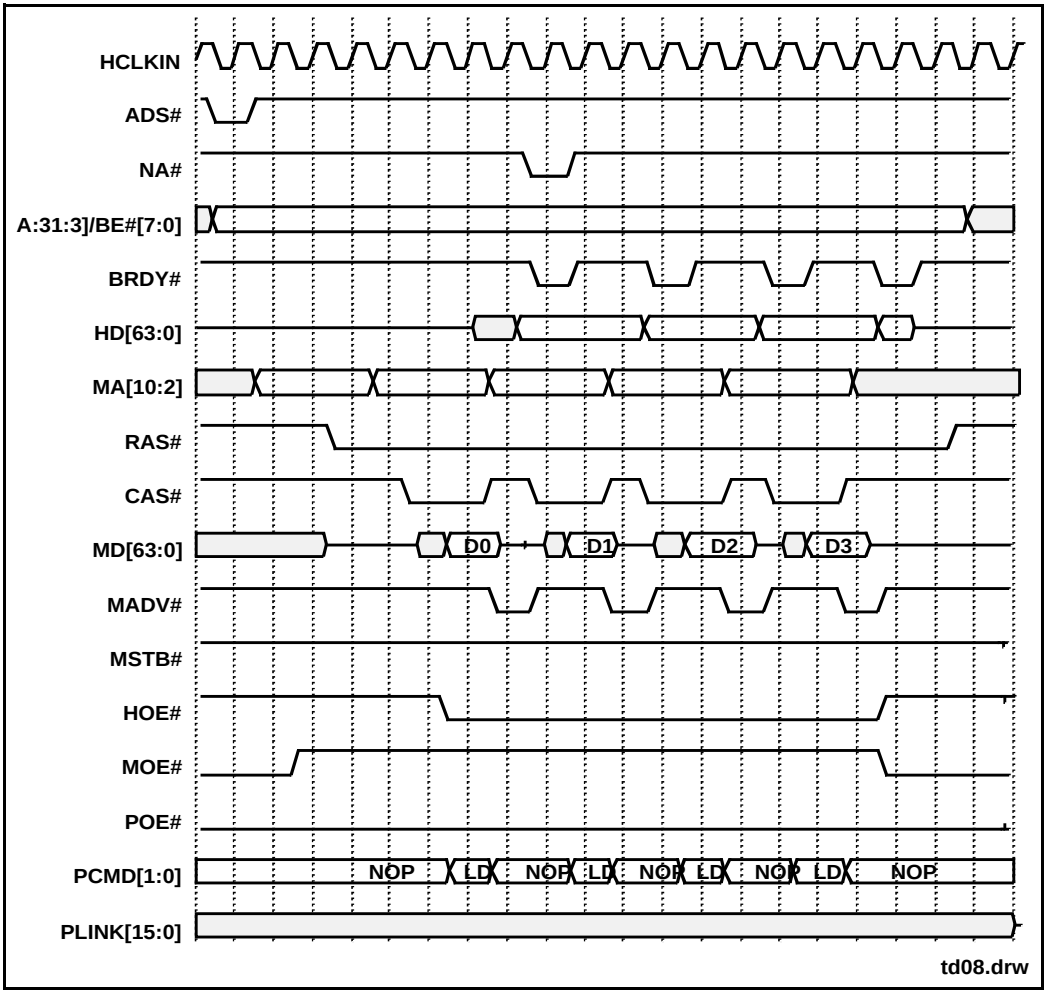

Figure 26. Burst Read Row Miss (Standard Page Mode)

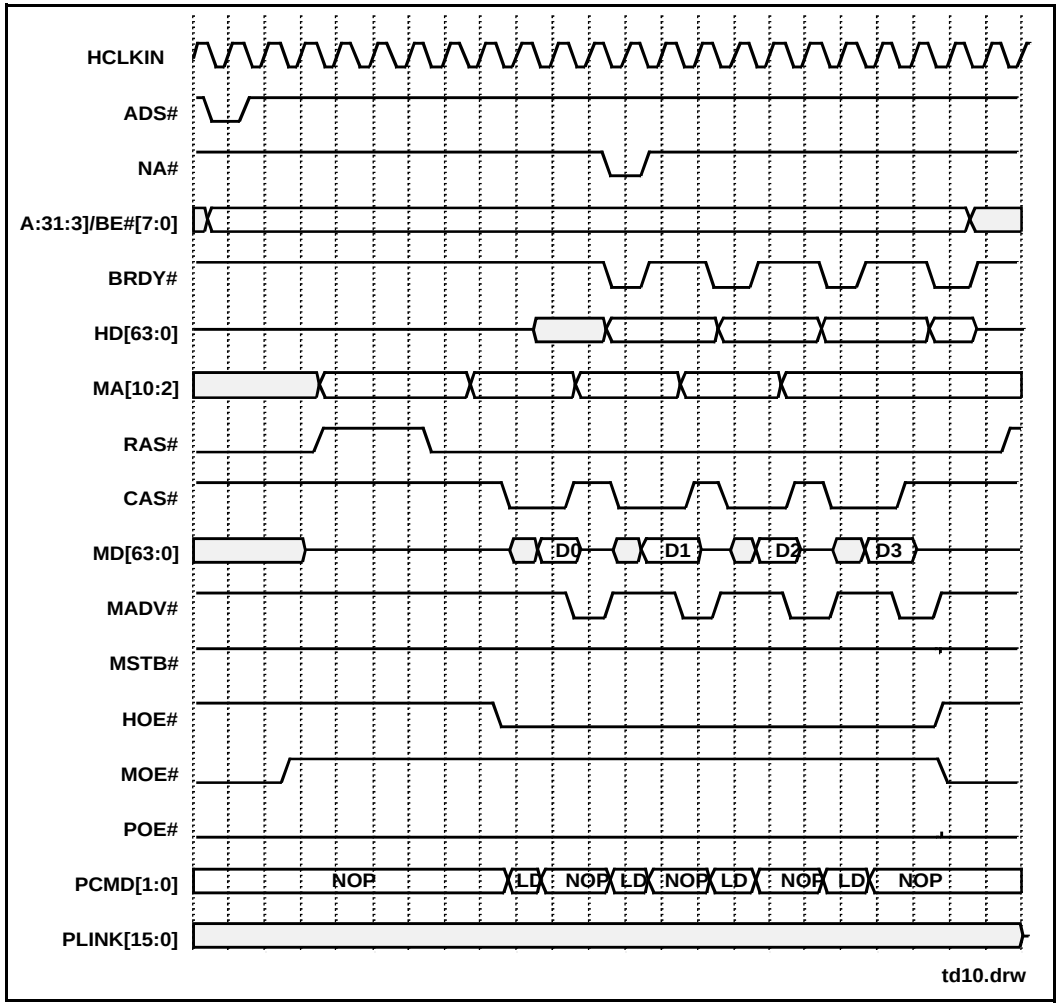

Figure 27. Burst Read Page Miss (Standard Page Mode)

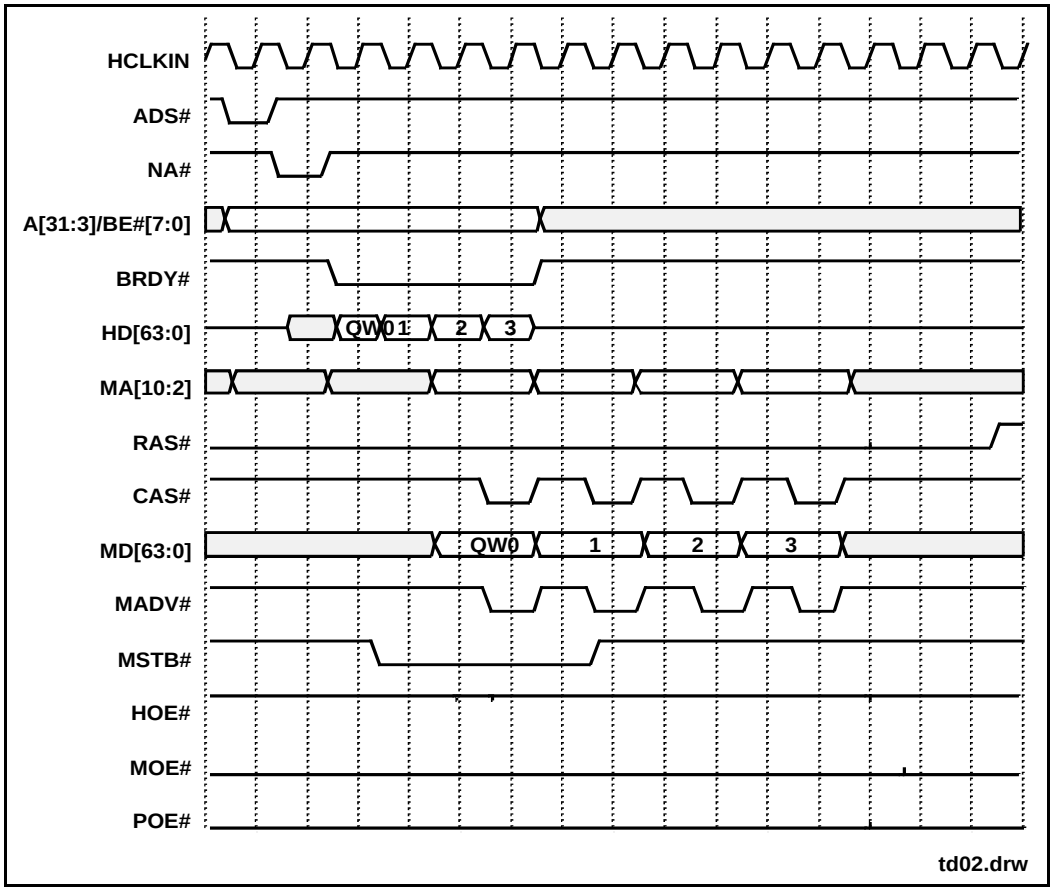

Figure 28. Posted Burst Write Page Hit

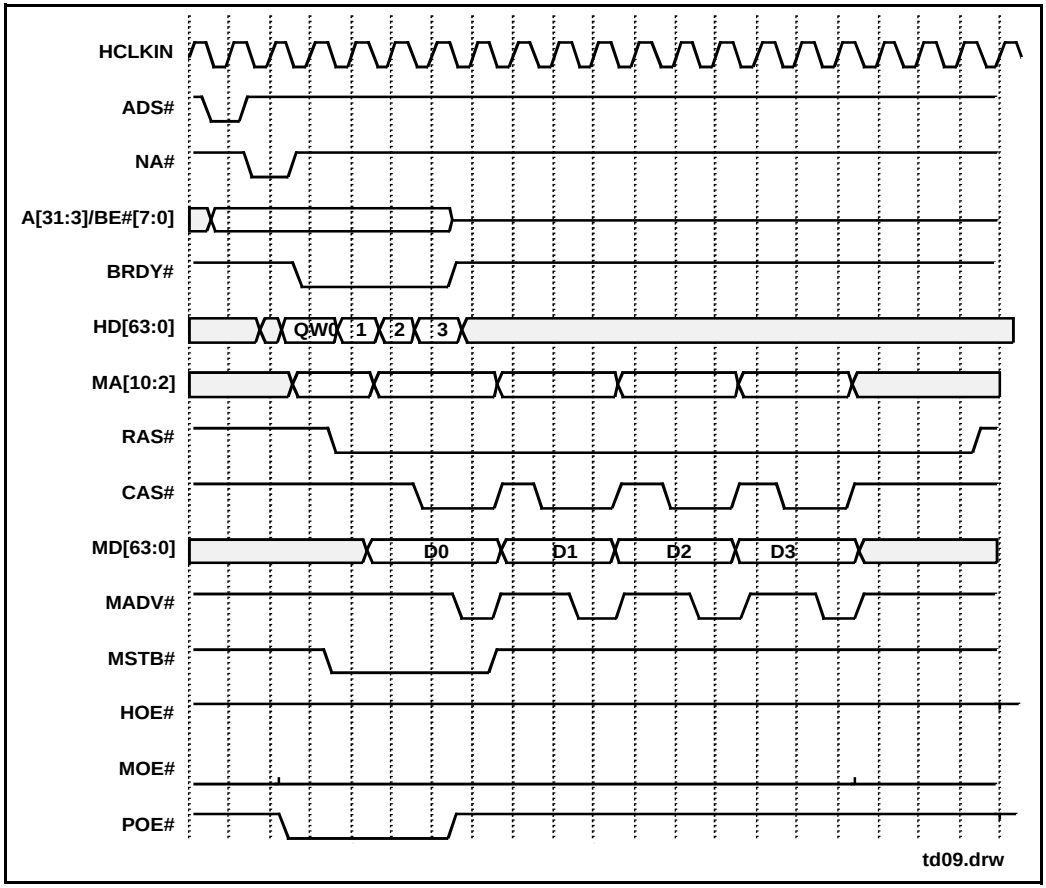

Figure 29. Burst Write Row Miss

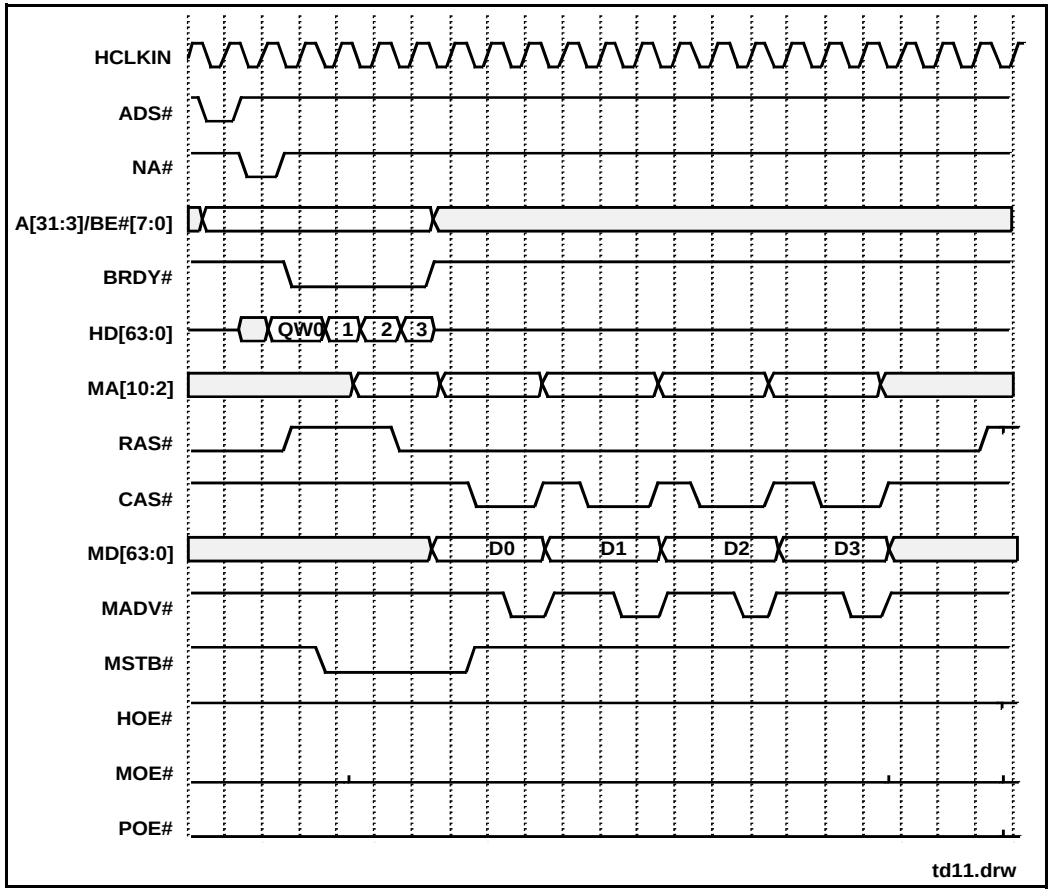

Figure 30. Burst Write Page Miss

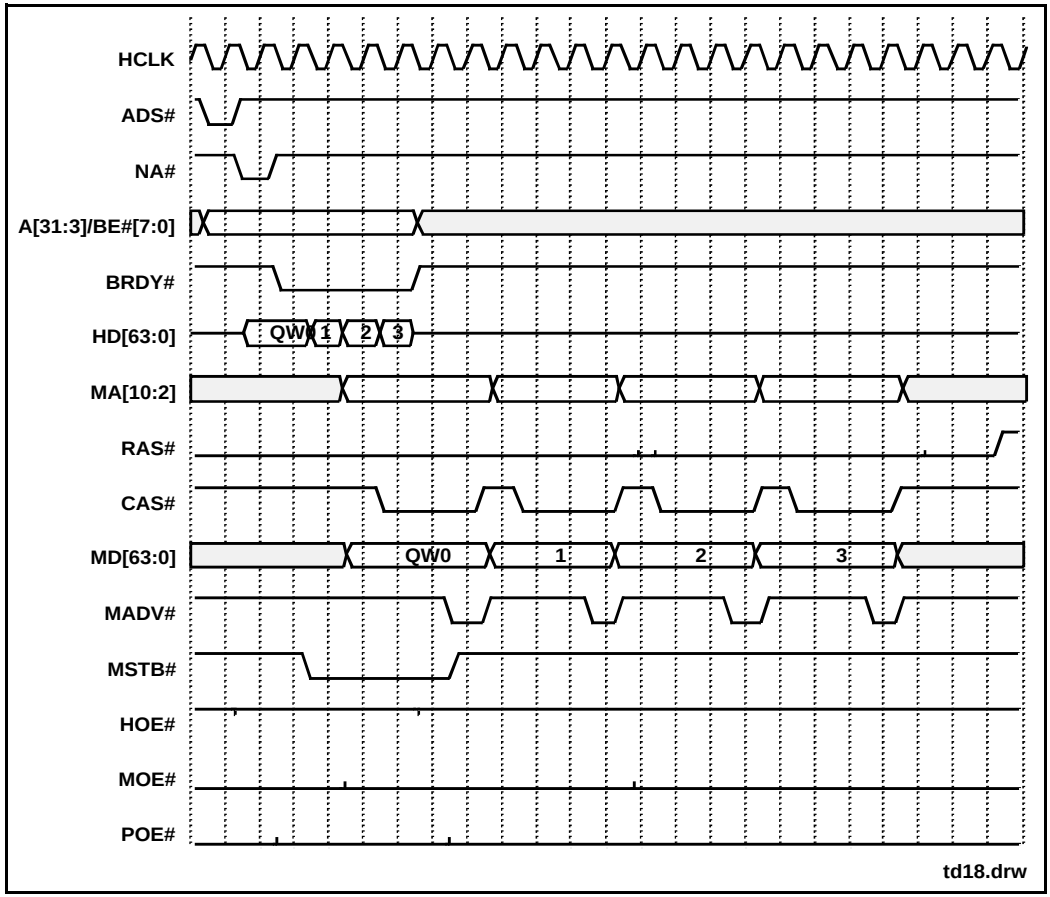

Figure 31. Burst Write

1.4.3 Additional Timing Relationships

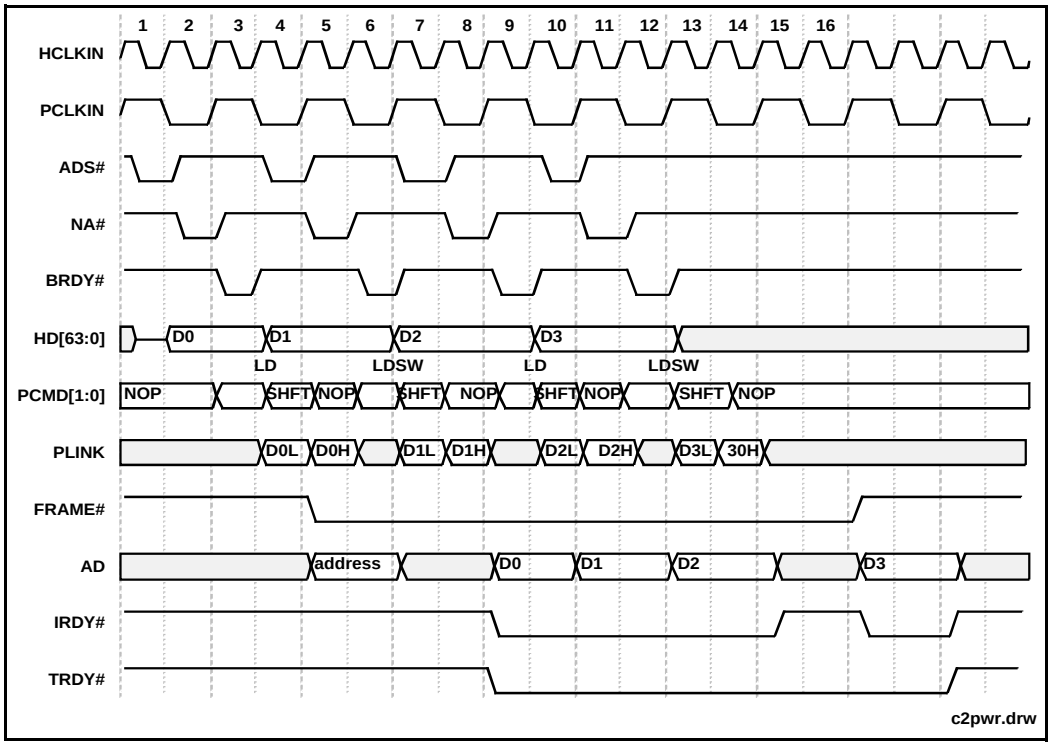

Figure 32. CPU to PCI Write Cycle

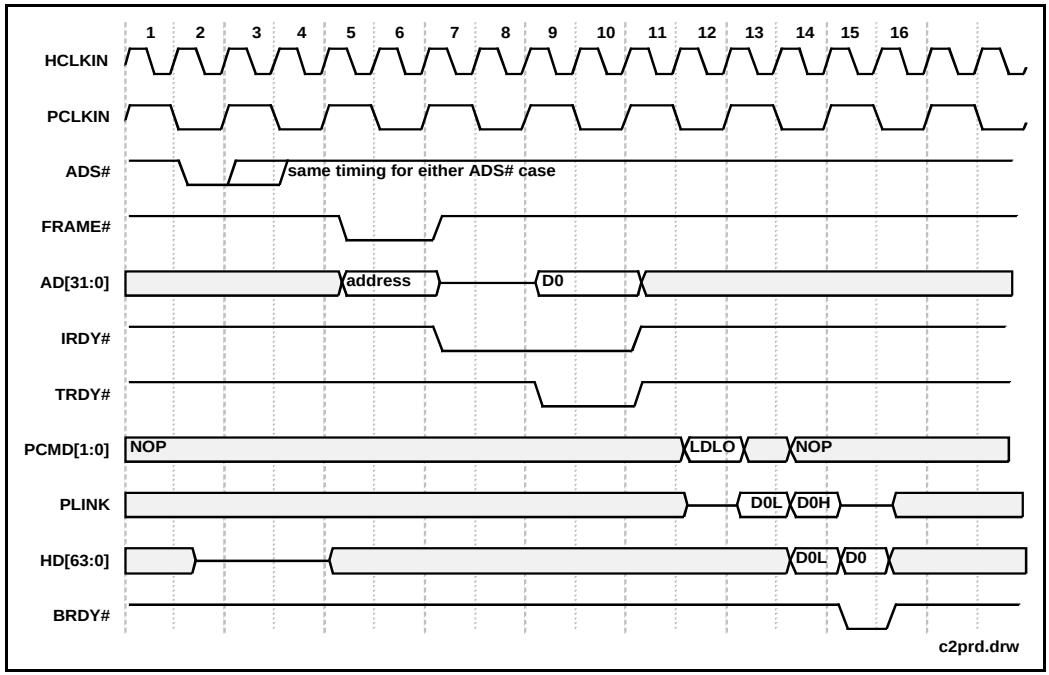

Figure 33. CPU to PCI Memory Read Cycle

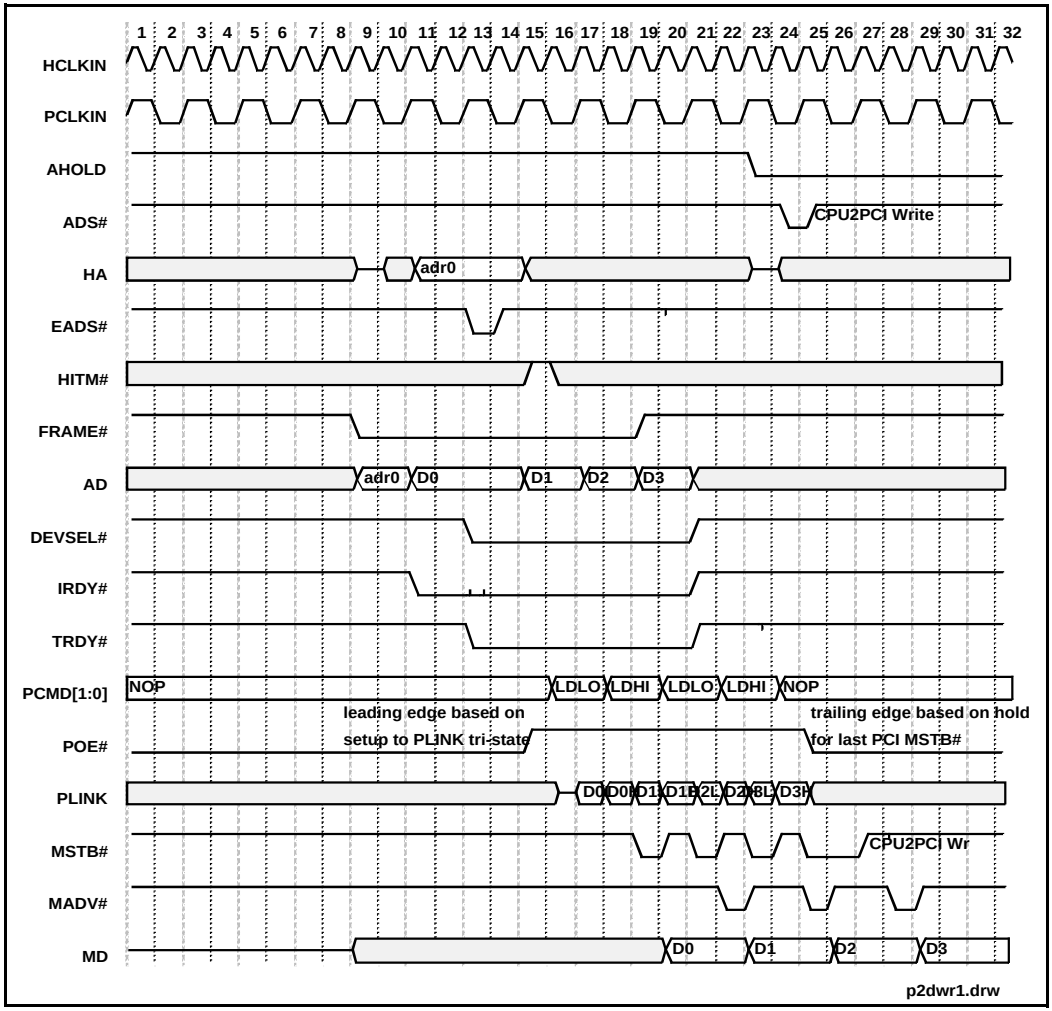

Figure 34. PCI Bus Master to DRAM Write Cycle

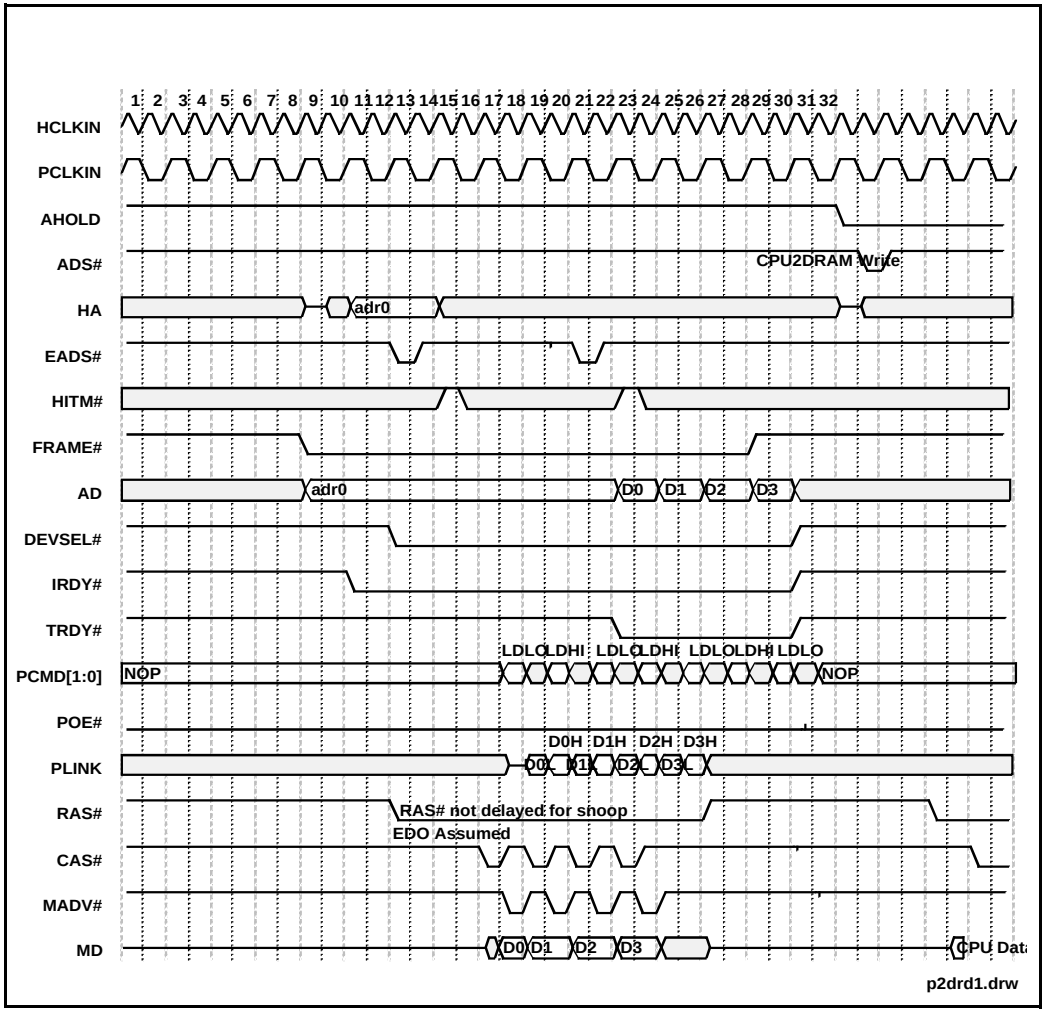

Figure 35. PCI Bus Master Read from DRAM

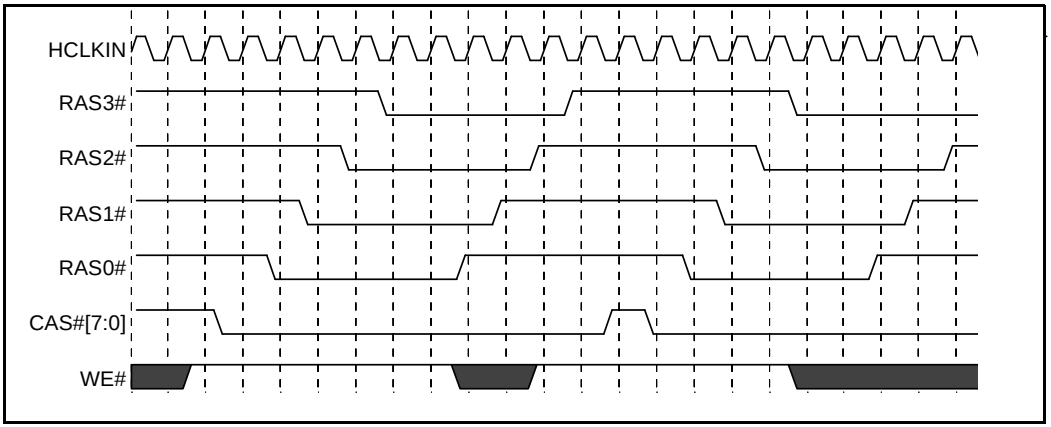

Figure 36. CAS Before RAS DRAM Refresh Cycle

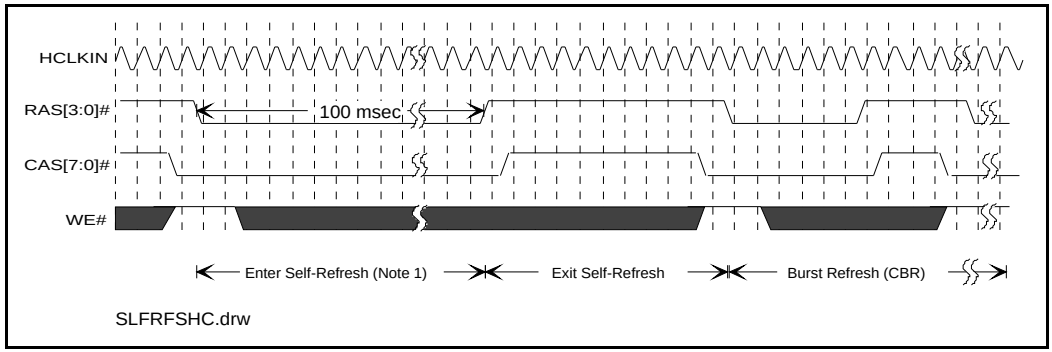

Figure 37. DRAM Self-Refresh

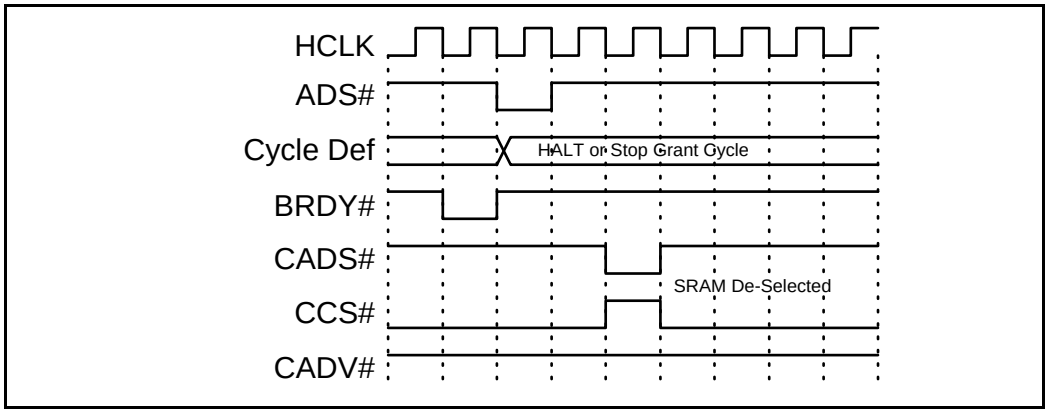

Figure 38. Deselect on STOPGRANT or HALT

2.0 82371MX PCI I/O IDE Xcelerator (MPIIX) SPECIFICATIONS

2.1 Absolute Maximum Ratings

Case Temperature Under Bias.....0°C to +85°C
Storage Temperature ..... -55°C to +150°C
Supply Voltage with respect to ground..... -0.3 V to V_{DD} + 0.3 V
Supply Voltage with respect to V_{SS}.....-0.3 V to +6.5 V

Maximum Power Dissipation..... 1.0 W

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

2.2 Thermal Characteristics

The 82371MX MPIIX is designed for operation at case temperatures between 0°C and 85°C. The thermal resistances of the 82371MX MPIIX TQFP package are given in Table 16.

Table 16. 82371MX MPIIX Package Thermal Resistance

Parameter	Air Flow 0.0 Meters/Second
θ_{JA}	35°C/W
θ_{JC}	6°C/W

2.3 Electrical Characteristics

2.3.1 DC Characteristics

Table 17. MPIIX DC Characteristics (Sheet 1 of 2)
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%, T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Notes
VIL1	Input Low Voltage	-0.3	0.8	V	
VIH1	Input High Voltage	2.0	V_{DD}/V_{DD3} + 0.3	V	
VIL2	Input Low Voltage	0.0	0.2 V_{DDR}	V	Note 1
VIH2	Input High Voltage	0.8 V_{DDR}	V_{DDR} + 0.3	V	Note 1
V_{T1-}	Schmitt Trigger Threshold Voltage, Falling Edge	0.7	1.35	V	Note 2, V_{DD}=5.0V
V_{T1+}	Schmitt Trigger Threshold Voltage, Rising Edge	1.4	2.2	V	Note 2, V_{DD}=5.0V
V_{H1}	Hysteresis Voltage	0.3	1.2	V	Note 2, V_{DD}=5.0V
V_{OL1}	Output Low Voltage		0.5	V	Notes 3,4,5,6
V_{OH1}	Output High Voltage	V_{DD}/V_{DD3} - 0.5		V	Notes 3,4,5,6
I_{OL1}	Output Low Current		4	mA	Note 3
I_{OH1}	Output High Current	-2		mA	Note 3
I_{OL2}	Output Low Current		8	mA	Note 4
I_{OH2}	Output High Current	-2		mA	Note 4

NOTES:

1. V_{IL2} and V_{IH2} apply to the following signals: PWROK, RTCCLK, RSMRST#, BATLOW#, SRBTN#, COMRI#, EXTSMI#, IRQ8#. The voltage reference is to the V_{DDR} "resume well" pin voltage.
2. V_{T1-}, V_{T1+} and V_{H1} apply to the following signals: IRQx, ZEROWS#, PWROK, EXTSMI#, MIRQ#.
3. I_{OL1}, I_{OH1} apply to the following signals (V_{OL1}, pertains to the I_{OL1}, condition and V_{OH1} pertains to the I_{OH1} condition): PHOLD#, DIOW#, DIOR#, SPKR, IGNNE#, INTR, SMI#, STPCLK#, CPURST,INIT, NMI,TC, DACK2#, SDIR, BIOSCS#, KBCCS#, HLTA20, GNTA#, GNTB#, SMOUT[5:0], HCLKO, RTCCLKO, PCICLKO.
4. I_{OL2}, I_{OH2} apply to the following signals (V_{OL1}, pertains to the I_{OL2}, condition and V_{OH1} pertains to the I_{OH2} condition): SYSCLK, SD[7:0], IOR#, IOW#, RSTDRV, SA[17:0], MEMR#, MEMW#.
5. I_{OL3}, I_{OH3} apply to the following signals (V_{OL1}, pertains to the I_{OL3}, condition and V_{OH1} pertains to the I_{OH3} condition): AD[31:0], C/BE[3:0]#, PCIRST#.
6. I_{OL4}, I_{OH4} apply to the following signals (V_{OL1}, pertains to the I_{OL4}, condition and V_{OH1} pertains to the I_{OH4} condition): FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, PAR.
7. These signals have weak internal pull-up resistors. IORDY, SD[7:0], ZEROWS#, IOCHRDY, EXTSMI#, IRQx, SYSACT#, CLKRUN#, MIRQ#, PIRQA#, PIRQB#, FERR#, COMRI#, PHLDA#, REQA#, REQB#, SYSCLK, DREQ2, MDRQ[2:0] (signals driven to inactive levels).
8. This value was determined using worst case instruction mix and at V_{DD} = V_{DDMAX}. See Application Note AP-734, *Intel 82430MX PCIset Power Measurement Analysis* (order number 272923-001) for complete power consumption data.

Table 17. MPIIX DC Characteristics (Sheet 2 of 2)
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%, T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Notes
I_{OL3}	Output Low Current		6	mA	Note 5
I_{OH3}	Output High Current	-2		mA	Note 5
I_{OL4}	Output Low Current		3	mA	Note 6
I_{OH4}	Output High Current	-2		mA	Note 6
I_{LI1}	Input Leakage Current		±1	µA	All, except I_{LI2} and I_{LI3}
I_{LI2}	Input Leakage Current		±300	µA	Note 7
I_{DD}	V_{DD} Supply Current		116 21 12 11	mA	Note 8, 5 V Core Note 8, 5 V Periphery Note 8, 3 V Periphery Note 8, 5 V/3 V Resume Well
C_{IN}	Input Capacitance		12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1 MHz

NOTES:

1. V_{IL2} and V_{IH2} apply to the following signals: PWROK, RTCCLK, RSMRST#, BATLOW#, SRBTN#, COMRI#, EXTSMI#, IRQ8#. The voltage reference is to the V_{DDR} "resume well" pin voltage.
2. V_{T1-}, V_{T1+} and V_{H1} apply to the following signals: IRQx, ZEROWS#, PWROK, EXTSMI#, MIRQ#.
3. I_{OL1}, I_{OH1} apply to the following signals (V_{OL1}, pertains to the I_{OL1}, condition and V_{OH1} pertains to the I_{OH1} condition): PHOLD#, DIOW#, DIOR#, SPKR, IGNNE#, INTR, SMI#, STPCLK#, CPURST,INIT, NMI,TC, DACK2#, SDIR, BIOSCS#, KBCCS#, HLTA20, GNTA#, GNTB#, SMOUT[5:0], HCLKO, RTCCLKO, PCICLKO.
4. I_{OL2}, I_{OH2} apply to the following signals (V_{OL1}, pertains to the I_{OL2}, condition and V_{OH1} pertains to the I_{OH2} condition): SYSCLK, SD[7:0], IOR#, IOW#, RSTDRV, SA[17:0], MEMR#, MEMW#.
5. I_{OL3}, I_{OH3} apply to the following signals (V_{OL1}, pertains to the I_{OL3}, condition and V_{OH1} pertains to the I_{OH3} condition): AD[31:0], C/BE[3:0]#, PCIRST#.
6. I_{OL4}, I_{OH4} apply to the following signals (V_{OL1}, pertains to the I_{OL4}, condition and V_{OH1} pertains to the I_{OH4} condition): FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, PAR.
7. These signals have weak internal pull-up resistors. IORDY, SD[7:0], ZEROWS#, IOCHRDY, EXTSMI#, IRQx, SYSACT#, CLKRUN#, MIRQ#, PIRQA#, PIRQB#, FERR#, COMRI#, PHLDA#, REQA#, REQB#, SYSCLK, DREQ2, MDRQ[2:0] (signals driven to inactive levels).
8. This value was determined using worst case instruction mix and at V_{DD} = V_{DDMAX}. See Application Note AP-734, *Intel 82430MX PCIset Power Measurement Analysis* (order number 272923-001) for complete power consumption data.

2.3.2 AC Characteristics

Table 18. MPIIX Clock/Reset Timings (Sheet 1 of 2)
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%, T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Units	Notes	Fig.
PCI Clock Timings (PCICLK)						
t1a	Period	30		ns		40
t1b	High Time	12.0		ns		40
t1c	Low Time	12.0		ns		40
t1d	Rise Time		3.0	ns		40
t1e	Fall Time		3.0	ns		40
EIO Clock Timings (SYSCLK)						
t1f	Period	120		ns		40
t1g	High Time	56		ns		40
t1h	Low time	56		ns		40
t1i	Rise Time		4	ns		40
t1j	Fall time		4	ns		40
Oscillator Clock Timings (OSC)						
t1k	OSC Period	67		ns		40
t1l	High Time	20		ns		40
t1m	Low time	20		ns		40

Table 18. MPIIX Clock/Reset Timings (Sheet 2 of 2)
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%, T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Units	Notes	Fig.
HCLK, HCLKO and PCICLKO Timings						
t1n	HCLKO to PCICLKO Skew	0	4	ns	at 1.5 V	63
t1o	HCLK Period	15		ns	at 1.5 V	40
t1p	HCLK High Time	4		ns		40
t1q	HCLK Low Time	4		ns		40
t1r	HCLK Rise Time		1.5	ns		40
t1s	HCLK Fall Time		1.5	ns		40
t1t	HCLKO Period	15		ns		40
t1u	HCLKO High Time	5.5		ns		40
t1v	HCLKO Low Time	5.5		ns		40
t1w	HCLKO Rise Time		1.2	ns		40
t1x	HCLKO Fall Time		1.2	ns		40
Reset Timings						
t2a	CPURST, PCIRST#, RSTDRV Driven Inactive After PWROK is Driven Active High.	2		PCI-CLK		41
t2b	CPURST, PCIRST#, RSTDRV Active Pulse Width. Initiated via the RC Register.	1		ms		42
t2c	CPURST Valid Delay from PCICLK Rising	3	25	ns		57
t2d	INIT Pulse Width	15		PCI-CLKs		60

Table 19. MPIIX System Power Management Timings
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%, T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Units	Notes	Fig.
SMI#						
t3a	Valid Delay from PCICLK	2	30	ns		44
t3b	Active Pulse Width	3		PCI-CLKI		43
t3c	Inactive Pulse Width	4		PCI-CLKI		43
EXTSMI#						
t3d	Active Pulse Width	2 PCICLK				43
t3e	Inactive Pulse Width	4 PCICLK				43
STPCLK#						
t3h	Valid Delay from PCICLK	2	30	ns		44
t3i	STPCLK# Inactive Pulse Width	5		PCLKIN		43

Table 20. EIO Bus Timings (Sheet 1 of 5)
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%, T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Units	Type	Notes	Fig.
Memory and I/O Timings							
SA[17:0]							
t6c	SA[17:0] Setup to MEMx#, IOx# Active	100		ns	M,I/O		45,46
t6e	SA[17:0] Valid Hold from MEMx#, IOx# Inactive	46		ns	M,I/O		45,46
MEMR#, MEMW#, IOR# and IOW#							
t7d	MEMx# or IOx# Active Pulse Width (std)	520		ns	M,I/O		45,46
t7e	MEMx# or IOx# Active Pulse Width (nws)	160		ns	M,I/O	1	45,46
t7g	MEMx# Inactive Pulse Width	163		ns	M		45
t7h	IOx# Inactive Pulse Width	163		ns	I/O		46
Read Data							
t9a	Read Data Driven from MEMR#, IOR# Active	0		ns	M,I/O		45,46
t9b	Read Data Valid Setup to MEMR#, IOR# Inactive	24		ns	M,I/O		45,46
t9c	Read Data Valid Hold from MEMR#, IOR# Inactive	0		ns	M,I/O		45,46
t9d	Read Data Three-stated from MEMR# and IOR# Inactive		41	ns	M,I/O		45,46
Write Data							
t10a	Write Data Valid Setup to MEMW# Active Write Data Valid Setup to IOW# Active	-40 -40		ns ns	M,I/O M,I/O		45,46
t10b	Write Data Valid Hold from MEMW#, IOW# Inactive	45		ns	M,I/O		45,46
t10c	Write Data Three-Stated from MEMW#, IOW# Inactive		105	ns	M,I/O		45,46
t10d	Write Data Driven Valid after Read MEMR#, IOR# Inactive	41		ns	M,I/O		45,46

NOTES:

1. No-wait-state (ZEROWS#) asserted.
2. This applies to the last cycle of a demand mode DMA transfer.
3. Output from MPIIX.
4. Type F transfers are selected via the MBDMAX Register.

Table 20. EIO Bus Timings (Sheet 2 of 5)
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%, T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Units	Type	Notes	Fig.
ZEROWS#							
t13b	ZEROWS# Driven Active from MEMx#, IOx# Active		80	ns	M,I/O		45,46
t13f	ZEROWS# Driven Active from SA[17:0]		200	ns	M,I/O		46
IOCHRDY							
t15b	IOCHRDY Driven Valid from MEMx#, IOx# Active		366	ns	M,I/O		45,46
t15e	IOCHRDY Inactive Pulse Width	120 ns	15.6 µs		M,I/O		45,46
Interrupt and NMI Timings							
NMI Timing							
t23a	SERR# Active to NMI Driven Active		200	ns			47
Interrupt Timing							
t24a	IRQx, MIRQx Inactive Pulse Width	100		ns			48
DMA Compatible Timings							
DREQ2, MDRQ							
t30a	DREQ2, MDRQx Active Hold from IOR# Active		558	ns		2	50
t30b	DREQ2, MDRQx, Active Hold from IOW# Active		315	ns		2	49
DACK2#, MDAKx#							
t31a	DACK2#, MDAKx# Active to IOR# Active	73		ns			50
t31b	DACK2#, MDAKx# Active to IOW# Active	312		ns			49
t31c	DACK2#, MDAKx# Active Hold from IOR# Inactive	70		ns			50
t31d	DACK2#, MDAKx# Active Hold from IOW# Inactive	155		ns			49
SA[17:0]							
t33c	SA[17:0] Valid Setup to IOx# Active	102		ns			49,50
t33d	SA[17:0] Valid Hold from IOx # Inactive	53		ns			49, 50
t33e	SA[15:8] Float from MDAKx# Active		40	ns			50

NOTES:
1. No-wait-state (ZEROWS#) asserted.
2. This applies to the last cycle of a demand mode DMA transfer.
3. Output from MPIIX.
4. Type F transfers are selected via the MBDMAX Register.

Table 20. EIO Bus Timings (Sheet 3 of 5)
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%, T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Units	Type	Notes	Fig.
IOR#, IOW#							
t34a	IOW# Active Pulse Width	465		ns			49
t34c	IOR# Active Pulse Width	766		ns			50
t34d	IOW# Inactive Pulse Width (continuous)	465		ns			49
t34e	IOR# Inactive Pulse Width (continuous)	160		ns			50
Read Data							
t36a	Read Data Valid from IOR# Active		237	ns			50
t36b	Read Data Valid Hold from IOR# Inactive	0		ns			50
t36c	Read Data Float from IOR# Inactive		61	ns			50
Write Data							
t37a	Write Data Valid Setup to IOW# Inactive	225		ns			49
t37b	Write Data Valid Hold from IOW# Inactive	36		ns			49
TC							
t39a	TC Active Setup to IOx# Inactive	511		ns		3	49,50
t39b	TC Active Hold from IOx# Inactive	71		ns		3	49,50
t39h	TC Pulse Width	700		ns			49,50
DMA Type "F" Timings							
DREQ2, MDRQx							
t55a	DREQ2, MDRQx Active Hold from IOR# Active		82	ns		2, 4	51
t55b	DREQ2, MDRQx Active Hold from IOW# Active		82	ns		2, 4	51
SA[17:0]							
t55c	SA[17:0] Valid Setup to IOx# Active	102		ns			51
t55d	SA[17:0] Valid hold from IOx# inactive	53		ns			51

NOTES:
1. No-wait-state (ZEROWS#) asserted.
2. This applies to the last cycle of a demand mode DMA transfer.
3. Output from MPIIX.
4. Type F transfers are selected via the MBDMAX Register.

Table 20. EIO Bus Timings (Sheet 4 of 5)
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%, T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Units	Type	Notes	Fig.
DACK2#, MDAKx#							
t56a	DACK2#, MDAKx# Active to IOR# Active	77		ns		4	51
t56b	DACK2#, MDAKx# Active to IOW# Active	77		ns		4	51
t56c	DACK2#, MDAKx# Active Hold from IOR# Inactive	30		ns		4	51
t56d	DACK2#, MDAKx# Active Hold from IOW# Inactive	30		ns		4	51
IOR# and IOW#							
t58a	IOR# Active Pulse Width	110		ns			51
t58b	IOW# Active Pulse Width	110		ns			51
t58c	IOR# Inactive Pulse Width (Continuous)	115		ns			51
t58d	IOW# Inactive Pulse Width (Continuous)	115		ns			51
Read Data							
t59a	Read Data Valid from IOR# Active		96	ns			51
t59b	Read Data Valid Hold from IOR# Inactive	2		ns			51
t59c	Read Data Float from IOR# Inactive		61	ns			51
Write Data							
t60a	Write Data Valid Setup to IOW# Inactive	73		ns			51
t60b	Write Data Valid Hold from IOW# Inactive	31		ns			51
TC							
t61a	TC Active Setup to IOR# Inactive	40		ns		3	51
t61b	TC Active Setup to IOW# Inactive	40		ns		3	51
t61c	TC Active Hold from IOx# Inactive	0		ns		3	51

NOTES:
1. No-wait-state (ZEROWS#) asserted.
2. This applies to the last cycle of a demand mode DMA transfer.
3. Output from MPIIX.
4. Type F transfers are selected via the MBDMAX Register.

Table 20. EIO Bus Timings (Sheet 5 of 5)
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%, T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Units	Type	Notes	Fig.
Chip Select Timings							
BIOSCS#, KBCCS#, RTCCS#, and PCS#							
t68a	xCS# Driven Active from SA[17:0] Valid		35	ns			52
t68b	xCS# Driven Inactive from SA[17:0] Invalid		35	ns			52
Miscellaneous Timings							
Mouse Timing Support							
t71a	IRQ12/M and IRQ1 Minimum Active Pulse Width (for Mouse Function and Keyboard)	180		ns			53
Coprocessor Error Support							
t73a	IGNNE# Active from IOW# Active from Port F0H Access		220	ns			53
t73b	IGNNE# Inactive from FERR# Inactive		230	ns			53
Real Time Clock Timing (RTCALE)							
t75a	RTCALE Pulse Width	200	300	ns			54
t75b	RTCALE Active from IOW# Active		85	ns			54
Speaker Timing							
t76a	SPKR Valid Delay from OSC Rising		200	ns			55
COMRI# and SRBTN#							
t76b	COMRI# Pulse Width		1	RTCCLK			60
t76c	SRBTN# Pulse Width		1	RTCCLK			60

NOTES:
1. No-wait-state (ZEROWS#) asserted.
2. This applies to the last cycle of a demand mode DMA transfer.
3. Output from MPIIX.
4. Type F transfers are selected via the MBDMAX Register.

Table 21. MPIIX PCI Interface Timing
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%, T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Units	Notes	Fig.
t77	AD[31:0] Valid Delay	2	11	ns	Min: 0 pF Max: 50 pF	57
t78	AD[31:0] Setup Time	7		ns		58
t79	AD[31:0] Hold Time	0		ns		58
t80	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL#, CLKRUN# Valid Delay from PCICLK Rising	2	11	ns	Min: 0 pF Max: 50 pF	57
t81	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL#, CLKRUN# Output Enable Delay from PCICLK Rising	2		ns		61
t82	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL#, CLKRUN# Float Delay from PCICLK Rising	2	28	ns		59
t83	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL#, CLKRUN# Setup Time to PCICLK Rising	7		ns		58
t84	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL#, CLKRUN# Hold Time from PCICLK Rising	0		ns		58
t85	PHLD# Valid Delay from PCICLK Rising	2	12	ns	1	57
t86	PHLDA# Setup Time to PCICLK Rising	10		ns		58
t87	PHLDA# Hold Time from PCICLK Rising	0		ns		58
t91	PIRQ[A,B]# Setup Time to PCICLK Rising				2, 3	58
t92	PIRQ[A,B]# Hold Time From PCICLK Rising				2, 3	58
t96	RST# Low Pulse Width	1		ms		60
t97	GNT[A:B] # Valid Delay from PCICLK Rising	2	12	ns		57
t98	REQ[A:B]# Setup Time to PCICLK Rising	12		ns		58
t99	REQ[A:B]# Hold Time from PCICLK Rising	0		ns	Min: 0 pF Max: 50 pF	58

NOTES:
1. 0 pF test load.
2. This signal is internally synchronized.
3. Timings not available.

Table 22. MPIIX PCI Bus IDE Timing
Functional Operating Range (V_{DD} = 5V ±5%, V_{DD3} = 3.3V ±5%, T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Units	Notes	Fig.
t102	DD[15:0] Valid Delay from PCICLK	2	20	ns		62
t103	DD[15:0] Setup to DIOR#	6		ns		62
t104	DD[15:0] Hold from DIOR#	5		ns		62
t105	DA[2:0] Valid Delay from PCICLK	2	20	ns		62
t108	SDIR# Valid Delay from PCICLK Rising	2	20	ns		62
t109	DOE# Valid Delay from PCICLK Rising	2	20	ns		62
t110	DIOx# Valid Delay from PCICLK Rising	2	10	ns		62
t111	DCS1#, DCS3#Valid Delay from PCICLK Rising	2	20	ns		62
t113	IORDY Setup to PCICLK Rising	7		ns	3	62
t114	IORDY Hold From PCICLK Rising	7		ns	3	62
t119	DIOx# Active Pulse Width			PCICLK	1	62
t120	DIOx# Inactive Pulse Width			PCICLK	2	62
t121	IORDY Sample Point From DIOx# Assertion			PCICLK	1	62

NOTES:

1. This parameter is programmable from 2-5 PCI clocks. Refer to the ISP field in the IDE Timing Register
2. This parameter is programmable from 1-4 PCI clocks. Refer to the RCT field in the IDE Timing Register.
3. IORDY is internally synchronized. This timing is to guarantee recognition on the next clock.

Table 23. MPIIX AC Test Loads

Capacitive Load	Signals
120pf	TC, SD[7:0], SA[17:0], MEMR#, MEMW#, IOR#, IOW#, IOCHRDY, ZEROWS#, RSTDRV, SYSCLK
50pf	DACK2#, SPKR, INTR, NMI, BIOSCS#, KBCCS#, RTCCS#, RTCALE, IGNNE#, DOE#, SDIR#, MDAK[2:0]#, DIOR#, DIOW#, PCS#, SMOUTx, ALTA20
20pf	HCLKO, RTCCLKO, CPURST, INIT, SMI#, FERR#, STPCLK#, PCICLKO

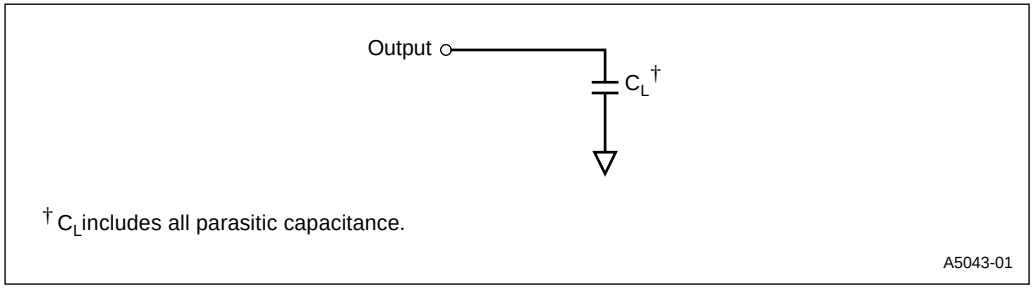

Figure 39. Test Load

2.4 MPIIX Timing Diagrams

2.4.1 Clock, Reset, EIO Bus, and Host Timing Diagrams

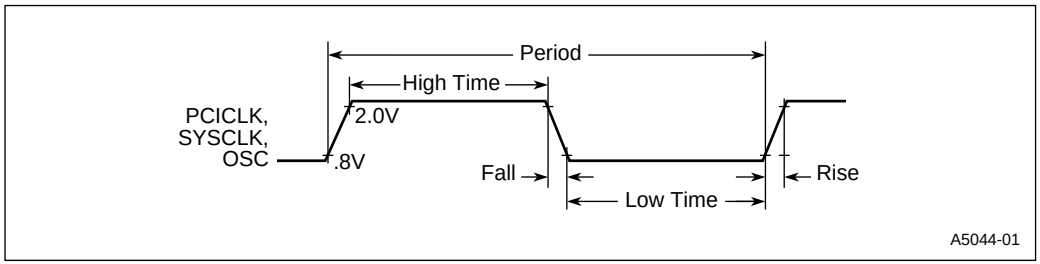

Figure 40. Clock Timing

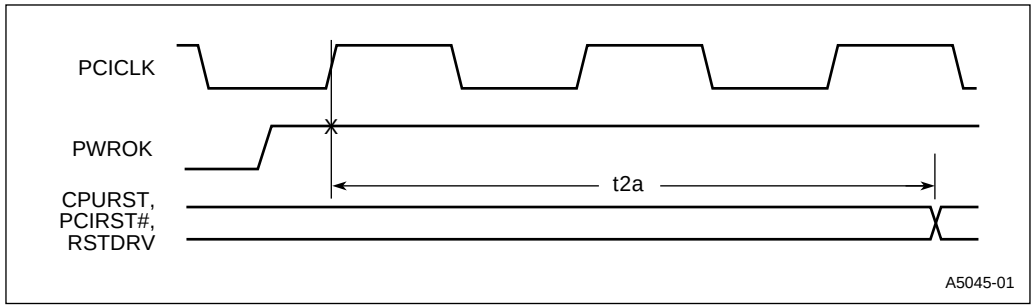

Figure 41. Reset Inactive After PWROK

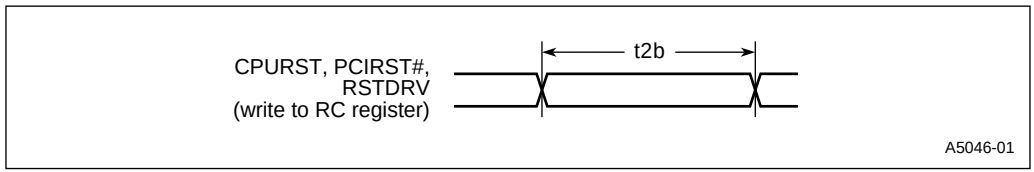

Figure 42. Reset Active Pulse Width

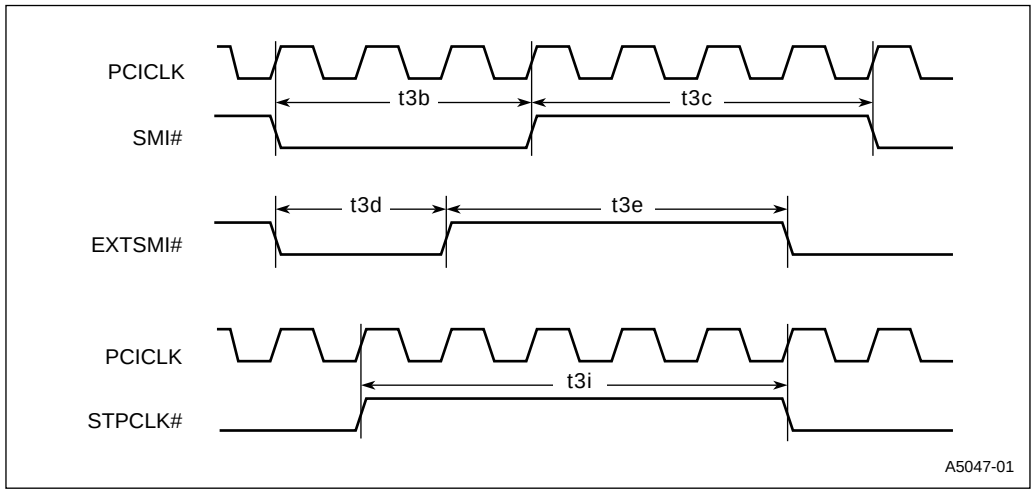

Figure 43. SMI#, EXTSMI#, and STPCLK# Timing

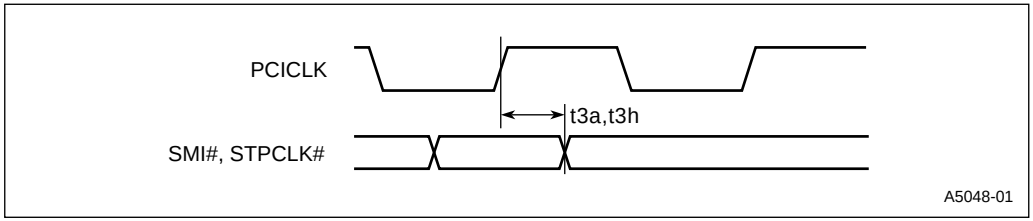

Figure 44. PCICLK to Output Valid Delay

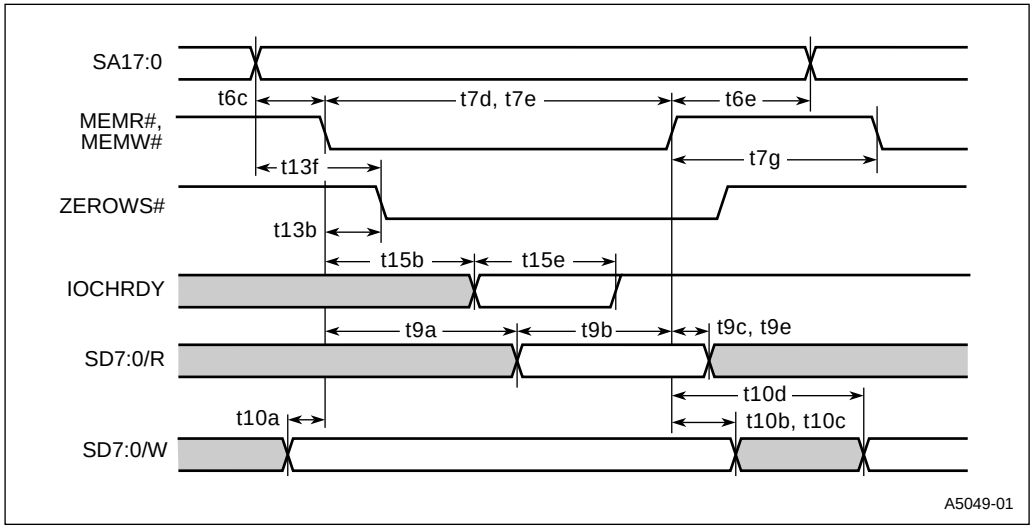

Figure 45. 8-Bit EIO BIOS Timing

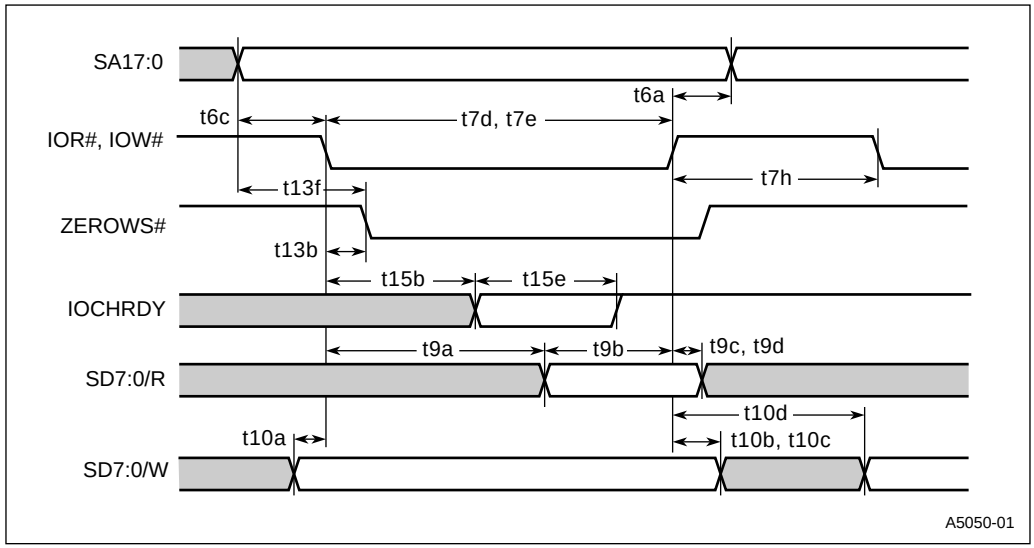

Figure 46. 8-Bit EIO I/O Slave Timing

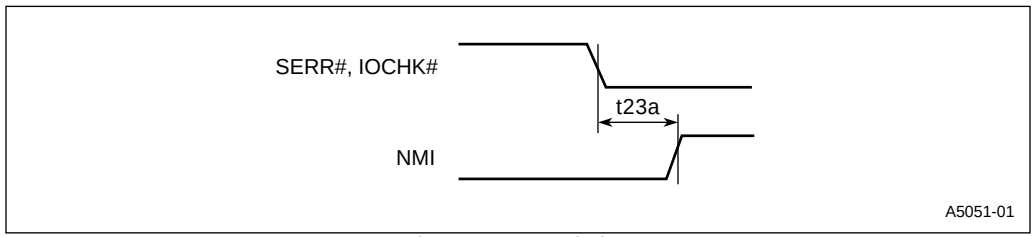

Figure 47. NMI Timing

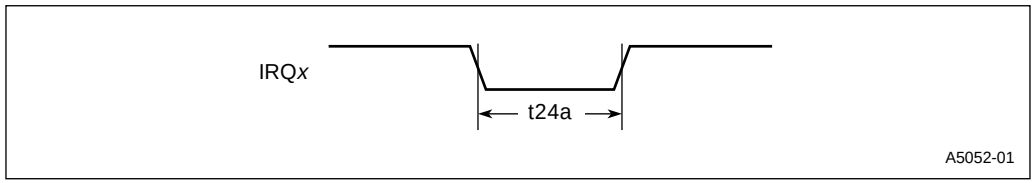

Figure 48. Interrupt Timing

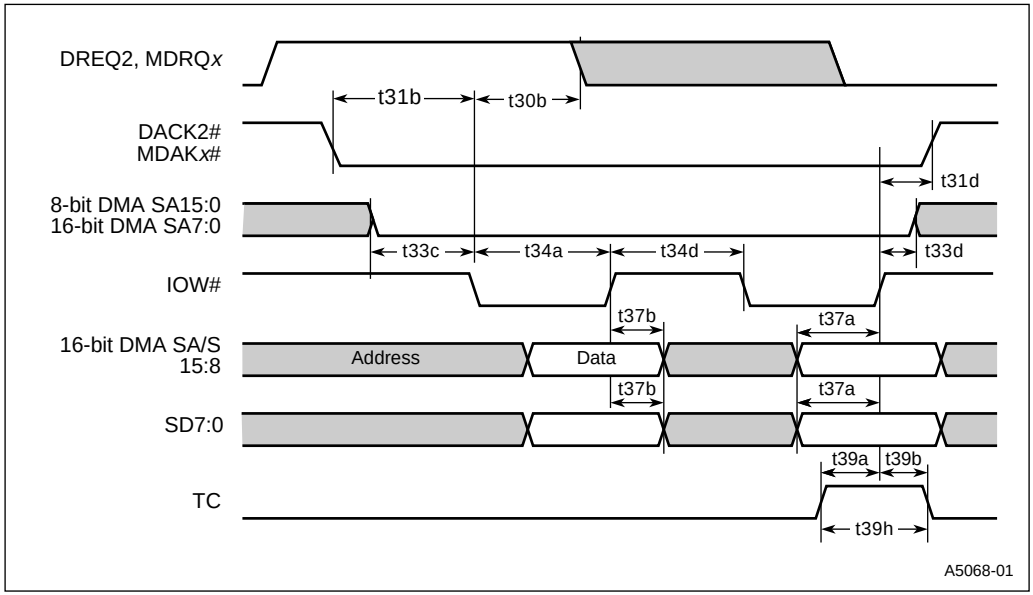

Figure 49. DMA Read Compatible Timing (I/O Write)

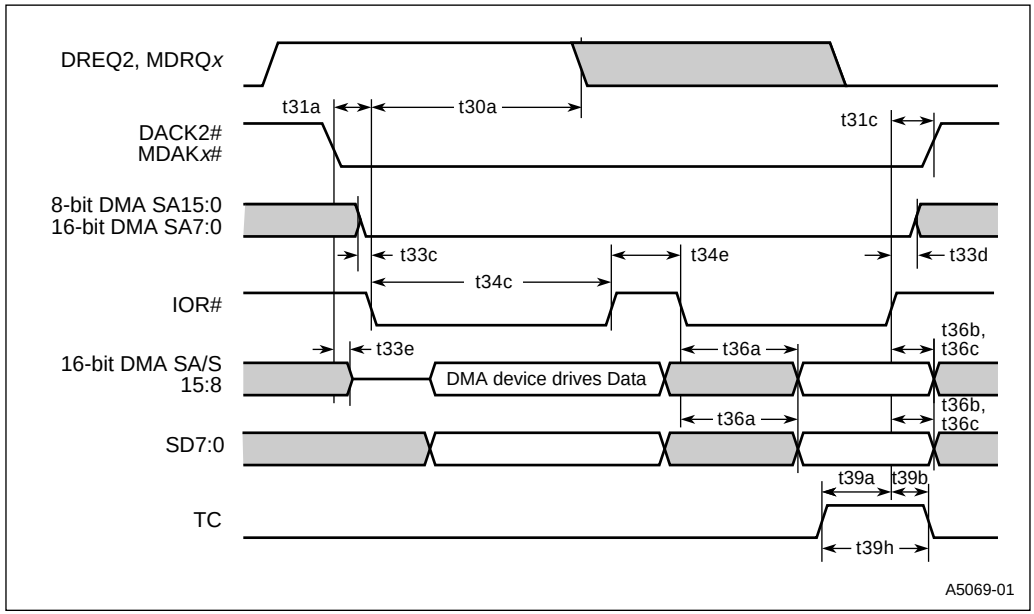

Figure 50. DMA Write Compatible Timing (I/O Read)

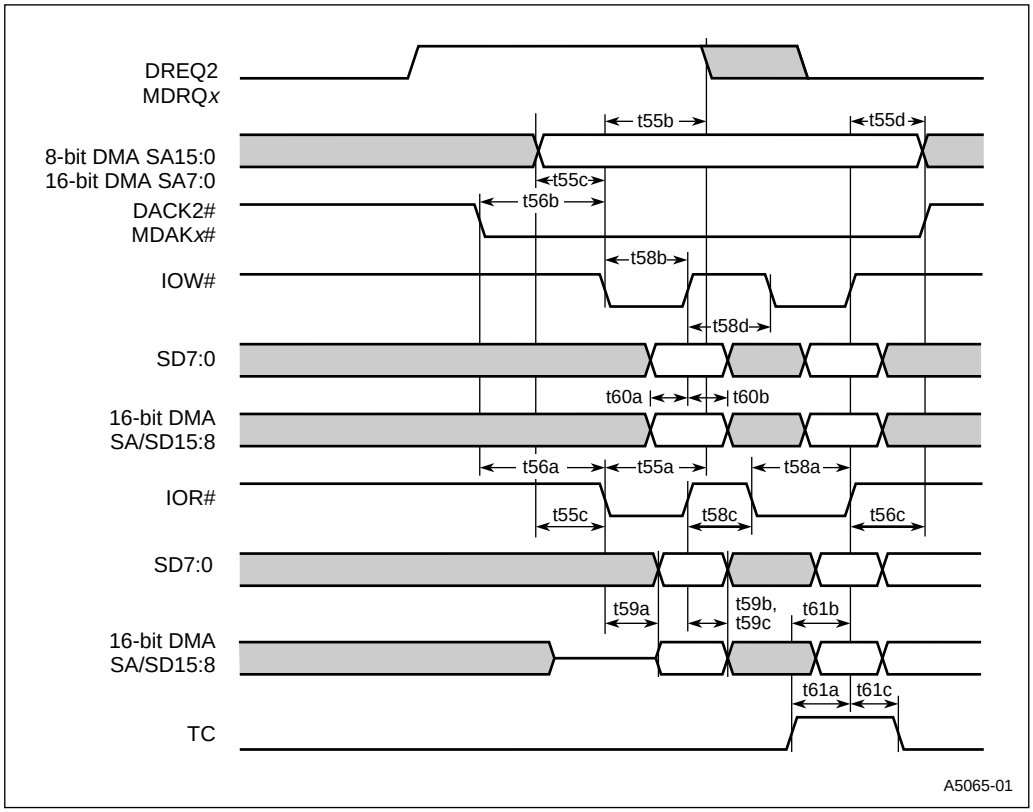

Figure 51. DMA Type F Timing

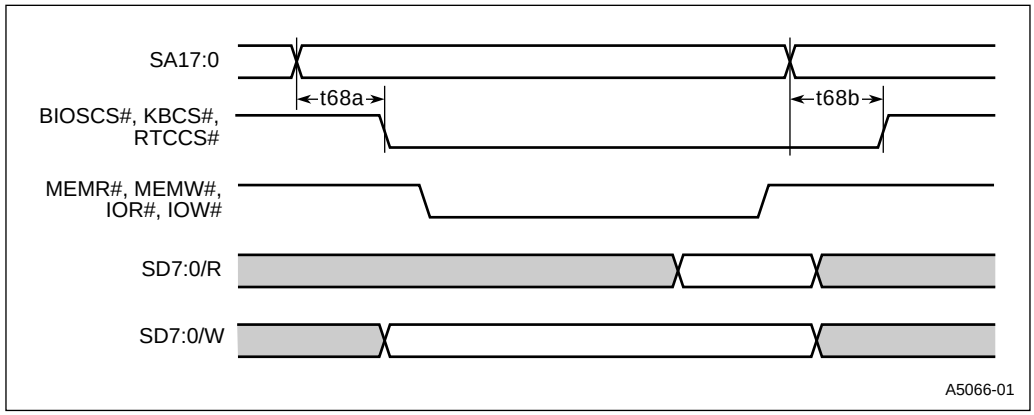

Figure 52. MPIIX Access to EIO Peripherals Timing

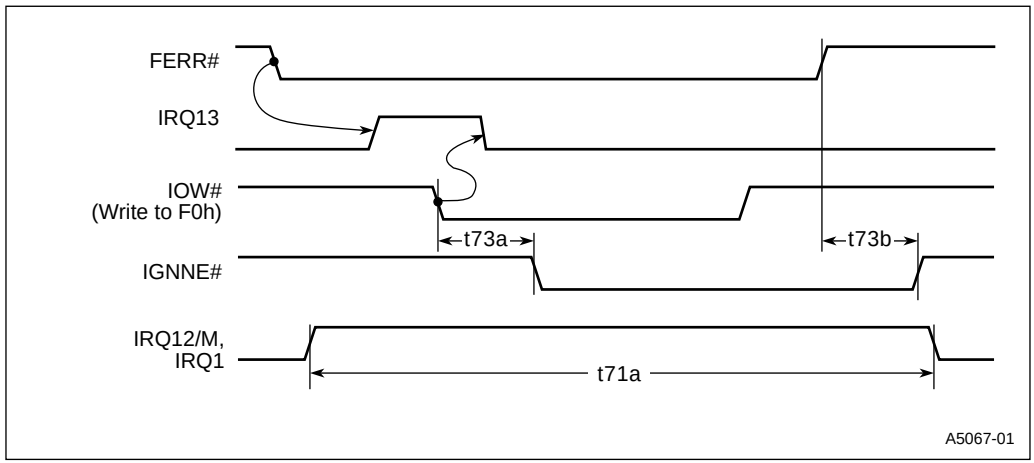

Figure 53. Coprocessor Error and Mouse Support Timing

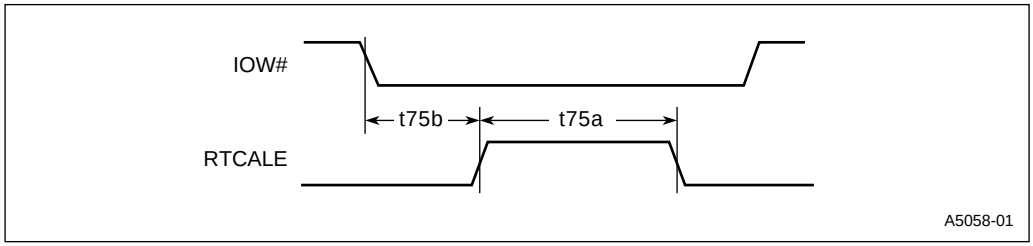

Figure 54. Real Time Clock Timing (RTCALE Generation)

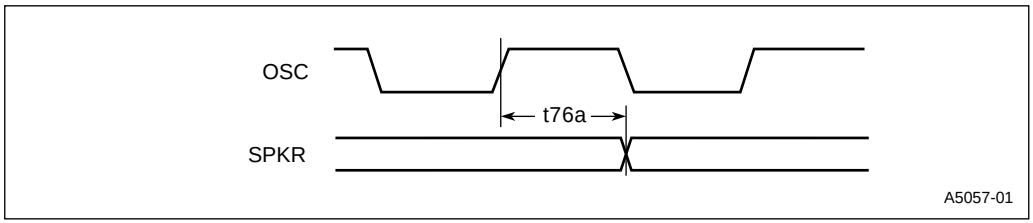

Figure 55. Speaker Timing

2.4.2 PCI Timing Diagrams

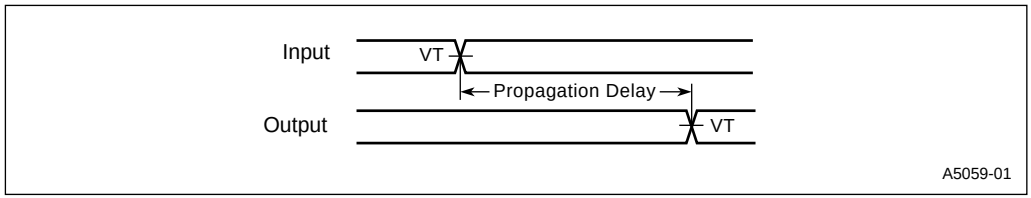

Figure 56. Propagation Delay

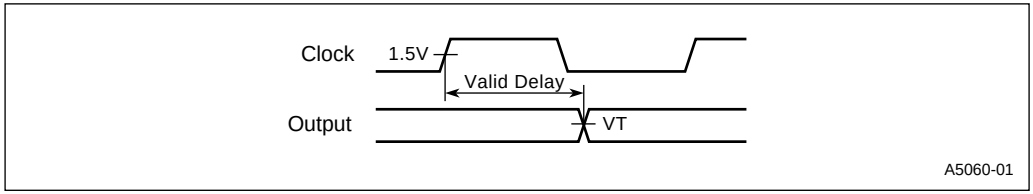

Figure 57. Valid Delay From Rising Clock Edge

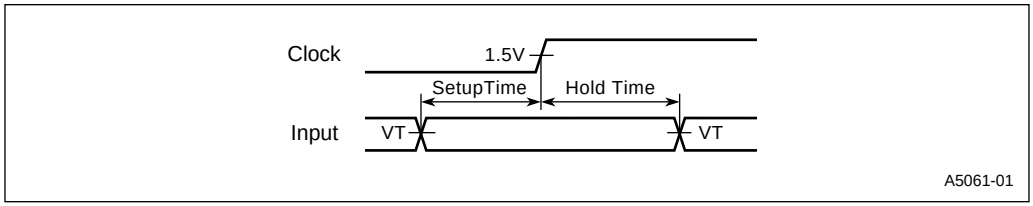

Figure 58. Setup and Hold Times

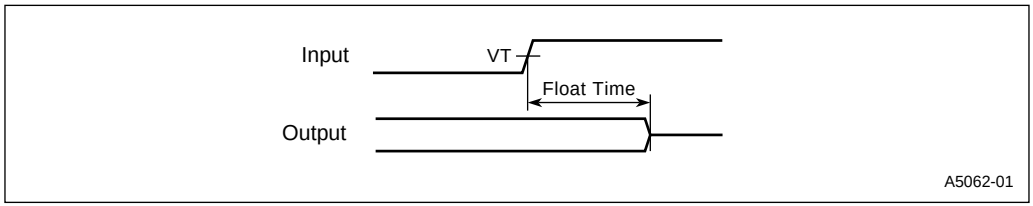

Figure 59. Float Delay

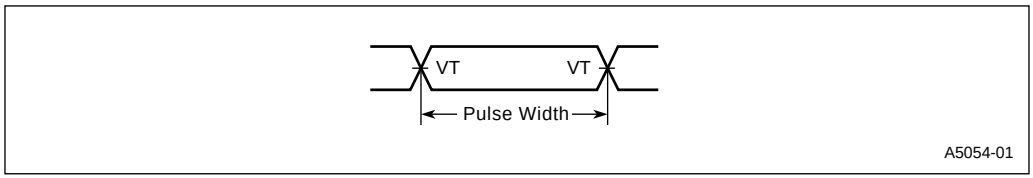

Figure 60. Pulse Width

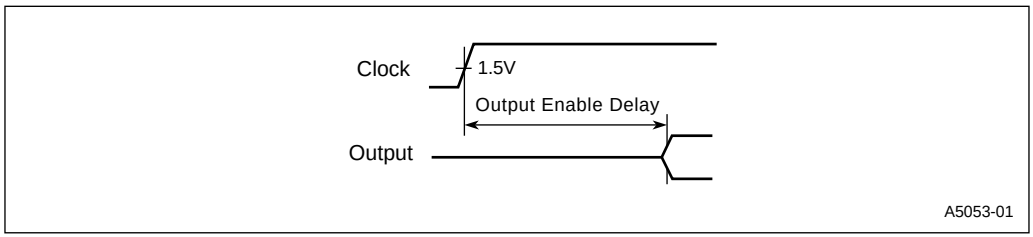

Figure 61. Output Enable Delay

2.4.3 IDE Timing Diagrams

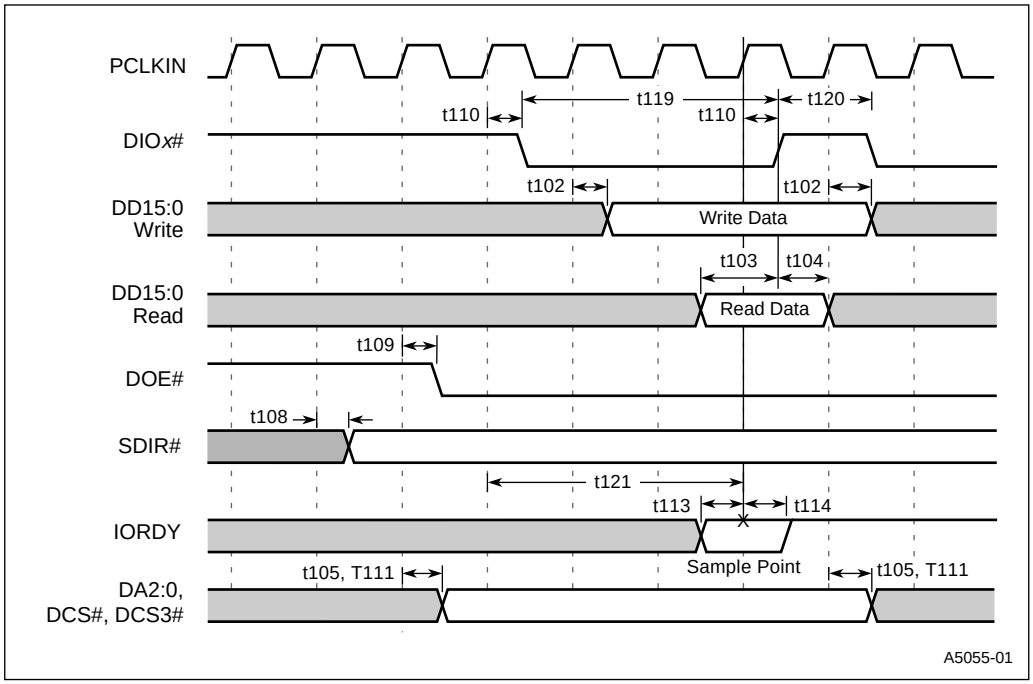

Figure 62. IDE PIO Mode

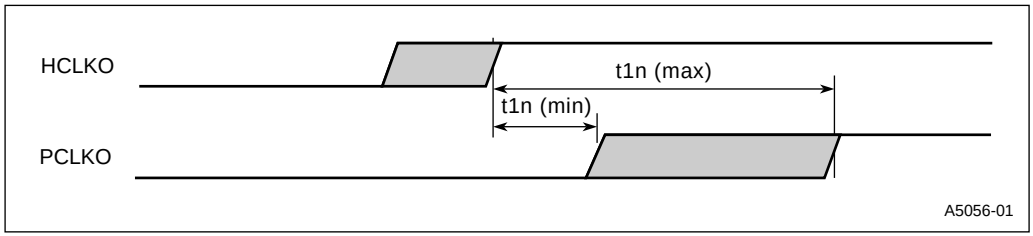

Figure 63. HCLKO to PCLKO Relationship