DATASHEET ADDENDUM

Intel 430TX PCIset System Controller (MTXC)
Timing Specification

273134-001

October, 1997

82439TX System Controller (MTXC) Features

- **Supports Mobile and Desktop**
- **Supports the Pentium® Processor Family Host Bus at 66 MHz and 60 MHz at 3.3 V and 2.5 V**
- **PCI 2.1 Compliant**
- **Integrated Data Path**
- **Integrated DRAM Controller**
  - **— 4 Mbytes to 256 Mbytes main memory**
  - **— 64-Mbit DRAM/SDRAM Technology Support**
  - **— FPM (Fast Page Mode), EDO and SDRAM DRAM Support**
  - **— 6 RAS Lines Available**
  - **— Integrated Programmable Strength for DRAM Interface**
  - **— CAS-Before-RAS Refresh, Extended Refresh and Self Refresh for EDO**
  - **— CAS-Before-RAS and Self Refresh for SDRAM**
- **Integrated L2 Cache Controller**
  - **— 64-MB DRAM Cacheability**
  - **— Direct Mapped Organization—Write Back Only**
  - **— Supports 256K and 512K Pipelined Burst SRAM and DRAM Cache SRAM**
  - **— Cache Hit Read/Write Cycle Timings at 3-1-1-1**
  - **— Back-to-Back Read/Write Cycles at 3-1-1-1-1-1-1-1**
  - **— 64K x 32 SRAM Also Supported**
- **Fully Synchronous, Minimum Latency 30/33-MHz PCI Bus Interface**
  - **— Five PCI Bus Masters (including PIIX4)**
  - **— 10 DWord PCI-to-DRAM Read Prefetch Buffer**
  - **— 18 DWord PCI-DRAM Post Buffer**
  - **— Multi-Transaction Timer to Support Multiple Short PCI Transactions**
- **Power Management Features**
  - **— PCI CLKRUN# Support**
  - **— Dynamic Stop Clock Support**
  - **— Suspend to RAM (STR)**
  - **— Suspend to Disk (STD)**
  - **— Power On Suspend (POS)**
  - **— Internal Clock Control**
  - **— SDRAM and EDO Self Refresh During Suspend**
  - **— ACPI Support**
  - **— Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM)**
  - **— SMM Writeback Cacheable in E_SMRAM Mode up to 1 Mbyte**
  - **— 3.3/5V DRAM, 3.3/5V PCI 3.3/5V Tag and 3.3/2.5 SRAM Support**
- **Test Features**
  - **— NAND Tree Support for all Pins**
- **Supports the Universal Serial Bus (USB)**
- **324-Pin mBGA 430TX PCIset Xcelerated Controller (MTXC) with Integrated Data Paths**

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheet published for the Intel 82439TX System Controller (MTXC). Please refer to the standard package datasheet (order number 290559) for product information and specifications not found in this document.

NOTICE: This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

FIGURES

TABLES

1.0 Electrical Characteristics

1.1 Absolute Maximum Ratings

Case Temperature under Bias ..... 0°C to +85°C
Storage Temperature ..... -55°C to +150°C

Voltage on 5 V tolerant pins with respect to ground ..... -0.3 to V_{CC}5REF + 0.3
Voltage on 3.3 V pins with respect to ground ..... -0.3 to V_{CC} + 0.3
Supply Voltage with respect to V_{SS} ..... -0.3 to +3.6 V
(2.5 V CPU) Supply Voltage with respect to V_{SS} ..... -0.2 to +2.7 V

Maximum Power Dissipation ..... 1.0 W

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

1.2 Thermal Characteristics

The MTXC is designed for operation at case temperatures between 0°C and 85°C. The thermal resistances of the MTXC are provided in Table 1.

Table 1. MTXC Package Thermal Resistance

Parameter	Air Flow Meters/Second (Linear Feet per Minute)	
	0 (0)	1.0 (196.9)
θ_{ja} (°C/Watt)	34	26
θ_{jc} (°C/Watt)	8	

1.3 MTXC DC Characteristics

Table 2. MTXC DC Characteristics (Sheet 1 of 2)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V VREF = 5 V ± 5%; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	-0.3	0.8	V	Notes 1, 2, 3 V_{CC} =3.135 V
V_{IL2}	Input Low Voltage	-0.3	0.7	V	Note 1 V_{CC}(CPU) = 2.375 V
V_{IH1}	Input High Voltage (3.3 V signals)	2.2	V_{CC} + 0.3	V	Notes 1, 2, 3 V_{CC} = 3.6 V
V_{IH2}	Input High Voltage (2.5 V signals)	1.7	V_{CC} + 0.3	V	Note 1 V_{CC} = 2.7 V
V_{IH3}	Input High Voltage (5 V signals)	2.2	VREF + 0.3	V	Note 2 VREF = 5.25 V
V_{OL1}	Output Low Voltage IOL = 1 mA (all signals except as noted below) IOL = 3 mA (Note 4) IOL = 6 mA (Note 5)		0.4	V	3.3 V signals (Note 7)
V_{OL2}	Output Low Voltage IOL = 100 µA IOL = 1 mA IOL = 2 mA		 0.2 0.3 0.4	V	2.5 V Signals Note 1

NOTES:

1. These signals are CPU V_{CC} (3.3 V or 2.5 V):
   A[31:3], BE[7:0]#, BRDY#, NA#, AHOLD, EADS#, HD[63:0], KEN#/INV, HLOCK#, M/IO#,D/C#, W/R#, ADS#, HITM#, CACHE#, SMIACT#, HCLKIN, V_{CC}(CPU)
2. These signals are 3.3 V with 5.0 V tolerance:
   TIO[7:0], AD[31:0], C/BE[3:0]#, PLOCK#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, REQ[3:0]#, PCLKIN, PHLD#, MD[63:0], TESTIN#, PCLKIN, VREF, LOCK#, PHLDA#, CLKRUN#, RST#
3. These signals are 3.3 V:
   KRQAK, TWE#, BWE#, GWE#, COE#, CCS#, CADS#, CADV#, CKEB, CKE, SCAS[A,B]#, MWE#, MWEB#, MA[11:0], CAS[7:0]# or DQM[7:0], RAS[5:0]# or CS[5:0]#, V_{CC}(SUS), V_{CC}, SUSTAT1#, SUSCLK, GNT[3:0]#
4. I_{OL} and I_{OH} apply to the following signals: AD[31:0], C/BE[3:0]#, PAR
5. I_{OL} and I_{OH} apply to the following signals: FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, LOCK#
6. I_{IL} applies to the following signals: HD[63:0], MD[63:0], KRQAK, TIO[7:0], A27. These signals have internal pulldown resistors.
7. All signals from note 1 when the CPU V_{CC} is 3.3 V; All signals from notes 2 and 3.
8. Threshold voltage for all delay and pulse width measurements.

Table 2. MTXC DC Characteristics (Sheet 2 of 2)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V VREF = 5 V ± 5%; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	Min	Max	Unit	Notes
V_{OH1}	Output High Voltage IOH = -1 mA (all signals except as noted below) IOH = -2 mA (Notes 4,5)	2.4		V	3.3 V signals (Note 7)
V_{OH2}	Output High Voltage IOH = -100 µA IOH = -1 mA IOH = -2 mA	 2.1 1.9 1.7		V	2.5 V Signals Note 1
V_{T1}	Threshold Voltage (3.3 V Signals)	1.5	1.5	V	Note 8
V_{T2}	Threshold Voltage (2.5 V Signals)	1.25	1.25	V	Note 8
I_{IL1}	Input Leakage Current		±10	µA	0 V<Vin<V_{CC}
I_{IL2}	Input Leakage Current		±300	µA	Note 6 0 V<Vin<V_{CC}
C_{IN}	Input Capacitance		12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1 MHz

NOTES:

1. These signals are CPU V_{CC} (3.3 V or 2.5 V):
   A[31:3], BE[7:0]#, BRDY#, NA#, AHOLD, EADS#, HD[63:0], KEN#/INV, HLOCK#, M/IO#,D/C#, W/R#, ADS#, HITM#, CACHE#, SMIACT#, HCLKIN, V_{CC}(CPU)
2. These signals are 3.3 V with 5.0 V tolerance:
   TIO[7:0], AD[31:0], C/BE[3:0]#, PLOCK#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, REQ[3:0]#, PCLKIN, PHLD#, MD[63:0], TESTIN#, PCLKIN, VREF, LOCK#, PHLDA#, CLKRUN#, RST#
3. These signals are 3.3 V:
   KRQAK, TWE#, BWE#, GWE#, COE#, CCS#, CADS#, CADV#, CKEB, CKE, SCAS[A,B]#, MWE#, MWEB#, MA[11:0], CAS[7:0]# or DQM[7:0], RAS[5:0]# or CS[5:0]#, V_{CC}(SUS), V_{CC}, SUSTAT1#, SUSCLK, GNT[3:0]#
4. I_{OL} and I_{OH} apply to the following signals: AD[31:0], C/BE[3:0]#, PAR
5. I_{OL} and I_{OH} apply to the following signals: FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, LOCK#
6. I_{IL} applies to the following signals: HD[63:0], MD[63:0], KRQAK, TIO[7:0], A27. These signals have internal pulldown resistors.
7. All signals from note 1 when the CPU V_{CC} is 3.3 V; All signals from notes 2 and 3.
8. Threshold voltage for all delay and pulse width measurements.

Table 3. MTXC Pin States in Various System Modes (Sheet 1 of 2)

MTXC Signals		Power Plane	Type	Buffer[1]	During Reset	After Reset	Max	Chip Standby	During POS	During STR
Host Interface	A[31:3]	V_{CC}(CPU)	I/O	3.3/2.5 V	Low[2]	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	BE[7:0]#	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Toggling	Input	Input	Pwrdn
	ADS#	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Toggling	Input	Input	Pwrdn
	BRDY#	V_{CC}(CPU)	O	3.3/2.5 V	High	High	Toggling	High	High	Pwrdn
	NA#	V_{CC}(CPU)	O	3.3/2.5 V	High	High	Toggling	High	High	Pwrdn
	AHOLD	V_{CC}(CPU)	O	3.3/2.5 V	High	Low	Toggling	Low	Low	Pwrdn
	EADS#	V_{CC}(CPU)	O	3.3/2.5 V	High	High	Toggling	High	High	Pwrdn
	BOFF#	V_{CC}(CPU)	O	3.3/2.5 V	High	High	Toggling	High	High	Pwrdn
	HITM#	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Toggling	Input	Input	Pwrdn
	W/R#	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Toggling	Input	Input	Pwrdn
	HLOCK#	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Toggling	Input	Input	Pwrdn
	CACHE#	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Toggling	Input	Input	Pwrdn
	KEN#/INV	V_{CC}(CPU)	O	3.3/2.5 V	Low	Low	Toggling	Low	Low	Pwrdn
	SMIACT#	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Toggling	Input	Input	Pwrdn
	HD[63:0]	V_{CC}(CPU)	I/O	3.3/2.5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
DRAM Interface	RAS[5:0]#/ CS[5:0]#	V_{CC}(SUS)	O	3.3 V	Undef	High	Toggling	Toggling	Toggling	Toggling
	CAS[7:0]#/ DQM[7:0]	V_{CC}(SUS)	O	3.3 V	Undef	Undef	Toggling	Toggling	Toggling	Toggling
	MA[11:0]	V_{CC}	O	3.3 V	Undef	Undef	Toggling	Low	Low	Pwrdn
	MWE# MWEB#	V_{CC}(SUS)	O	3.3 V	High	High	Toggling	High	High	High
	SRAS[A,B}#	V_{CC}	O	3.3 V	High	High	Toggling	Toggling	Low	Pwrdn
	SCAS[A,B]#	V_{CC}	O	3.3 V	High	High	Toggling	Toggling	Low	Pwrdn
	CKE	V_{CC}(SUS)	O	3.3 V	Undef	High	High	High	Low	Low
	CKEB	V_{CC}	O	3.3 V	Undef	High	High	High	Low	Pwrdn
	MD[63:0]	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn

NOTES:

1. 3.3/2.5 V indicates the buffer is 3.3 V or 2.5 V only, depending upon the V_{CC}(CPU) voltage. 3.3/5 V indicates that the output is 3.3 V, and input is 3.3 V with 5 V tolerance. 5 V indicates 3.3 V input with 5 V tolerance.
2. A[31:26] are inputs during Reset.

Table 3. MTXC Pin States in Various System Modes (Sheet 2 of 2)

MTXC Signals		Power Plane	Type	Buffer[1]	During Reset	After Reset	Max	Chip Standby	During POS	During STR
L2 Cache Interface	CADV#	V_{CC}	O	3.3 V	High	High	Toggling	High	High	Pwrdn
	CADS#	V_{CC}	O	3.3 V	High	High	Toggling	High	High	Pwrdn
	CCS#	V_{CC}	O	3.3 V	Low	Low	Low	Low	Low	Pwrdn
	COE#	V_{CC}	O	3.3 V	High	High	Toggling	High	High	Pwrdn
	GWE#	V_{CC}	O	3.3 V	High	High	Toggling	High	High	Pwrdn
	BWE#	V_{CC}	O	3.3 V	High	High	Toggling	High	High	Pwrdn
	TIO[7:0]	V_{CC}	I/O	3.3 V	Low	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	TWE#	V_{CC}	O	3.3 V	Low	High	Toggling	High	High	Pwrdn
	KRQAK / CS4_64#	V_{CC}	I/O	3.3 V	Input	Input	Toggling	Input	Input	Pwrdn
PCI Interface	AD[31:0]	V_{CC}	I/O	3.3/5 V	Low	Hi-Z	Toggling	Last	Last	Pwrdn
	C/BE[3:0]#	V_{CC}	I/O	3.3/5 V	Low	Hi-Z	Toggling	Last	Last	Pwrdn
	FRAME#	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	DEVSEL#	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	IRDY#	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	TRDY#	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	STOP#	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	LOCK#	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Toggling	Hi-Z	Hi-Z	Pwrdn
	REQ[3:0]#	V_{CC}	I	3.3/5 V	Input	Input	Input	Input	Input	Pwrdn
	GNT[3:0]#	V_{CC}	O	3.3 V	Hi-Z	High	Toggling	High	High	Pwrdn
	PHLD#	V_{CC}	I	3.3/5 V	Input	Input	Input	Input	Input	Pwrdn
	PHLDA#	V_{CC}	O	3.3 V	High	High	Toggling	High	High	Pwrdn
	PAR	V_{CC}	I/O	3.3/5 V	Low	Undef	Toggling	Undef	Undef	Pwrdn
	CLKRUN#	V_{CC}	I/O	3.3/5 V	Hi-Z	Hi-Z	Low	Low	High	Pwrdn
	RST#	V_{CC}	I	3.3/5 V	Input	Input	High	Input	Input	Pwrdn
Test / Clock Signals	TEST#	V_{CC}	I	3.3/5 V	Input	Input	Input	Input	Input	Pwrdn
	HCLKIN	V_{CC}(CPU)	I	3.3/2.5 V	Input	Input	Input	Input	Input	Pwrdn
	PCLKIN	V_{CC}	I	3.3/5 V	Input	Input	Input	Input	Input	Pwrdn
Power Management	SUSCLK	V_{CC}(SUS)	I	3.3 V	Input	Input	Input	Input	Input	Input
	SUSSTAT1#	V_{CC}(SUS)	I	3.3 V	Input	Input	Input	Input	Input	Input

NOTES:

1. 3.3/2.5 V indicates the buffer is 3.3 V or 2.5 V only, depending upon the V_{CC}(CPU) voltage. 3.3/5 V indicates that the output is 3.3 V, and input is 3.3 V with 5 V tolerance. 5 V indicates 3.3 V input with 5 V tolerance.
2. A[31:26] are inputs during Reset.

For the Standby State, the following assumptions are made:

- Host bus is idle
- PCI bus is idle
- DRAM bus is idle except for DRAM refresh cycles
- All external clocks are running: HCLK (66 MHz), PCLOCK (33 MHz), SUSCLK (32 KHz)
- Not in any suspend state
- No PCI activity

For the MAX state, the following assumptions are made:

- Host Bus cycle in progress
- PCI bus cycle in progress
- DRAM bus cycle in progress

1.4 MTXC AC Characteristics

All timings are in nanoseconds (ns) unless otherwise specified.

Table 4. Host Clock Timing: 66 MHz (MTXC)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V; VREF = 5 V ± 5%; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t1	HCLKIN Period	15.0	20.0	1	
t1s	HCLKIN Period Stability		±250		pS
t1H	HCLKIN High Time	5.5		1	
t1L	HCLKIN Low Time	5.5		1	
t1r	HCLKIN Rise Time		1.5	1	
t1f	HCLKIN Fall Time		1.5	1	

Table 5. CPU Interface Timing: 66 MHz (MTXC)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V; VREF = 5 V ± 5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t2	ADS# Setup Time to HCLKIN Rising	5.0		4	
t3	W/R# Setup Time to HCLKIN Rising	5.7		4	
t4	BE[7:0]# Setup Time to HCLKIN Rising	3.4		4	
t5	HITM# Setup Time to HCLKIN Rising	5.3		4	
t6	CACHE# Setup Time to HCLKIN Rising	5.0		4	
t7	M/IO# Setup Time to HCLKIN Rising	5.3		4	
t8	D/C# Setup Time to HCLKIN Rising	5.0		4	
t9	HLOCK#, SMIACT# Setup Time to HCLKIN Rising	4.0		4	
t11	ADS#, HITM#, W/R#, M/IO#, D/C#, BE[7:0]#, HLOCK#, CACHE#, SMIACT# Hold Time from HCLKIN Rising	1.0		4	
t12	A[31:0] Setup Time to HCLKIN Rising	3.5		4	
t13	A[31:0] Hold Time from HCLKIN Rising	1.0		4	
t14	A[31:0] Valid Delay from HCLKIN Rising	2.0	13.0	3	0 pF
t15	A[31:0] Output Enable From HCLKIN Rising	0.0	13.0	8	
t16	A[31:0] Float Delay from HCLKIN Rising	0.0	13.0		
t17	HD(63:0) Setup Time to HCLK Rising	3.75			
t18	HD(63:0) Hold Time from HCLK Rising	1.0			
t19	HD(63:0) Valid Delay from HCLK Rising	1.5	7.0		0 pF
t20	HD(63:0) Flow Through Delay from MD[63:0], 66 MHz, 5-2-2-2	1.5	6.0		0 pF
t21	BRDY# Valid Delay from HCLKIN Rising	1.5	8.0	3	0 pF
t22	NA# Valid Delay from HCLKIN Rising	1.5	8.0	3	0 pF
t23	AHOLD Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF
t24	BOFF# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF
t25	EADS# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF
t26	KEN#/INV Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF

Table 6. Second-Level Cache Timing: 66 MHz (MTXC)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V; VREF = 5 V ± 5%; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t27	COE# Valid Delay from HCLKIN Rising	2.0	8.0	3	0 pF
t28	GWE# Valid Delay from HCLKIN Rising	2.0	9.5	3	0 pF
t29	BWE# Valid Delay from HCLKIN Rising	2.0	9.0	3	0 pF
t30	KRQAK Valid Delay from HCLKIN	1.5	7.0		0 pF
t31	KRQAK setup time to HCLKIN	2.8			
t32	KRQAK Hold Time from HCLKIN	1.0			
t33	TIO[7:0] Valid Delay from HCLKIN Rising	2.0	8.0	3	0 pF
t34	TIO[7:0] Setup time to HCLKIN Rising	2.2		4	
t35	TIO[7:0] Hold time to HCLKIN Rising	2.0		4	
t36	CCS# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF
t37	CADS# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF
t38	CADV# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF
t39	TWE# Valid Delay	2.0	9.0	3	0 pF

Table 7. EDO/FPM DRAM Interface Timing; 66 MHz (MTXC)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V; VREF = 5 V ± 5%; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		Fig.	Notes
		Min	Max		
t40	RAS[5:0]# Valid Delay from HCLK Rising	1.5	7.0	3	0 pF
t41	CAS[7:0]# Valid Delay from HCLKIN Rising	1.5	6.0	3	0 pF
t42	MWE#, MWEB# Valid Delay From HCLKIN Rising	1.5	19.0	3	0 pF
t43	MA[13:0] Flow Through Delay from HA (read col addr)	2.0	8.0		0 pF
t44	MA[13:0] Valid Delay from HCLK Rising (read row addr)	2.0	9.0		0 pF
t45	MA[11:0] Valid Delay from HCLK Rising (read col addr burst cycles)	2.0	6.5		0 pF (Also applies when CKE pins are used as copies of MA[1:0])
t46	MA[1:0] Valid Delay from HCLK Rising (Write Row and Col Addr)	2.0	10.0		0 pF
t48	MD[63:0] set up to HCLK Rising	1.1			
t49	MD[63:0] hold time from HCLK Rising	4.0			
t50	MD[63:0] Valid delay from HCLK Rising	2.0	8.0		0 pF
SDRAM Interface Timing					
t51	SRAS[B:A]# Valid Delay from HCLKIN Rising (two clock path)	5.0	19.0		0 pF
t52	SCAS[B:A]# Valid Delay from HCLKIN Rising (two clock path)	5.0	19.0		0 pF
t56	MWE#,MWEB# Valid delay from HCLKIN Rising (Two Clock Path)	5.0	19.0	3	0 pF
t57	CKE, CKEB Valid Delay from HCLKIN Rising	1.5	6.0		0 pF
t58	CS[5:0]# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pF
t59	DQM[7:0] Valid Delay from HCLKIN Rising	1.5	6.0	3	0 pF
t60	MA[11:0] Valid Delay from HCLKIN Rising	2.0	16.0	3	0 pF
t61	MD[63:0] set up to HCLK Rising	3.5			0 pF
t62	MD[63:0] hold time from HCLK Rising	1.0			0 pF
t62a	MD[63:0] Valid Delay from HCLK Rising	2.0	8.0		0 pF

Table 8. PCI Clock Timing; 66 MHz (MTXC)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V; VREF = 5 V ± 5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Figure	Notes
		Min	Max		
PM and TEST Timing					
t63	SUSSTAT1# Setup Time	7			
t64	SUSSTAT1# Hold Time	2			
t64s	SUSCLK	Async			
t64t	TESTIN#	Async			
PCI Clocks					
t65	PCLKIN High Time	12.0		1	
t66	PCLKIN Low Time	12.0		1	
t66r	PCLKIN Rise Time		3.0	1	
t66f	PCLKIN Fall Time		3.0	1	

Table 9. PCI Interface Timing; 66 MHz (MTXC)

Functional Operating Range (V_{CC} = 3.13 V to 3.6 V; V_{CC}(CPU) = 2.37 V to 2.62 V / 3.13 V to 3.6 V; VREF = 5 V ± 5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t67	AD[31:0] Valid Delay	2	11	3	
t68	AD[31:0] Setup Time	7		4	
t63	AD[31:0] Hold Time from PCLKIN	0		4	
t70	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Valid Delay from PCLKIN Rising	2.0	11.0	3	
t71	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Output Enable Delay from PCLKIN Rising	2.0	11.0	8	
t72	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Float Delay from PCLKIN Rising	2.0	11.0	5	
t73	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Setup Time to PCLKIN Rising	7.0		4	
t74	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Hold Time from PCLKIN Rising	0.0		4	
t75	PHLDA# Valid Delay from PCLKIN Rising	2	9.0	3	
t76	GNT[3:0] # Valid Delay from PCLKIN Rising	2	9.0		
t77	REQx#, PHLD# Setup Time from PCLKIN Rising	12.0			
t78	REQx#, PHLD# Hold Time from PCLKIN Rising	0.0			
t79	RST# Low Pulse Width	1 ms		7	
t80	CLKRUN#	Async			

2.0 MTXC Timing Diagrams

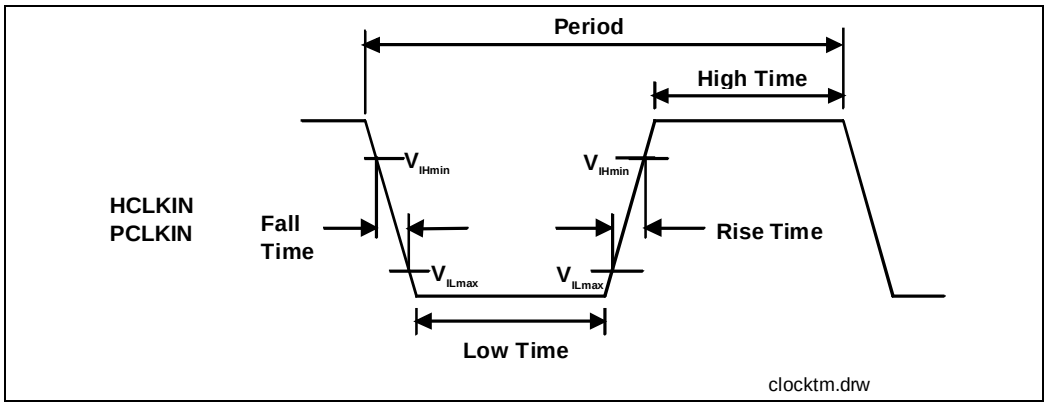


Figure 1. Clock Timing

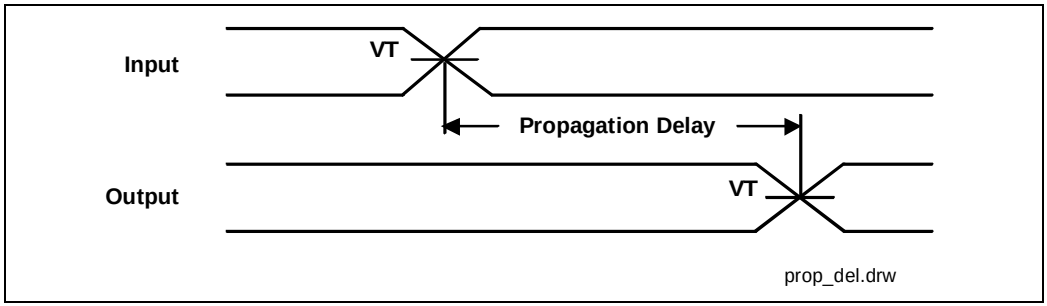


Figure 2. Propagation Delay

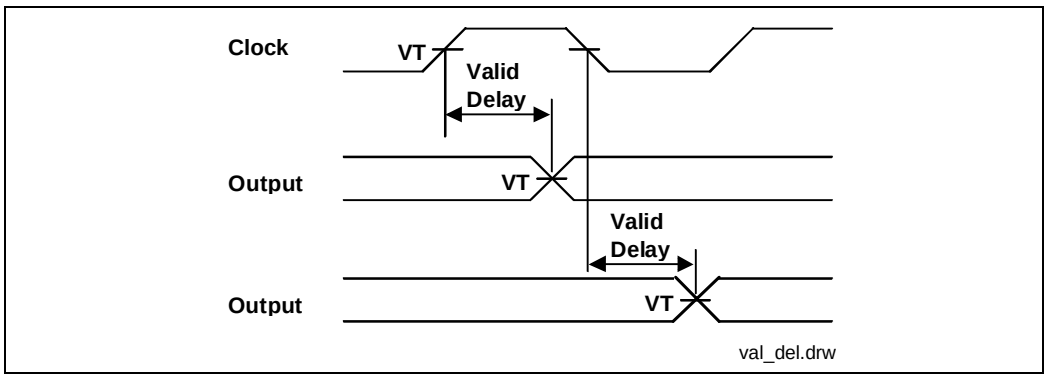


Figure 3. Valid Delay From Rising Clock Edge

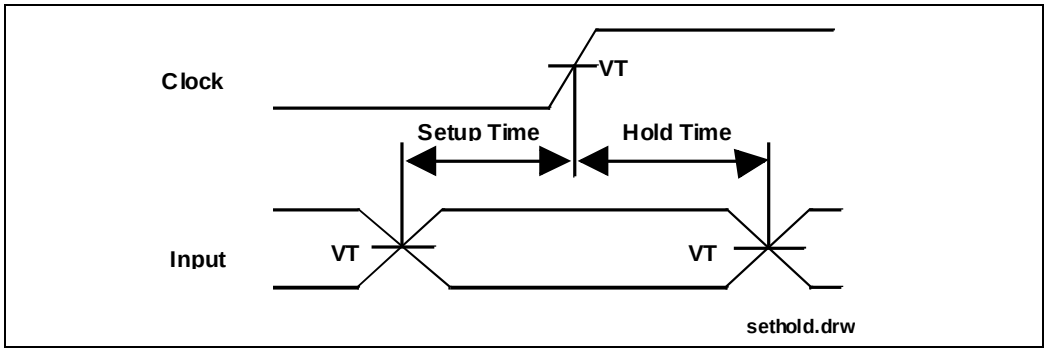


Figure 4. Setup and Hold Times

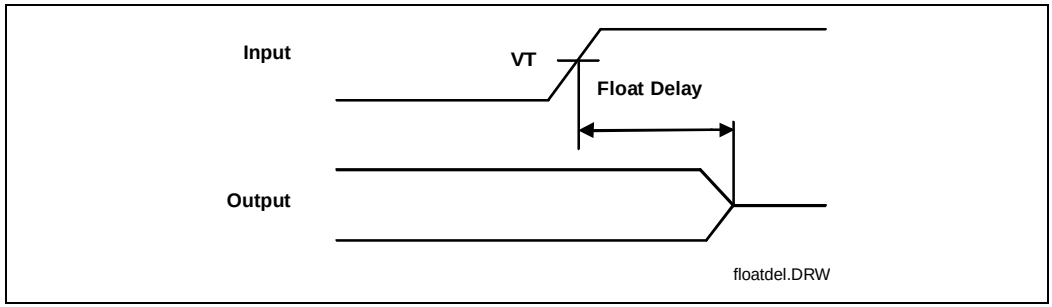
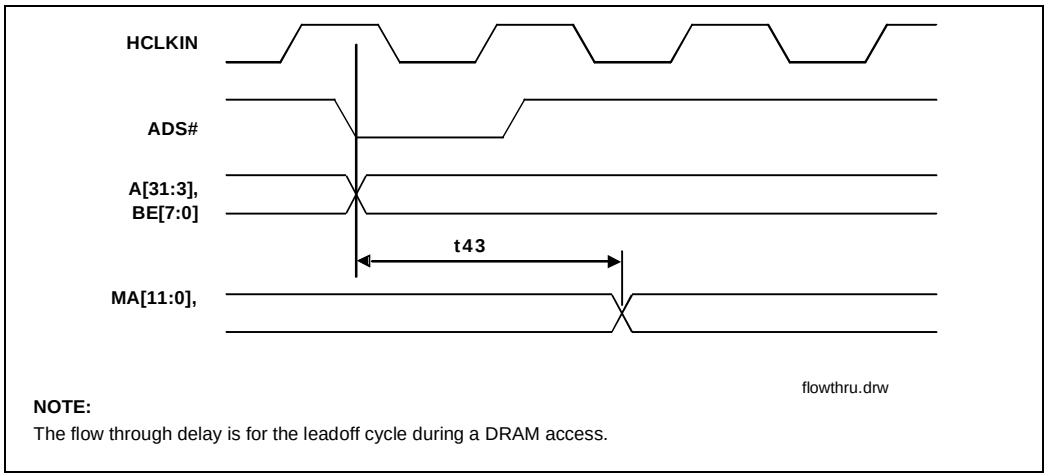


Figure 5. Float Delay



NOTE:
The flow through delay is for the leadoff cycle during a DRAM access.

Figure 6. Flow Through Delay

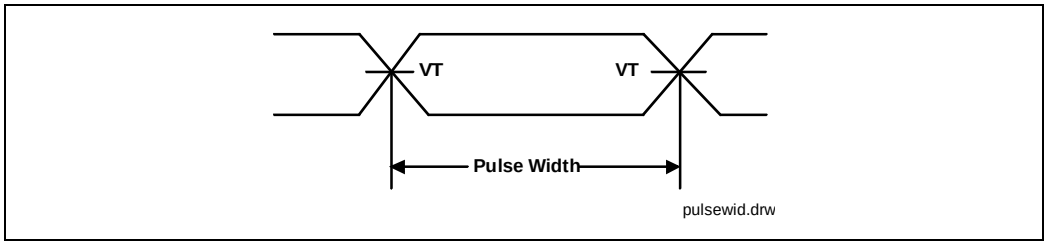


Figure 7. Pulse Width

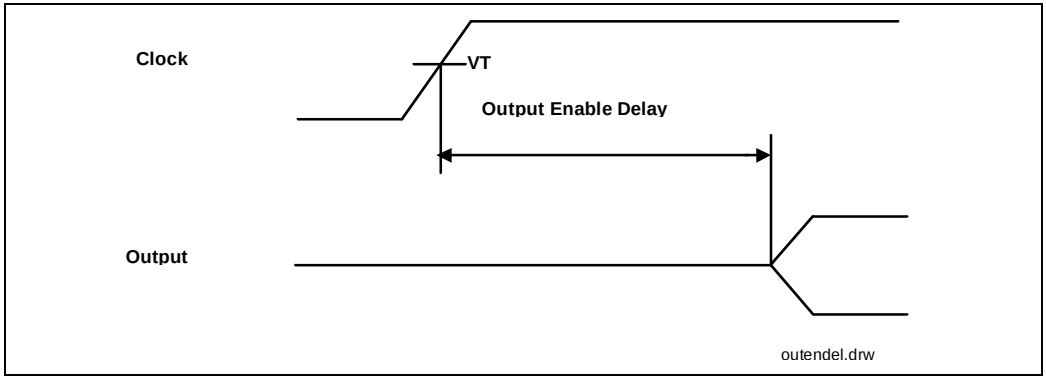


Figure 8. Output Enable Delay