

Description



The new PRISM chipset provides a complete solution from antenna to computer bus for 11Mbps WLAN products. The parts provide improved performance and lower power

consumption compared to first generation PRISM products.

The chip set is comprised of 5 parts:

- HFA3683 2.4GHz RF/IF Converter and Synthesizer
- HFA3783 AGC Quadrature Modem and Synthesizer
- HFA3983 PA with Detector
- HFA3861 Baseband Processor with Rake Receiver
- CW10 Media Access Controller

The RFIC's are produced in advanced SiGe technology to realize improvements in integration, performance, and power consumption. Integral PLL's in both the RF and IF parts eliminate the need for an external synthesizer. The HFA3683's internal LNA noise figure is improved so that an external LNA IC is no longer needed. The chip set is designed so that the parts can be interfaced with few external components.

The IF is a linear design with AGC. This permits the use of equalizers in the BBP. An IF overload detector and a selectable low gain LNA mode work with the BBP to extend dynamic range without sacrificing sensitivity.

The PA incorporates an integral power detector that is monitored by the BBP to control the IF gain to maintain constant output levels.

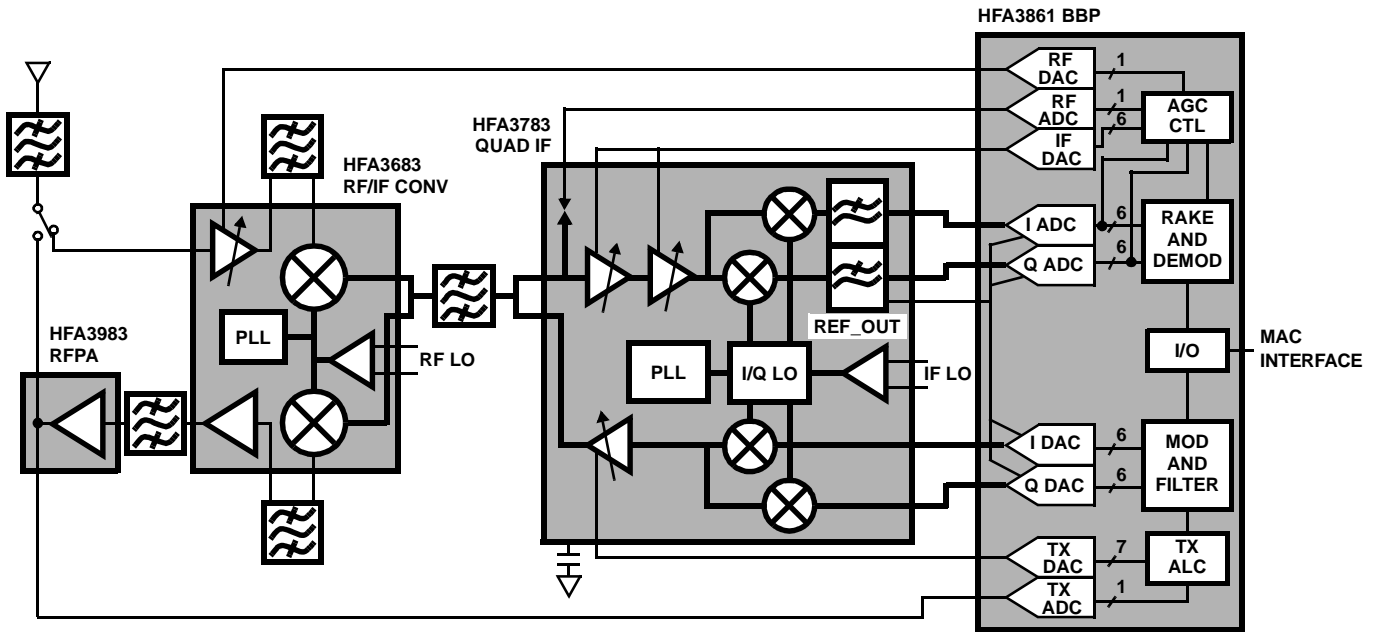
The baseband processor uses CCK modulation and a Rake architecture to reduce the effects of multipath distortion. This reduces the error rates in typical office environments to improve overall data throughput. An optional fast acquisition mode further improves throughput.

The MAC utilizes a processor optimized for control of the WLAN protocol. It supports the 11Mbps data rate with low power consumption.

Intersil will provide a complete reference design with software to minimize the time to market for WLAN products.

Features

- Complete 2.4GHz WLAN Adapter Solution in 5 IC's
- Compliant to IEEE 802.11 DSSS Standard at 1 and 2 MBPS
- Compliant to DRAFT IEEE 802.11 Extension at 5.5MBPS and 11MBPS
- RFIC's Built in Advanced SiGe Process
- Power Consumption Reduced By Nearly 50%
- Rake Architecture for Improved Multipath Performance
- AGC IF for Linear Operation
- IF Overload Detector
- Low Gain Mode in the LNA for High Level Inputs
- Gain Control Loop for RF and IF Integrated into BBP
- PLL Integrated in RFIC's
- All Parts Operate at 3VDC
- DC Coupling at the Baseband Interface
- Low Noise Figure (1.8dB)
- PA Includes Integral Detector
- Transmit Level Control Provided
- Integral Digital Filtering for Baseband Output
- Seamless Interface Between Chips
- Differential Interfaces at IF and Baseband for Noise Immunity
- Short Preamble Mode for Higher Throughput
- Single IF Filter for Transmit and Receive



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