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Introduction

All physical interface signals provided by the HFA3841 to the HFA3860B conform to the timing specified in the HFA3860B data sheet. The timings are mostly created and controlled by the PHY adaptation firmware.

The HFA3860B uses TX_PE and PA_PE for power control of the transmit sequence. PA_PE should be asserted 2µs after TX_PE, and PA_PE should be de-asserted 2µs before TX_PE.

The HFA3841 does not have 5V tolerance on all IO Pins. This application note assumes that the HFA3841, RAM, and HFA3860B are all operated at a 3.3V supply.

Low speed Flash EPROMs ($T_A \leq 150$ns) may be used for firmware storage in a HFA3841 design. When the HFA3841 is reset, the clock prescaler is initialized to its maximum division ratio (divide by 16). The firmware is then copied from the Flash memory to SRAM, and control is passed to the SRAM control store area before the firmware sets the clock prescaler to the normal operational value.

With the current Intersil chipset, the data and clock are shared between the baseband chip and the synthesizer. This could potentially cause spurious noise to be propagated through the synthesizer when the baseband is accessed through the MMI.

TABLE 1. HFA3841 TO INTERSIL HFA3860B CONNECTION

HFA3841 PIN	HFA3841 NAME	HFA3841 PORT	INTERSIL HFA3860B PIN	INTERSIL HFA3860B NAME	DESCRIPTION [1], [2]
15	TXE	PL0	2	TX_PE (Also Drives PA_PE for Radio)	When active, the transmitter is configured to be operational, otherwise the transmitter is in standby mode. TX_PE is an input from the HFA3841 to the HFA3860B. The rising edge of TX_PE will start the internal transmit state machine and the falling edge will initiate shut down of the state machine. TX_PE envelopes the transmit data except for the last bit. The TXE signal shall remain asserted for 3µs after the clocking of the last bit of the MPDU, to allow for internal pipeline delays in the transmitter.
17	TXD	-	3	TXD	TXD is an input, used to transfer MAC Payload Data Unit (MPDU) data from the HFA3841 to the HFA3860B. The data is received serially with the LSB first. The data is clocked in the HFA3860B at the rising edge of TXCLK. The LSB is received first and the data is clocked in the baseband processor at the falling edge of TXC. A data bit high = "one".
18	TXC	-	4	TXCLK	TXCLK is a clock output used to receive the data on the TXD from the HFA3841 to the HFA3860B, synchronously. Transmit data on the TXD bus is clocked into the HFA3860B on the rising edge. The clocking edge is also programmable to be on either phase of the clock. The rate of the clock will be dependent upon the data rate that is programmed in the signalling field of the header.
32	SDI/SDDIR/ MISO	PJ2	8	R/$\overline{W}$	R/$\overline{W}$ is an input to the HFA3860B used to change the direction of the SD bus when reading or writing data on the SD bus. R/$\overline{W}$ also enables the serial shift register used in a read cycle. R/$\overline{W}$ must be set up prior to the rising edge of SCLK. A high level indicates read while a low level is a write.
29	SDE0	PJ3	9	CS	CS is a Chip Select for the device to activate the serial control port. The CS doesn't impact any of the other interface ports and signals, i.e., the TX or RX ports and interface signals. This is an active low signal. When inactive SD, SCLK, and R/$\overline{W}$ become “don't care” signals.
31	SCLK	PJ0	24	SCLK	SCLK is the clock for the SD serial bus. The data on SD is clocked at the rising edge. SCLK is an input clock and it is asynchronous to the internal master clock (MCLK) The maximum rate of this clock is 11MHz or one half the master clock frequency, whichever is lower.
30	SDO/SDIO/ MOSI	PJ1	25	SD	SD is a serial bidirectional data bus which is used to transfer address and data to/from the internal registers. The bit ordering of an 8-bit word is MSB first. The first 8 bits during transfers indicate the register address immediately followed by 8 more bits representing the data that needs to be written or read at that register.
26	PHYRESET	PL2	28	RESET	When active TX and RX functions are disabled. If RESET is kept low the HFA3860B goes into the power standby mode. RESET does not alter any of the configuration register values nor does it preset any of the registers into default values.

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TABLE 1. HFA3841 TO INTERSIL HFA3860B CONNECTION (Continued)

HFA3841 PIN	HFA3841 NAME	HFA3841 PORT	INTERSIL HFA3860B PIN	INTERSIL HFA3860B NAME	DESCRIPTION [1], [2]
40	XTALI		30	MCLK	Master Clock for device. The nominal frequency of this clock is 44MHz. This is used internally to generate all other internal necessary clocks and is divided by 2 or 4 for the transceiver clocks. This clock is supplied by another source to both the HFA3860B and the HFA3841.
22	MBUSY	PK6	32	CCA	Clear Channel Assessment (CCA) is an output used to signal that the channel is clear to transmit. The CCA algorithm makes its decision as a function of RSSI, Energy Detect (ED), and Carrier Sense (CRS). The CCA algorithm and its features are described elsewhere in the data sheet. Logic 0 = Channel is clear to transmit. Logic 1 = Channel is NOT clear to transmit (busy). This polarity is programmable and can be inverted.
27	RXE/PHYSLP_	PL1	33	RX_PE	When active, the receiver is configured to be operational, otherwise the receiver is in standby mode. This is an active high input signal. In standby, RX_PE inactive, all A/D converters are disabled.
21	PDA	PK5	34	MD_RDY	MD_RDY is an output signal to the HFA3841, indicating header data and a data packet are ready to be transferred to the processor. MD_RDY is an active high signal and it envelopes the data transfer over the RXD serial bus. MD_RDY goes active when the SFD is detected and returns to its inactive state when RX_PE goes inactive or an error is detected in the header.
19	RXD	-	35	RXD	RXD is an output to the HFA3841, transferring demodulated Header information and data in a serial format. The data is sent serially with the LSB first. The data is frame aligned with MD_RDY.
20	RXC	-	36	RXCLK	RXCLK is the bit clock output. This clock is used to transfer Header information and payload data through the RXD serial bus to the HFA3841. This clock reflects the bit rate in use. RXCLK is held to a logic "0" state during the CRC16 reception. RXCLK becomes active after the SFD has been detected. Data should be sampled on the rising edge. This polarity is programmable and can be inverted.

TABLE 2. OTHER HFA3841 SIGNALS INTERFACING TO PHY FUNCTIONS NOT IN THE HFA3860B

HFA3841 PIN	HFA3841 SIGNAL	HFA3841 PORT	PRISM® EVAL NAME	PRISM EVAL PIN	DESCRIPTION
8	MREQ_	PJ5	SYNTH_LE	21	SYNTH_LE, CLK/SYNTH_CLK and SD/SYNTH_DATA signals are used to program the synthesizer. SYNTH_LE latches a frame of 22 bits after it has been shifted by the CLK/SYNTH_CLK into the synthesizer registers. Please note that the clock and data lines are shared also by the baseband processor.
23	EDET	PK7	RADIO_PE	24	This signal is the master power control for the RF section. When asserted high, enables all of the PHY. It does not control power to the HFA3860B, so register settings are retained. This signal should be kept high during operation of this card. (Master Power enable; must be set up by FW during initialization.)
63	GPDS0	PK3	TX_PE_RF	29	IF Power Enable. When active high the transmit IF chain is in transmit mode. Note: This signal must be truly complementary to RX_PE_RF. These should be controlled from the same port so they will change at the same time. If they are ever both high, it causes problems for analog chips in the radio. If both signals are low, the radio is in standby mode.
64	GPDS1	PK4	RX_PE_RF	27	Power control signal for front end and IF receiver electronics. (See note above regarding complementary operation with TX_PE_RF.)

NOTES:

1. There is the potential for confusion between the signal names used on the PRISM-EVAL board (MACless radio) and the HFA3860B baseband chip. Some names specified on the interface to the PRISM-EVAL board are identical to pin names on the HFA3860B, but they do ***not*** represent the same signal. Two such signals, TX_PE and RX_PE, have been renamed to TX_PE_RF and RX_PE_RF in the table above to prevent confusion.
2. The PRISM1RC-EVAL signals OSC_START and BB_AS are not needed. BB_AS connects to the SDI signal on the HFA3860B, and should be tied high. OSC_START on the PRISM-EVAL should be tied low.

TABLE 3. HFA3841 SIGNALS UNUSED IN HFA3860B APPLICATION

HFA3841 PIN	HFA3841 SIGNAL	HFA3841 PORT
65	SDE1	PJ4
7	MGNTb/LED2	PJ6
9	CPATNb/LED1	PJ7
28	ANTSEL	PL3
43	MA19/LED0	PL4
12	MA20/BK512b	PL5
11	MA21/CSCSb/BOOTCS	PL6
93	TXR	PL7
35	GPCK	PK0
34	GPDO/UTXD	PK1
33	GPDI/URXD	PK2

System Memory Connection

The HFA3841 was designed to implement 16-bit wide memory by using two 8-bit RAM chips. The HFA3841 provides high and low write enable signals (MWEH_ and MWEL_), and a single output enable (MOE_). This allows a direct connection, enabling a pair of 8-bit SRAMs to function as a 16-bit device.

Some 16-bit SRAMs use the connections shown in Figure 1: A single Write Enable, and Upper and Lower byte enables, which control both read and write cycles. Thus, external logic is required to generate the required signals. Figure 1 shows the logical function required.

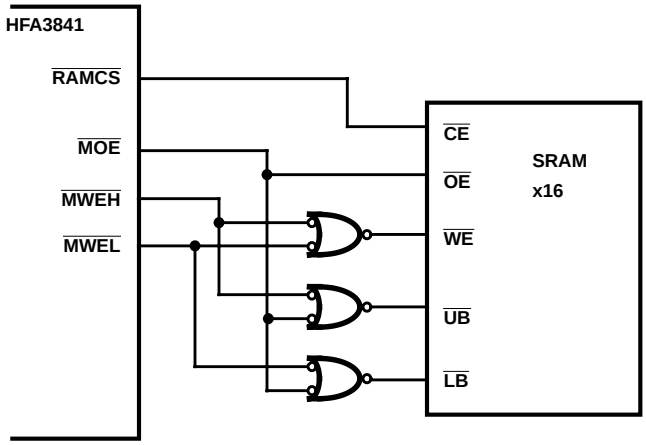
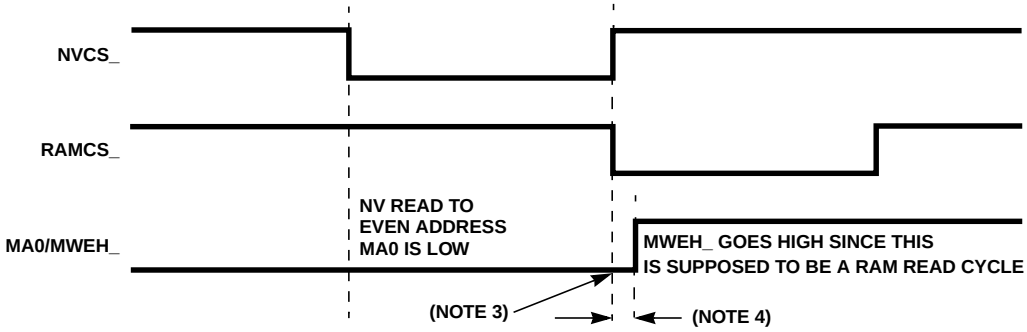


FIGURE 1. 3/4 QUAD AND GATE

A Potential Problem

It is important to note that implementing this logic as shown can result in erroneous operation when fast SRAM devices are used in conjunction with 8-bit Flash. The problem results from the change in function of the MA0/MWEH pin for 16-bit and 8-bit memory devices. Figure 2 illustrates the problem.



NOTES:

3. Function of MA0/MWEH_ changes from MA0 for 8-bit Flash to MWEH_ for 16-bit SRAM here.
4. The gate delay in the MWEH_ path is longer than in the RAMCS_ path, so a spurious write can occur in the RAM if it is fast enough to respond.

FIGURE 2.

Solutions to Mixed 8-Bit and 16-Bit Memory Connection Timing Issues

This issue applies only to the HFA3841. The HFA3842 will have direct support of 16-bit SRAM by providing upper and lower byte enable pins.

The best solution is to use all 16-bit memory in the system. In some applications, 16-bit Flash memory is not appropriate, though.

Another option is to use two 8-bit SRAMs for the memory.

If neither of these options is appropriate for the application, then a gate-delay based workaround described in the next figure may be considered.

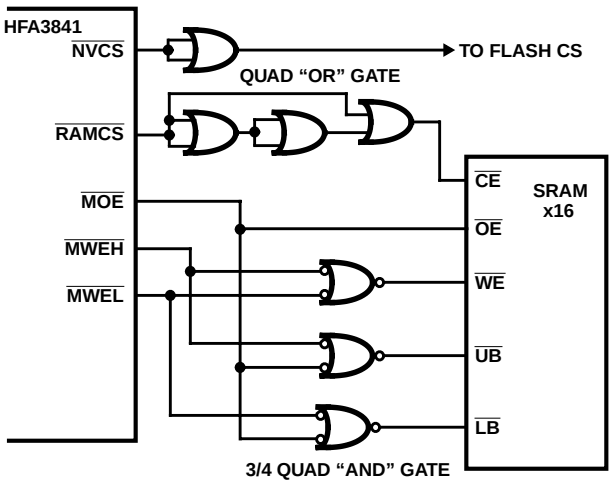


FIGURE 3.

This circuit generates two additional gate delays on the falling edge of the RAM enable. This ensures that the MWEH_ signal will have gone high before the RAM enable is asserted.

References

For Intersil documents available on the web, see http://www.intersil.com/
Intersil AnswerFAX (407) 724-7800.

[1] *AN9808 Application Note, "PRISM1-EVAL - 2.4GHz MACless DSSS Radio User's Guide",* Intersil Corporation, AnswerFAX #99808.

[2] *HFA3860B Data Sheet, "Direct Sequence Spread Spectrum Baseband Processor",* Intersil Corporation, AnswerFAX #4594.

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