LSI LOGIC

Full Duplex

HURRICANE™

84302

Quad 100/10 Mbps Ethernet Controller with RMON/SNMP Management Counters

99176

This document is an LSI Logic document. Any reference to SEEQ Technology should be considered LSI Logic.

Note: Check for latest Data Sheet revision before starting any designs.

SEEQ Data Sheets are now on the Web, access SEEQ Home Page www.seeq.com

- or -

LSI Logic at www.lsilogic.com

FEATURES

- ***Improved Version of SEEQ 84301 & 84C300***
- ***Four Independent MAC Channels***
- ***100/10 Mbps***
- ***Full RMON, SNMP, and Ethernet Management Counter Support Per Port***
- ***Flow Control for Full and Half Duplex***
  Full Duplex - IEEE 802.3x
  Half Duplex - Automatic JAM
- ***32-Bit , 50 MHz Interface To External Bus -1.6 Gbps Bandwidth***
- ***MII and 7-Wire Interface To External PHY***
- ***16-Bit Interface to Internal Registers and Management Counters***
- ***Management Interface (MI) to External PHY***
- ***Independent 128 Byte Receive & Transmit FIFO's per Port With Programmable Watermarks***
- ***Full and Half Duplex***
- ***Automatic CRC Generation and Checking***
- ***Retransmission of Packet upon Collision***
- ***Automatic Packet Error Discarding***
- ***Programmable Transmit Start Threshold***
- ***Interrupt Capability***
- ***Meets all IEEE 802.3 Specifications***
- ***256L PQFP***

DESCRIPTION

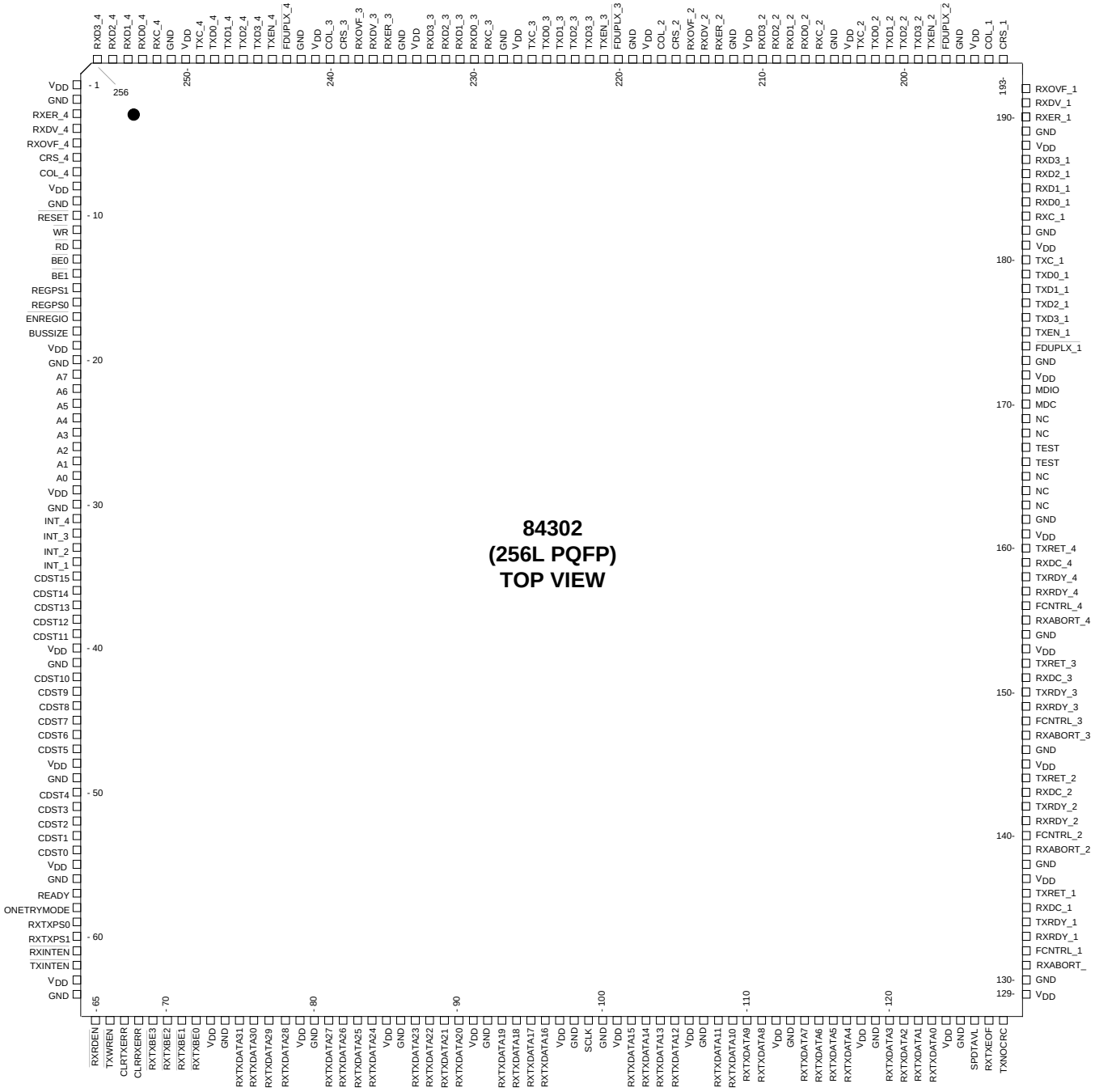
The 84302 is an Ethernet Media Access Controller (MAC) for 100 and 10 Mbps applications. The device integrates four independent channels on one IC.

The 84302 is an improved version of the SEEQ 84301 and 84C300 MAC's. Many new features have been added to improve performance and enhance ease of use.

The 84302 contains flow control for both full and half duplex operation. Full duplex flow control is implemented per IEEE 802.3x; half duplex flow control is collision based. For both cases, the flow control messages can be sent automatically without any host intervention.

The 84302 has a set of management counters that complies completely with the management objectives of the RMON Statistics Group, SNMP Interfaces group, IEEE 802.3 Ethernet, and Ethernet-Like MIB.

The 84302 is ideal as a Ethernet controller for Ethernet switch ports, uplinks, backbones, and other embedded applications.


84302
(256L PQFP)
TOP VIEW
1
256
65
70
80
90
100
110
120
129
130
140
150
160
170
180
190
193
200
210
220
230
240
250
RXD3_4
RXD2_4
RXD1_4
RXD0_4
RXC_4
GND
VDD
TXC_4
TXD0_4
TXD1_4
TXD2_4
TXD3_4
TXEN_4
FDUPLX_4
GND
VDD
COL_3
CRS_3
RXOVF_3
RXDV_3
RXER_3
GND
VDD
RXD3_3
RXD2_3
RXD1_3
RXD0_3
RXC_3
GND
VDD
TXC_3
TXD0_3
TXD1_3
TXD2_3
TXD3_3
TXEN_3
FDUPLX_3
GND
VDD
COL_2
CRS_2
RXOVF_2
RXDV_2
RXER_2
GND
VDD
RXD3_2
RXD2_2
RXD1_2
RXD0_2
RXC_2
GND
VDD
TXC_2
TXD0_2
TXD1_2
TXD2_2
TXD3_2
TXEN_2
FDUPLX_2
GND
VDD
COL_1
CRS_1
VDD
GND
RXER_4
RXDV_4
RXOVF_4
CRS_4
COL_4
VDD
GND
RESET
WR
RD
BE0
BE1
REGPS1
REGPS0
ENREGIO
BUSSIZE
VDD
GND
A7
A6
A5
A4
A3
A2
A1
A0
VDD
GND
INT_4
INT_3
INT_2
INT_1
CDST15
CDST14
CDST13
CDST12
CDST11
VDD
GND
CDST10
CDST9
CDST8
CDST7
CDST6
CDST5
VDD
GND
CDST4
CDST3
CDST2
CDST1
CDST0
VDD
GND
READY
ONETRYMODE
RXTXPS0
RXTXPS1
RXINTEN
TXINTEN
VDD
GND
RXRDEN
TXWREN
CLRTXERR
CLRRXERR
RXTXBE3
RXTXBE2
RXTXBE1
RXTXBE0
VDD
GND
RXTXDATA31
RXTXDATA30
RXTXDATA29
RXTXDATA28
VDD
GND
RXTXDATA27
RXTXDATA26
RXTXDATA25
RXTXDATA24
VDD
GND
RXTXDATA23
RXTXDATA22
RXTXDATA21
RXTXDATA20
VDD
GND
RXTXDATA19
RXTXDATA18
RXTXDATA17
RXTXDATA16
VDD
GND
SCLK
GND
VDD
RXTXDATA15
RXTXDATA14
RXTXDATA13
RXTXDATA12
VDD
GND
RXTXDATA11
RXTXDATA10
RXTXDATA9
RXTXDATA8
VDD
GND
RXTXDATA7
RXTXDATA6
RXTXDATA5
RXTXDATA4
VDD
GND
RXTXDATA3
RXTXDATA2
RXTXDATA1
RXTXDATA0
VDD
GND
SPDTAVL
RXTXEOF
TXNOCRC
RXOVF_1
RXDV_1
RXER_1
GND
VDD
RXD3_1
RXD2_1
RXD1_1
RXD0_1
RXC_1
GND
VDD
TXC_1
TXD0_1
TXD1_1
TXD2_1
TXD3_1
TXEN_1
FDUPLX_1
GND
VDD
MDIO
MDC
NC
NC
TEST
TEST
NC
NC
NC
GND
VDD
TXRET_4
RXDC_4
TXRDY_4
RXRDY_4
FCNTRL_4
RXABORT_4
GND
VDD
TXRET_3
RXDC_3
TXRDY_3
RXRDY_3
FCNTRL_3
RXABORT_3
GND
VDD
TXRET_2
RXDC_2
TXRDY_2
RXRDY_2
FCNTRL_2
RXABORT_2
GND
VDD
TXRET_1
RXDC_1
TXRDY_1
RXRDY_1
FCNTRL_1
RXABORT_
GND
VDD

1.0 Pin Description

Pin #	Pin Name	I/O	Description
System Interface			
61	RXINTEN	I	**Receive Interface Enable Input.** This active low input enables the System Interface for a receive operation and activates the output drivers on RXDC_[1:4] and RXRDY_[1:4]. This input is clocked in on rising edges of the system clock, SCLK.
62	TXINTEN	I	**Transmit Interface Enable Input.** This active low input enables the System Interface for a receive operation and activates the output drivers on TXRET_[1:4] and TXRDY_[1:4]. This input is clocked in on rising edges of the system clock, SCLK.
65	RXRDEN	I	**Receive Read Enable Input.** This input has to be asserted active low (along with RXINTEN) in order for data on RXTXDATA[31:0] to be read from the receive FIFO for the selected port. This input is clocked in on rising edges of the system clock, SCLK.
66	TXWREN	I	**Transmit Write Enable Input.** This input has to be asserted active low (along with TXINTEN) in order for data on RXTXDATA[31:0] to be written into the transmit FIFO for the selected port. This input is clocked in on rising edges of the system clock, SCLK.
99	SCLK	I	**System Interface Clock Input.** This input clocks data in and out of the receive and transmit FIFO's on RXTXDATA[31:0]. All System Interface inputs and outputs are also clocked in and out on rising edges of SCLK. The SCLK clock frequency must be between 25-50 Mhz.
60 59	RXTXPS1 RXTXPS0	I	**Port Select Input.** These inputs select which of the four ports will be accessed on the System Interface. 11 = Port 4 Accessed Over System Interface 10 = Port 3 Accessed Over System Interface 01 = Port 2 Accessed Over System Interface 00 = Port 1 Accessed Over System Interface
69 70 71 72	RXTXBE3 RXTXBE2 RXTXBE1 RXTXBE0	I/O	**Receive-Transmit Byte Enable Input/Output.** These bidirectional signals indicate which bytes of the current 32-bit data word on RXTXDATA[31:0] contain valid data. When the device is selected for a transmit FIFO write operation to a selected port, these pins are configured as inputs and indicate which bytes on RXTXDATA contain valid data. When the device is selected for a receive FIFO read operation from a selected port, these pins can be configured to be either inputs or outputs, depending on how they are programmed via an internal register bit. If they are configured as inputs, they dictate which bytes the data from the receive FIFO will be read out on. When configured as outputs, these pins indicated which bytes contain valid data. RXTXBE[3:0] is clocked in/out on rising edges of the system clock SCLK.
133 141 149 157	RXRDY_1 RXRDY_2 RXRDY_3 RXRDY_4	O	**Receive FIFO Ready Output.** These outputs, one per port, indicate that the RX FIFO data has either exceeded the programmable threshold value or an end of a packet was loaded into the RX FIFO. These outputs are clocked out on rising edges of the system clock, SCLK, and are put in high impedance state when RXINTEN is deasserted. 1 = RX FIFO Data ≥ RXFIFO Threshold Or End Of Frame Loaded Into RX FIFO 0 = Below Threshold

1.0 Pin Description (continued)

Pin #	Pin Name	I/O	Description
134 142 150 158	TXRDY_1 TXRDY_2 TXRDY_3 TXRDY_4	O	**Transmit FIFO Ready Output.** These outputs, one per port, indicate that the TX FIFO space exceeds the programmable threshold value. These outputs are clocked out on rising edges of the system clock, SCLK, and are put in high impedance state when TXINTEN is deasserted. 1 = TX FIFO Space ≥ TX FIFO Threshold 0 = Below Threshold
126	SPDTAVL	O	**FIFO Space/Data Available Output.** For RX FIFO Reads: 1 = More than 1 Double Word of Data in RX FIFO 0 = Data Not Available For TX FIFO Writes: 1 = More than 2 Double Words of TX FIFO Space Available 0 = Space Not Available This output is clocked out on rising edges of the system clock, SCLK, and is for the selected port.
192 215 238 5	RXOVF_1 RXOVF_2 RXOVF_3 RXOVF_4	O	**Receive FIFO Overflow Output.** 1 = RX FIFO Full 0 = Not Full These outputs, one per port, are clocked out on rising edges of the system clock, SCLK .
127	RXTXEOF	I/O	**Receive-Transmit End of Frame Input/Output.** This bidirectional pin indicates that the current data word, for the selected port, is the last double word of the packet. During receive FIFO reads, this pin is an output and is asserted active high when the last word of a receive packet is being read out of the receive FIFO on RXTXDATA[31:0]. During transmit writes, this pin is an input and needs to be asserted active high when the last word of the packet is being written into the transmit FIFO on RXTXDATA[31:0]. This signal is clocked in/out on rising edges of the system clock, SCLK.
128	TXNOCRC	I	**Transmit No CRC Input.** 1 = CRC is not Appended 0 = CRC is Calculated and Appended to Current Transmit Packet being Input on System Interface This input is clocked in on rising edges of the system clock, SCLK, and is for the selected port.

1.0 Pin Description (continued)

Pin #	Pin Name	I/O	Description
75 76 77 78 81 82 83 84 87 88 89 90 93 94 95 96 102 103 104 105 108 109 110 111 114 115 116 117 120 121 122 123	RXTXDATA[31:0]	I/O	**Receive-Transmit Data Input/Output.** This bidirectional bus contains data read or written to/from the FIFO's for the selected port. During receive reads, these pins are outputs and contain data read from the receive FIFO. During transmit reads, these pins are inputs and contain data to be written to the transmit FIFO. RXTXDATA[31:0] is clocked in/out on rising edges of the system clock, SCLK. **Note:** Pin #75 = RXTXDATA 31, Pin #123 = RXTXDATA 0
131 139 147 155	RXABORT_1 RXABORT_2 RXABORT_3 RXABORT_4	I	**Receive Abort Input.** 1 = Abort Packet, Discard RX FIFO Data, Block RX FIFO Input Until Start of Next Packet. 0 = No Discard These inputs, one per port, are clocked in on rising edges of the system clock, SCLK.
135 143 151 159	RXDC_1 RXDC_2 RXDC_3 RXDC_4	O	**Receive Discard Output.** 1 = RX FIFO Data Discarded Due to Receive Error 0 = No Discard RXDC_[1:4], one per port, are clocked out on rising edges of the system clock, SCLK, and are placed in high impedance state when $\overline{\text{RXINTEN}}$ is deasserted. RXDC_[1:4] are latched high until cleared with the CLRRXERR pin. As long as RXDC_[1:4] is latched high, no new packets will be loaded into the receive FIFO.
136 144 152 160	TXRET_1 TXRET_2 TXRET_3 TXRET_4	O	**Transmit Retry Output.** 1 = TX FIFO Data Discarded Due to Transmit Error 0 = No Discard TXRET_[1:4], one per port, are clocked out on rising edges of the system clock, SCLK, and are placed in high impedance state when $\overline{\text{TXINTEN}}$ is deasserted. TXRET_[1:4] are latched high until it is cleared with the CLRTXERR pin. As long as TXRET_[1:4] are latched high, no new packets can be transmitted out of the transmit FIFO.
68	CLRRXERR	I	**Clear Receive Error Input.** 1 = RXDC_[1:4] Pin for Selected Port is Cleared Low 0 = Not Cleared This input is clocked in on rising edges of the system clock, SCLK .

1.0 Pin Description (continued)

Pin #	Pin Name	I/O	Description
67	CLRTXERR	I	**Clear Transmit Error Input.** 1 = TXRET_[1:4] Pin for Selected Port is Cleared Low 0 = Not Cleared This input is clocked in on rising edges of the system clock, SCLK .
132 140 148 156	FCNTRL_1 FCNTRL_2 FCNTRL_3 FCNTRL_4	I	**Flow Control Input.** In Half Duplex Mode: 1 = JAM Packet Transmitted When Receive Data Detected. 0 = Normal Operation In Full Duplex Mode: 1 = MAC Control Pause Frames Transmitted When Receive Data Detected. 0 = Normal Operation These inputs, one per port, are clocked in on rising edges of the system clock, SCLK .
PHY Interface (MII and 10 Mbps Serial)			
180 203 226 249	TXC_1 TXC_2 TXC_3 TXC_4	I	**Transmit Clock Input.** These inputs, one per port, clock out the transmit data on TXD[3:0]_[1:4] and TXEN_[1:4] to an external Physical Layer device on rising edges of this clock in MII mode, and on falling edges of the clock in 10 Mbps Serial mode.
175 198 221 244	TXEN_1 TXEN_2 TXEN_3 TXEN_4	O	**Transmit Enable Output.** These outputs, one per port, are asserted active high to indicate that data on TXD[3:0] for that port is valid. These outputs are clocked out on rising edges of TXC_[1:4] in MII mode and falling edges in 10 Mbps Serial Mode.
176 177 178 179 199 200 201 202 222 223 224 225 245 246 247 248	TXD[3:0]_1 TXD[3:0]_2 TXD[3:0]_3 TXD[3:0]_4	O	**Transmit Data Output.** These outputs, one per port, contain nibble wide transmit data to an external Physical Layer device and are clocked in on rising edges of TXC_[1:4] in MII Mode. In 10 Mbps Serial mode, only TXD0 is used and data is clocked in on falling edges of TXC_[1:4].
183 206 229 252	RXC_1 RXC_2 RXC_3 RXC_4	I	**Receive Clock Input.** These inputs, one per port, clock in receive data on RXD[3:0]_[1:4], RXDV_[1:4], and RXER_[1:4] from an external Physical Layer device on rising edges of this clock.
193 216 239 6	CRS_1 CRS_2 CRS_3 CRS_4	I	**Receive Carrier Sense Input.** These inputs, one per port, have to be asserted active high to indicate that receive data has been detected on the Physical Layer device for that port.
191 214 237 4	RXDV_1 RXDV_2 RXDV_3 RXDV_4	I	**Receive Data Valid Port 1 Input.** These inputs, one per port, have to be asserted active high on rising edges of RXC_[1:4] to indicate when receive data is valid on RXD[3:0]_[1:4]. This pin is not used in 10 Mbps Serial mode.

1.0 Pin Description (continued)

Pin #	Pin Name	I/O	Description
187 186 185 184 210 209 208 207 233 232 231 230 256 255 254 253	RXD[3:0]_1 RXD[3:0]_2 RXD[3:0]_3 RXD[3:0]_4	I	**Receive Data Port 1 Input.** These inputs, one per port, contain receive nibble wide receive data from an external Physical Layer device and are clocked in on rising edges of RXC_[1:4] in MII mode. In 10 Mbps Serial Mode, only RXD0 is used and data is clocked out on falling edges of RXC_[1:4].
190 213 236 3	RXER_1 RXER_2 RXER_3 RXER_4	I	**Receive Data Error Input.** These inputs, one per port, indicate that an external Physical Layer device has detected a symbol error. This input is clocked in on rising edges of RXC_[1:4]. This pin is not used in 10 Mbps Serial mode.
194 217 240 7	COL_1 COL_2 COL_3 COL_4	I	**Collision Input.** These inputs, one per port, indicate that an external Physical Layer device has detected a collision between transmit and receive data.
Management Interface (MI)			
170	MDC	O	**Management Interface (MI) Clock Output.** This MI clock shifts serial data in and out of MDIO on rising edges from an external Physical Layer device.
171	MDIO	I/O	**Management Interface (MI) Data I/O.** This bidirectional pin contains serial data that is clocked in and out on rising edges of the MDC clock from an external Physical Layer device.
Register Interface			
17	$\overline{\text{ENREGIO}}$	I	**Enable Register I/O Operation Input.** This input must be asserted active low to enable reading and writing of data on the Register Interface input and output signals. This input is clocked in on falling edges of $\overline{\text{WR}}$ and $\overline{\text{RD}}$.
11	$\overline{\text{WR}}$	I	**Write Strobe Input.** This input is a write enable input signal which has to be asserted active low in order for data to be written into the addressed register for a given port.
12	$\overline{\text{RD}}$	I	**Read Strobe Input.** This input is a read enable input signal which has to be asserted active low in order for data to be read from the addressed register for a given port. This input must remain asserted until data is outputted onto CDST[15:0] or until the READY output is asserted.
15 16	REGPS1 REGPS0	I	**Register Port Select Input.** These inputs determine which port's registers are being accessed over the Register Interface. These inputs are clocked in on falling edges of $\overline{\text{WR}}$ and $\overline{\text{RD}}$. 11 = Port 4 Accessed Over Register Interface 10 = Port 3 Accessed Over Register Interface 01 = Port 2 Accessed Over Register Interface 00 = Port 1 Accessed Over Register Interface
21 22 23 24 25 26 27 28	A[7:0]	I	**Register Select Address Input.** These inputs provide the address for the specific internal register to be accessed for a selected port. These inputs are clocked in on falling edges of $\overline{\text{WR}}$ and $\overline{\text{RD}}$. **Note:** Pin #21 = A7, Pin # 28 = A0

1.0 Pin Description (continued)

Pin #	Pin Name	I/O	Description
18	BUSSIZE	I	**Register Interface Bus Size Select.** 1 = Register Interface Bus is 16-Bits Wide (CDST[15:0]) 0 = Register Interface Bus is 8-Bits Wide (CDST[7:0])
14 13	$\overline{BE1}$ $\overline{BE0}$	I	**Register Byte Enable Inputs.** These inputs determine which bytes of the current 16-bit word on CDST[15:0] contain valid data. These inputs are clocked in on falling edges of $\overline{WR}$ and $\overline{RD}$. 11 = No Valid Data 10 = Valid data on CDST[7:0] 01 = Valid data on CDST[15:8] 00 = Valid data on CDST[15:0]
35 36 37 38 39 42 43 44 45 46 47 50 51 52 53 54	CDST[15:0]	I/O	**Register Data Input.** These bidirectional bus is the 16-bit data path to and from the internal registers for a selected port. Data is read/written from/to the internal registers on falling edges of $\overline{WR}$ and $\overline{RD}$. These pins are high impedance until their output drivers are enabled by $\overline{RD}$ and $\overline{ENREGIO}$ being asserted low. **Note:** Pin #35 = CDST 15, Pin #54 = CDST 0
57	READY	O	**Register Ready Indication Output.** This active high output indicates that data being read out on CDST[15:0] is valid. READY goes active high after $\overline{RD}$ has been asserted, and will stay high until $\overline{RD}$ is deasserted. READY goes into High Impedance State when $\overline{ENREGIO}$ is deasserted.
34 33 32 31	INT_1 INT_2 INT_3 INT_4	O	**Interrupt Output.** These outputs, one per port, are asserted active high when certain interrupt bits are asserted. These pins remain latched high until all interrupt bits causing the interrupt condition are read.
Miscellaneous			
174 197 220 243	$\overline{FDUPLX\_1}$ $\overline{FDUPLX\_2}$ $\overline{FDUPLX\_3}$ $\overline{FDUPLX\_4}$	I	**Full Duplex Mode Input.** 1 = Half Duplex 0 = Full Duplex Full Duplex mode can also be selected by setting the Full Duplex bit in the Configuration 2 register. Half Duplex mode is selected when both this pin and the Full Duplex mode bit are set to Half Duplex.
58	ONETRYMODE	I Pull down	**One Try Transmit Mode Input.** 1 = No transmission retry attempted after a collision 0 = Normal
10	$\overline{RESET}$	I	**Hardware Reset Input.** 1 = Normal 0 = Device Reset, FIFO's Cleared, Counters Cleared, Register Bits Set to Defaults.

1.0 Pin Description (continued)

Pin #	Pin Name	I/O	Description
166 167	TEST	I	**Factory Test Mode.** These pins are reserved for factory test modes and must be tied low for proper operation.
163 164 165 168 169	NC	—	**No Connect.** These pins are should be left floating.
Power Supplies			
1 8 19 29 40 48 55 63 73 79 85 91 97 101 106 112 118 124 129 137 145 153 161 172 181 188 195 204 211 218 227 234 241 250	VDD	—	**Positive Supply.** +5v +/-5% Volts.
2 9 20 30 41 49 56 64 74 80 86 92 98 100 107 113 119 125 130 138 146 154 162 173 182 189 196 205 212 219 228 235 242 251	GND	—	**Ground.** 0 Volts.

2.0 Block Diagram

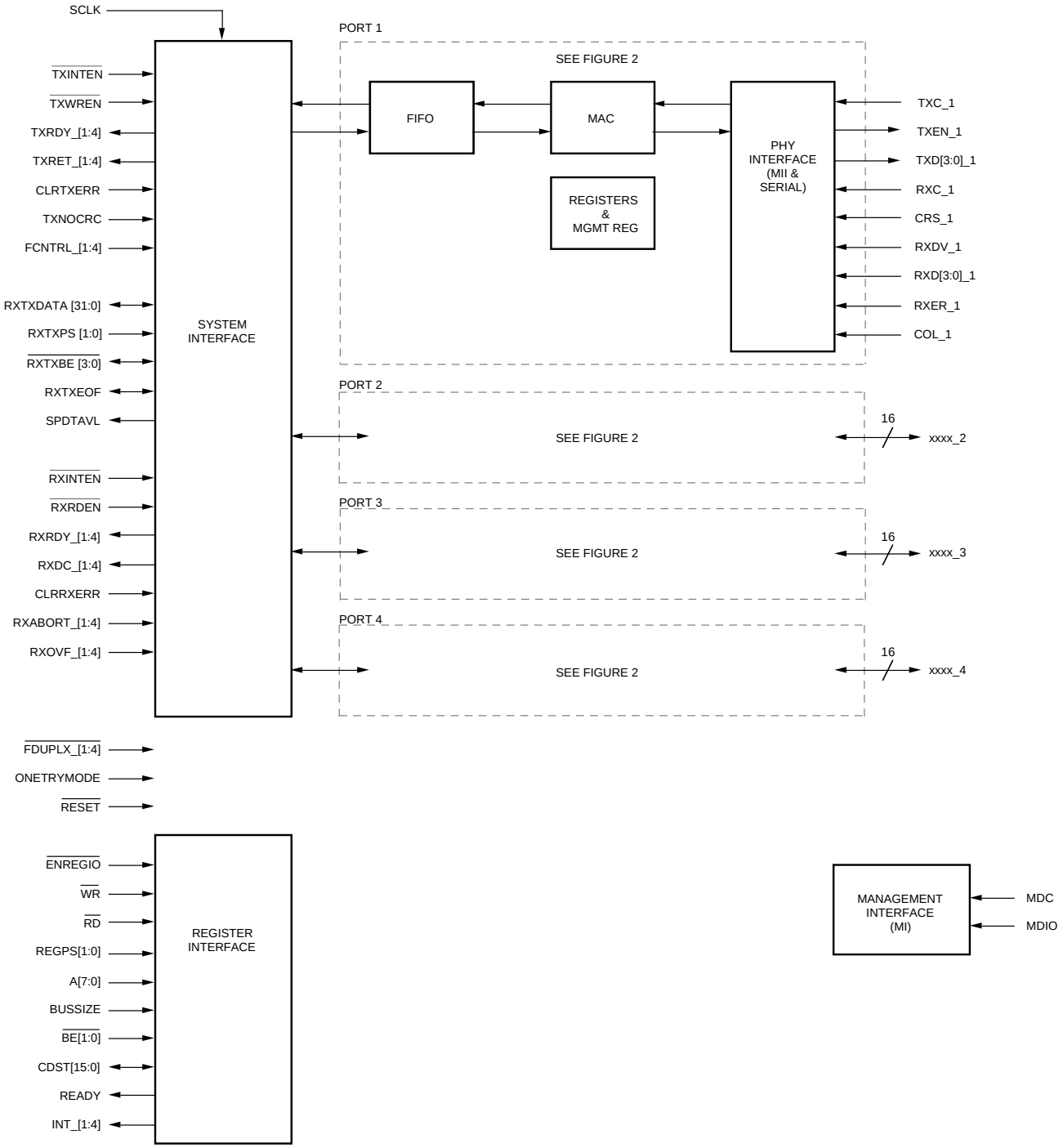


Figure 1. 84302 Top Level Block Diagrtam

2.0 Block Diagram

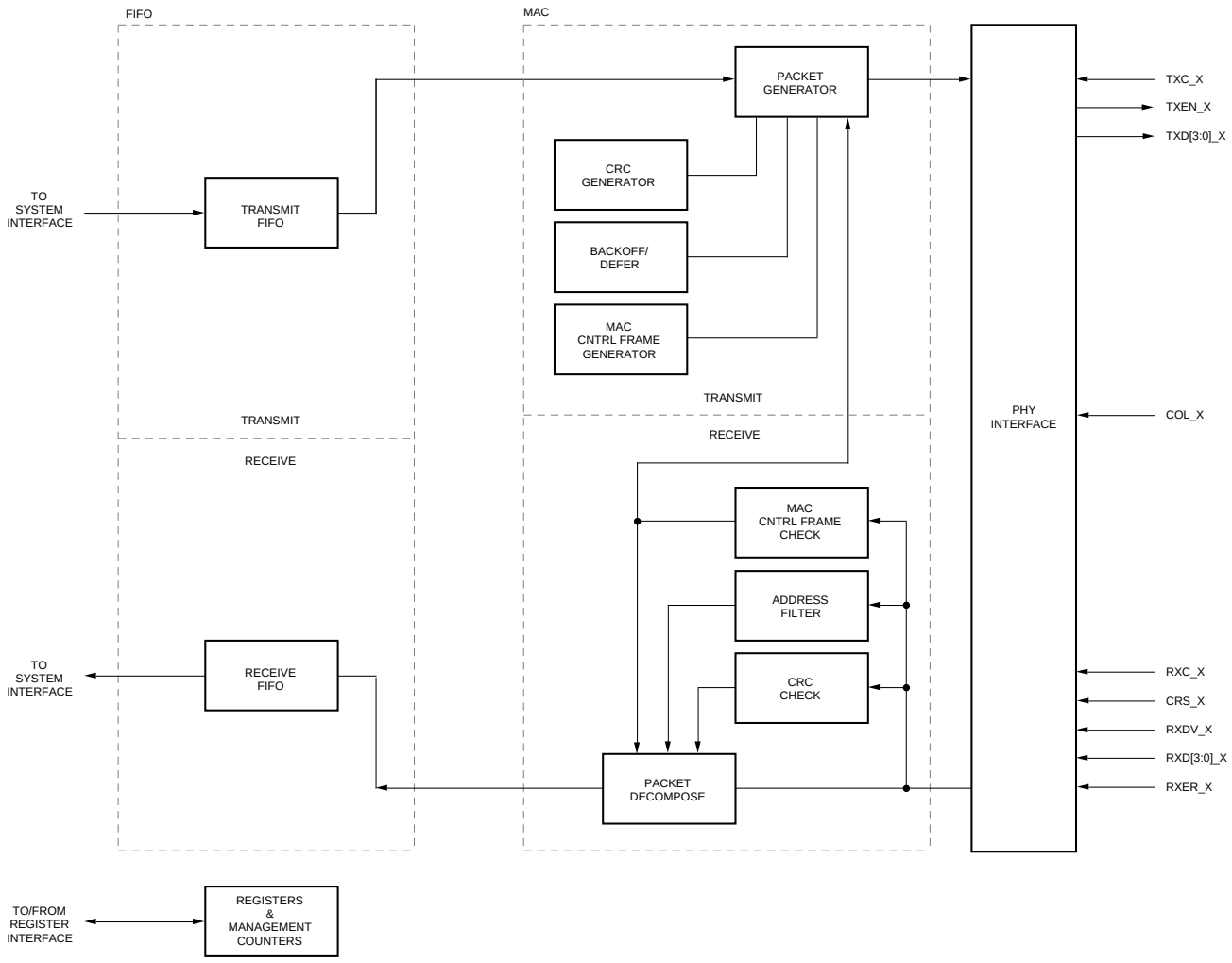


Figure 2. 84302 Individual Port Block Diagram

FUNCTIONAL DESCRIPTION

GENERAL

The 84302 is a quad Ethernet Controller for 100/10 Mbps Ethernet systems. The 84302 integrates four independent MAC (Media Access Control) sublayers, as defined in IEEE 802.3. The 84302 has seven main sections: System Interface, MAC, FIFO's, PHY Interface, Management Interface, Register Interface, and Registers. Each of the sections is replicated four times, once per port, with the exception of the four interfaces (System, Register, PHY, and Management), which are common to all four ports. A top level block diagram is shown in Figure 1, and a block diagram of each individual port is shown in Figure 2.

For each port, The 84302 has a transmit data path and a receive data path. The transmit data path goes in the System Interface and out the PHY Interface, as shown in the top half of Figure 2. The receive data path goes in the PHY Interface and out the System Interface, as shown in the bottom half of Figure 2.

On the transmit data path, data for all four ports is input into the System Interface from an external bus. One port has to be selected, and the data is then sent to the transmit FIFO of the selected port. The transmit FIFO provides temporary storage of the data until it is sent to the transmit MAC section for that port. The transmit MAC takes the data and formats it into an Ethernet packet per IEEE 802.3 specifications and shown in Figure 3. The Ethernet packet then goes to the PHY Interface for formatting and transmission to an external PHY chip. There are two PHY Interface modes on the 84302: MII and 10 Mbps Serial. The formatting of the data on the PHY Interface is done according to IEEE 802.3 specifications and is also shown in Figure 4. The transmit side manages collisions via the internal backoff and defer algorithms and also generates MAC Control Pause frames.

On the receive data path, the PHY Interface receives incoming data from an external PHY chip for each port. The incoming data must be in either MII or 10 Mbps Serial format as specified in IEEE 802.3 and shown in Figure 4. The PHY Interface converts the data from MII/10 Mbps Serial format to Ethernet packet data. The Ethernet packet data is then sent to the receive MAC section for that port. The receive MAC section decomposes the packet, checks the validity of the packet against certain error criteria and address filters, and checks for MAC Control frames. The receive MAC then sends valid packets to the receive FIFO for that port. The receive FIFO provides temporary storage of data until it is demanded by the System Interface. The receive FIFO's for all four ports can be individually selected and accessed by the System Interface. The System Interface outputs the data for the selected port to an external bus.

The Register Interface is a separate bidirectional 16-bit data bus through which configuration inputs can be set and status outputs can be read from the internal registers and management counters. The internal register bank is replicated four times, once per port.

The Management Interface, referred to as the MI, is serial interface for passing data to/from and external PHY.

Each block plus the operating modes are described in more detail in the following sections.

ETHERNET FRAME FORMAT

General

Information in an Ethernet network is transmitted and received in packets or frames. The basic function of the 84302 is to process Ethernet frames. An Ethernet frame is defined in IEEE 802.3 and consists of a preamble, start of frame delimiter (SFD), destination address (DA), source address (SA) , length/type field (L/T), data, frame check sequence (FCS), and interpacket gap (IPG). The format for the Ethernet frame is shown in Figure 3.

An Ethernet frame is specified by IEEE 802.3 to have a minimum length of 64 bytes and a maximum length of 1518 bytes, exclusive of the preamble and SFD. Packets which are less than 64 bytes or greater than 1518 bytes are referred to as undersize and oversize packets, respectively.

Preamble & SFD

The preamble & SFD is a combined 64-bit field consisting of 62 alternating 1's and 0's followed by a 11 end of preamble indicator. The first 56-bits of 1's and 0's are considered to be the preamble, and the last 8-bits of 10101011 are considered to be the SFD (Start of Frame Delimiter).

Destination Address

The destination address is a 48-bit field containing the address of the station(s) to which the frame is directed. The format of the address field is the same as defined in IEEE 802.3 and shown in Figure 3b. The destination address can be either a unicast address to a specific station, a multicast address to a group of stations, or a broadcast address to all stations. The first and second bits determine whether an address is unicast, multicast or broadcast, and the remaining 46-bits are the actual address bits, as shown in Figure 3b.

Source Address

The source address is a 48-bit field containing the specific station address from which the frame originated. The format of the address field is the same as defined in IEEE 802.3 and shown in Figure 3b.

Length/Type Field

The 16-bit length/type field takes on the meaning of either packet length or packet type, depending on its numeric value, as described in Table 1.

Table 1. Length/Type Field Definition

Length/Type Field Value (Decimal)	Length or Type	Definition
0-1500	Length	Total Number of Bytes In Data Field Minus any Padding.
1501-1517	Neither	Undefined
>=1518	Type	Frame Type

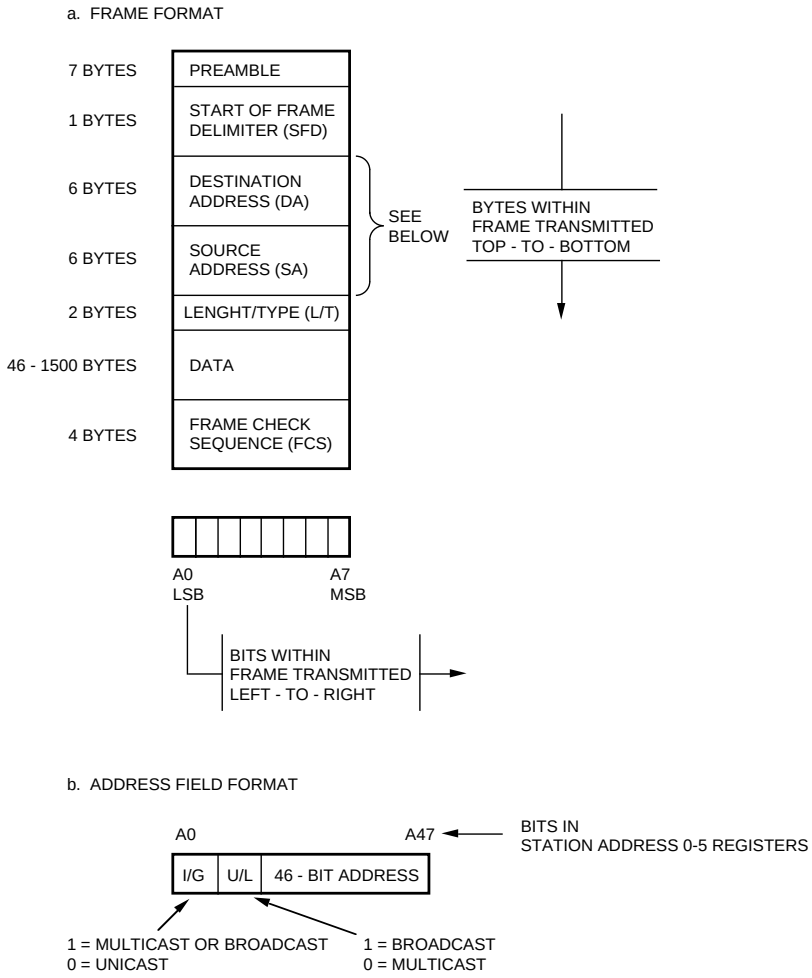


Figure 3. Ethernet MAC Frame Format

Data

The data is a 46-1500 byte field containing the actual data to be transmitted between two stations. If the actual data is less than 46 bytes, extra 0's are added to increase the data field to the 46 byte minimum. Adding these extra 0's is referred to as padding.

Frame Check Sequence

The frame check sequence (FCS), is a 32-bit cyclic redundancy check (CRC) value computed on the entire frame, exclusive of preamble & SFD. The FCS algorithm is defined in IEEE 802.3. The FCS is appended to the end of the frame and is used to determine frame validity.

Interpacket Gap

The interpacket gap (IPG) is the time interval between packets. The minimum IPG value is defined to be 96 bits, where 1 bit=10ns for 100 Mbps Ethernet & 1 bit=100nS for 10 Mbps Ethernet. There is no maximum IPG limit.

SYSTEM INTERFACE

General

The System Interface is a 32-bit wide bidirectional parallel data interface. Data to/from any of the four independent ports is input and output through the System Interface.

The System Interface consists of 64 signals: 32 bidirectional data I/O (RXTXDATA[31:0]), four bidirectional byte enable I/O (RXTXBE[3:0]), one receive and one transmit enable input (RXINTEN and TXINTEN), one receive read enable and one transmit write enable input (RXRDEN and TXWREN), two port select inputs (RXTXPS[1:0]), one bidirectional end of frame I/O (RXTXEOF), one transmit and one receive FIFO watermark output (RXRDY and TXRDY), one transmit and one receive discard output (RXDC and TXRET), one receive and one transmit discard clear input (CLR_RXERR and CLRTXERR), one transmit CRC enable input (TXNOCRC), four flow control inputs (FCNTRL_[1:4], one per port), one FIFO space/data available output (SPDTAVL), four receive FIFO overflow indication outputs (RXOVF_[1:4], one per port), and four receive FIFO abort inputs (RXABORT_[1:4], one per port). All data is clocked in/out on rising edges of the system clock, SCLK. SCLK can operate between 25-50 MHZ.

Data Format and Bit Order

The format of the data word on RXTXDATA[31:0] and its relationship to the MAC frame format and PHY Interface format is shown in Figure 4. Note that the device can be programmed to append an additional 32-bit status word to the end of the receive packet; refer to the Receive Status Word section for more details on this status word.

Byte Order

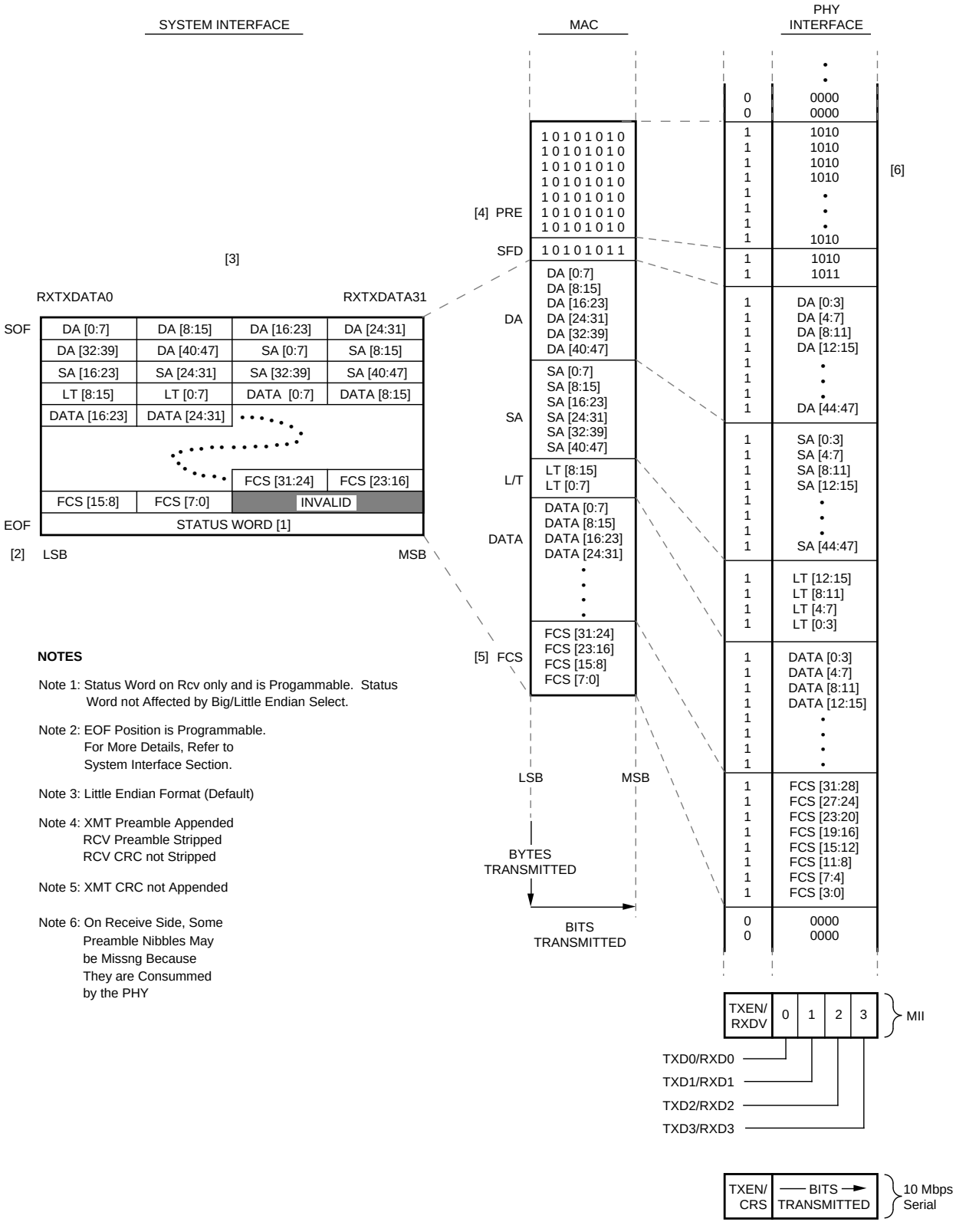
The byte ordering of the RXTXDATA data bits is programmable by appropriately setting the endian select bit in the Configuration 2 register. The byte order shown in Figure 4 is the little endian format (default). If big endian format is selected, then the byte order shown in Figure 4 is reversed, that is, DA[0:7] occurs on pins RXTXDATA[24:31], DA[24:31] occurs on pins RXTXDATAD[0:7], etc. This difference between little endian and big endian format is illustrated in Figure 5. Note that the byte order of the Status word appended to Receive Packets is not affected by Big/Little Endian Selection

Transmit Write Operation

All receive and transmit data is clocked in/out on rising edges of the system clock, SCLK. The SCLK input needs to be continuously input to the device at a frequency between 25-50 MHz.

The System Interface is bidirectional. When it is configured for a transmit write operation, data is input into the device and stored in the transmit FIFO. A transmit write operation is initiated by asserting TXINTEN and TXWREN. TXINTEN acts as a general transmit enable input, and asserting TXINTEN also activates the output drivers for the TXRDY and TXRET pins and removes them from high impedance state. Coincident or after TXINTEN is asserted, TXWREN has to be asserted to actually start the write operation. If TXWREN is then asserted while TXINTEN is asserted, the data word on the RXTXDATA[31:0] I/O pins is clocked into the transmit FIFO on each rising edge of the SCLK clock for the port selected by the RXTXPS[1:0] inputs. TXINTEN and TXWREN can be continuously asserted and deasserted as many times as desired while a packet is being written into the device. The last word of the packet must be indicated to the device by asserting RXTXEOF on the same SCLK rising edge that clocks in the last word of the packet. TXWREN does not need to be deasserted between the end of one packet and the start of the next. RXTXDATA[31:0] input data is 32-bit wide packet data whose format and relationship to the MAC packet and PHY Interface is described in Figure 4.

The byte enable pins, RXTXBE[3:0], are used for both transmit and receive operation, and they determine which bytes of the 32-bit RXTXDATA[31:0] data word contain valid data. RXTXBE[3:0] are inputs during a transmit write operation, and are clocked in on rising edges of SCLK along with each RXTXDATA[31:0] data word. The correspondence between the byte enable inputs and the valid bytes of each data word on RXTXDATA[31:0] is defined in Table 2. Any logic combination of RXTXBE[3:0] inputs is allowed, with the one exception that RXTXBE[3:0] must not be 1111.



NOTES

Note 1: Status Word on Rcv only and is Progammable. Status Word not Affected by Big/Little Endian Select.

Note 2: EOF Position is Programmable. For More Details, Refer to System Interface Section.

Note 3: Little Endian Format (Default)

Note 4: XMT Preamble Appended
RCV Preamble Stripped
RCV CRC not Stripped

Note 5: XMT CRC not Appended

Note 6: On Receive Side, Some Preamble Nibbles May be Missng Because They are Consummed by the PHY

Figure 4. Frame Formats and Bit Ordering

Table 2. Byte Enable Pin vs. Valid Byte Position

$\overline{\text{RXTXBE[3:0]}}$ Pins	Valid Byte Position on RXTXDATA[31:0]
$\overline{\text{RXTXBE3}}$	RXTXDATA[31:24]
$\overline{\text{RXTXBE2}}$	RXTXDATA[23:16]
$\overline{\text{RXTXBE1}}$	RXTXDATA[15:8]
$\overline{\text{RXTXBE0}}$	RXTXDATA[7:0]

The end of frame I/O pin, RXTXEOF, indicates which data word is the last word of the Ethernet data packet. RXTXEOF is configured to be an input during a write operation. RXTXEOF is input on the same SCLK rising edge as the first and last word of the data packet.

There are four transmit FIFO ready outputs, one per port, on the TXRDY_[1:4] pins. The transmit FIFO ready output is a transmit FIFO watermark signal which indicates when the transmit FIFO space has exceeded the programmable transmit FIFO threshold value. TXRDY_[1:4] will be asserted or deasserted by the device on rising edges of SCLK, depending on the fullness of the transmit FIFO. Refer to the transmit FIFO section for more details on TXRDY_[1:4].

In addition to the TXRDY output, there is also a FIFO space/data available output indication on the SPDTAVL pin. During a write operation, the SPDTAVL output is a space available (almost full) indication for the transmit FIFO and it is asserted active high if there is more than 2 double words of space available in the transmit FIFO.

TXRET_[1:4] is a transmit packet discard output, one per port. TXRET_[1:4] is asserted when an error was detected on a transmit packet. When a transmit error is detected on a packet, the remaining contents of the packet is flushed from the TX FIFO and TXRET_[1:4] is latched active high to indicate that the error occurred. TXRET_[1:4] for the selected port can be cleared by asserting the clearing signal, CLRTXERR. While TXRET_[1:4] is latched high, the TX FIFO input is blocked and no data can be loaded into it until it is cleared with CLRTXERR. See the Packet Discard section for more details on discards and TXRET_[1:4].

TXNOCRC is an input which can disable the internal generation and appending of the 4 byte CRC value onto the end of the data packet. TXNOCRC is sampled on rising edges of SCLK and can be asserted on any SCLK cycle between the first and last double word of a packet to cause the removal or addition of the CRC to that packet. CRC generation can also be disabled by setting the transmit CRC disable bit in the Configuration 1 register. The interaction between the TXNOCRC pin and CRC disable bit is defined in Table 3.

FCNTRL_[1:4] is an input, one per port, which will cause the automatic generation and transmission of a MAC Control Pause frame in Full Duplex mode and JAM packet in Half Duplex mode. FCNTRL_[1:4] is input on rising edges of SCLK. See the Flow Control, Auotmatic JAM, and MAC Control Frame sections for more details about these features.

Receive Read Operation

All receive and transmit data is clocked in/out on rising edges of the system clock, SCLK. The SCLK input needs

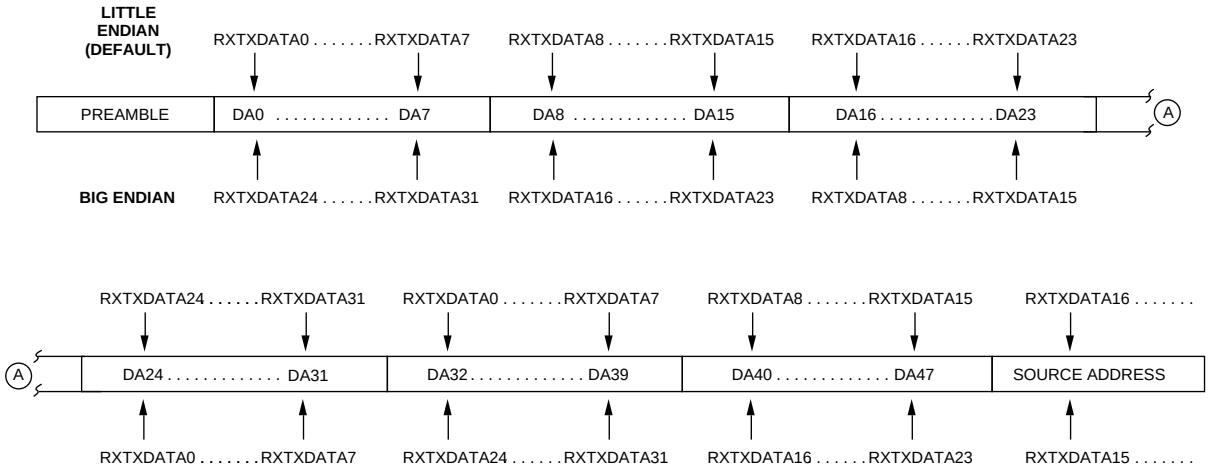


Figure 5. Little Endian vs. Big Endian Format

to be continuously input to the device at a frequency between 25-50 MHz.

The System Interface is bidirectional. When it is configured for a receive read operation, data that is stored in the receive FIFO is output to the System Interface. A receive read operation is initiated by asserting RXINTEN and RXRDEN. RXINTEN acts as a general receive enable input, and asserting RXINTEN also activates the output drivers for the RXRDY and RXDC pins and removes them from high impedance state. Coincident or after RXINTEN is asserted, RXRDEN has to be asserted to actually start the read operation. If RXRDEN is then asserted while RXINTEN is asserted, the oldest data word in the receive FIFO is clocked out onto the RXTXDATA[31:0] I/O pins on each rising edge of the SCLK clock for the port selected by the RXTXPS[1:0] inputs. RXINTEN and RXRDEN can be continuously asserted and deasserted as many times as desired while a packet is being written into the device. The last word of the packet is indicated by the assertion of RXTXEOF on the same SCLK rising edge that clocks out the last word of the packet. Once the entire packet has been clocked out, then no more data is clocked out on RXTXDATA[31:0] for 8 SCLK cycles, thus allowing extra dribble SCLK clock cycles to occur after the end of packet, up to a maximum of 8 SCLK's. After 8 extra dribble SCLKs without a RXRDEN deassertion, the next packet will be read out of the receive FIFO. If there is no packet in FIFO after 8 extra dribble SCLKs, then invalid data will be read out. RXTXDATA[31:0] input data is 32- bit wide packet data whose format and relationship to the MAC packet and PHY Interface is described in Figure 4.

The byte enable pins, RXTXBE[3:0], are used for both transmit and receive operation, and they determine which bytes of the 32-bit RXTXDATA[31:0] data word contain valid data. RXTXBE[3:0] can be configured to be either inputs or outputs during a receive read operation by appropriately setting the byte enable direction bit in the Configuration 3 register. When they are configured as outputs, RXTXBE[3:0] are clocked out on rising edges of SCLK along with each data word and indicate which bytes of the 32-bit RXTXDATA[31:0] data word contain valid data. Note that RXTXBE[3:0]=0000 for all words of the packet except the last word; the last word of the packet may end on any one of the four byte boundaries of the 32-bit data word. When they are configured as inputs, RXTXBE[3:0] are clocked in on rising edges of SCLK along with each RXTXDATA[31:0] data word and indicate to the device which bytes contain the actual data. The correspondence between the byte enable inputs and the valid bytes of each data word on RXTXDATA[31:0] is defined in Table 2. Any logic combination of RXTXBE[3:0] inputs is allowed, with the one exception that RXTXBE[3:0] must not be 1111.

The end of frame I/O pin, RXTXEOF, indicates which data word is the last word of the Ethernet data packet. RXTXEOF is configured to be an output during a receive read operation, and is output on the rising edges of SCLK. The position of RXTXEOF during System Interface read operations can be programmed to occur either (1) when the receive status word is read out, or (2) when both the last data word of packet and the receive status word are read out. This selection of either a single RXTXEOF at status word or a double RXTXEOF at end of data and status word is accomplished by appropriately setting the receive EOF position select bit in the Configuration 2 register. The selection of the EOF position is also affected by the setting of the status word disable bit in Configuration 3 register. The EOF position as a function of both the EOF position bit and status word disable bit is shown in Table 2a. More details about the status word can be found in the Receive Status Word section.

Table 2a. RXTXEOF Position

PEOF (Bit 2, Cfg Reg.2)	**SWRD_DIS** (Bit 1, Cfg Reg.3)	**RXTXEOF Position**
0	0	Status Word
0	1	Data
1	0	Data & Status Word
1	1	Data

There are four receive FIFO ready outputs, one per port, on the RXRDY_[1:4] pins. The receive FIFO ready output is a receive FIFO watermark signal which indicates when the receive FIFO data has exceeded the programmable receive FIFO threshold value. RXRDY_[1:4] will be asserted or deasserted by the device on rising edges of SCLK, depending on the fullness of the receive FIFO. Refer to the receive FIFO section for more details on RXRDY_[1:4].

In addition to the RXRDY output, there is also a FIFO space/data available output indication on the SPDTAVL pin. During a read operation, the SPDTAVL output is a data available (almost empty) indication for the receive FIFO and it is asserted active high if there is more than 1 double words of data present in the receive FIFO.

RXDC_[1:4] is a receive packet discard output, one per port. RXDC_[1:4] is asserted when an error was detected for a receive packet. When a receive error is detected on a packet, the remaining contents of the RX FIFO are flushed and RXDC_[1:4] is latched active high to indicate the error condition. RXDC_[1:4] for the selected port can be cleared by asserting the clearing signal, CLRRXERR. While RXDC_[1:4] is latched high, the RX FIFO input is

blocked and no data can be loaded into it until it is cleared with CLRRXERR and the start of a new packet is detected. See the Packet Discard section for more details on discards and RXDC_[1:4].

The RXABORT input, when asserted, will discard the contents of the receive FIFO, and halt the reception of any more data into the receive FIFO until the start of the next packet is detected. Refer to the Packet Discard section for more information about discarded packets. The device can be programmed to disable and ignore the RXABORT pin by setting the RXABORT pin disable bit in the Configuration 2 register.

A status word can be appended to the end of the receive packet, if desired. Refer to the Receive Status Word section for more details on the status word. The status word is always output on the next full 32-bit word boundary after the data packet has ended, as shown in Figure 4.

TRANSMIT MAC

General

The transmit MAC (Media Access Control) section receives data from the transmit FIFO and generates an Ethernet MAC frame from this transmit FIFO data by (1) generating preamble & SFD, (2) padding undersize packet with 0's to meet minimum packet size requirements, (3) calculating and appending CRC value, and (4) maintaining the required minimum interpacket gap to meet the defer requirements. In addition, the transmit MAC will also retransmit data in the event of a collision. Each of the above operations can be individually disabled and modified, if desired. The transmit MAC then sends the fully formed Ethernet packet to the PHY Interface for transmission. The transmit MAC section also generates MAC Control frames. The status of the last two packets transmitted is available in the TX Status register.

Preamble & SFD Generation

The transmit MAC normally appends the preamble and SFD to the packet. The device can be programmed to ***not*** *append the preamble & SFD to the transmit packet by setting the transmit preamble disable bit in the Configuration 1 register.*

AutoPad

AutoPadding is the process of automatically adding enough zeroes on packets with data fields less than 46 bytes to make the data field exactly 46 bytes in length and meet the 46 byte minimum data field requirement of IEEE 802.3. The device can be programmed to AutoPad by setting the AutoPad enable bit in the Configuration 1 register.

CRC Generation

The transmit MAC computes the CRC value on the packet, and it normally appends this CRC value to the end of the data packet from the transmit FIFO. The device can be programmed to ***not*** *append the CRC value to the end of the packet by asserting the TXNOCRC pin or by setting the transmit CRC disable bit in the Configuration 1 register. The logic interaction between the TXNOCRC pin and CRC disable bit is described in Table 3.*

Table 3. TXCRC Bit & TXNOCRC Pin Logic

TXCRC_DIS Bit 1=No Append 0=Append	TXNOCRC Pin 1=No Append 0=Append	CRC Appended to End of Packet?
1	1	No
1	0	No
0	1	No
0	0	Yes

Interpacket Gap

The interval between packets is called the interpacket gap, also referred to as IPG. The minimum IPG is controlled by the defer mechanism. The defer mechanism is an internal algorithm which computes a defer time. If packets from the transmit FIFO arrive at the transmit MAC sooner than the defer time, the defer mechanism will add enough IPG time between packets to equal the defer time value.

In Half Duplex mode, the defer time is defined as the time from the falling edge of CRS to the next rising edge of TXEN (CRS is normally asserted during half duplex mode transmission due to PHY loopback behavior). In Full Duplex mode, the defer time is defined as the time from the falling edge of TXEN to the next rising edge of TXEN.

The defer time is split into two separate periods. The first period is programmable using the bits in the Transmit Defer register. The second period is fixed. The total defer time, also referred to as minimum IPG is determined by the following equations:

100 & 10 Mbps MII Mode:

t_{DEFER} = INT((INT(t_D/40)+5+DEFER)2)+2

10 Mbps Serial Mode:

t_{DEFER} = INT((INT(t_D/100)+17+DEFER/8)+2

t_{DEFER} = Defer Time in Bytes
INT(x) = Use Whole Number Portion of x
t_D = Delay from falling edge of TXEN to falling edge of CRS (Half Duplex)
= 0 (Full Duplex)
DEFER = Decimal Value of Transmit Defer Register Bits DEFER[7:0]

The computed defer time (minimum IPG) values for each setting of the transmit defer register bits are also shown in Appendix A.

Transmit Control

Packet transmission by the MAC is initiated once the packet data has exceeded the programmable Transmit Control threshold or an entire packet has been loaded in the transmit FIFO. This function is described in more detail in the Transmit FIFO section.

AutoRetransmission Upon Collision

In Half Duplex mode, the device will automatically retransmit a packet that has been interrupted due to a collision. This is described in more detail in the Collision section.

TX Status

Each port contains two TX Status registers which store the status of the last two packets transmitted. With each transmission attempt, successful or not, one of the status registers is written with the status for that packet. When a TX Status register is written, the transmit status update bit is set in that register to indicate that the register contains new information. The data remains latched in the TX Status registers until it is read out via the Register Interface. When a TX Status register is read, the transmit status update bit is cleared low to indicate that it does not contain new data since the last read. After a TX Status Resigter has been read, that register is available to be written with new status information for another packet.

These two TX Status registers share the same register address. If both registers contain new status information, the first read to that register address will give the status of the second to last packet transmitted, and the second read will give the status of the last packet transmitted.

There are three register bits which can modify the operation of the TX Transmit Status registers:

(1) The TX Status registers can be disabled, i.e. status is never loaded into them, by setting the transmit status disable bit inthe Configuration 2 register.
(2) The TX Status registers can be configured to update continuously and not stay latched until read by setting the transmit status register update select bit in the Configuration 2 register.
(3) The TX Status registers can be configured to not store status for packets affected by a collision by setting the transmit status disable bit in the Configuration 3 register.

The bits in the TX Status register are a combination of error detect and packet status bits. Bit 3 in the TX Status register indicates if the transmit packet had an error, i.e. was it successfully transmitted or not. If the transmit packet was not successfully transmitted due to error, the error is reported in Bits 0, 2, 4, and 6 (FIFO underflow, 16 collision error, carrier sense error, and late collision). Bit 1 is a status bit and indicates if a collision occurred during the transmission of the packet. Bit 5 indicates if the transmission of the packet was deferred waiting for the completion of receiving a packet. Bit 7 in the TX status register indicates whether the register has been updated for a new packet since the last read. All the bits in the TX Status register are latched high, stay high until they are read, and cleared low when read.

All the bits in the TX Status register assert interrupt with the exception of the defer detect (Bit 5) bit and the TX Status update bit (Bit 7). Interrupts caused by all of these bits will normally be disabled but can be enabled by setting the appropriate interrupt enable bits in the TX Command register. A summary of all the bits that assert interrupt and their associated enable/disable bits is described in Table 13.

MAC Control Frame Generation

The transmit MAC can automatically generate and transmit MAC Control Pause frames. MAC Control Pause frames are used for flow control. This function is described in more detail in the MAC Control Frame section.

RECEIVE MAC

General

The receive MAC (Media Access Control) section decomposes Ethernet packets received from the receive MII by (1) stripping off the preamble & SFD, (2) stripping off the CRC, (3) checking the destination address against the address filters to determine packet validity, (4) checking frame validity against the discard conditions, and (5) checking the length/type field for MAC Control frames. Each of the above operations can be individually disabled, if desired. The receive MAC then sends any valid data to the receive FIFO for storage. The status of the last packet received is available in the RX Status register.

Preamble & SFD Stripping

The receive MAC strips the preamble and SFD from all receive packets before they are sent to the receive FIFO for storage.

CRC Stripping

The receive MAC normally strips the FCS from the receive packet. The device can be programmed to not strip the FCS field by setting the receive CRC enable bit in the Configuration 1 register. When this bit is set, the last 4-bytes of the packet containing the CRC value are left on the receive packet and are stored in the receive FIFO as part of the packet.

Unicast Address Filter

Unicast packets are filtered by comparing the destination address of the receive packet against the 48-bit value stored in the six Station Address 0-5 registers. When the destination address of a unicast packet matches the value stored in these Station Address registers, the unicast packet is deemed valid and passed to the receive FIFO; otherwise, the packet is rejected. The correspondence between the bits in the Station Address Registers and the incoming bits in the destination address of the receive packet is defined in the Station Address Register definition table.

The device can be programmed to disable the unicast address filter function and reject all unicast packets, regardless of their address, by appropriately setting the receive address match select bits in the RX Command register.

The device can also be programmed to ignore the last 4 bits of the receive destination address when comparing the DA to the SA for unicast packets. This mode can be enabled by setting the group address mode enable bit in the Configuration 1 register.

The reception of MAC Control frames is unaffected by any of the unicast packet address filtering functions and is controlled by other bits described in the MAC Control Frame section.

Multicast Address Filter

Multicast packets can be filtered by processing the destination address with the multicast address filter function. The multicast address filter function computes the CRC on the incoming DA and produces a 6-bit number that is compared against the 64 values stored in the eight Hash Filter 0-7 Registers. When the multicast packet destination address passes the address filter, the packet is deemed valid and passed to the receive FIFO; otherwise, the packet is rejected.

The multicast address filter requires 64 address filter bits to be written into the Hash Filter 0-7 Registers. The multicast address filtering algorithm is as follows:

(1) Compute a separate 32-bit CRC on the destination address field using the same IEEE 802.3 defined method that computes the transmit CRC.
(2) Use bits 0-3 of the destination address FCS to select one of the bytes in the 64-bit address filter, as shown in Table 4.
(3) Use bits 4-6 of the destination address FCS to select one of the bits within the byte selected in (2) as shown in Table 4.
(4) If the bit selected in (3) is a “1”, the destination address passes the filter; otherwise, the address fails the filter and the packet is rejected and discarded.

Note that if all 64-bits of the address filter are programmed to all 1’s, then the address filter passes all multicast addresses.

The Hash filter function is normally disabled. It can be enabled by setting the receive hash filter enable bit in the Configuration 2 register.

The device can be programmed to reject all multicast packets, regardless of their address, by appropriately setting the receive address match select bits in the RX Command register.

The reception of MAC Control frames is unaffected by any of the multicast packet address filtering functions and is

controlled by other bits described in the MAC Control Frame section

Table 4. Multicast Address Filter Map

FCS Bits [0:2]	Address Filter Byte	FCS Bits [3:5]	Address Filter Bit
000	F0[7:0]	000	Fx[0]
001	F1[7:0]	001	Fx[1]
010	F2[7:0]	010	Fx[2]
011	F3[7:0]	011	Fx[3]
100	F4[7:0]	100	Fx[4]
101	F5[7:0]	101	Fx[5]
110	F6[7:0]	110	Fx[6]
111	F7[7:0]	111	Fx[7]

F[7:0] are bytes in Hash Filter 0-7 Registers.
Fx[7:0] are bits within each byte in Hash Filter 0-7 Registers.
Bits 0-5 are the six least signficant bits of the CRC.

Broadcast Address Filter

The device does not do any filtering on broadcast packets. However, the device can be programmed to accept or reject broadcast packets, regardless of their address, by appropriately setting the receive address match select bits in the RX Command register.

The reception of MAC Control frames is unaffected by any of the broadcast packet address filtering functions and is controlled by other bits described in the MAC Control Frame section

Reject Or Accept All Packets

The device can be programmed to accept or reject all packets regardless of type or whether the packet passes the address filter by appropriately setting the receive address match select bits in the RX Command register.

The reception of MAC Control frames is unaffected by these bits and is controlled by other bits described in the MAC Control Frame section.

Frame Validity Checks

The receive MAC determines the validity of each receive packet by checking for (1) valid FCS, (2) oversize packet, and (3) undersize packet.

Valid FCS is determined by computing the CRC value on the incoming receive packet per IEEE 802.3 specifications and comparing it against the actual CRC value present in the FCS field of the received packet. If the values are not the same, (1) the frame is determined to be invalid and the packet is discarded, if the discard feature is enabled (2) the CRC error detect bit is set in the RX Status register, (3) the CRC error bit is set in the receive status word for the packet and (4) the interrupt pin for the port is asserted provided the interrupt function is enabled. Refer to the Packet Discard section for more information about discards. The device can be programmed to ***not*** *discard and accept all receive packets with bad FCS by setting the CRC error accept bit in the RX Command register.*

Oversize packets are packets whose length is greater than the maximum packet size. If a received packet is an oversize packet, then (1) the packet is determined to be invalid and it is discarded if the discard feature is enabled, (2) the oversize packet detect bit is set in the RX Status register, and (3) the interrupt pin for the port is asserted provided the interrupt function is enabled. Refer to the Packet Discard section for more information about discards. The maximum packet size can be programmed to be any one of sixteen values between 1518 bytes and 1533 bytes, exclusive of preamble & SFD, by appropriately setting the maximum packet size select bits in the Configuration 5 register. The device also can be programmed to ***not*** *discard and accept all receive oversize packets, regardless of size, by setting the oversize packet accept bit in the RX Command register.*

Undersize packets are packets whose length is less than the minimum packet size. Minimum packet size is defined to be 64 bytes, exclusive of preamble & SFD. If a received packet is an undersize packet, then (1) the frame is determined to be invalid and it is discarded if the discard feature is enabled, (2) the undersize packet detect bit is set in the RX Status register, and (3) the interrupt pin for the port is asserted provided the interrupt function is enabled. Refer to the Packet Discard section for more information about discards. The device can also be programmed to ***not*** *discard and accept all receive undersize packets by setting the undersize packet accept bit in the RX Command register.*

If a receive packet contains dribble bits, that is, the receive packet contains a non-integer number of bytes, the condition is indicated by setting the dribble error detect bit in the RX Status register.

RX Status Register

Each port contains one RX Status register which stores the status of the last packet received. With each reception attempt, whether the packet is discarded or not, the status register is written with the status for that packet. When the RX Status register is written, the receive status update bit is set in that register to indicate that the register contains new information. The data remains latched in the RX Status register until it is read out via the Register Interface. Thus, no new receive status for a packet can be written until the register is read. When the RX Status register is read, the receive status update bit is cleared low to indicate

that it does not contain new data since the last read. After the RX Status register has been read, that register is available to be written with new status information.

The bits in the RX Status register are a combination of error detect and packet status bits. Bit 5 in the RX Status register indicates if the receive packet had an error, i.e. is it good or not. If the receive packet had an error, the error is reported in Bits 0-4 (FIFO overflow, CRC error, undersize packet, oversize packet, and dribble error). Bit 6 indicates that the first 12 bytes of the packet have been successfully received (the first 12 bytes contain the packet header). Bit 7 in the RX status register indicates whether the register contain information on a new packet. All the bits in the RX Status register are latched high, stay high until they are read, and cleared low when read.

All the bits in the RX Status register assert interrupt with the exception of the dribble error detect (Bit 2) and RX update (Bit 7) bits. An interrupt caused by the good packet bit (Bit 5) and the receive first 12-Bytes bit (Bit 6) will normally be disabled but can be enabled by setting the appropriate interrupt enable bits in the RX Command register. Interrupts caused by all the receive bits can also be disabled by setting the receive interrupt disable bit in the Configuration 1 register. A summary of all the bits that assert interrupt and their associated enable/disable bits is described in Table 13.

MAC Control Frame Check

The length/type field is checked to detect whether the packet is a valid MAC Control frame. Refer to the MAC Control Frame section for more details on MAC Control frames.

TRANSMIT FIFO

General

The transmit FIFO acts as a temporary buffer between the System Interface and transmit MAC section. The transmit FIFO size is 128 bytes. Data is clocked into the transmit FIFO with the System Interface clock, SCLK. Data is automatically clocked out of the transmit FIFO with the PHY Interface TXC clock whenever (1) a full packet is loaded into the FIFO (evidenced by an EOF being written into the FIFO on the System Interface), or (2) the FIFO data exceeds the Transmit Control threshold setting. There is one programmable watermark output and one almost empty output which aid in managing the data flow into the transmit FIFO.

Transmit Control Threshold

The Transmit Control feature causes a packet in the transmit FIFO to be automatically transmitted once the transmit FIFO data exceeds the Transmit Control threhold or a full packet has been loaded into the transmit FIFO (an EOF write occurred for that packet).

The Transmit Control threshold is programmable over the entire 128 byte transmit FIFO range. The Transmit Control threshold can be programmed with the four Transmit Control threshold setting bits that reside in the Transmit Control/Product ID register. Once the data in the FIFO exceeds this threshold, then the packet is automatically transmitted to the MAC and over the PHY Interface.

Watermark

There is one watermark for the transmit FIFO. This watermark is output on the TXRDY pin. This watermark is asserted when the transmit FIFO space exceeds or equals the programmable threshold associated with the watermark.

The transmit watermark threshold for TXRDY can be programmed over the entire 128 byte TX FIFO range. The watermark threshold can be programmed with four bits that reside in the FIFO Threshold register. Once the space in the FIFO exceeds or equals the threshold of the watermark, then the watermark output pin TXRDY is asserted active low. The watermark stays asserted until the space in the FIFO goes below the threshold.

Normally, the TXRDY watermark is asserted/deasserted when the FIFO space goes below/above the TX FIFO threshold, respectively. TXRDY can be configured to deassert when either the threshold limit is exceeded or an EOF is written to the TX FIFO by setting the TXRDY function select bit in the Configuration 2 register. When this bit is set, TXRDY will remain deasserted until the packet in the TX FIFO has been completely transmitted out of the TX FIFO.

Almost Full Indication

There is an almost full output indication for the the transmit FIFO on the SPDTAVL pin. When a TX FIFO write operation is in progress, the SPDTAVL ouput pin will be asserted active low if there is less than 3 double words of TX FIFO space available in the transmit FIFO.

TX Underflow

The transmit FIFO underflow condition occurs when the TX FIFO is empty but the MAC still is requesting data to complete the transmission of a packet. If the transmit FIFO underflows, then (1) TXRET is asserted and latched, (2) packet transmission to the MII is halted with TXEN being deasserted, (3) all input data to the TX FIFO is blocked until the TXRET signal is cleared with CLRERR. Refer to the Packet Discard section for more information about discards.

Discards

Certain error conditions detected for a given packet will cause the data for that packet to be discarded or flushed from the TX FIFO. Packet discards are described in more detail in the Packet Discard section.

RECEIVE FIFO

General

The receive FIFO acts as a temporary buffer between the receive MAC section and System Interface. The receive FIFO size is 128 bytes. Data is clocked into the receive FIFO with the PHY Interface TXC clock. Data is clocked out of the receive FIFO with theSystem Interface clock, SCLK. There is one programmable watermark output and one almost full output which aid in managing the data flow out of the receive FIFO.

Watermarks

There is one watermark for the receive FIFO. This watermark is output on the RXRDY pin. This watermark is asserted when the receive FIFO data exceeds or equals the thresholds associated with the watermark.

The receive watermark threshold for RXRDY and can be programmed over the entire 128 byte receive FIFO range. The watermark threshold can be programmed with four bits that reside in the FIFO Threshold register. Once the data in the FIFO exceeds or equals the threshold of the watermark, then the watermark pin on RXRDY is asserted active high. RXRDY is also asserted if a complete packet is loaded into the receive FIFO from the MII. The watermark stays asserted until the data in the FIFO goes below the programmable threshold.

Almost Empty Indication

There is an almost empty output indication for the the receive FIFO on the SPDTAVL pin. When a RX FIFO read operation is in progress, the SPDTAVL ouput pin will be asserted active low if there is less than 3 double words of data in the receive FIFO.

RX Overflow

The receive FIFO overflow condition occurs when the receive RX FIFO is full and additional data is still being written into it from the MAC. If the receive FIFO overflows, then (1) RXDC is asserted and latched, (2) all data in the RX FIFO is discarded, (3) all input data to the RX FIFO is blocked until the RXDC signal is cleared with CLRRXERR, (4) the RX FIFO overflow bit is set as an indication of this condition in the RX Status register, and (5) the interrupt pin is asserted for that port provided the interrupt function is enabled. Refer to the Packet Discard section for more information about discards. The device can be programmed to not discard and subsequently accept all packets corrupted by overflow by setting the RX FIFO overflow bit in the RX Command register.

Discards

Certain error conditions detected for a given packet will cause the all the data to be discarded or flushed from the RX FIFO. Packet discards are described in more detail in the Packet Discard section.

COLLISION

General

Collisions occur when transmission and reception occur at the same time on the physical media. Collisions on the physical media are detected by an external Physical Layer device and indicated to the 84302 by the assertion of the COL pin on the PHY interface for that port. A collision causes the transmission of a packet to be halted and automatically retransmitted at a later time, according to the backoff algorithm.

Collisions only apply to Half Duplex mode; the collision function is disabled and COL pin ignored in Full Duplex mode.

Backoff and Retransmission

When a collision is signalled to the device from the PHY during the first 512 bits of a transmit packet, the backoff algorithm halts transmission for a predetermined amount of time, per IEEE 802.3 specification. This predetermined interval is referred to as the backoff interval. The backoff interval is a random number that is an exponential function of the number of times a collision has occurred while attempting to transmit a particular packet. After the backoff internal has expired, the packet is automatically retransmitted.

The random number generator used by the backoff algorithm can be reset separately for each port by setting the backoff counter reset bit in the Configuration 3 register.

Per IEEE 802.3 specifications, if a particular packet has been halted 16 times because of collisions and another collision occurs, then the packet transmission will be permantly halted and that transmit packet will be discarded. Refer to the Packet Discard section for more details on packet discards.

The 16 retries and automatic retransmission of a packet after a collision can be turned off by asserting the ONETRYMODE pin. When this pin is pinstrapped active high, the transmit packet will be discarded if the transmission is unsuccessful due to a single collision, i.e. no transmission retry is attempted after a collision.

Late Collision

When a collision is signalled to the device from the PHY after the first 512 bits of a transmit packet, the collision is determined to be a late collision. Late collision, per IEEE 802.3 specifications, are considered errors. Upon the detection of a late collision, the transmit packet affected by the late collision is discarded. Refer to the Packet Discard section for more details on packet discards.

Collision Indication

There are status bits related to collisions in the TX Status register indicating that (1) one or more collisions have occurred while attempting transmission of a packet, (2) 16 or more collisions have occurred while attempting transmission of a packet, and (3) a late collision has occurred during packet transmission. These three bits will also assert the interrupt pin for a given port.

PACKET DISCARD

General

The device can be programmed to discard receive and transmit packets when certain error conditions are detected. The detection of these error conditions can occur in either the MAC or FIFO sections.

Transmit Discards

Transmit packets will be automatically discarded if certain error conditions are detected. These error conditions are described in Table 5. When a discard error is detected for a transmit packet, (1) transmission is terminated for that packet (i.e. TXEN is deasserted), (1) the packet is discarded, that is, all data in the packet containing the error is flushed from the transmit FIFO, and (3) TXRET is asserted if the packet was being input from the System Interface when the discard occurred.

Table 5. Transmit Discard Conditions

Discard Condition	Description
Transmit FIFO Underflow	TX FIFO empty while transmitting the packet. TXEN is deasserted
Late Collision	A late collision occurred while transmitting the packet.
Carrier Sense Error	CRS never went active during transmission or went from an active to inactive state during transmission.
16 Collisions	16 attempts to transmit the packet all resulted in transmit collision.
ONETRYMODE and Collision	The ONETRYMODE pin is high and a collisions occurs.

Receive Discards

Receive packets can be discarded if certain error conditions are detected. These error conditions are described in Table 6. When a discard condition is detected on a receive packet, (1) all data is flushed from the receive FIFO, (2) the input to the RX FIFO is blocked until the beginning of the next packet and (3) the error condition is indicated by the assertion of the RXDC pin. The packet can then be discarded by asserting the RXABORT pin.

Each of the receive discard conditions can be individually removed as a discard condition by appropriately setting the discard bits in the RX Command register. When these bits are set, a packet that is afflicted with the error condition indicated by that bit will not be discarded.

Table 6. Receive Discard Conditions

Discard Condition	Description
Receive FIFO Overflow	Receive FIFO full.
CRC Error	Receive packet has CRC Error.
Oversize Packet	Receive packet is greater than maximum packet size, exclusive of preamble & SFD. Maximum packet size is programmable between 1518-1533 bytes.
Undersize Packet	Receive packet is less than 64 bytes, exclusive of preamble & SFD
RXABORT Pin	RXABORT pin was asserted while the receive packet was read out on the System Interface.

Discard Output Indication

When a packet that is being receive/transmitted over the System Interface has been automatically discarded, the TXRET and RXDC output pins are asserted to indicate that the discard happened. TXRET and RXDC are normally latched high when a discard takes place. TXRET and RXDC for the selected port can be cleared low by asserting the clearing pin, CLRTXERR and CLRRXERR, respectively.

When TXRET and RXDC are asserted, all data is prevented from being written to the transmit and receive FIFO's, respectively, as long as the respective signals are latched high. When these signals are cleared, then the respective FIFO's can be written to.

RECEIVE STATUS WORD

General

A 32-bit status word can be appended to the end of each receive data packet and stored in the receive FIFO. This status word contains a byte count and error information for the receive data packet.

Format and Bit Order

The format for the status word is shown in Table 7. The top 16-bits contain the actual byte count for the packet, and the bottom 16-bits contain the status information related to the packet.

The byte count value in the status word is the total number of bytes stored in the RX FIFO for the particular packet. The byte count always includes the 4 bytes associated with the CRC, independent of whether the CRC has been removed or not by the receive MAC. The byte count also does not include the preamble octets.

The Receive Status Word is always read out of the system interface on the next full 32-bit word boundary, following the end of packet data, as shown in Figure 4.

Status Word Disable

The status word is normally appended to the end of all good receive packets. The receive status word can be not appended to the end of the packet and thus disabled by setting the status word disable bit in the Configuration 3 register.

Table 7. Receive Status Word Definition

RXTXDATA31 RXTXDATA16

BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
							RXER	RXAB		GOOD	OSIZE	USIZE	DRIB	CRC	OVFL

RXTXDATA15 RXTXDATA0

Symbol	Name	Definition	Position On RXTXDATA[31:0] Pins
BC[15:0]	Byte Count	Contains Actual Byte Count of Receive Packet	RXTXDATA[31:16]
—	—	Reserved	RXTXDATA[15:9]
RXER	RXER Error	1 = Receive Packet had RXER symbol error reported over MII from external PHY	RXTXDATA8
RXAB Packet	RXABORT	1 = Receive Packet was aborted with RXABORT pin	RXTXDATA7
—	—	Reserved	RXTXDATA6
GOOD	Good Packet	1 = Receive Packet is a Good Frame	RXTXDATA5
OSIZE	Oversize Error	1 = Receive Packet is Greater Than Minimum Size	RXTXDATA4
USIZE	Undersize Error	1 = Receive Packet is Less Than Minimum Size	RXTXDATA3
DRIB	Dribble Error	1 = Receive Packet has a Non-Integer # of Bits or Nibbles (Dribble)	RXTXDATA2
CRC	CRC Error	1 = Receive Packet has a CRC Error	RXTXDATA1
OVFL	RX FIFO Overflow Error	1 = Receive FIFO is Full and more Data is Attempting to be Inputted	RXTXDATA0

PHY INTERFACE

General

The PHY Interface provides the connection between the 84302 and an external Physical Layer device. There are two PHY Interfaces on the 84302: (1) MII, and (2) 10 Mbps Serial. The MII (short for Media Independent Interface) will operate in both 100 and 10 Mbps modes and meets all the requirements outlined in IEEE 802.3 Clause 22. The 10 Mbps Serial Interface only operates at 10 Mbps and is compatible with common industry standards for the 7-wire serial interface. The selection of either MII or 10Mbps serial interface is done by appropriately setting the PHY interface select bit in the TX command register. The device can directly connect, without any external logic, to any Physical Layer device which complies with the either IEEE 802.3 Clause 22 or the common 7-wire 10 Mbps interface.

Data Format and Bit Order

The format and bit order of the MII and 10 Mbps serial data word on TXD[3:0] and RXD[3:0] and its relationship to the MAC frame and the System Interface data words is shown in Figure 4 (for MII, this is same format as specified in IEEE 802.3 Clause 22). Note that Figure 4 has the device in the little endian format (default). If the device is in the big endian format, the byte order of the System Interface data word is flipped. See the System Interface section for more details if needed.

MII Signals

The MII consists of fifteen signals per port: one transmit clock input (TXC), four transmit data outputs (TXD[3:0]), one transmit enable output (TXEN), one receive clock input (RXC), four receive data inputs (RXD[3:0]), one carrier sense input (CRS), one receive data valid input (RXDV), one receive data error input (RXER), and one collision input (COL). The transmit and receive clocks operate at 25 MHz in 100 Mbps mode and 2.5 MHz in 10 Mbps mode.

MII Transmit Operation

On the transmit side, TXC needs to be continuously input at a frequency of 25 MHz in 100 Mbps mode and 2.5 MHz in 10 Mbps mode. When no data is to be transmitted, TXEN is deasserted, TXER is held low, and TXD[3:0] are held low. When packet data is to be transmitted, TXEN is asserted on the rising edge of TXC, and data on TXD[3:0] is clocked out on rising edges of the TXC clock output while TXEN is asserted active high. TXD[3:0] input data is nibble wide packet data whose format needs to be the same as specified in IEEE 802.3 and shown in Figure 4. To terminate the transmission of a packet, TXEN is deasserted on the the same rising edge of TXC as the last data nibble.

MII Receive Operation

On the receive side, RXC needs to be continuously input at a frequency of 25 MHZ in 100 Mbps mode and 2.5 MHZ in 10 Mbps mode. When data not being sent from an external Physical Layer device, CRS has to be input low, RXDV has to be input low, RXER has to be input low, and any data on RXD[3:0] is ignored. An external Physical Layer device signals the start of a packet to the device by asserting CRS and holding it asserted for the entire packet reception. While CRS is asserted, valid data is indicated to the device when RXDV is asserted on the falling edge of RXC. While RXDV is asserted, data on RXD[3:0] is considered valid and input to the receive MAC on falling edges of RXC. The RXD[3:0] data has the same frame structure as the TXD[3:0] data and is specified in IEEE 802.3 and shown in Figure 4. The end of packet is detected when CRS and RXDV are deasserted.

RXER is a receive error input which is asserted by the external Physical Layer device when it detects an error on a data nibble. RXER is asserted on the falling edge of RXC for the duration of the RXC clock cycle during which the nibble containing the error is being input on RXD[3:0]. Per IEEE 802.3 specifications, packets with containing RXER's are treated as if the FCS value is incorrect.

The collision input, COL, is asserted by the Physical Layer device whenever it detects the collision condition.

10 Mbps Serial Interface

The 10 Mbps Serial Interface uses only 7 pins in contrast to the 15 pin MII. The 10 Mbps Serial Interface only operates at 10 Mbps. The 10 Mbps serial mode is selected by setting the PHY interface select bit in TX command register. The 10 Mbps Serial Interface is identical to the MII at 10 Mbps except: (1) TXC and RXC frequency is 10 MHz instead of 2.5 MHZ, (2) Data is serial wide using only data pins RXD0 and TXD0 instead of nibble wide, (3) RXDV is not used, (4) RXER is not used, and (5) the transmit data signals are referenced to TXC falling edge instead of rising edge.

Clock Frequency Sense

As stated earlier, TXC must be continously input at a frequency of 25 MHz in 100 Mbps mode and 2.5 MHz in 10 Mbps mode. The TXC frequency is monitored by an internal clock frequency sense circuit and the detected TXC frequency is stored in the TXC frequency detect bit in the Miscellaneous Status register.

SQE

SQE (short for Signal Quality Error) is a pulse outputted on the COL pin by an external PHY after the reception of each receive packet. SQE is only enabled in 10 Mbps Serial mode. The detection of SQE pulses by the 84302 is reported on the SQE detect bit in the Miscellaneous Status register.

MANAGEMENT INTERFACE (MI)

General

The Management Interface, referred to as the MI, is a serial interface for passing data between an internal register and an external PHY. The MI meets all IEEE 802.3 Clause 22 requirements.

The MI consists of two signals: one MI clock output (MDC), and one bidirectional data line (MDIO).

Data Format and Bit Order

The format of a MI data transfer cycle is defined in IEEE 802.3 Clause 22 and shown in Figure 6. The definition of each bit transmitted over the MI is defined in Table 8. An MI data transfer cycle consists of 64 bits: (1) The first 32 bits are the idle pattern, (2) the next 16 bits are always written from the device to an external PHY and contain command information related to the MI data transfer cycle, and (3) the last 16 bits contain the actual data transferred over the MI. These last sixteen bits are output from the device when a write cycle is selected; they are input to the device when a read cycle is selected.

Bit Definition

The bits comprising a MI data transfer cycle are defined in Table 8. Some of the bits in a MI data transfer cycle are read from/written to specific register bits. Other MI data transfer cycle bits are generated by internal logic. The source of each MI data transfer bit is defined in Table 8. Note that the registers are replicated per port; thus, the values used on any particular MI data transfer cycle are obtained from the MI registers of the selected port.

Write Operation

A write operation is defined to be an MI data transfer cycle where the last 16 bits of data in the frame are obtained from the MI Data 0-1 Registers and are output onto the MDIO pin and written to the external PHY. A write operation is selected by appropriately setting the read/write select bit in the MI Command/Status 1 register. After this bit is written, then a write MI data transfer cycle is initiated on the MDC and MDIO pins. After the write MI cycle has completed and all the data is successfully written out, the MI status bit in the MI Command/Status 1 register is set to indicate that the operation is complete. The interrupt pin will be asserted after a write operation has completed if the interrupt bit is set in the MI Command/Status 1 register. After the completion of a write operation, the MDC clock is turned off and MDIO is held high.

Read Operation

A read operation is defined to be an MI data transfer cycle where the last 16 bits of data in the frame are read from an external PHY and latched into the device from the MDIO pin and internally stored in the MI Data 0-1 Registers. A read operation is selected by appropriately setting the read/write select bit in the MI Command/Status 1 register. After this bit is written, then a read MI data transfer cycle is initiated on the MDC and MDIO pins. After a read MI cycle has completed and all the data is successfully loaded into the MI Data registers, the MI status bit in the MI Command/Status 1 register is set to indicate that the operation is complete. The interrupt pin will be asserted after a read operation has completed if the interrupt bit is set in the MI Command/Status 1 register. After the completion of a read operation, the MDC clock is turned off and MDIO is held high.

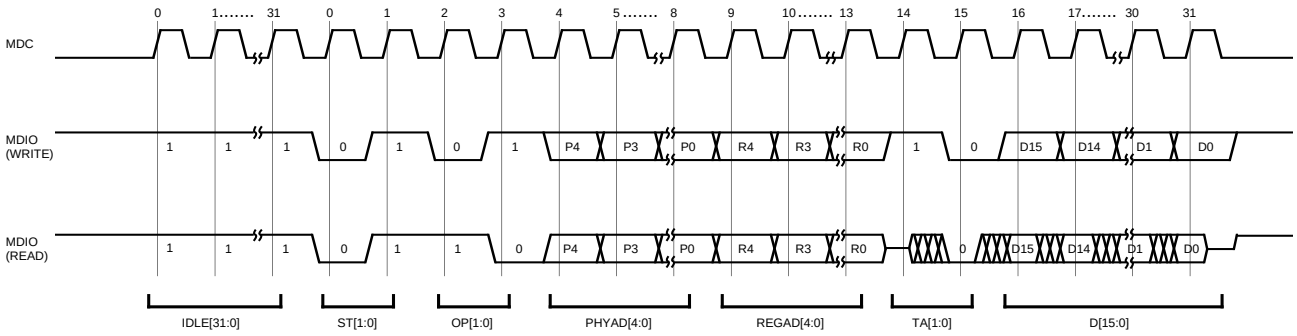


Figure 6. MI Frame Format and Bit Order

MDC Cycle Time

The MDC clock period is programmable and is a function of (1) the system clock period, SLCK, and (2) the clock period select bits in the MI Command/Status 0 register according to the equation shown in the MI Command/ Status 0 register definition table.

FULL DUPLEX

General

Half Duplex mode is the normal CSMA/CD operation defined in IEEE 802.3. Full Duplex operation is a mode that allows transmission and reception to occur simultaneously. As such, when the device is placed in Full Duplex mode, the collision function is disabled and the loopback of transmit to receive (TXEN to CRS) caused by the external Physical Layer device has to be ignored.

Enabling Full Duplex

The device can be placed in Full Duplex mode, on a per port basis, by either setting the $\overline{\text{FDUPLX}}$_[1:4] pin for that port to Full Duplex mode or by setting the Full Duplex select bit in the Configuration 1 register for that port to Full Duplex mode. The interaction of the pin and bit is described in Table 9. Note that both the pin and bit must be set to Half Duplex for Half Duplex mode to be selected.

Table 9. FDX Bit & $\overline{\text{FDUPLX}}$ Pin Logic

FDX Bit in Config. 1 Reg. 1=Full Duplex 0=Half Duplex	$\overline{\text{FDUPLX}}$ Pin 1=Half Duplex 0=Full Duplex	
1	1	Full Duplex
1	0	Full Duplex
0	1	Half Duplex
0	0	Full Duplex

Full Duplex Indication

The Duplex state of the device, either Full or Half, is reported on the duplex status bit in the Miscellaneous Status register.

Loopback Disable

In Half Duplex operation, an external PHY device will always loopback a transmit packet to the receive side over the PHY interface. This loopbacked receive packet can be automatically ignored and discarded by setting the Receive Own Transmit Ignore bit in the Configuration 1 register.

Table 8. MI Bit Definitions

Symbol	Name	I/O	Definition	Where Bits Come From
IDLE[31:0]	Idle Pattern	O	These 32 bits are always 1's, and they provide the necessary spacing between MI data transfer cycles.	Internally Generated
ST1 ST0	Start Bits	O	These two bits always contain the 01 pattern. This bit pattern (following an Idle Pattern) signals the start of an MI data transfer cycle.	Internally Generated
OP1 OP0	Opcode Select	O	10 = Read Cycle 01 = Write Cycle	MI Command/Status 1 Register
PHYAD[4:0]	Physical Device Address	O	These bits contain the address of the external PHY that is selected for the MI data transfer.	MI Command/Status 1 Register
REGAD4[4:0]	Register Address	O	These bits contain the address of the register in the external PHY that is selected for the MI data transfer.	MI Command/Status 0 Register
TA1 TA0	Turnaround Time	I/O	These bits provide some turnaround time for MDIO between write and read operations. For Write Cycle Output TA[1:0] = 10 For Read Cycle, Input TA[1:0] = Z0	Internally Generated
D[15:0]	Data	I/O	These 16 bits contain data to/from the selected register in the selected external PHY.	MI Data 0-1 Registers

IDLE31 is shifted out first on MDIO

In Full Duplex operation, the Receive Own Transmit Ignore bit has be set to a "0" for proper operation. This bit will be automatically set to 0 in Full Duplex mode if the ROWNT override bit is set in the Configuration 3 register.

FLOW CONTROL

Flow control refers to the ability to cause a remote station to temporarily halt sending packets in order to prevent packet loss in a congested system. The 84302 has separate flow control mechanisms for Half and Full Duplex modes. Half Duplex uses a collision based flow control mechanism, Full Duplex uses MAC Control frames for flow control. The Half Duplex flow control mechanism is described in the Automatic JAM section. The Full Duplex flow control mechanism is described in the MAC Control Frame section. Refer to these sections for more details on the respective flow control schemes.

AUTOMATIC JAM

The automatic JAM feature is intended for Half Duplex flow control and is only enabled if the device is in Half Duplex mode. The automatic JAM feature is enabled by asserting the FCNTRL_[1:4] pin for the a given port. If a receive packet is detected while the FCNTRL_[1:4] pin is in the asserted state, then a JAM packet is internally generated and automatically transmitted by the transmit MAC over the PHY Interface for that port. This autogenerated JAM packet will create a collision which will cause a remote station to temporarily cease transmission due to its backoff algorithm.

MAC CONTROL FRAMES

General

MAC Control frames are special packets which only contain signaling information. MAC Control frames are specified in IEEE 802.3 Clause 31 for Full Duplex operation only and are used primarily for Full Duplex flow control.

MAC Control frames defined in IEEE 802.3 Clause 31 are differentiated from other packets by having the unique value of 8808H in the length/type field. MAC Control frames have the same packet format as normal Ethernet packets except the Data field is composed of an opcode field and a parameter field. The opcode field contains an opcode command, the parameter field contains a value associated with the opcode command. The only opcode command defined to date by IEEE 802.3x is the Pause opcode; the parameter field for the Pause opcode defines the pause time. MAC Control frames with the Pause opcode, referred to as Pause frames, are only allowed to have a destination address equal to a specific reserved multicast address or the address of the receive station itself. The value of the reserved multicast address is 01-80-C2-00-00-01H.

The 84302 normally treats MAC Control frames according to the IEEE 802.3 Clause 31 algorithm. When the receive MAC detects a MAC Control frame with a Pause opcode and with the destination address equal to the reserved multicast address or the address stored in the MAC Station Address 0-5 registers, then the transmitter is paused for a time equal to the number of pause times specified in the parameter field. Each unit of pause time equals 512 bits (5.12 uS for 100 Mbps, 51.2 uS for 10 Mbps). If a Pause frame is received while another packet is being transmitted, then the transmission is completed for the current packet being transmitted, and then the transmitter is paused. If there are other packets in the transmit FIFO, their transmission will be delayed until the pause timer has expired. MAC Control frames are not normally passed into the receive FIFO; they are terminated in the receive MAC.

The 84302 also has incorporated some additional features to facilitate MAC Control frame operation. These features are described in the following sections.

Automatic Pause Frame Generation

MAC Control Pause frames can be automatically generated by asserting the FCNTRL pin. When the FCNTRL pin is asserted, a series of Pause frames will be internally generated and transmitted over the MII Interface. These Pause frames are referred to as autogenerated Pause frames. The transmission of autogenerated Pause frames is not affected by the reception of a receive Pause frame; receive Pause frames only inhibit the transmission of regular packets from the transmit FIFO.

If a packet transmission is in progress when the FCNTRL pin is asserted, the device will wait until the transmission of that packet has completed and then transmit the autogenerated Pause frame before any other subsequent packets in the TX FIFO are transmitted. When the first autogenerated Pause frame begins transmission, an internal timer will start, whose value is equal to the pause_time value in the Pause frame (and obtained from Flow Control Pause Time 0-1 registers). If the FCNTRL pin is still asserted when the internal pause timer expires, then another autogenerated Pause frame will be transmitted. This process will continue to repeat itself as long as FCNTRL remains asserted. When FCNTRL is deasserted, then one last autogenerated Pause frame of pause_time=0 will be transmitted. To compensate for latency, the internal pause timer will be internally shorten itself by 32 units from the value programmed into the Flow Control Pause Time 0-1 registers.

The device can be programmed to eliminate the last autogenerated Pause frame with pause_time=0 by clearing low the MAC Control frame end pause bit in the Configuration 4 register.

The structure of the autogenerated Pause frame is described in Figure 7. Note that the source address and pause_time parameter fields are programmable through internal registers as shown in Figure 7.

Transmitter Pause Disable

Receive MAC Control frames normally pause the transmitter. Receive MAC Control frames can be programmed to not pause the transmitter by clearing the MAC Control frame enable bit in the Configuration 4 Register. When this bit cleared low, received Pause frames do not affect the transmitter.

Passthrough to FIFO

Receive MAC Control frames are normally discarded and not passed to the receive FIFO. Receive MAC Control frames can be passed to the receive FIFO by appropriately setting the MAC Control frame passthrough bits in the Configuration 4 register. These bits allow either all MAC Control frames or just non-Pause frames to be passed to the receive FIFO.

Reserved Multicast Address Disable

Receive MAC Control frames are normally rejected as invalid if they do not have the reserved multicast address in the destination address field. Receive MAC Control frames can be accepted without regard to the contents of the destination address field by appropriately setting the MAC Control frame address filter bit in the Configuration 4 register. When this bit is cleared low, any value in the destination address field will be accepted as a valid address.

RESET

The device has three resets. All three resets are described in Table 10.

From Table 10, note that the device reset is controlled by a pin, and it must be asserted at powerup in order to properly initialize the device. When this device reset is initiated, it forces the other two reset bits to their default states of logic 1; these two reset bits must then be cleared to logic 0 for normal device operation to begin.

The RESET pin or bit should be asserted for a minimum of 10 µs. During the RESET period, the TXC and RXC input clocks from the external PHY must be active. After the RESET pin or bit has been deaasserted, the device should be ready for normal operation after 40 SCLK cycles.

Table 10. Reset Description

Name	Initiated By	Reset Action
Device Reset	$\overline{\text{RESET}}$ Pin Asserted Low	Reset Datapath
		Flush Transmit FIFO
		Flush Receive FIFO
		Reset Bits to Defaults
		Reset Counters to 0
Datapath Reset	Data Path Reset Bit in Configuration 4 Register	Reset Datapath
		Flush Transmit FIFO
		Flush Receive FIFO
Counter Reset	Counter Reset Bit in Configuration 4 Register	Reset Counters to 0

COUNTERS

General

The 84302 has a set of 51 counters per port. These counters provide the necessary statistics to completely support the following specifications:

(1) RMON Statistics Group (IETF RFC 1757)
(2) SNMP Interfaces Group (IETF RFC 1213 & 1573)
(3) Ethernet-Like MIB (IETF RFC 1643)
(4) Ethernet MIB (IEEE 802.3u Clause 30)

The counter set includes the packet and octet statistics for transmit side. The RMON specs literally state that packet and octet counters should only tabulate received information. This is sometimes interpreted to mean both transmitted and received information because Ethernet was originally a shared media protocol. As such, transmit packet and octet counters are also available in counters #17-26 and can be summed with the receive packet and octet counts if desired.

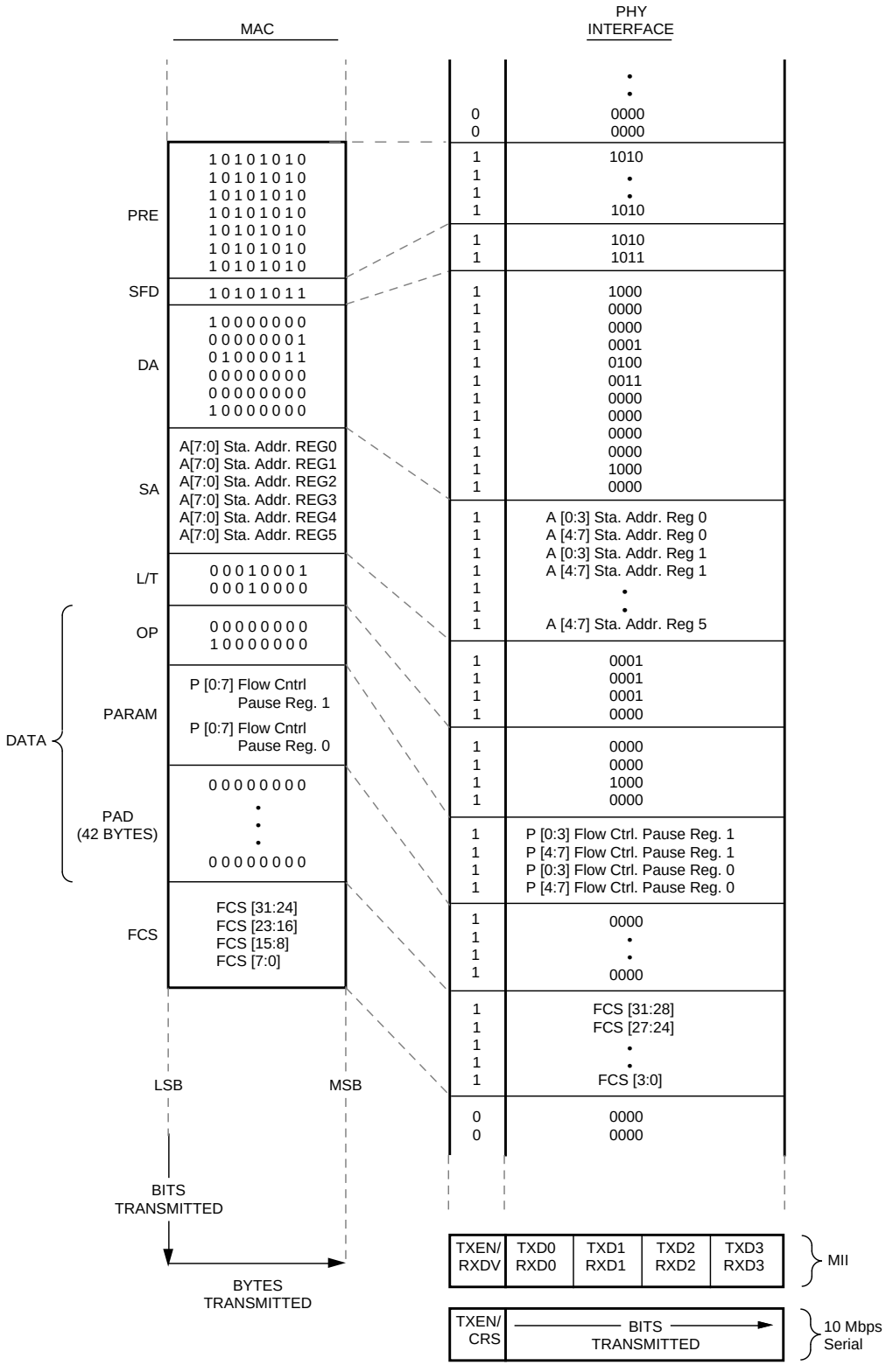


Figure 7. Autogenerated Pause Frame Format

A complete list of the counters along with their definitions is shown in Table 11. The exact correspondence of the actual MIB objects from the above IETF and IEEE specifications to the actual 84302 counters locations is described in the Applications section and is shown there in Tables 38-41.

The current count for each counter is stored in individual Counter Registers. The address location for each Counter Register is also shown in Table 11. Note that all the counters are 32-bit long but the Counter Register length is only 16-bit. The entire 32-bits can be read out of the device by doing two successive 16-bit reads from the same address (or 4 reads if BUSSIZE is set for 8-bit bus width). The first 16-bit read outputs the upper 16-bits (MS byte), the second 16-bit word outputs the lower 16-bits (LS byte).

Each counter is responsible for tabulating the number of times a specific event occurs. When a counter is read out, the count can be automatically reset to 0 or it can remain unchanged (programmable). Counters can be configured to either stop counting when they reach their maximum count or rollover (programmable). When a counter read operation is initiated, the 32-bit counter result to be accessed is transferred to two internal 16-bit holding registers. These holding registers freeze and store the counter result for the duration of the read operation while allowing the internal counter to continue to increment if needed.

Counter Overflow

Each 32-bit counter has a status output bit associated with that counter. The status output bits are stored in the Counter Status 0-6 registers. These status bits are set when the counter value reaches 80000000H (i.e. MSB bit goes from a 0 to a 1). Thus, the status bits are set when the counter becomes half full.

The counter status bits stay latched high until they read out (R/LHI bits). When a counter status bit is read out, it is then cleared low. Counter status bits are also interrupt bits; that is, the setting of any counter status bit will cause the assertion of the interrupt pin, INT_[1:4] for that port. When a counter status bit is read, the interrupt caused by that bit is cleared. Note that INT_[1:4] stays asserted until all interrupt bits are cleared. Each counter status bit can be individually programmed to not assert interrupt by setting the mask bit associated with that counter bit in Counter Interrupt Enable 1-7 registers.

Counter Reset On Read

The counter value is normally unaffected by a read operation on that counter. However, the counters can be programmed to automatically reset the count to 0 when read out by setting the counter reset on read bit in the Configuration 3 Register. When this bit is set high, the counter is reset to 0 when read out; when this bit is cleared low, the count inside the counters is unaffected by a read as long as the counter is not at maximum count. If a counter is at maximum count, it's count is always reset to 0's when it is read out.

Counter Rollover

The counters normally rollover to 0 when they exceed their maximum count (i.e. receive an increment when counter is at maximum count). The counters can be programmed to freeze and stop counting once they reach their maximum count by setting the counter rollover bit in the Configuration 3 register.

Maximum Packet Size

The maximum packet size used for the management counter statistics can be set to any value between 1518-1533 bytes by appropriately setting the counter maximum packet size select bit in the Configuration 4 register and the maximum packet size select bits in Configuration 5 register. The maximum packet size default is 1518 bytes.

Counter Reset

All counters, for a given port, can be reset to all 0's by setting and then clearing the counter reset bit in the Configuration 4 register for that port. Asserting the device reset pin $\overline{RESET}$ will also set the counter reset bits to their default values of 1 and subsequently force the counters in all ports to 0. When this device reset occurs, the counter reset bits will be set to their default value of 1, and they must be cleared to 0, on each port, in order for the counters on that port to be functional.

Table 11. Counter Definition

Ctr. #	Counter Name (MIB Object Name)	Counter Definition			
		RX/ TX	Description	Size (Bits)	Register Address A[7:1]
	RMON Statistics Group (RFC 1757)				
1	etherStatsDropEvents	RX	Packets with receive FIFO overflow error.	32	0010111
2	etherStatsCRCAlignErrors	RX	Packets of legal-length with CRC error or alignment error.	32	0011000
3	etherStatsUndersizePkts	RX	Packets of length <64 bytes with no other errors.	32	0011001
4	etherStatsOversizePkts	RX	Packets of length > Max_Packet_Length with no other errors.	32	0011010
5	etherStatsFragments	RX	Packets of length < 64 bytes with CRC error or alignment error.	32	0011011
6	etherStatsJabber	RX	Packets of length > Max_Packet_Length with CRC error or alignment error.	32	0011100
7	etherStatsOctets	RX	Bytes, exclusive of preamble, in good or bad packets. Bytes in packets with bad SFD are excluded.[6]	32	0011101
8	etherStatsPkts	RX	All packets, good or bad.[6]	32	0011110
9	etherStatsBroadcastPkts	RX	Broadcast packets, good only.[6]	32	0011111
10	etherStatsMulticastPkts	RX	Multicast packets, good only.[6]	32	0100000
11	etherStatsPkts64Octets	RX	Packets of length = 64 bytes, good or bad.[6]	32	0100001
12	etherStatsPkts65to127Octets	RX	Packets of length between 65-127 bytes, inclusive, good or bad.[6]	32	0100010
13	etherStatsPkts128to255Octets	RX	Packets of length between 128-255 bytes, inclusive, good or bad.[6]	32	0100011
14	etherStatsPkts256to511Octets	RX	Packets of length between 256 and 511 bytes, inclusive, good or bad.[6]	32	0100100
15	etherStatsPkts512to1023Octets	RX	Packets of length between 512 and 1023 bytes, inclusive, good or bad.[6]	32	0100101
16	etherStatsPkts1024to1518Octets	RX	Packets of length between 1024 and Max_Packet_Length , inclusive, good or bad.[6]	32	0100110
17	etherStatsOctets_TX	TX	Bytes, exclusive of preamble, in good or bad packets. This includes retries.[6]	32	0100111
18	etherStatsPkts_TX	TX	All packets, good or bad. No retries.[6]	32	0101000
19	etherStatsBroadcastPkts_TX	TX	Broadcast packets, good only. No retries.[6]	32	0101001
20	etherStatsMulticastPkts_TX	TX	Multicast packets, good only. No retries.[6]	32	0101010
21	etherStatsPkts64Octets_TX	TX	Packets of length = 64 bytes, good or bad.[6]	32	0101011
22	etherStatsPkts65to127Octets_TX	TX	Packets of length between 65-127 bytes, inclusive, good or bad.[6]	32	0101100

Ctr. #	Counter Name (MIB Object Name)	Counter Definition			
		RX/ TX	Description	Size (Bits)	Register Address A[7:1]
23	etherStatsPkts128to255Octets_TX	TX	Packets of length between 128-255 bytes, inclusive, good or bad.[6]	32	0101101
24	etherStatsPkts256to511Octets_TX	TX	Packets of length between 256 and 511 bytes, inclusive, good or bad.[6]	32	0101110
25	etherStatsPkts512to1023Octets_TX	TX	Packets of length between 512 and 1023 bytes, inclusive, good or bad.[6]	32	0101111
26	etherStatsPkts1024to1518Octets_TX	TX	Packets of length between 1024 and Max_Packet _Length, inclusive, good or bad.[6]	32	0110000
27	etherStatsCollisions	TX/ RX	CRS asserted and one or more collisions has occurred, exclusive of SQE.	32	0110001
SNMP MIB-II Interfaces Group (RFC 1213 & 1573)					
	ifInDiscards	RX	Packets with receive FIFO overflow error. Equivalent to “etherStatsDropEvents”		Use Ctr. #1
28	ifOutDiscards	TX	Packets with transmit FIFO underflow error.	32	0110010
	ifInErrors	RX	All packets, bad only. Equivalent to “etherStatsCRCAlignError + etherStatsUndersizePkts + etherStatsOversizePkts”		Use Ctr. # 2+3+4
29	ifOutErrors	TX	All packets, bad only. No retries.	32	0110011
30	ifInOctets	RX	Bytes, including preamble, in good or bad packets.	32	0110100
31	ifOutOctets	TX	Bytes, including preamble, in good or bad packets. This includes retries.	32	0110101
32	ifInUcastPkts	RX	Unicast packets, good only.	32	0110110
33	ifOutUcastPkts	TX	Unicast packets, good and bad. No retries	32	0110111
	ifInNUcastPkts	RX	Broadcast and multicast packets, good only. Equivalent to “etherStatsBroadcastPkts + etherStatsMulticastPkts”		Use Ctr. # 9+10
	ifOutNUcastPkts	TX	Broadcast and multicast packets, good only. Equivalent to “etherStatsPkts - ifOutUcastPkts”		Use Ctr. # 8-33
Ethernet MIB (802.3 Clause 30)					
	aFramesTransmittedOK	TX	All packets, good only. Equivalent to “etherStatsPkts - ifOutErrors”		Use Ctr. # 8-29
34	aSingleCollisionFrames	TX	Packets successfully transmitted after one and only one collision (i.e.: attempt value=2).	32	0111000
35	aMultipleCollisionFrames	TX	Packets successfully transmitted after more than one collision (i.e.: 2<attempt value<16).	32	0111001

Ctr. #	Counter Name (MIB Object Name)	Counter Definition			
		RX/ TX	Description	Size (Bits)	Register Address A[7:1]
	aFramesReceivedOK	RX	All packets, good only. Equivalent to "ifInUcastPkts + etherStatsBroadcastPkts+ etherStatsMulticastPkts"		Use Ctr.# 32+9+10
36	aFrameCheckSequenceErrors	RX	Packets with CRC error only.	32	0111010
37	aAlignmentErrors	RX	Packets with alignment error only.	32	0111011
38	aOctetsTransmittedOK	TX	Bytes, exclusive of preamble, in good packets only. No retries.	32	0111100
39	aFramesWithDeferredXmissions	TX	Packets deferred, i.e. packets whose transmission was delayed due to busy medium, on first attempt only. This does not include collisions.	32	0111101
40	aLateCollisions	TX	Packets that encounter a late collision, i.e. encountered collisions more than 512 bit times into transmitted packet. A late collision is counted twice, as a collision and a late collision.	32	0111110
41	aFrameAbortedDueToXSCollisions	TX	Packets not successfully transmitted after more than 15 collisions (i.e.: attempt value=16).	32	0111111
	aFrameAbortedDue ToIntMACXmitError	TX	Packets with transmit FIFO underflow error. Equivalent to "ifOutDiscards"		Use Ctr. # 28
42	aCarrierSenseErrors	TX	Carrier sense dropout errors, i.e. number of times that carrier sense is not asserted or deasserted during packet transmission, without a collision.	32	1000000
43	aOctetsReceivedOK	RX	Bytes, exclusive of preamble, in good packets only.		1000001
	aFramesLostDueToIntMACRcvrError	RX	Packets with receive FIFO overflow error. Equivalent to "etherStatsDropEvents"		Use Ctr. # 1
	aMulticastFrameXmittedOK	TX	Multicast packets, good only. Equivalent to "etherStatsMulticastPkts_TX"		Use Ctr. # 20
	aBroadcastFramesXmittedOK	TX	Broadcast packets, good only. Equivalent to "etherStatsBroadcastPkts_TX"		Use Ctr. # 19
44	aFramesWithExcessiveDefferal	TX	Packets with excessive deferral, i.e. packets waiting for transmission longer than two max packet times.	32	1000010
	aMulticastFramesReceivedOK	RX	Multicast packets, good only. Equivalent to "etherStatsMulticastPkts"		Use Ctr. # 10
	aBroadcastFramesReceivedOK	RX	Broadcast packets, good only. Equivalent to "etherStatsBroadcastPkts"		Use Ctr. # 9
45	aInRangeLengthErrors	RX	Packets of legal-length whose actual length is different from length/type field value.	32	1000011

Ctr. #	Counter Name (MIB Object Name)	Counter Definition			
		RX/ TX	Description	Size (Bits)	Register Address A[7:1]
46	aOutofRangeLengthField	RX	Packets with length/type field value > Max_Packet_Length.	32	1000100
	aFrameTooLongErrors	RX	Packets of length > Max_Packet_Length with no other errors. Equivalent to “etherStatsOversizePkts”		Use Ctr. # 4
47	aSymbolErrorDuringCarrier	RX	CRS asserted and one or more symbol errors (RXER pin asserted) received from a PHY, exclusive of collision.	32	1000101
48	aPauseMACCtrlFramesTransmitted	TX	Valid MAC Control packets with Pause opcode.	32	1000110
49	aPauseMACCtrlFramesReceived	RX	Valid MAC Control packets with Pause opcode.	32	1000111
	aMACControlFramesTransmitted	TX	Valid MAC Control packets. Equivalent to “aPauseMACCtrlFrames Transmitted"		Use Ctr. # 48
	aMACControlFramesReceived	RX	Valid MAC Control packets. Equivalent to “aPauseMACCtrlFrames Received”		Use Ctr. # 49
50	aUnsupportedOpcodesReceived	RX	Valid MAC Control packets with non-Pause opcode.	32	1001000
51	aSQETESTErrors	RX	Number of times SQE was detected.	32	1001001
Ethernet-Like MIB (RFC 1643)					
	dot3StatsSingleCollisionFrames	TX	Packets successfully transmitted after one and only one collision (i.e.: attempt value=2). Equivalent to “aSingleCollisionFrames”		Use Ctr. # 34
	dot3StatsMultipleCollisionFrames	TX	Packets successfully transmitted after more than one collision (i.e.: 2<attempt value<16). Equivalent to “aMultipleCollisionFrames”		Use Ctr. # 35
	dot3StatsFCSErrors	RX	Packets with CRC error only. Equivalent to “aFrameCheckSequenceErrors”		Use Ctr. # 36
	dot3StatsAlignment Errors	RX	Packets with alignment error only. Equivalent to “aAlignmentErrors”		Use Ctr. # 37
	dot3DeferredTransmissions	TX	Packets deferred, i.e. packets whose transmission was delayed due to busy medium, on first attempt only. This does not include collisions. Equivalent to “aFramesWithDeferredXmissions”		Use Ctr. # 39
	dot3StatsLateCollisions	TX	Packets that encounter a late collision, i.e. encountered collisions more than 512 bit times into transmitted packet. A late collision is counted twice, as a collision and a late collision. Equivalent to “aLateCollisions”		Use Ctr. # 40

Ctr. #	Counter Name (MIB Object Name)	Counter Definition			
		RX/ TX	Description	Size (Bits)	Register Address A[7:1]
	dot3StatsExcessiveCollisions	TX	Packets not successfully transmitted after more than 15 collisions (i.e.: attempt value=16). Equivalent to "aFrameAbortedDueToXSCollisions"		Use Ctr. # 41
	dot3StatsInternalMACTransmitErrors	TX	Packets with transmit FIFO underflow error. Equivalent to "aFrameAbortedDueToIntMACXmitError"		Use Ctr. # 28
	dot3StatsCarrierSenseErrors	TX	Carrier sense dropout errors, i.e. number of times that carrier sense is not asserted or deasserted during packet transmission, without a collision. Equivalent to "aCarrierSenseErrors"		Use Ctr. # 42
	dot3StatsInternalMACReceiveErrors	RX	Packets with receive FIFO overflow error. Equivalent to "aFramesLostDueToIntMACRcvrError"		Use Ctr. # 1
	dot3StatsFrameTooLongs	RX	Packets of length > Max_Packet_Length with no other errors. Equivalent to "aFrameTooLongErrors"		Use Ctr. # 4
	dot3StatsSQETESTErrors	RX	Number of times SQE was detected. Equivalent to "aSQETESTErrors"		Use Ctr. # 51

Notes:

1. Bad RX packet = legal-length error, CRC error , alignment error.
   CRC Error is bad FCS with an integral number of octets.
   Alignment Error is bad FCS with non-integral number of octets.
2. Bad TX packet = legal length error , carrier sense dropout error, late collision, excess collision, transmit FIFO underflow
3. Legal-length packet is between 64 and Max_Packet_Length in bytes. Preamble is not included in length count.
4. Max_Packet_Length defaults to 1518 bytes but can be programmed to any value from 1518-1533 bytes.
5. All TX packet counts include retries, unless specifically excluded.
6. RMON specs literally state that packet and octet counters should only tabulate received information. This is sometimes interpreted to mean both transmitted and received information because Ethernet was originally a shared media protocol. As such, transmit packet and octet counters are also available in counters #17-26 and can be summed with the receive packet and octet counts if desired.

REGISTER INTERFACE

General

The Register Interface is a selectable 8/16-bit bidirectional data interface that allows access to the internal registers.

Timing

The Register Interface consists of thirty seven signals: sixteen bidirectional data I/O pins (CDST[15:0]), eight register address inputs (A[7:0]), one chip select input ($\overline{ENREGIO}$), one read select input ($\overline{RD}$), one write select input ($\overline{WR}$), two port select inputs (REGPS[1:0], one bus size select input (BUSSIZE), two byte enable inputs (BE[1:0]), one data ready output (READY), and four interrupt outputs, one per port (INT_[1:4]).

To access a register through the Register Interface, $\overline{ENREGIO}$ must first be asserted active low. Then either $\overline{RD}$ or $\overline{WR}$ needs to be asserted active low, and which signal is asserted will determine whether this is a read or write cycle. On that same falling edge of either $\overline{RD}$ or $\overline{WR}$, the address of the register that will be accessed needs to be present on A[7:0], and the port to be selected must be present on REGPS[1:0]. If the cycle is a write cycle ($\overline{WR}$ asserted), then the data on CDST[15:0] will be written to the designated register. If the cycle is a read cycle ($\overline{RD}$ asserted), then data from the designated register will be output on CDST[15:0] after some delay after the falling edge of $\overline{RD}$. The READY output will then go active high to indicate that the data on CDST[15:0] is valid. READY will stay high as long as $\overline{RD}$ is asserted, and return low after $\overline{RD}$ is deasserted. READY is placed in high impedance state when $\overline{ENREGIO}$ is deasserted and driven when $\overline{ENREGIO}$ is asserted. $\overline{ENREGIO}$ can remain low for multiple read or write cycles so that many registers can be read or written to in one $\overline{ENREGIO}$ assertion.

Bus Width

The bus width of the Register Interface can be selected to be either 8 or 16-bits wide by appropriately setting the BUSSIZE pin.

When the bus width is set to 8-bits wide (BUSSIZE=0), all registers have a unique address as determined by the A[7:0] pins, as shown in Table 15. To read out the 32-bit counter result over the 8-bit Register Interface bus, four successive reads on the same address will have to be done to output all 4 bytes of the 32-bit result. The first 8-bit word that is read out contains the upper 8-bits of the counter result (MS byte), and the fourth 8-bit contains the lowest 8-bits (LS byte). Note that when the bus width is set to 8-bit wide, the byte enables inputs on $\overline{BE[3:0]}$ are ignored.

When the bus width is set to 16-bits wide (BUSSIZE=1), the address pin A0 is ignored, and all registers have a unique address determined by A[7:1], as shown in Table 15. To read out the 32-bit counter result over the 16-bit Register Interface bus, two successive reads on the same address will have to be done to output all 2 double words of the 32-bit result. The first 16-bit word that is read out contains the upper 16-bits of the counter result (MS word), and the last 16-bit contains the lower 16-bits (LS word). Note that when the bus width is set to 16-bit wide, the A0 address input is ignored.

The Byte Enable pins, $\overline{BE[1:0]}$, control which byte of the 16-bit word is accessed when the Register Interface is configured for 16-bit bus width. The Byte Enable pins are ignored when the Register Interface is configured to be 8-bits.

Bit Types

The Register Interface is bidirectional, and there are many types of bits in the registers. Write bits (W) are inputs during a write cycle and are logic 0 during a read cycle. Read bits (R) are outputs during a read cycle and are high impedance and ignored during a write cycle. Read/Write bits (R/W) are actually write bits which can be read out during a read cycle. R/LH bits are read bits that latch themselves when they go high, and they stay latched high until read. After they are read, they are cleared low. R/LHI bits are the same as R/LH bits except that they also assert

interrupt when they latch high. Some of the R/LHI bits can also be programmed to not assert, or mask, the interrupt function. This is described in more detail in the Interrupt section. The bit type definitions are summarized in Table 12.

Table 12. Register Bit Type Definition

Sym.	Name	Definition	
		Write Cycle	Read Cycle
W	Write	Input	No Operation, 0's
R	Read	No Operation, Hi Z	Output
R/W	Read/ Write	Input	Ouput
R/LH	Read/ Latching High	No Operation, Hi Z	Output When Bit Goes High, Bit Latched. When Bit Is Read, Bit Updated.
R/LHI	Read/ Latching High With Interrupt	No Operation, Hi Z	Output When Bit Goes High Bit Latched And Interrupt Asserted (If Not Masked) When Bit Is Read, Bit Updated And Interrupt Cleared

Interrupt

An interrupt is triggered when certain output status bits are set. These bits are called interrupt bits and are designated as R/LHI bits as described in the previous section. When R/LHI or interrupt bits are set high, they stay latched high until read and the interrupt pin for that port is asserted. When interrupt bits are read, they are cleared low and the interrupt pin for that port is deasserted (provided there are no other interrupt bits set. All of the interrupt bits can be enabled or disabled, some individually. Disabling (also referred to as masking) an interrupt bit prevents that interrupt bit from causing an interrupt for that port. Table 13 lists all the bits that assert interrupt and the their associated disable/mask bits.

Table 13. Interrupt Bit vs. Corresponding Enable/Disable Bit

Interrupt Bit		Corresponding Interrupt Enable/Disable Bit	
Name	**Location**	**Name**	**Location**
MISTS	MI Command/ Status 1	INT_MISTS	MI Command/ Status 1
CSTS[0:7]	Counter Status 1-7	INT_CSTS [0:7]	Counter Interrupt Enable 1-7
OVF	RX Status	INT_RXDIS	Configuration 1
CRC	RX Status	INT_RXDIS	Configuration 1
USIZE	RX Status	INT_RXDIS	Configuration 1
OSIZE	RX Status	INT_RXDIS	Configuration 1
GOOD_RX	RX Status	INT_RX	RX Command
		INT_RXDIS	Configuration 1
12BYTES	RX Status	INT_12BYTE	RX Command
		INT_RXDIS	Configuration 1
RXUPDATE	RX Status	INT_RXDIS	Configuration 1
UNF	TX Status	INT_UNF	TX Command
COL	TX Status	INT_COL	TX Command
COL_16	TX Status	INT_TXERR	TX Command
GOOD_TX	TX Status	INT_TX	TX Command
CSN	TX Status	INT_TXERR	TX Command
COL_LATE	TX Status	INT_TXERR	TX Command

Register Structure

As stated previously, the device has both 8-bit wide, and 32-bit wide internal registers and the bus can be configured to be either 8 or 16-bits wide. The name and location of all registers is described in Table 15. The definition of each bit in each register is described in Tables 16-37.

Table 15. Register Address Table (Per Port)

Register Address A[7:1]	Register Name	
	BUSSIZE = 1, $\overline{BE[1:0]}$ = 00 [1]	
	BUSSIZE = 1, $\overline{BE[1:0]}$ = 01 [1]	**BUSSIZE = 1, $\overline{BE[1:0]}$ = 10** [1]
	BUSSIZE = 0, A0 = 1 [2]	**BUSSIZE = 0, A0 = 0** [2]
0000000	Station Address 1	Station Address 0
0000001	Station Address 3	Station Address 2
0000010	Station Address 5	Station Address 4
0000011	TX Command	RX Command
0000100	Hash Filter 1	Hash Filter 0
0000101	Hash Filter 3	Hash Filter 2
0000110	Hash Filter 5	Hash Filter 4
0000111	Hash Filter 7	Hash Filter 6
0001000	Transmit Defer	FIFO Threshold
0001001	Configuration 2	Configuration 1
0001010	Configuration 4	Configuration 3
0001011	Transmit Control/Product ID	Configuration 5
0001100	Flow Control PAUSE Time 1	Flow Control PAUSE Time 0
0001101	MI Data 1	MI Data 0
0001110	MI Command/Status 1	MI Command/Status 0
0001111	Counter Interrupt Enable 2	Counter Interrupt Enable 1
0010000	Counter Interrupt Enable 4	Counter Interrupt Enable 3
0010001	Counter Interrupt Enable 6	Counter Interrupt Enable 5
0010010	Counter Status 1	Counter Interrupt Enable 7
0010011	Counter Status 3	Counter Status 2
0010100	Counter Status 5	Counter Status 4
0010101	Counter Status 7	Counter Status 6
0010110	TX Status	RX Status
0010111	Counter 1 - etherStatsDropEvents	
0011000	Counter 2 - etherStatsCRCAlignErrors	
0011001	Counter 3 - etherStatsUndersizePkts	
0011010	Counter 4 - etherStatsOversizePkts	
0011011	Counter 5 - etherStatsFragments	
0011100	Counter 6 - etherStatsJabber	
0011101	Counter 7 - etherStatsOctets	
0011110	Counter 8 - etherStatsPkts	
0011111	Counter 9 - etherStatsBroadcastPkts	
0100000	Counter 10 - etherStatsMulticastPkts	
0100001	Counter 11 - etherStatsPkts64Octets	

Register Address A[7:1]	Register Name	
	BUSSIZE = 1, $\overline{\text{BE[1:0]}}$ = 00 [1]	
	BUSSIZE = 1, $\overline{\text{BE[1:0]}}$ = 01 [1]	**BUSSIZE = 1, $\overline{\text{BE[1:0]}}$ = 10** [1]
	BUSSIZE = 0, A0 = 1 [2]	**BUSSIZE = 0, A0 = 0** [2]
0100010	Counter 12 - etherStatsPkts65to127Octets	
0100011	Counter 13 - etherStatsPkts128to255Octets	
0100100	Counter 14 - etherStatsPkts256to511Octets	
0100101	Counter 15 - etherStatsPkts512to1023Octets	
0100110	Counter 16 - etherStatsPkts1024to1518Octets	
0100111	Counter 17 - etherStatsOctets_TX	
0101000	Counter 18 - etherStatsPkts_TX	
0101001	Counter 19 - etherStatsBroadcastPkts_TX	
0101010	Counter 20 - etherStatsMulticastPkts_TX	
0101011	Counter 21 - etherStatsPkts64Octets_TX	
0101100	Counter 22 - etherStatsPkts65to127Octets_TX	
0101101	Counter 23 - etherStatsPkts128to255Octets_TX	
0101110	Counter 24 - etherStatsPkts256to511Octets_TX	
0101111	Counter 25 - etherStatsPkts512to1023Octets_TX	
0110000	Counter 26 - etherStatsPkts1024to1518Octets_TX	
0110001	Counter 27 - etherStatsCollisions	
0110010	Counter 28 - ifOutDiscards	
0110011	Counter 29 - ifOutErrors	
0110100	Counter 30 - ifInOctets	
0110101	Counter 31 - ifOutOctets	
0110110	Counter 32 - ifInUcastPkts	
0110111	Counter 33 - ifOutUcastPkts	
0111000	Counter 34 - aSingleCollisionFrames	
0111001	Counter 35 - aMultipleCollisionFrames	
0111010	Counter 36 - aFrameCheckSequenceErrors	
0111011	Counter 37 - aAlignmentErrors	
0111100	Counter 38 - aOctetsTransmittedOK	
0111101	Counter 39 - aFramesWithDeferredXmissions	
0111110	Counter 40 - aLateCollisions	
0111111	Counter 41 - aFramesAbortedDueToXSCollisions	
1000000	Counter 42 - aCarrierSenseErrors	

Register Address A[7:1]	Register Name	
	BUSSIZE = 1, $\overline{\text{BE[1:0]}}$ = 00 [1]	
	BUSSIZE = 1, $\overline{\text{BE[1:0]}}$ = 01 [1]	**BUSSIZE = 1, $\overline{\text{BE[1:0]}}$ = 10** [1]
	BUSSIZE = 0, A0 = 1 [2]	**BUSSIZE = 0, A0 = 0** [2]
1000001	Counter 43 - aOctetsReceivedOK	
1000010	Counter 44 - aFramesWithExcessiveDefferal	
1000011	Counter 45 - aInRangeLengthErrors	
1000100	Counter 46 - aOutofRangeLengthField	
1000101	Counter 47 - aSymbolErrorDuringCarrier	
1000110	Counter 48 - aPauseMACCtrlFramesTransmitted	
1000111	Counter 49 - aPauseMACCtrlFramesReceived	
1001000	Counter 50 - aUnsupportedOpcodesReceived	
1001001	Counter 51 - aSQETESTErrors	
1001010	Reserved	Miscellaneous Status
1001011 thru 1111111	Reserved	

[1] When BUSSIZE = 1, A0 = don’t care

[2] When BUSSIZE = 0, $\overline{\text{BE[1:0]}}$ = don’t care

Table 16. Station Address 0-5 Register Definition

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7	A7	Station Address	These six registers contain the 48-Bit MAC Station Address. A0 in Station Address 0 Register corresponds to the first MAC address bit received in the data stream on the System Interface (shown as DA[0] in Figure 4); A7 in Station Address 5 Register corresponds to the last address bit received The Station Address is used for (1) receive unicast address matching against the incoming DA, and (2) automatic MAC Control Pause frame generation.	R/W	0
6	A6				0
5	A5				0
4	A4				0
3	A3				0
2	A2				0
1	A1				0
0	A0				0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 17. RX Command Register Definition

7	6	5	4	3	2	1	0
ADDR1	ADDR0	INT_RX	INT_12BYTE	ACPT_USIZE	ACPT_OSIZE	ACPT_CRC	ACPT_OVF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7 6	ADDR1 ADDR0	Receive Address Matching Select	11 = Receiver Accepts Frames Where DA Matches: (1) Station Address (2) Any Broadcast Address (3) Multicast Address That Passes Hash Filter 10 = Receiver Accepts Frames Where DA Matches: (1) Station Address (2) Any Broadcast Address 01 = Receiver Accepts All Frames 00 = Receiver Rejects All Frames	R/W	0 0
5	INT_RX	Good RX Packet Interrupt Enable	1 = Inerrupt Generated When Good Packet Received, i.e Packet Had no Errors 0 = Not Generated	R/W	0
4	INT_12BYTE	12 Bytes Received Interrupt Enable	1 = Interrupt Generated After First 12 Bytes Received 0 = Not Generated	R/W	0
3	ACPT_USIZE	Undersize Packet Accept Enable	1 = Undersize Packets Accepted 0 = Not Accepted, RXDC Asserted When Detected	R/W	0
2	ACPT_OSIZE	Oversize Packet Accept Enable	1 = Oversize Packets Accepted 0 = Not Accepted, RXDC Asserted When Detected	R/W	0
1	ACPT_CRC	CRC Error Accept Enable	1 = Packets with CRC Errors Accepted 0 = Not Accepted, RXDC Asserted When Detected	R/W	0
0	ACPT_OVF	RX FIFO Overflow Accept Enable	1 = Packets that Overflow RX FIFO Accepted 0 = Not Accepted, RXDC Asserted When Detected	R/W	0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 18. TX Command Register Definition

7	6	5	4	3	2	1	0
TEST	0	0	PHYINTF	INT_TX	INT_TXERR	INT_COL	INT_UNF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7	TEST	Test Mode	Reserved for Factory Test, Must Remain at Default Value or be Written to 0 for Proper Operation	R/W	0
6 5			Reserved, Must Always Remain at Default or Written to 0 for Proper Operation	R/W	0 0
4	PHYINTF	PHY Interface Select	1 = Interface to External PHY is MII 0 = Interface to External PHY is 10 Mbps Serial	R/W	0
3	INT_TX	Good TX Packet Interrupt Enable	1 = Interrupt Generated When Good Packet Has Been Successfully Transmitted 0 = Not Generated	R/W	0
2	INT_TXERR	TX Error Interrupt Enable	1 = Interrupt Generated When Transmit Error Occurs (16 Collisions, Late Collisions, or CSN Error) 0 = Not Generated	R/W	0
1	INT_COL	Collision Interrupt Enable	1 = Interrupt Generated When a Collision Occurs 0 = Not Generated	R/W	0
0	INT_UNF	TX FIFO Underflow Interrupt Enable	1 = Interrupt Generated When TX FIFO Underflow Detected 0 = Not Generated	R/W	0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 19. Hash Filter 0-7 Register Definition

7	6	5	4	3	2	1	0
F7	F6	F5	F4	F3	F2	F1	F0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7	F7	Hash Filter	These eight registers contain 64-bits that are used by the receive hash filter. The receive Hash Filter is used for filtering the Destination Address on Multicast Packets. Refer to the Multicast Address Filter section for more details about the hash filter function and what these bits represent.	R/W	0
6	F6				0
5	F5				0
4	F4				0
3	F3				0
2	F2				0
1	F1				0
0	F0				0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 20. Transmit Defer Register Definition

7	6	5	4	3	2	1	0
DEFER7	DEFER6	DEFER5	DEFER4	DEFER3	DEFER2	DEFER1	DEFER0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7	DEFER7		This register contains an 8-bit number that is used by the Transmit MAC to calculate the minimum interpacket gap. Refer to the Transmit MAC, Interpacket Gap section for more details. Bit 0 is the LSB.	R/W	0
6	DEFER6				0
5	DEFER5				0
4	DEFER4				0
3	DEFER3				0
2	DEFER2				0
1	DEFER1				0
0	DEFER0				0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 21. FIFO Threshold Register Definition

7	6	5	4	3	2	1	0
RXTHR3	RXTHR2	RXTHR1	RXTHR0	TXTHR3	TXTHR2	TXTHR1	TXTHR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7 6 5 4	RXTHR3 RXTHR2 RXTHR1 RXTHR0	RX FIFO Threshold Settings	These bits set the threshold in the RX FIFO which cause RXRDY to be asserted when the amount of data in the RX FIFO is greater than or equal to the threshold below: 1111 = 30 Double Words of Data in RX FIFO 1110 = 28 . . . 1101 = 26 . . . 1100 = 24 . . . 1011 = 22 . . . 1010 = 20 . . . 1001 = 18 . . . 1000 = 16 . . . 0111 = 14 . . . 0110 = 12 . . . 0101 = 10 . . . 0100 = 8 . . . 0011 = 6 . . . 0010 = 4 . . . 0001 = 2 . . . 0000 = 1 . . .	R/W	0 0 0 0
3 2 1 0	TXTHR3 TXTHR2 TXTHR1 TXTHR0	TX FIFO Threshold Settings	These bits set the threshold in the TX FIFO which cause TXRDY to be asserted when the amount of space in the TX FIFO is greater than or equal to the threshold below: 1111 = 30 Double Words of Space in TX FIFO 1110 = 28 . . . 1101 = 26 . . . 1100 = 24 . . . 1011 = 22 . . . 1010 = 20 . . . 1001 = 18 . . . 1000 = 16 . . . 0111 = 14 . . . 0110 = 12 . . . 0101 = 10 . . . 0100 = 8 . . . 0011 = 6 . . . 0010 = 4 . . . 0001 = 2 . . . 0000 = 1 . . .	R/W	0 0 0 0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 22. Configuration 1 Register Definition

7	6	5	4	3	2	1	0
INT_RXDIS	RXCRC	FDX	TXCRC_DIS	ROWNT	TXPRE_DIS	AUTOPAD	GRPADR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7	INT_RXDIS	Receive Interrupt Disable	1 = Receive Interrupts Disabled, i.e. No Interrupts Are Produced By a Port's Receiver 0 = Enabled	R/W	0
6	RXCRC	Receive CRC Enable	1 = CRC is Not Stripped Off of Receive Packet and is Loaded into RX FIFO Along With Data 0 = CRC Stripped Off	R/W	0
5	FDX	Full Duplex Enable	1 = Full Duplex 0 = Half Duplex Full Duplex Mode is Enabled if Either this Bit Is Set to 1 or FDUPLX Pin is Low as shown in Table 9.	R/W	0
4	TXCRC_DIS	Transmit CRC Disable	1 = CRC Not Appended to End of Transmit Packet 0 = CRC Appended CRC is Disabled if Either this Bit is Set to 1 or if the TXNOCRC pin is Low as shown in Table 3.	R/W	0
3	ROWNT	Receive Own Transmit Ignore Select	1 = Ignore Any Packet Received While a Packet is Being Transmitted 0 = Do Not Ignore	R/W	0
2	TXPRE_DIS	Transmit Preamble Disable	1 = Preamble Not Added to Beginning of TX Packet 0 = Preamble Added	R/W	0
1	AUTOPAD	AutoPad Enable	1 = All Undersize Xmt Packets Padded to 64 Bytes 0 = No Padding	R/W	0
0	GRPADR	Group Address Mode Enable	1 = Group Address Mode Enabled, i.e. Ignore Last 4 Bits of Receive Destination Address (DA) when Comparing Unicast DA to Station Address 0 = Disabled	R/W	0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 23. Configuration 2 Register Definition

7	6	5	4	3	2	1	0
TXRDY	0	ENDIAN	RXAB_DIS	HASH	PEOF	TXOFF	TXSTS_DIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7	TXRDY	TXRDY Function Select	1 = TXRDY Deasserted When EOF Written Into TX FIFO & Stays Deasserted Until Pkt Transmitted. TXRDY Also Deasserted by Threshold Limit. 0 = TXRDY Deasserted by TX FIFO Threshold only	R/W	0
6			Reserved. Must always be left at Default or Written to 0 for Proper Operation	R/W	0
5	ENDIAN	Endian Select	1 = RXTXDATA[31:0] in Big Endian Format 0 = RXTXDATA[31:0] in Little Endian Format	R/W	0
4	RXAB_DIS	RXABORT Pin Disable	1 = RXABORT Pin Disabled, i.e. Receive Pkts Are Not Discarded When RXABORT Pin Asserted 0 = RXABORT Pin Enabled	R/W	0
3	HASH	Receive Hash Filter Enable	1 = Receive Hash Filter On for Multicast Operation 0 = Hash Filter Off	R/W	0
2	PEOF	Receive EOF Position Select	1 = Receive EOF Occurs at End of Packet Data and on Status Word 0 = Receive EOF Occurs on Status Word	R/W	0
1	TXOFF	Transmit Off When Status Full	1 = No More Packets Transmitted if Both TX Status Registers are Full 0 = Transmit Operation not Affected by TX Status Registers	R/W	0
0	TXSTS_DIS	Transmit Status Disable	1 = TX Status Disabled, i.e. TX Packet Status Will Not be Loaded into Either of the Two Internal TX Status Registers 0 = TX Status Enabled	R/W	0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 24. Configuration 3 Register Definition

7	6	5	4	3	2	1	0
CTRROLL	CTRRD	TXSTS_COL	BOFFRST	ROWNT_OR	0	SWRD_DIS	BIDIRBE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7	CTRROLL	Counter Rollover Stop Enable	1 = Counters Stop at Maximum Count 0 = Counters Rollover to 0 After Maximum Count	R/W	0
6	CTRRD	Counter Reset On Read Enable	1 = Counters Reset to 0 When Read (or 1 if a Count Occurred During Read) 0 = No Reset On Read	R/W	0
5	TXSTS_COL	Transmit Status Disable On Collision	1 = Transmit Status Register not updated if Collision Occurs While Packet is Being Transmitted 0 = Updated	R/W	0
4	BOFFRST	Backoff Counter Reset	1 = Normal 0 = Reset the Polynomial Counter Used by the Transmitter to Randomize the Backoff Interval Upon Collision.	R/W	0
3	ROWNT_OR	ROWNT Override Select	1 = ROWNT Bit (Bit 3, Config. 1 Reg.) is Forced to "0" When Device is Put in Full Duplex Mode 0 = Not Forced	R/W	0
2			Reserved, Must Always Remain at Default be Written to 0 for Proper Operation	R/W	0
1	SWRD_DIS	Status Word Disable	1 = Status Word Not Appended to End of Receive Packet 0 = Status Word Appended	R/W	0
0	BIDIRBE	Bidirectional Byte Enable Select	1 = $\overline{\text{TXRXBE[3:0]}}$ Pins are Bidirectional, i.e. Inputs During TX FIFO Writes and Outputs During RX FIFO Reads. 0 = $\overline{\text{TXRXBE[3:0]}}$ Pins are Always Inputs, i.e. Inputs During TX FIFO Writes and Inputs During RX FIFO Reads.	R/W	0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 25. Configuration 4 Register Definition

7	6	5	4	3	2	1	0
CTRPKTSIZE	CTRRST	DATARST	MCENDPS	MCPASS1	MCPASS0	MCFLTR	MC_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7	CTRPKTSIZE	Counter Maximum Packet Size Select	1 = Maximum Packet Size for Counters is Determined by Bits 0-3 in Configuration 5 Reg. 0 = Maximum Packet Size for Counters is 1518 Byte	R/W	0
6	CTRRST	Counter Reset	1 = All Counters Reset to 0, 0 = No Reset	R/W	1
5	DATARST	Data Path Reset	1 = Reset TX/RX Data Paths and TX/RX FIFO's 0 = Normal	R/W	1
4	MCENDPS	MAC Control Frame End Pause Enable	1 = When FNCTRL Deasserted, Send Transmit MAC Control Frame With pause_time=0 0 = Normal	R/W	1
3 2	MCPASS0 MCPASS1	MAC Control Frame Passthrough Enable	11 = Reserved 10 = Valid MAC Control Frames That Have nonPause Opcode are Passed Thru to RX FIFO 01 = Valid MAC Control Frames That Have Any Opcode are Passed Thru to RX FIFO 00 = MAC Control Frames are Not Passed Thru to RX FIFO	R/W	0 0
1	MCFLTR	MAC Control Frame Address Filter Enable	1 = Use Any Address as the DA to Determine MAC Control Pause Frame Validity 0 = Use Reserved Multicast Address or Station Address as the DA To Determine MAC Control Pause Frame Validity	R/W	0
0	MC_EN	MAC Control Frame Enable	1 = Valid Receive MAC Control Frames Cause Transmitter To Pause (Enabled) 0 = Transmitter Not Paused (Disabled)	R/W	1

Bit 0 Occurs On CDST0/CDST8 Pin

Table 26. Configuration 5 Register Definition

7	6	5	4	3	2	1	0
0	0	0	0	MAXPKT3	MAXPKT2	MAXPKT1	MXPKT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7 6 5 4			Reserved, Must Always Remain at Default or Written to 0 for Proper Operation	R/W	0 0 0 0
3 2 1 0	MAXPKT3 MAXPKT2 MAXPKT1 MAXPKT0	Maximum Packet Size Select	These Bits Determine the Maximum Packet Size for the MAC. These Bits Will Also Determine Maximum Packet Size for Counters if Bit 7 in Configuration 4 Register is set to 1. 1111 = 1533 Bytes 1110 = 1532 Bytes . . . . . . 0010 = 1520 Bytes 0001 = 1519 Bytes 0000 = 1518 Bytes	R/W	0 0 0 0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 27. Transmit Control/Product ID Register Definition

7	6	5	4	3	2	1	0
ID3	ID2	ID1	ID0	TXCTRL3	TXCTRL2	TXCTRL1	TXCTRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7 6 5 4	ID3 ID2 ID1 ID0	Product ID	This register contains a revision identification number which is unique for each device revision.	R/W	— — — —
3 2 1 0	TXCTRL3 TXCTRL2 TXCTRL1 TXCTRL0	Transmit Control Threshold	These Bits Determine the Transmit Control Threshold. When the data in the TX FIFO exceeds this threshold, data is sent to the MAC for transmission out of the device. 1111 = Transmit Starts when 30 Double Word in FIFO 1110 = . 28 . 1101 = . 26 . 1100 = 24 . 1011 = 22 . 1010 = 20 . 1001 = 18 . 1000 = 16 . 0111 = . 14 . 0110 = 12 . 0101 = 10 . 0100 = . 8 . 0011 = 6 . 0010 = . 4 . 0001 = . 2 . 0000 = 1	R/W	0 0 0 0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 28. Flow Control Pause Time 0-1 Register Definition

7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7 6 5 4 3 2 1 0	P7 P6 P5 P4 P3 P2 P1 P0	Pause Time	These two registers contain the 16-bit word that is inserted into the pause_time parameter field of all autogenerated transmit MAC Control Pause frames. Upon successful reception of these autogenerated Pause frames, a remote device will not transmit data for a time interval equal to the decimal value of this register times 512 bit times (100 Mbps bit time=10nS, 10 Mbps bit time=100nS) Bit 0 of Register 0 corresponds to the LSB of the pause_time paramter. Bit 7 of Register 1 corresponds to the MSB of the pause_time parameter. The MSByte and LSBit of the pause_time parameter is transmitted first, as shown in Figure 7. A value of 32_H is internally added to this word. Any pause_time Value <=32_H Will Be Sent As 32_H.	R/W	0 0 0 0 0 0 0 0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 29. MI Data Register 0-1 Register Definition

7	6	5	4	3	2	1	0
MDIO7	MDIO6	MDIO5	MDIO4	MDIO3	MDIO2	MDIO1	MDIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7	MDIO7	MDIO Data	These two registers contain the 16-bit data portion of the 32-bit MI word that is either written to or read from an external PHY over the MDIO bidirectional I/O pin. Bit 7 of Register 1 corresponds to the first bit transmitted/received on MDIO of the data word portion of the 32-bit MI word; Bit 0 of Register 0 is the last bit transmitted/received.	R/W	0
6	MDIO6				0
5	MDIO5				0
4	MDIO4				0
3	MDIO3				0
2	MDIO2				0
1	MDIO1				0
0	MDIO0				0
					0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 30. MI Command/Status 0 Register Definition

7	6	5	4	3	2	1	0
MDCPER2	MDCPER1	MDCPER0	REGAD4	REGAD3	REGAD2	REGAD1	REGAD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7 6 5	MDCPER2 MDCPER1 MDCPER0	MDC Clock Period Select	These 3 bits determine the period of the MDC clock to the external PHY according to the formula: MDC Period = (SCLK Period) x 2 x (MDCPER[2:0] +1)	R/W	1 1 1
4 3 2 1 0	REGAD4 REGAD3 REGAD2 REGAD1 REGAD0	PHY Register Address Select	These 5 bits contain the address of the register to be accessed in the external PHY. REGAD0 corresponds the register address LSB and is transmitted last.	R/W	0 0 0 0 0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 31. MI Command/Status 1 Register Definition

7	6	5	4	3	2	1	0
MISTS	INT_MISTS	MIRW	PHYAD4	PHYAD3	PHYAD2	PHYAD1	PHYAD0
R/LHI	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7	MISTS	MI Status	1 = MI Write/Read Cycle Completed 0 = Not Complete	R/LHI	0
6	INT_MISTS	MI Read/Write Interrupt Enable	1 = Interrupt Enabled at Completion of MI Write/Read Cycle 0 = Not Enabled	R/W	0
5	MIRW	MI Read/Write Select	1 = MI Write Cycle 0 = MI Read Cycle	R/W	0
4 3 2 1 0	PHYAD4 PHYAD3 PHYAD2 PHYAD1 PHYAD0	PHY Register Address Select	These 5 bits contain the physical device address of the external PHY. PHYAD0 corresponds the physical device address LSB and is transmitted last.	R/W	0 0 0 0 0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 32. Counter Interrupt Enable 1-7 Register Definition

7	6	5	4	3	2	1	0
INT_CSTS7	INT_CSTS6	INT_CSTS5	INT_CSTS4	INT_CSTS3	INT_CSTS2	INT_CSTS1	INT_CSTS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7 6 5 4 3 2 1 0	INT_CSTS7 INT_CSTS6 INT_CSTS5 INT_CSTS4 INT_CSTS3 INT_CSTS2 INT_CSTS1 INT_CSTS0	Counter Status Interrupt Enable	These seven registers contain 51 counter interrupt enable bits. The counter interrupt enable bits determine whether the counter status bits cause the assertion of an interrupt for that port. Each bit corresponds to one of the 51 counters and its associated counter status bit. Bit 0 of Register 1 corresponds to Counter 1 as defined in Table 15; Bit 2 of Register 7 corresponds to Counter 51. 1 = Interrupt Asserted When Specific Counter Status Bit is Set, i.e. Interrupt Asserted when Counter Reaches a Count of 80000000_H. 0 = Interrupt Disabled for Specific Counter	R/W	0 0 0 0 0 0 0 0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 33. Counter Status 1-7 Register Definition

7	6	5	4	3	2	1	0
CSTS7	CSTS6	CSTS5	CSTS4	CSTS3	CSTS2	CSTS1	CSTS0
R/LHI	R/LHI	R/LHI	R/LHI	R/LHI	R/LHI	R/LHI	R/LHI

Bit	Symbol	Name	Definition	R/W	Def.
7	CSTS7	Counter Status	These seven registers contain 51 counter status bits. The counter status bits indicate when a counter is half full. Each bit corresponds to one of the 51 counters. Bit 0 of Register 1 corresponds to Counter 1 as defined in Table 15; Bit 2 of Register 7 corresponds to Counter 51. 1 = Counter Has Reached a Count of 80000000_H, i.e. Half Full. 0 = Count < 80000000_H.	R/LHI	0
6	CSTS6				0
5	CSTS5				0
4	CSTS4				0
3	CSTS3				0
2	CSTS2				0
1	CSTS1				0
0	CSTS0				0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 34. RX Status Register Definition

7	6	5	4	3	2	1	0
RXUPDATE	12BYTES	GOOD_RX	OSIZE	USIZE	DRIBBLE	CRC	OVF
R/LH	R/LHI	R/LHI	R/LHI	R/LHI	R/LH	R/LHI	R/LH

Bit	Symbol	Name	Definition	R/W	Def.
7	RXUPDATE	Receive Status Updated	1 = Status Has Not Been Updated Since Last Read 0 = Updated	R/LH	1
6	12BYTES	First 12 Bytes Detect	1 = First 12 Bytes of the Packet Have Been Received 0 = Not Received	R/LHI	0
5	GOOD_RX	Good Receive Packet Detect	1 = Receive Packet was Good, i.e. Had No Errors 0 = No Good	R/LHI	0
4	OSIZE	Oversize Packet Detect	1 = Receive Packet Was Oversize 0 = No Error	R/LHI	0
3	USIZE	Undersize Packet Detect	1 = Receive Packet Was Undersize 0 = No Error	R/LHI	0
2	DRIBBLE	Dribble Error Detect	1 = Receive Packet Had Dribble Bits or Nibbles 0 = No Error	R/LH	0
1	CRC	CRC Error Detect	1 = Receive Packet Had CRC Error 0 = No Error	R/LHI	0
0	OVF	RX FIFO Overflow Detect	1 = Receive Packet Corrupted By RX FIFO Overflow 0 = No Error	R/LHI	0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 35. TX Status Register Definition

7	6	5	4	3	2	1	0
TXUPDATE	COL_LATE	DEFER	CSN	GOOD_TX	COL_16	COL	UNF
R/LH	R/LHI	R/LH	R/LHI	R/LHI	R/LHI	R/LHI	R/LHI

Bit	Symbol	Name	Definition	R/W	Def.
7	TXUPDATE	Transmit Status Updated	1 = Status Has Not Been Updated Since Last Read 0 = Updated Since the Last Read	R/LH	1
6	COL_LATE	Late Collision Error Detect	1 = Late Collision Occured While Packet Transmitted 0 = No Error	R/LHI	0
5	DEFER	Packet Defer Detect	1 = Transmission of Packet Was Deferred 0 = No Defer	R/LH	0
4	CSN	Carrier Sense Error Detect	1 = Carrier Sense Error Detected While Packet Was Being Transmitted 0 = No Error	R/LHI	0
3	GOOD_TX	Good Transmit Packet Detect	1 = Transmit Packet was Good, i.e. Successfully Transmitted Without Errors or Collisions 0 = No Good	R/LHI	0
2	COL_16	16 Collision Error Detect	1 = 16 or More Collisions Occured While the Packet was being Transmitted 0 = No Error	R/LHI	0
1	COL	Collision Detect	1 = One or More Collisions Occurred While the Packet was being Transmitted 0 = No Collision	R/LHI	0
0	UNF	TX FIFO Underflow Detect	1 = Packet Corrupted By TX FIFO Underflow Error 0 = No Error	R/LHI	0

Bit 0 Occurs On CDST0/CDST8 Pin

There are 2 TX Transmit Status Registers that store the Status of the Last Two Packets Transmitted when TXOFF = 1 in configuration 2 register. When TXOFF = 0, the two TX Status Registers contain the oldest and newest packet since the last read.

Table 36. Counter 1-51 Register Definition

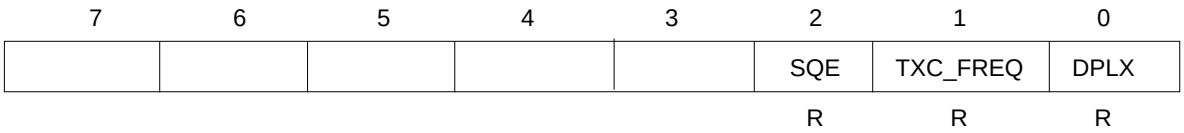
15	14	13	12	11	10	9	8
C15	C14	C13	C12	C11	C10	C9	C8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
15	C15	Counter	These fifty one registers contain the contents of the fifty one 32-bit management counters. Each register corresponds to a one specific counter. The register address and definition for each counter is shown in Table 11. The entire 32-bit word is obtained by doing two consecutive read operations from the same register address. The upper 16-bit word is outputted on the first read, the lower 16-bit word on the second read. C0 of the lower 16-bit word is the counter LSB.	R/W	0
14	C14				0
13	C13				0
12	C12				0
11	C11				0
10	C10				0
9	C9				0
8	C8				0
7	C7				0
6	C6				0
5	C5				0
4	C4				0
3	C3				0
2	C2				0
1	C1				0
0	C0				0

Bit 0 Occurs On CDST0/CDST8 Pin

Table 37. Miscellaneous Status Register Definition



Bit	Symbol	Name	Definition	R/W	Def.
7 thru 3			Reserved, Must be Written to 0 for Proper Operation		
2	SQE	SQE Detect	1 = SQE Pulses Detected from PHY Interface 0 = No Detect	R	0
1	TXC_FREQ	TXC Frequency Detect	1 = 2.5 MHz Clock Detected on TXC (10 Mbps) 0 = 25 MHz Clock Detected on TXC (100 Mbps)	R	0
0	DPLX	Duplex Status	1 = Device Has Been Placed in Full Duplex Mode 0 = Device Has Been Placed in Half Duplex Mode	R	0

Bit 0 Occurs On CDST0/CDST8 Pin

APPLICATION INFORMATION

EXAMPLE SCHEMATICS

A typical example of a switch port using the 84302 is shown in Figure 8.

MANAGEMENT COUNTERS

Relationship to IETF and IEEE Specs

The 84302 management counters provide the necessary statistics, on a per port basis, to completely support the following IETF and IEEE specifications:

(1) IETF RFC 1757: RMON Statistics Group
(2) IETF RFC 1213: SNMP Interfaces Group
(3) IETF RFC 1643: Ethernet-Like MIB
(4) IEEE 802.3/Cl. 30: Ethernet MIB

A complete list of the counters along with their definitions was already defined in Table 11. A map of the actual MIB objects from the above specifications to the specific counters on the 84302 is shown below in Tables 38-41.

TX Packet and Octet Counters

The 84302 counter set includes packet and octet counters for the transmit packets as well as receive. The RMON specs literally state that packet and octet counters should only tabulate received information. This is sometimes interpreted to mean both transmitted and received information because Ethernet was originally a shared media protocol. As such, the tables below only point to receive packet and octet counters, but the transmit packet and octet counters are also available in counters #17-26 and can be summed with the receive packet and octet counts if desired.

Figure 8. 100/10 Mbps Port Using the SEEQ 84302 and 80220

Table 38
MIB Objects vs. Counter Location
For RMON Statistics Group
(RFC 1757)

MIB Objects	Counter Location	
	Ctr. #	Register Address
etherStatsDropEvents	1	0010111
etherStatsOctets	7	0011101
etherStatsPkts	8	0011110
etherStatsBroadcastPkts	9	0011111
etherStatsMulticastPkts	10	0100000
etherStatsCRCAlignErrors	2	0011000
etherStatsUndersizePkts	3	0011001
etherStatsOversizePkts	4	0011010
etherStatsFragments	5	0011011
etherStatsJabber	6	0011100
etherStatsCollisions	27	0110001
etherStatsPkts64Octets	11	0100001
etherStatsPkts65to127Octets	12	0100010
etherStatsPkts128to255Octets	13	0100011
etherStatsPkts256to511Octets	14	0100100
etherStatsPkts512to1023Octets	15	0100101
etherStatsPkts1024to1518Octets	16	0100110

Table 39
MIB Objects vs. Counter Location
For SNMP Interfaces Group
(RFC 1573 & 1573)

MIB Objects	Counter Location	
	Ctr. #	Register Address
ifInOctets	30	0110100
ifInUcastPkts	32	0110110
ifInNUcastPkts	9 + 10	0011111 + 0100000
ifInDiscards	1	0010111
ifInErrors	2 + 3 + 4	0011000 + 0011001 + 0011010
ifOutOctets	31	0110101
ifOutUcastPkts	33	0110111
ifOutNUcastPkts	8 - 33	0011110 - 0110111
ifOutDiscards	28	0110010
ifOutErrors	29	0110011

POWER SUPPLY DECOUPLING

There are thirty three VDD's (VDD) and thirty six GND's (GND) on the 84302.

All VDD's should be connected together as close as possible to the device with a large VDD plane. If the VDD's vary in potential by even a small amount, noise and latchup can result. The VDD's should be kept to within 50 mV of each other.

All GND's should also be connected together as close as possible to the device with a large ground plane. If the GND's vary in potential by even a small amount, noise and latchup can result. The VDD's should be kept to within 50 mV of each other.

A 0.01-0.1uF decoupling capacitor should be connected between VDD and GND for every eight sets of VDD/GND placed as close as possible to the device pins, preferably within 0.5". The value should be chosen on whether the noise from VDD-GND is high or low frequency. A conservative approach would be to use two decoupling capacitors on each VDD/GND set, one 0.1uf for low frequency and one 0.001uf for high frequency noise on the power supply.

The PCB layout and power supply decoupling discussed above should provide sufficient decoupling to achieve the following when measured at the device: (1) The resultant AC noise voltage measured across each VDD/GND set should be less than 100 mVpp, (2) All VDD's should be within 50 mVpp of each other, and (3) All GND's should be within 50 mVpp of each other.

Table 40
MIB Objects vs. Counter Location
For Ethernet-Like MIB(RFC 1643)

MIB Objects	Counter Location	
	Ctr. #	Register Address
dot3StatsAlignmentErrors	37	0111011
dot3StatsFCSErrors	36	0111010
dot3StatsSingleCollisionFrames	34	0111000
dot3StatsMultipleCollisionFrames	35	0111001
dot3StatsSQETESTErrors	51	1001001
dot3DeferredTransmissions	39	0111101
dot3StatsLateCollisions	40	0111110
dot3StatsExcessiveCollisions	41	0111111
dot3StatsInternalMacTransmitErrors	28	0110010
dot3StatsCarrierSenseErrors	42	1000000
dot3StatsFrameTooLongs	4	0011010
dot3StatsInternalMacReceiveErrors	1	0010111

Table 41
MIB Objects vs. Counter Location
For Ethernet MIB
(IEEE 802.3 Clause 30)

MIB Objects	Counter Location	
	Ctr. #	Register Address
aFramesTransmittedOK	8 - 29	0011110-0110011
aSingleCollisionFrames	34	0111000
aMultipleCollisionFrames	35	0111001
aFramesReceivedOK	32+ 9+ 10	0110110+ 0011111+ 0100000
aFrameCheckSequenceErrors	36	0111010
aAlignmentErrors	37	0111011
aOctetsTransmittedOK	38	0111100
aFramesWithDeferredXmissions	39	0111101
aLateCollisions	40	0111110
aFrameAbortedDueToXSCollisions	41	0111111
aFrameAbortedDueToIntMACXmitError	28	0110010
aCarrierSenseErrors	42	1000000
aOctetsReceivedOK	43	1000001
aFramesLostDueToIntMACRcvrError	1	0010111
aMulticastFrameXmittedOK	20	0101010
aBroadcastFramesXmittedOK	19	0101001
aFramesWithExcessiveDefferal	44	1000010
aMulticastFramesReceivedOK	10	0100000
aBroadcastFramesReceivedOK	9	0011111
aInRangeLengthErrors	45	1000011
aOutofRangeLengthField	46	1000100
aFrameTooLongErrors	4	0011010
aSQETESTErrors	51	1001001
aSymbolErrorDuringCarrier	47	1000101
aMACControlFramesTransmitted	48	1000110
aMACControlFramesReceived	49	1000111
aUnsupportedOpcodesReceived	50	1001000
aPauseMACCtrlFramesTransmitted	48	1000110
aPauseMACCtrlFramesReceived	49	1000111

Specifications

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limits beyond which may cause permanent damage to the device or affect device reliability. All voltages are specified with respect to GND, unless otherwise specified.

VCC Supply Voltage .....-0.3V to 6.0V
All Inputs and Outputs .....-0.3V toVCC+.3V
Package Power Dissipation .....2.2 Watt @ 70°C
Storage Temperature .....-65 to +150°C
Temperature Under Bias .....-10 to +80°C
Lead Temperature (Soldering, 10 Sec) .....260°C
Body Temperature (Soldering, 30 Sec) .....220°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all test conditions are as follows:

1. T_A= 0 to +70°C
2. V_{CC}= 5V +/-5%
3. SCLK = 50 Mhz +/- 0.01%
4. TXC = 25 MHz +/-0.01%

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
VIL	Input Low Voltage			0.8	Volt	All Inputs Except SCLK
				0.6	Volt	SCLK
VIH	Input High Voltage	2.0			Volt	All Inputs Except SCLK
		2.4			Volt	SCLK
IIL	Input Low Current			-1	uA	VIN=GND
IIH	Input High Current			1	uA	VIN=VCC
IOZ	Output Hi-Z Current			10	uA	VOUT=GND-VCC, Output in High Impedance State
VOL	Output Low Voltage			0.4	Volt	IOL=-2 mA All Except RXRXDATA[31:0], RXTXEOF, TXRDY_[1:4], RXRDY_[1:4], TXRET_[1:4], RXDC_[1:4], TXD[3:0]_[1:4], TXEN[3:0]_[1:4]
				0.4	Volt	IOL=-4 mA TXD[3:0]_[1:4], TXEN[3:0]_[1:4]
				0.4	Volt	IOL=-8 mA RXRXDATA[31:0], RXTXEOF, TXRDY_[1:4], RXRDY_[1:4], TXRET_[1:4], RXDC_[1:4]
VOH	Output High Voltage	2.4			Volt	IOL=2 mA All Except RXRXDATA[31:0], RXTXEOF, TXRDY_[1:4], RXRDY_[1:4], TXRET_[1:4], RXDC_[1:4], TXD[3:0]_[1:4], TXEN[3:0]_[1:4]
		2.4			Volt	IOL=4 mA TXD[3:0]_[1:4], TXEN[3:0]_[1:4]
		2.4			Volt	IOL=8 mA RXRXDATA[31:0], RXTXEOF, TXRDY_[1:4], RXRDY_[1:4], TXRET_[1:4], RXDC_[1:4]
CIN	Input Capacitance		5		pF	
CIO	I/O Capacitance		5		pF	
ICC	VCC Supply Current			300	mA	No output load

AC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all test conditions are as follows:

1. T_A= 0 to +70°C
2. V_{CC}= 5V +/-5%
3. SCLK = 50 Mhz +/- 0.01%,
4. TXC = 25 Mhz +/- 0.01%
5. Input conditions:
   - All Inputs: tr, tf<=10nS @ 0.4V to 2.4V
6. Output Loading
   - All Other Digital Outputs: 50pF
7. Measurement Points:
   - Data Active to Hi-Z: 200mV Change
   - Data Hi-Z to Active: 200mV Change
   - All inputs and outputs: 1.4V
   - Rise and Fall Times: 0.4V to 2.4V

SYSTEM CLOCK TIMING CHARACTERISTICS

Refer To Figure 10 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_1	SCLK Period	1/25		1/50	1/Mhz	
t_2	SCLK High Time	8			nS	
t_3	SCLK Low Time	8			nS	

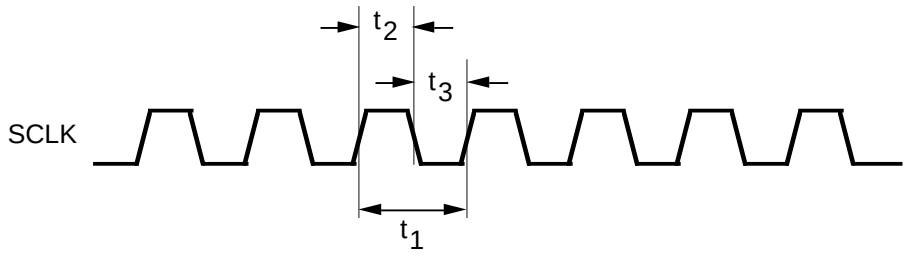


Figure 10. System Clock Timing

SYSTEM INTERFACE TIMING CHARACTERISTICS, TRANSMIT OPERATION

Refer To Figure 11 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{11}	$\overline{\text{TXINTEN}}$ Setup Time	5			nS	
t_{12}	$\overline{\text{TXINTEN}}$ Hold Time	0			nS	
t_{13}	$\overline{\text{TXINTEN}}$ Deassert Time	1 SCLK Cycle			nS	
t_{14}	TXRDY Hi-Z to Active Delay	3		15	nS	
t_{15}	TXRDY Delay	4		15	nS	
t_{16}	TXRDY Active to Hi-Z Time	3		15	nS	
t_{17}	$\overline{\text{TXINTEN}}$ Assert/Deassert to $\overline{\text{TXWREN}}$ Assert/Deassert	0			nS	
t_{18}	$\overline{\text{TXWREN}}$ Setup Time	5			nS	
t_{19}	$\overline{\text{TXWREN}}$ Hold Time	0			nS	
t_{20}	$\overline{\text{TXWREN}}$ Deassert Time	1 SCLK Cycle			nS	
t_{21}	RXTXPS[1:0], RXTXDATA[31:0], RXTXBE[3:0], RXTXEOF, TXNOCRC Setup Time	5			nS	RXTXDATA[31:0], RXTXBE[3:0], and RXTXEOF are Inputs
t_{22}	RXTXPS, RXTXDATA, RXTXBE, RXTXEOF, TXNOCRC Hold Time	0			nS	RXTXDATA[31:0], RXTXBE[3:0], and RXTXEOF are Inputs
t_{23}	SPDTAVL Hi-Z to Active Delay	3		15	nS	
t_{24}	SPDTAVL Delay	4		15	nS	
t_{25}	SPDTAVL Active to Hi-Z Delay	3		15	nS	

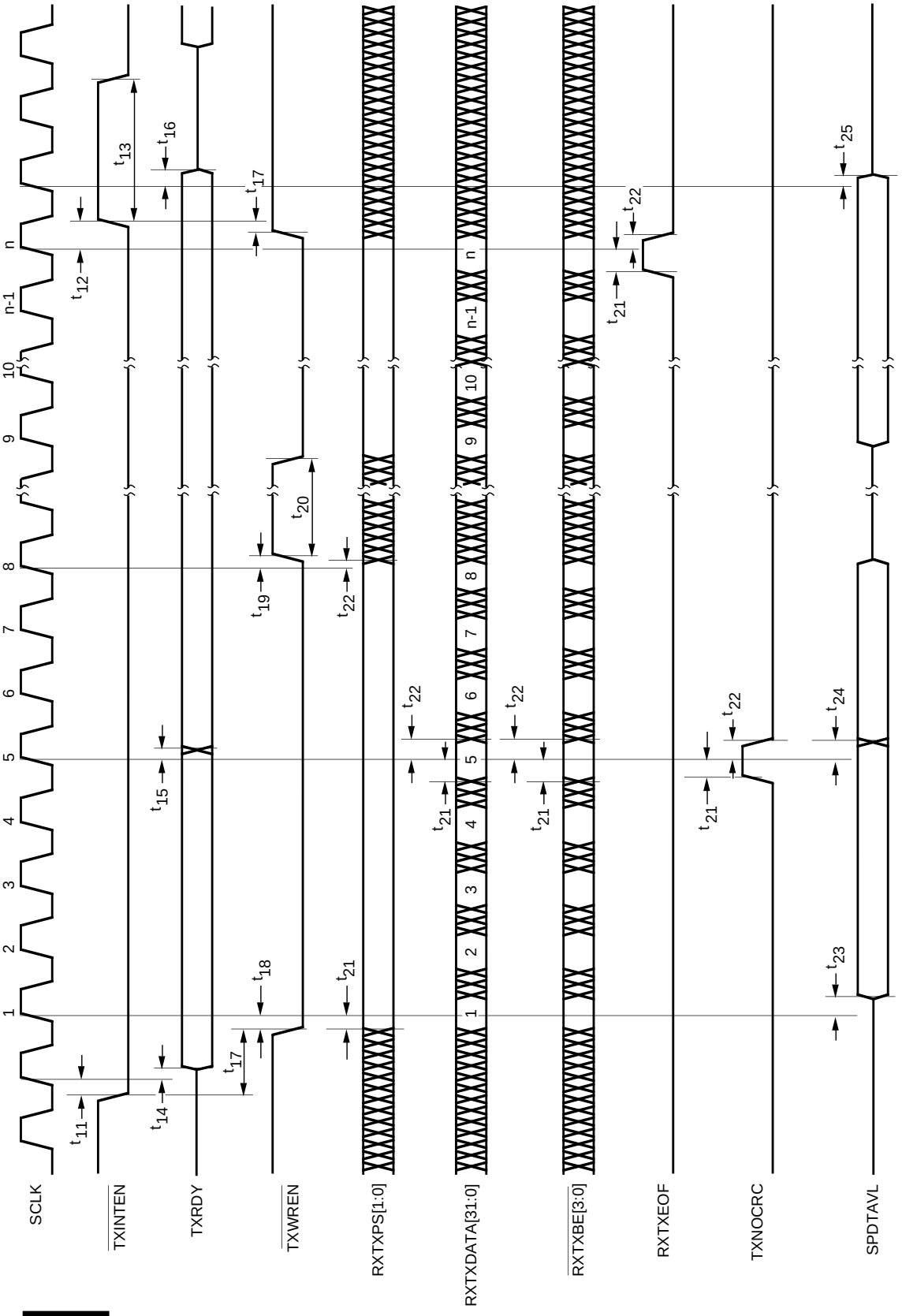


Figure 11. System Interface Timing, Transmit Operation

SYSTEM INTERFACE TIMING CHARACTERISTICS, RECEIVE OPERATION

Refer To Figure 12 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{31}	$\overline{\text{RXINTEN}}$ Setup Time	5			nS	
t_{32}	$\overline{\text{RXINTEN}}$ Hold Time	0			nS	
t_{33}	$\overline{\text{RXINTEN}}$ Deassert Time	1 SCLK Cycles			nS	
t_{34}	RXRDY Hi-Z to Active Delay	5		15	nS	
t_{35}	RXRDY Delay Time	5		15	nS	
t_{36}	RXRDY Active to Hi-Z Delay	5		15	nS	
t_{37}	$\overline{\text{RXRDEN}}$ Setup Time	5			nS	
t_{38}	$\overline{\text{RXRDEN}}$ Hold Time	0			nS	
t_{39}	$\overline{\text{RXRDEN}}$ Deassert Time	1 SCLK Cycles			nS	
t_{40}	$\overline{\text{RXINTEN}}$ Assert/Deassert to $\overline{\text{RXRDEN}}$ Assert/Deassert	0			nS	
t_{42}	RXTXDATA[31:0], RXTXBE[3:0], RXTXEOF Hi-Z to Active Delay	5		15	nS	RXTXDATA[31:0], RXTXBE[3:0], and RXTXEOF are Outputs
t_{43}	RXTXDATA[31:0], RXTXBE[3:0], RXTXEOF Delay Time	5		15	nS	RXTXDATA[31:0], RXTXBE[3:0], and RXTXEOF are Outputs
t_{44}	RXTXDATA[31:0], RXTXBE[3:0], RXTXEOF Active to Hi-Z Delay	5		15	nS	RXTXDATA[31:0], RXTXBE[3:0], and RXTXEOF are Outputs

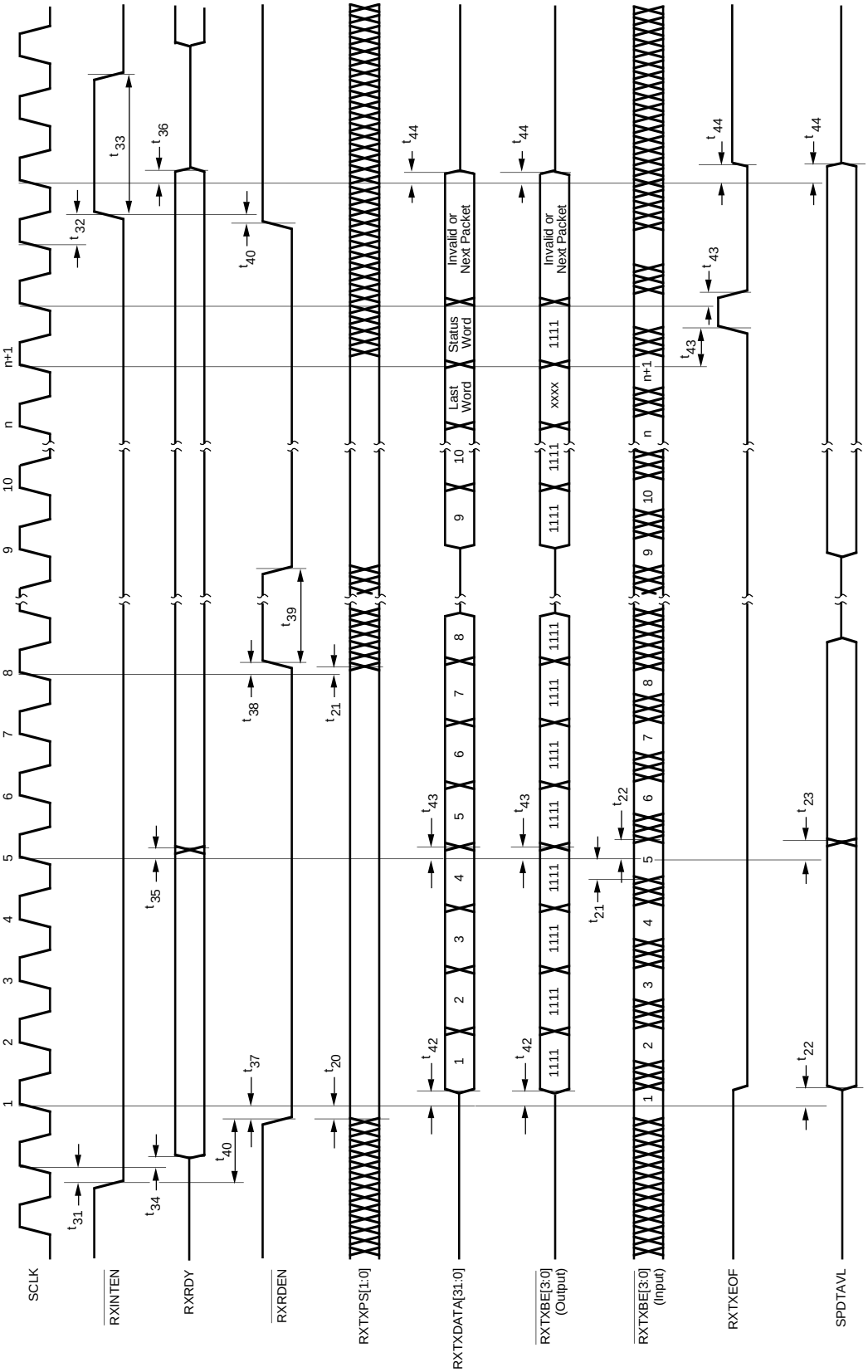


Figure 12. System Interface Timing, Receive Operation

SYSTEM INTERFACE TIMING CHARACTERISTICS, RXABORT OPERATION

Refer To Figure 13 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{51}	RXABORT to RXRDY Deassert Delay	1 SCLK Cycles + 5ns		1 SCLK Cycles + 15 ns	nS	
t_{52}	RXABORT to RXRDEN Deassert Delay	1 SCLK Cycles + 5ns		1 SCLK Cycles + 15 ns	nS	
t_{53}	RXABORT Setup Time	5			nS	
t_{54}	RXABORT Hold Time	0			nS	
t_{55}	RXABORT High Time	1.5 RXC			nS	
t_{56}	RXABORT to RXTXDATA[31:0], RXTXBE[3:0] Invalid Delay	1 SCLK Cycles + 5ns		1 SCLK Cycles + 15 ns	nS	
t_{57}	RXABORT to SPDTAVL Deassert Delay	1 SCLK Cycles + 5ns		1 SCLK Cycles + 15 ns	nS	

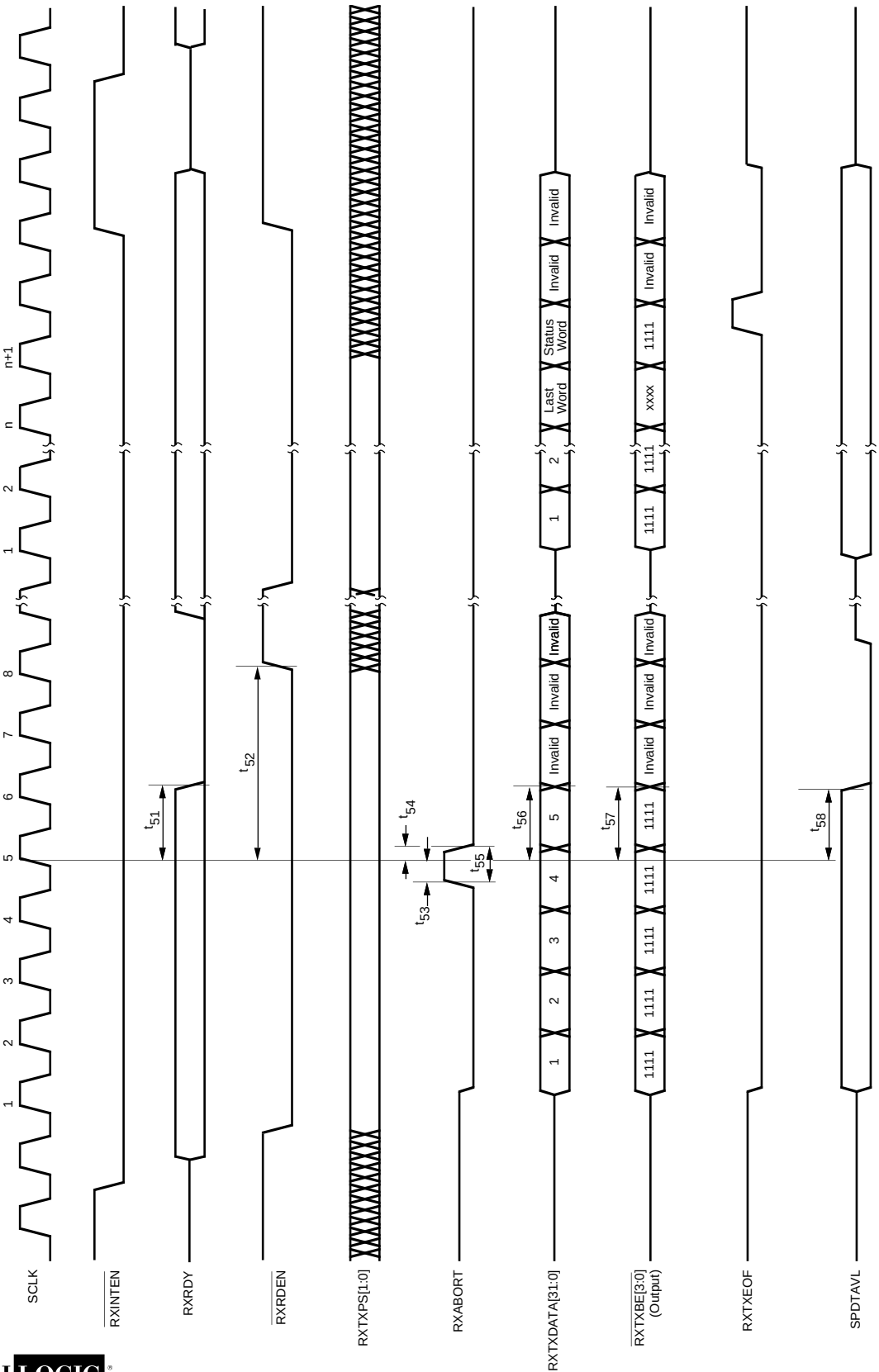


Figure 13. System Interface Timing, receive RXABORT Operation

SYSTEM INTERFACE TIMING CHARACTERISTICS, RXDC/TXRET OPERATION

Refer To Figure 14 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{61}	RXDC/TXRET Hi-Z to Active Delay	3		15	nS	
t_{62}	RXDC/TXRET Delay Time	3		15	nS	
t_{63}	RXDC/TXRET Active to Hi-Z Delay	3		15	nS	
t_{64}	CLRRXERR/CLRTXERR Setup Time	5			nS	
t_{65}	CLRRXERR/CLRTXERR Hold Time	0			nS	
t_{66}	CLRRXERR/CLRTXERR Assert to RXDC/TXRET Deassert Delay	1 TXC + 1 SLCK + 5 nS		2 TXC + 2 SLCK + 15 nS	nS	CLRTXERR
		1 RXC + 3 SLCK + 5 nS		2 RXC + 4 SLCK + 15 nS	nS	CLRRXERR

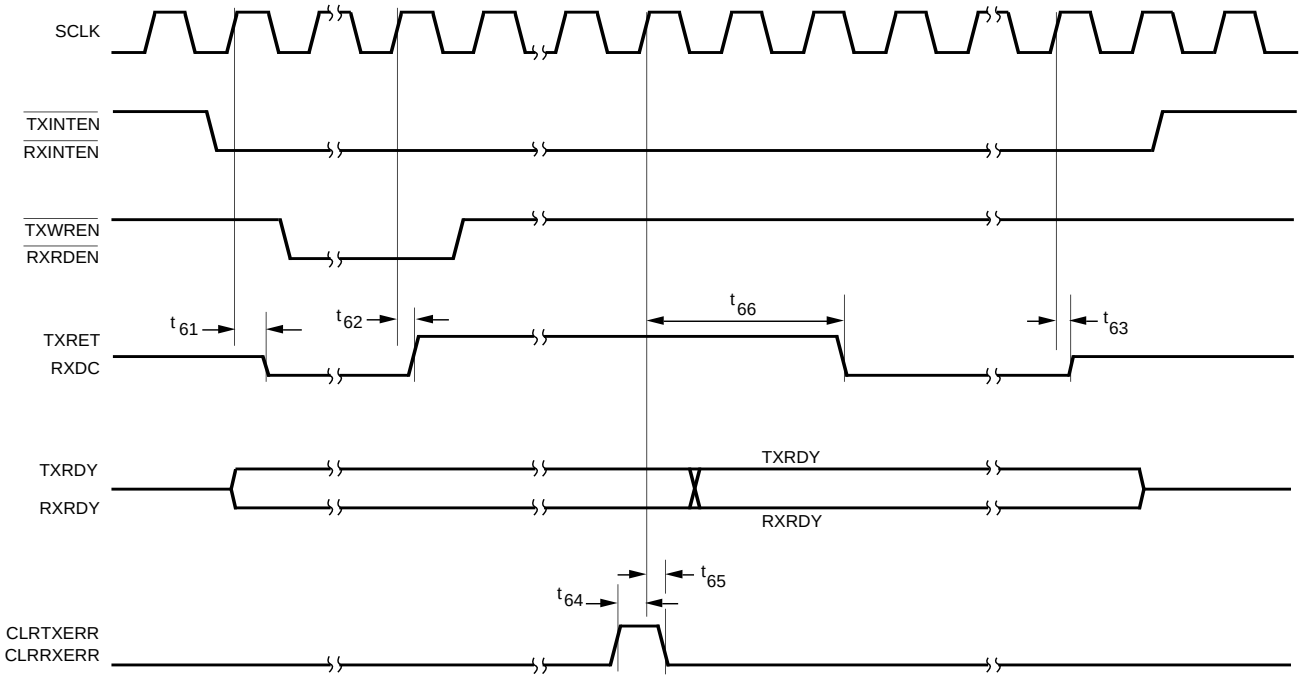


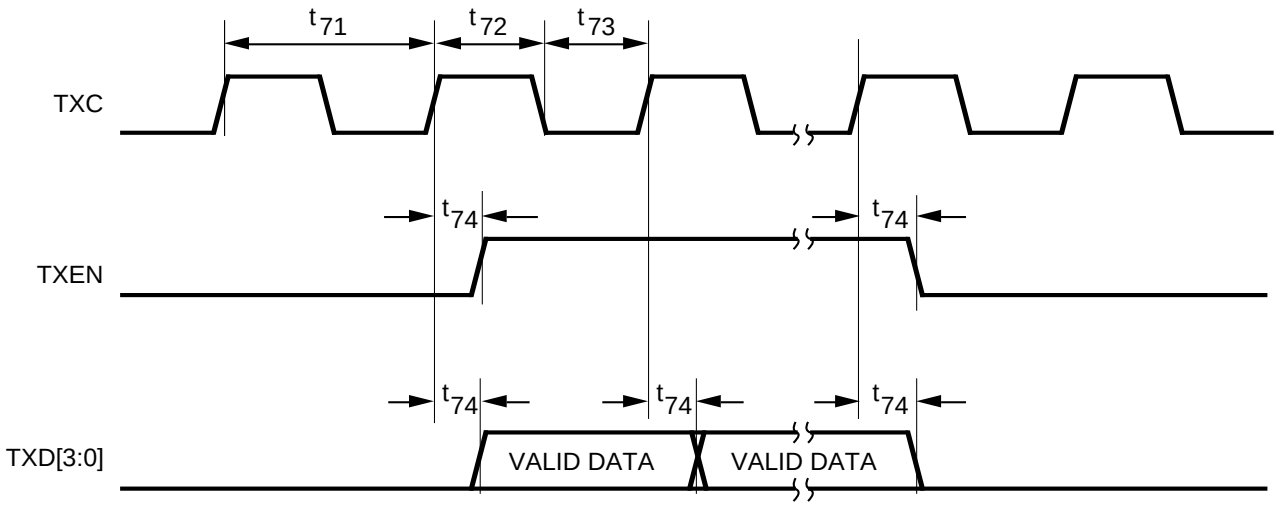
Figure 14. System Interface Timing, RXDC/TXRET Operation

TRANSMIT PHY INTERFACE TIMING CHARACTERISTICS

Refer To Figure 15 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{71}	TXC Cycle Time	1/25 - 0.01%	1/25	1/25 + 0.01%	1/Mhz	100 Mbps MII
		1/2.5 - 0.01%	1/2.5	1/2.5 + 0.01%	1/Mhz	10 Mbps MII
		1/10 - 0.01%	1/10	1/10 + 0.01%	1/Mhz	10 Mbps Serial
t_{72}	TXC HighTime	1/2 TXC Cycle Time - 5 nS			nS	
t_{73}	TXC Low Time	1/2 TXC Cycle Time - 5 nS			nS	
t_{74}	TXC to TXD, TXEN Delay	5		22	nS	

MII Mode



10 Mbps Serial Mode

Same as MII Mode except:
(1) All data us referenced to falling edge of TXC (TXC inverted)
(2) Data on TXD0 only

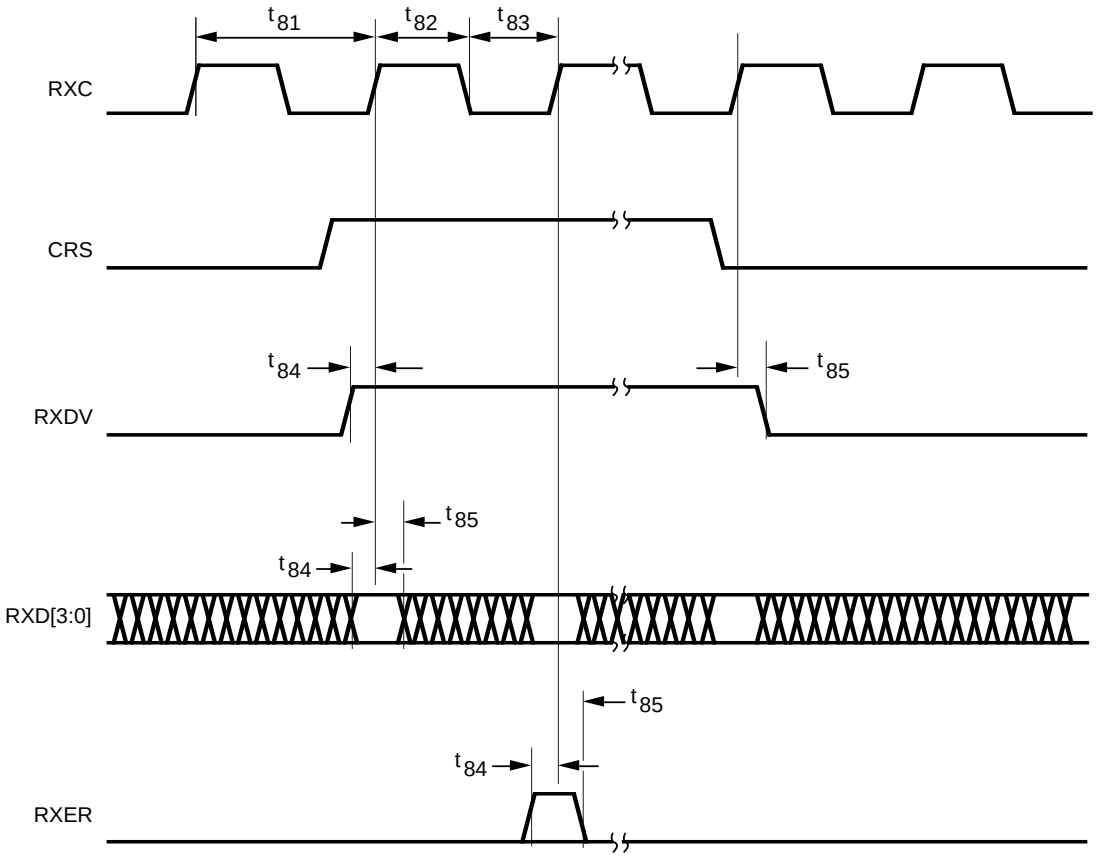
Figure 15. Transmit PHY Interface Timing

RECEIVE PHY INTERFACE TIMING CHARACTERISTICS

Refer To Figure 16 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{81}	RXC Cycle Time	1/25 - 0.01%	1/25	1/25 + 0.01%	1/Mhz	100 Mbps MII
		1/2.5 - 0.01%	1/2.5	1/2.5 + 0.01%	1/Mhz	10 Mbps MII
		1/10 - 0.01%	1/10	1/10 + 0.01%	1/Mhz	10 Mbps Serial
t_{82}	RXC HighTime	1/2 RXC Cycle Time -5 nS			nS	
t_{83}	RXC Low Time	1/2 RXC Cycle Time -5 nS			nS	
t_{84}	RXD, RXDV, RXER Setup Time	5			nS	
t_{85}	RXD, RXDV, RXER Hold Time	5			nS	

MII Mode



10 Mbps Serial Mode

Same as MII Mode except:
(1) Data on RXD0 only
(2) RXDV not used
(3) RXER not used

Figure 16. Receive PHY Interface Timing

REGISTER INTERFACE TIMING CHARACTERISTICS

Refer To Figures 17 and 18 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{91}	$\overline{WR}$ Low Time	20			nS	
t_{92}	$\overline{WR}$ High Time	20			nS	
t_{93}	$\overline{RD}$ Low Time	4 SLCK + 50 nS			nS	RX Status, TX Status, Counter 1-51, Counter Status 1-6 Registers
		50			nS	All Other Registers
t_{94}	$\overline{RD}$ High Time	3 SLCK + 50 nS			nS	RX Status, TX Status, Counter 1-51, Counter Status 1-6 Registers
		50			nS	All Other Registers
t_{95}	$\overline{ENREGIO}$, REGPS[1:0], A[7:0], BE[1:0], CDST[15:0] Setup Time	0			nS	
t_{96}	$\overline{ENREGIO}$, REGPS[1:0], A[7:0], BE[1:0], CDST[15:0] Hold Time	10			nS	
t_{97}	$\overline{RD}$ Assert to READY Assert Delay			4 SLCK + 50 nS	nS	RX Status, TX Status, Counter 1-51, Counter Status 1-6 Registers
				50	nS	All Other Registers
t_{98}	$\overline{RD}$ Deassert to READY Deassert Delay			3 SLCK + 50 nS	nS	RX Status, TX Status, Counter 1-51, Counter Status 1-6 Registers
				50	nS	All Other Registers
t_{99}	CDST[15:0], READY Hi-Z to Active Delay			3	nS	
t_{100}	CDST[15:0] Valid to READY Assert Delay	1			nS	
t_{101}	CDST[15:0], READY Active to Hi-Z Delay			3	nS	

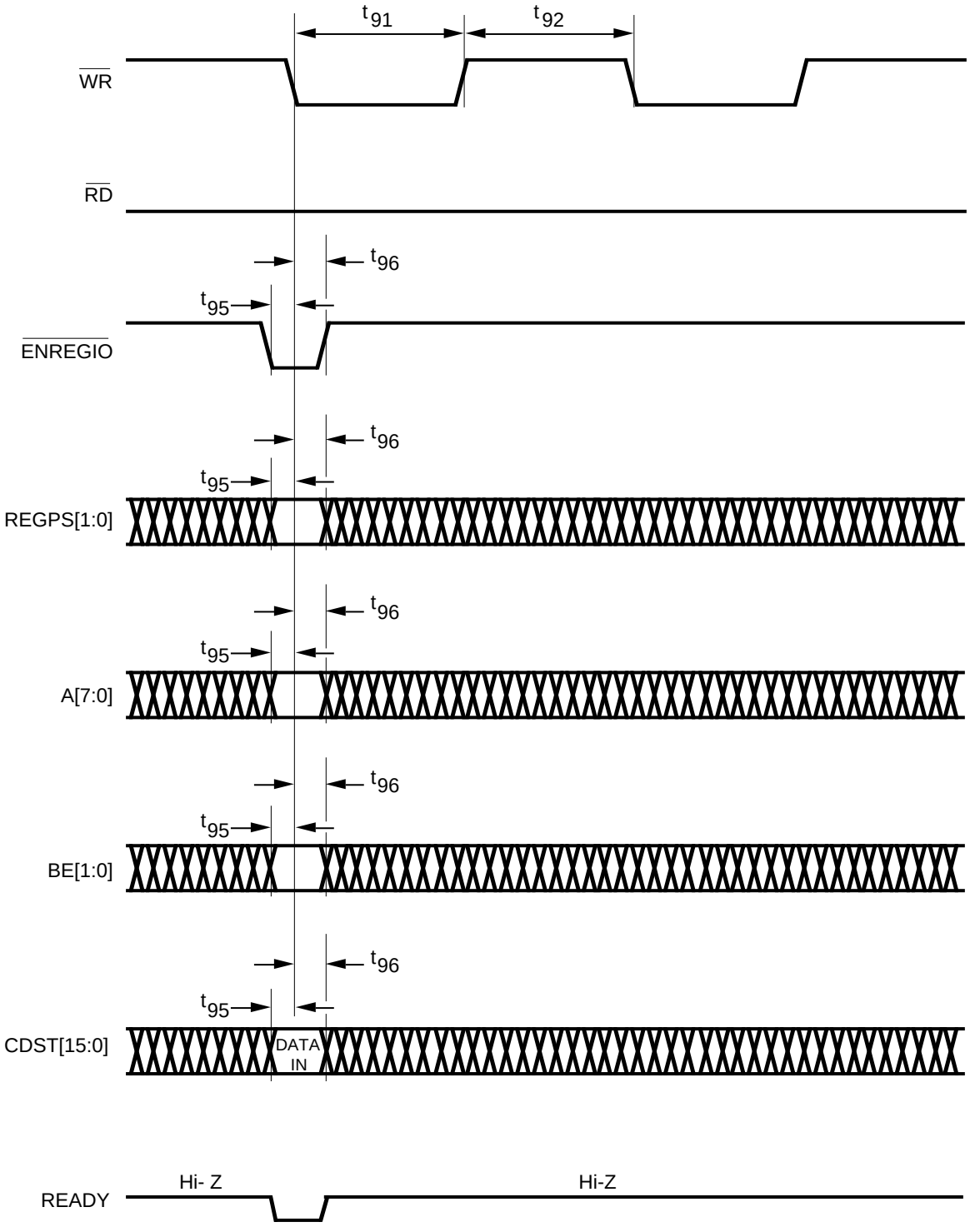
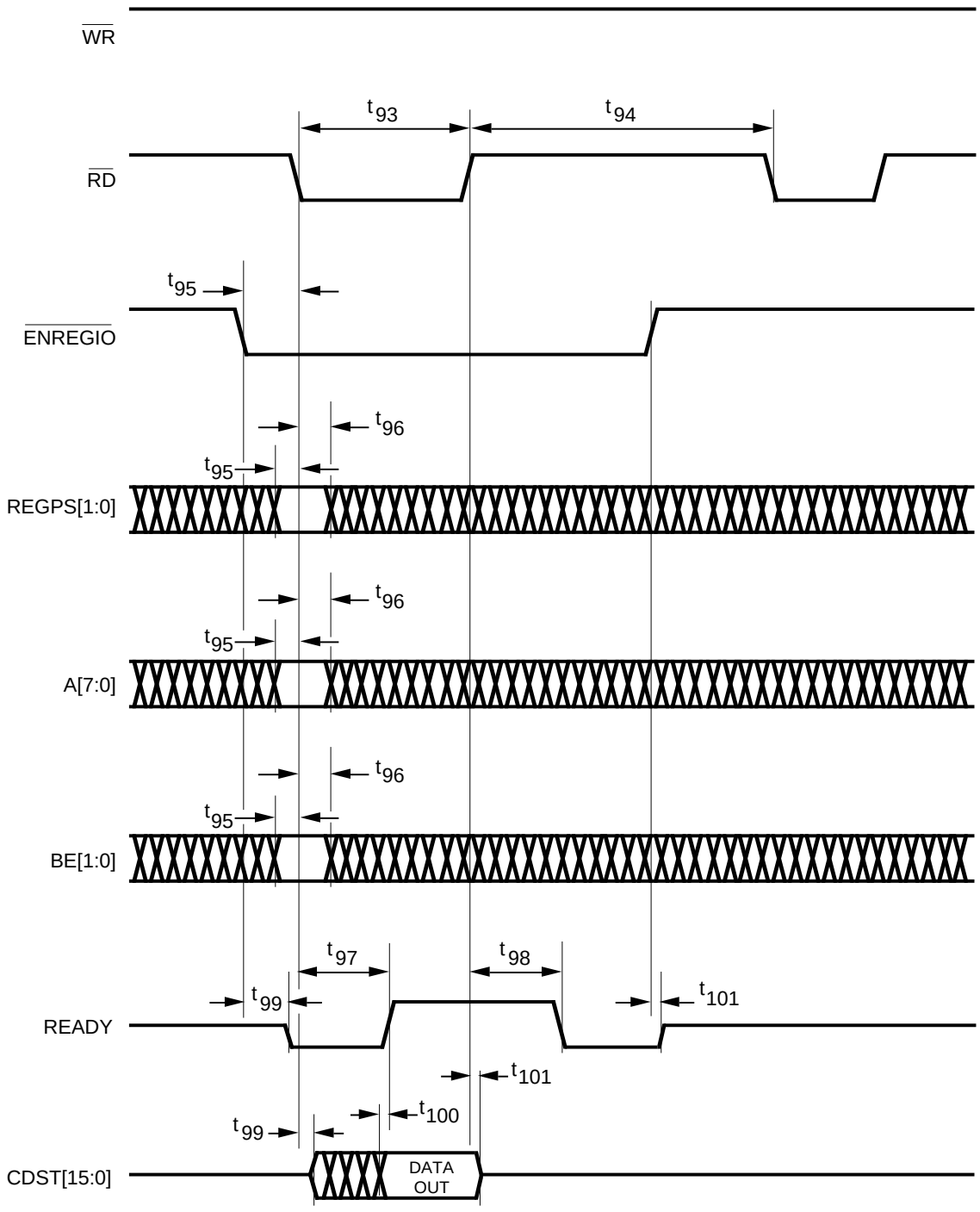


Figure 17. Register Interface Timing, Write Operation



Note 1. $\overline{\text{ENREGIO}}$ can be deasserted anytime after valid data is read out on CDST [15:0]. When $\overline{\text{ENREGIO}}$ is deasserted, both READY and CDST[15:0] go into High Impedance State.

Figure 18. Register Interface Timing, Read Operation

MANAGEMENT INTERFACE (MI) TIMING CHARACTERISTICS

Refer To Figure 19 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{111}	MDC Cycle Time	See MI Command/Status 0 Register Definition Table				
t_{112}	MDC Duty Cycle	40		60	%	
t_{113}	MDC to MDIO Delay			50	nS	Write Bits
t_{114}	MDIO Setup Time	20			nS	Read Bits
t_{115}	MDIO Hold Time	0			nS	Read Bits
t_{116}	MDIO Active to Hi-Z Delay			50	nS	Write-Read Bit Transition
t_{117}	MDIO Hi-Z to Active Delay			50	nS	Read-Write Bit Transition

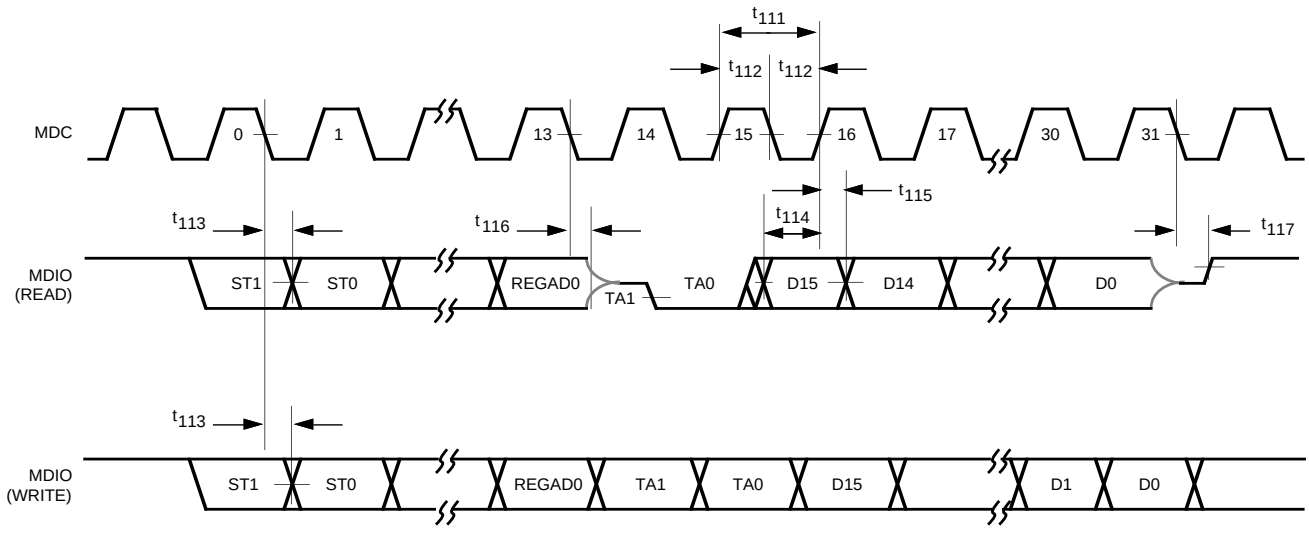


Figure 19. Management Interface (MI) Timing

RESET TIMING CHARACTERISTICS

Refer To Figure 20 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{121}	Asynchronous Reset Pulse Width	10			µs	All clocks must be active during this period of time
t_{122}	Reset Complete to Start of Normal Operation Delay	10 SCLK Cycles			nS	

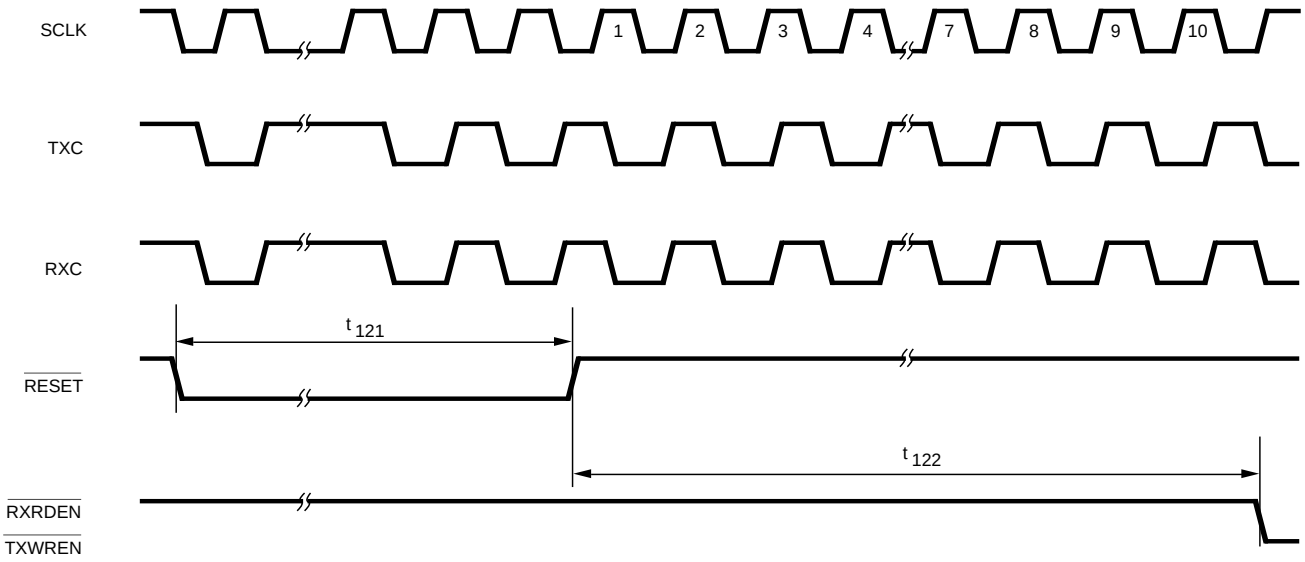
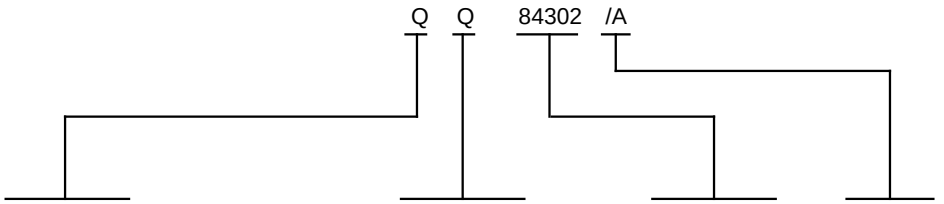


Figure 20. Reset Timing

Ordering Information



Revision History

Initial Release: 10/29/97

Special Note*: upon release this document does not have a Table of Contents. Table of Contents with section headings will be added later, also document does not have a Figure 9. Figure 9 will also be added later.*

12/2/97

12/2/97 Document Revision changed to MD400171/A

Page 10, 2.0 Block Diagram
- System Interface inputs from Ports, 1, 2, 3, and 4 are now input outputs.

Page 38, Register Interface
- Timing section has changed.

Page 45, Table 18. Command Register Definition
- Bit 3, PHYINTF is now INT_TX
- Bit 4, INT_TX is now PHYINTF

7/15/98

7/15/98 Document Revision changed to MD400171/B

Page 3: 1.0 Pin Description
- Pin #133, 141, 149, 157, Description, 1 = RX FIFO ≥ RX FIFO has been changed to, 1 = RX FIFO Data ≥ RX FIFO.

Page 4: 1.0 Pin Description
- Pin # 126, Description, RX FIFO Reads; 0 = Space Not Available, has been changed to, 0 = Data Not Available

Page 8: 1.0 Pin Description
- Pin # 174, 197, 220, 243, Description; copy should now read, 1 = Half Dulex, 0 = Full Duplex
- Pin # 57, Description, copy has been changed.

Page 9: 1.0 Pin Description
- Pin # 18 should be 1, 8

Revision History

Page 14: Section, Transmit Write Operation
- Paragraph 3, references to 0000 has been changed to 1111, and RXTXBE[3:0] has been changed to $\overline{\text{RXTXBE[3:0]}}$.

Page 15: Figure 4, Frame Formats and Bit Ordering
- Changes to Notes 2, and 4

Page 17: Section, Receive Read Operation
- Paragraph two, copy has changed.
- Paragraph four, copy has changed, new Table 2a has been added.
- New paragraph at the end of the section.

Page 17: Section, Pack 2-Byte Mode
- Byte Mode has been deleted.

Page 17: Section, Receive Read Operations
- Paragraph 3, references to 0000 has been changed to 1111, and RXTXBE[3:0] has been changed to $\overline{\text{RXTXBE[3:0]}}$.

Page 18: Section, Interpacket Gap
- New paragraph at end of section

Page 25: Section, Format and Bit Order
- New paragraph at end of section

Page 30: Section, Reset
- New copy at the end of the section

Page 32: Section, Counter General
- Paragraph five has been changed

Page 38: Section Timing, Paragraph two has been changed.

Pages 43 - 64: Bit order for all tables has been reversed.

Page 45: Table 18, Definition copy change to bits 5, 6.

Page 50: Table 23, Definition copy change to bits 6, 2.

Page 51: Table 24, Definition copy change to bits 1, 2.

Page 53: Table 26, Definition copy change to bits 4, 5, 6, 7.

Page 64: Table 37, bits 3 thru 7, R/W and Def. are now blank.

Page 65: Figure 8 has been changed

Page 74: Figure 12 has been changed

Page 83: Register Interface Timing Charactristics
- Sym t_{97}, (Min) is now blank and (Max) has been changed to 4 SLCK + 50 nS
- Sym t_{98}, (Min) is now blank and (Max) has been changed to 3 SLCK + 50 nS
- Sym t_{99}, Parameter has been changed.
- Sym t_{100}, Parameter has been changed.

Page 84: Figure 17, Ready, timing wave has been changed.

Page 85: Figure 18, has been changed.

Page 87: New Table Reset Timing, and Figure 20 have been added.

Page 90: Appendix A is new.

Revision History

6/24/99

6/24/99 Document Revision changed to MD400171/C

Page 4: 1.0 Pin Description (continued)
- Pin #s 134, 142, 150, 158, Description : Copy changes to Description.

Page 5: 1.0 Pin Description (continued)
- Pin #68, Description: Copy changes to Description.

Page 6: 1.0 Pin Description (continued)
- Pin #67, Description: Copy changes to Description.

Page 7: 1.0 Pin Description (continued)
- Pin #s 17, 11, 12, 15, 16, Description: Copy changes to Descriptions.
- Pin #s 21 - 28, Description: Copy change to Descriptions.

Page 8: 1.0 Pin Description (continued)
- Pin #s 13, 14, Description: Copy changes to Descriptions.
- Pin #s 35 - 54, Description: Copy changes to Descriptions.

Page 15: Figure 4. Frame Formats and Bit Ordering
- References to LT[0:7] have been changed to LT[8:15] and references to LT[8:16] have been changed to LT[7:0], and references to DATA[7:15] have been changed to [8:15]

Page 16: Section Transmit Write Operation
- Paragraphs #5, #7 have had a copy change.

Page 17: Section Receive Read Operation
- Paragraphs #5 and #7 have a copy change.

Page 19: Section Interpacket Gap
- Paragraph #3 copy change.
- Equation change.
- Paragraph #4 copy change.

Page 22: Section Watermark
- Paragraph #s 1, 2, 3, have had copy changes.

Page 23: Section Watermark
- Paragraph #s 1, 2, have had copy changes.

Page 24: Section Discard Output Indication
- Paragraph #1, has a copy change.

Page 26: Section MII Transmit Operation
- Paragraph #1, has a copy change.

Page 31: Figure 7. Autonegotiated Pause Frame Format
- MAC, SA and PARAM sections have been changed.

Page 35: Counter Definition
- Counter Name aFrameReceivedOK Description has been changed, and Register Address has been changed.

Revision History

Page 37: Notes
- Note #1 has been changed.

Page 48: Table 21. FIFO Threshold Register Definition
- Bit #s 7, 6, 5, 4, Definition has been changed.
- Bit #s 3, 2, 1, 0, Definition has been changed.

Page 50: Table 23. Configuration 2 Register Definition
- Bit #1 TXSTS_UPD has been changed to TXOFF.
- Bit #1, Row has been changed.

Page 62: Table 35. TX Status Register Definition
- Note has been changed.

Page 77: Table, System Interface Timing Charateristics, RXDC/TXRET Operation
- SYM, t_{66} conditions is now CLRTXERR.

Page 86: Table, Management Interface (MI) Timing Characteristics
- SYM t_{113}, (MAX) has been changed from 100 to 50
- SYM t_{114}, (MIN) has been changed from 10 to 20
- SYM t_{115}, (MIN) has been changed from 10 to 0 and (MAX) has been changed from 50 and is now blank.

Appendix A

84302 IPG Table

The following table lists the IPG values for a given DEFER REGISTER SETTING and a fixed CSN DELAY NUMBER.

CSN DELAY NUMBER This is the count of the number of positive TXC edges From the down going edge of TXEN to the down going Edge of CSN.

DEFER REGISTER SETTING : The programmed value in the defer register.

Serial 10 Mbit mode:

defer register setting	**IPG CSN delay number**						
	0	**1**	**2**	**3**	**4**	**5**	
0	9.6	9.6	9.6	9.6	9.6	9.6	***default**
1	3.2	3.2	3.2	3.2	3.2	3.2	
2	3.2	3.2	3.2	3.2	3.2	4.0	
3	3.2	3.2	3.2	3.2	4.0	4.0	
4	3.2	3.2	3.2	4.0	4.0	4.0	
5	3.2	3.2	4.0	4.0	4.0	4.0	
6	3.2	4.0	4.0	4.0	4.0	4.0	
7	4.0	4.0	4.0	4.0	4.0	4.0	
8	4.0	4.0	4.0	4.0	4.0	4.0	
9	4.0	4.0	4.0	4.0	4.0	4.0	
10	4.0	4.0	4.0	4.0	4.0	4.8	
11	4.0	4.0	4.0	4.0	4.8	4.8	
12	4.0	4.0	4.0	4.8	4.8	4.8	
13	4.0	4.0	4.8	4.8	4.8	4.8	
14	4.0	4.8	4.8	4.8	4.8	4.8	
15	4.8	4.8	4.8	4.8	4.8	4.8	
16	4.8	4.8	4.8	4.8	4.8	4.8	
17	4.8	4.8	4.8	4.8	4.8	4.8	
18	4.8	4.8	4.8	4.8	4.8	5.6	
19	4.8	4.8	4.8	4.8	5.6	5.6	
20	4.8	4.8	4.8	5.6	5.6	5.6	
21	4.8	4.8	5.6	5.6	5.6	5.6	
22	4.8	5.6	5.6	5.6	5.6	5.6	
23	5.6	5.6	5.6	5.6	5.6	5.6	
24	5.6	5.6	5.6	5.6	5.6	5.6	
25	5.6	5.6	5.6	5.6	5.6	5.6	
26	5.6	5.6	5.6	5.6	5.6	6.4	
27	5.6	5.6	5.6	5.6	6.4	6.4	
28	5.6	5.6	5.6	6.4	6.4	6.4	
29	5.6	5.6	6.4	6.4	6.4	6.4	
30	5.6	6.4	6.4	6.4	6.4	6.4	
31	6.4	6.4	6.4	6.4	6.4	6.4	
32	6.4	6.4	6.4	6.4	6.4	6.4	
33	6.4	6.4	6.4	6.4	6.4	6.4	
34	6.4	6.4	6.4	6.4	6.4	7.2	
35	6.4	6.4	6.4	6.4	7.2	7.2	

84302 IPG Table (continued)

Serial 10 Mbit mode:

defer register setting	IPG CSN delay number					
	0	**1**	**2**	**3**	**4**	**5**
36	6.4	6.4	6.4	7.2	7.2	7.2
37	6.4	6.4	7.2	7.2	7.2	7.2
38	6.4	7.2	7.2	7.2	7.2	7.2
39	7.2	7.2	7.2	7.2	7.2	7.2
40	7.2	7.2	7.2	7.2	7.2	7.2
41	7.2	7.2	7.2	7.2	7.2	7.2
42	7.2	7.2	7.2	7.2	7.2	8.0
43	7.2	7.2	7.2	7.2	8.0	8.0
44	7.2	7.2	7.2	8.0	8.0	8.0
45	7.2	7.2	8.0	8.0	8.0	8.0
46	7.2	8.0	8.0	8.0	8.0	8.0
47	8.0	8.0	8.0	8.0	8.0	8.0
48	8.0	8.0	8.0	8.0	8.0	8.0
49	8.0	8.0	8.0	8.0	8.0	8.0
50	8.0	8.0	8.0	8.0	8.0	8.8
51	8.0	8.0	8.0	8.0	8.8	8.8
52	8.0	8.0	8.0	8.8	8.8	8.8
53	8.0	8.0	8.8	8.8	8.8	8.8
54	8.0	8.8	8.8	8.8	8.8	8.8
55	8.8	8.8	8.8	8.8	8.8	8.8
56	8.8	8.8	8.8	8.8	8.8	8.8
57	8.8	8.8	8.8	8.8	8.8	8.8
58	8.8	8.8	8.8	8.8	8.8	9.6
59	8.8	8.8	8.8	8.8	9.6	9.6
60	8.8	8.8	8.8	9.6	9.6	9.6
61	8.8	8.8	9.6	9.6	9.6	9.6
62	8.8	9.6	9.6	9.6	9.6	9.6
63	9.6	9.6	9.6	9.6	9.6	9.6
64	9.6	9.6	9.6	9.6	9.6	9.6
65	9.6	9.6	9.6	9.6	9.6	9.6
66	9.6	9.6	9.6	9.6	9.6	10.4
67	9.6	9.6	9.6	9.6	10.4	10.4
68	9.6	9.6	9.6	10.4	10.4	10.4
69	9.6	9.6	10.4	10.4	10.4	10.4
70	9.6	10.4	10.4	10.4	10.4	10.4
71	10.4	10.4	10.4	10.4	10.4	10.4
72	10.4	10.4	10.4	10.4	10.4	10.4
73	10.4	10.4	10.4	10.4	10.4	10.4
74	10.4	10.4	10.4	10.4	10.4	11.2
75	10.4	10.4	10.4	10.4	11.2	11.2
76	10.4	10.4	10.4	11.2	11.2	11.2

84302 IPG Table (continued)

Serial 10 Mbit mode:

defer register setting	IPG CSN delay number					
	0	**1**	**2**	**3**	**4**	**5**
77	10.4	10.4	11.2	11.2	11.2	11.2
78	10.4	11.2	11.2	11.2	11.2	11.2
.						
.						
.						
246	27.2	28.0	28.0	28.0	28.0	28.0
247	28.0	28.0	28.0	28.0	28.0	28.0
248	28.0	28.0	28.0	28.0	28.0	28.0
249	28.0	28.0	28.0	28.0	28.0	28.0
250	28.0	28.0	28.0	28.0	28.0	28.8
251	28.0	28.0	28.0	28.0	28.8	28.8
252	28.0	28.0	28.0	28.8	28.8	28.8
253	28.0	28.0	28.8	28.8	28.8	28.8
254	28.0	28.8	28.8	28.8	28.8	28.8
255	28.8	28.8	28.8	28.8	28.8	28.8

MII 100 Mbit mode:

defer register value	IPG CSN delay number						
	0	**1**	**2**	**3**	**4**	**5**	
0	.96	1.04	1.04	1.12	1.12	1.2	* default
1	.40	.48	.48	.56	.56	.64	
2	.48	.48	.56	.56	.64	.64	
3	.48	.56	.56	.64	.64	.72	
4	.56	.56	.64	.64	.72	.72	
5	.56	.64	.64	.72	.72	.80	
6	.64	.64	.72	.72	.80	.80	
7	.64	.72	.72	.80	.80	.88	
8	.72	.72	.80	.80	.88	.88	
9	.72	.80	.80	.88	.88	.96	
10	.80	.80	.88	.88	.96	.96	
11	.80	.88	.88	.96	.96	1.04	
12	.88	.88	.96	.96	1.04	1.04	
13	.88	.96	.96	1.04	1.04	1.12	
14	.96	.96	1.04	1.04	1.12	1.12	
15	.96	1.04	1.04	1.12	1.12	1.2	
16	1.04	1.04	1.12	1.12	1.2	1.2	
17	1.04	1.12	1.12	1.2	1.2	1.28	

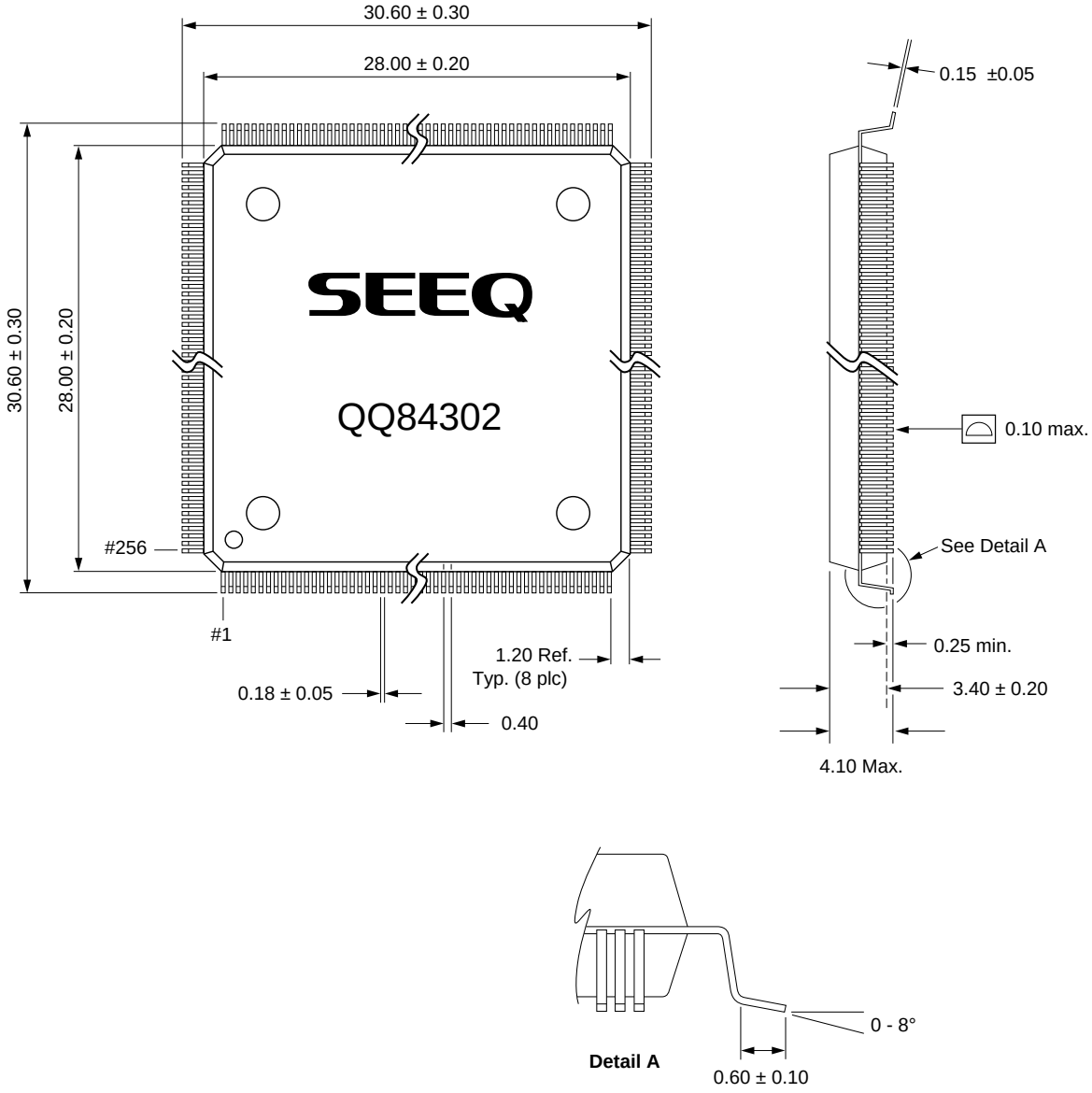
84302 IPG Table (continued)

MII 100 Mbit mode:

defer register value	IPG CSN delay number					
	0	**1**	**2**	**3**	**4**	**5**
18	1.12	1.12	1.2	1.2	1.28	1.28
19	1.12	1.2	1.2	1.28	1.28	1.36
.						
.						
.						
252	10.48	10.48	10.56	10.56	10.64	10.64
253	10.48	10.56	10.56	10.64	10.64	10.72
254	10.56	10.56	10.64	10.64	10.72	10.72
255	10.56	10.64	10.64	10.72	10.72	10.80

For MII 10 Mbit mode, scale the IPG by 10.

256 Pin PQFP



1. All dimensions are in millimeters.