Advance Information

MPC8560EC/D
Rev. 1.1, 2/2003

MPC8560
Integrated Processor
Hardware Specifications

The MPC8560 integrates a processor that implements the PowerPC architecture with system logic required for networking, storage, and general-purpose embedded applications. For functional characteristics of the processor, refer to the *MPC8560 PowerQUICC III™ Integrated Communications Processor Preliminary Reference Manual*.

To locate any published errata or updates for this document, contact your Motorola sales office.

1.1 Overview

The following section provides a high-level overview of the MPC8560 features. Figure 1 shows the major functional units within the MPC8560.

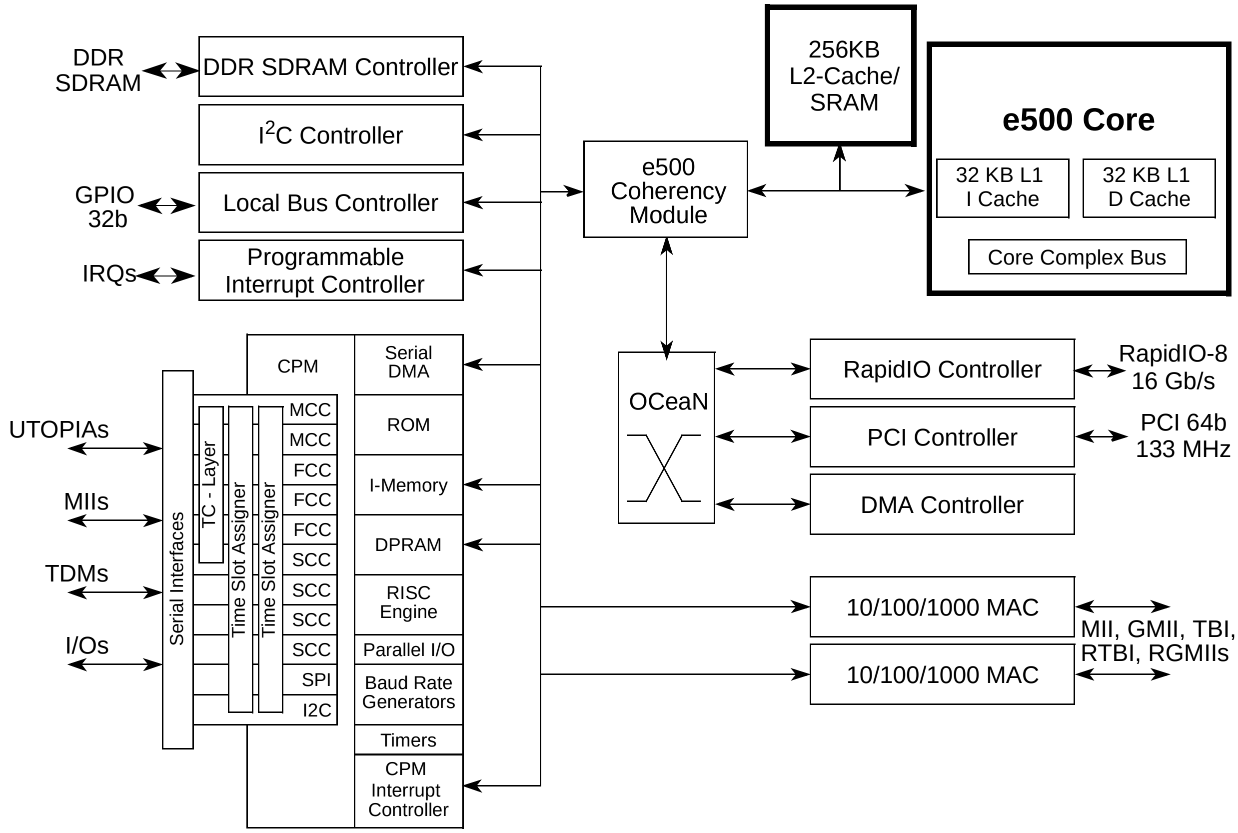


Figure 1. MPC8560 Block Diagram

1.1.1 Key Features

Major features of the MPC8560 are as follows:

- Embedded e500 Book E-compatible core
  - — High-performance, 32-bit Book E enhanced core that implements the PowerPC architecture
  - — Dual issue superscalar, seven-stage pipeline design
  - — 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection
  - — Lockable L1 caches—entire cache or on a per-line basis
  - — Separate locking for instructions and data
  - — Single processing engine auxiliary processing unit (SPE APU)
  - — Single-precision floating-point single-instruction, multiple-data (SIMD) operations.
  - — Memory management unit especially designed for embedded applications
  - — Enhanced hardware and software debug support
  - — Dynamic power management
  - — Performance monitor facility
- 256 Kbytes of on-chip memory
  - — Can act as a 256-Kbyte level 2 cache

- Can act as a 256-Kbyte or two 128-Kbyte memory-mapped SRAM arrays
- Can be partitioned into 128-Kbyte L2 cache plus 128-Kbyte SRAM
- Full ECC support on 64-bit boundary in both cache and SRAM modes
- SRAM operation supports relocation and is byte-accessible
- Cache mode supports instruction caching, data caching, or both
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types
- Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
- Supports locking the entire cache or selected lines
- Individual line locks set and cleared through Book E instructions or by externally mastered transactions
- Global locking and flash clearing done through writes to L2 configuration registers
- Instruction and data locks can be flash cleared separately
- Read and write buffering for internal bus accesses

• High-performance RISC CPM operating at up to 333 MHz
  - CPM software compatibility with previous PowerQUICC families
  - One instruction per clock
  - Executes code from internal ROM or instruction RAM
  - 32-bit RISC architecture
  - Tuned for communication environments: instruction set supports CRC computation and bit manipulation
  - Internal timer
  - Interfaces with the embedded e500 core processor through a 32-Kbyte dual-port RAM and virtual DMA channels for each peripheral controller
  - Handles serial protocols and virtual DMA
  - Three full-duplex fast serial communications controllers (FCCs) support the following protocols:
    - ATM protocol through UTOPIA interface (FCC1 and FCC2 only)
    - IEEE802.3/Fast Ethernet
    - HDLC
    - Totally transparent operation
  - Two multi-channel controllers (MCCs) that together can handle up to 256 HDLC/transparent channels at 64 Kbps each, multiplexed on up to 8 TDM interfaces
  - Four full-duplex serial communications controllers (SCCs) support the following protocols:
    - High level/synchronous data link control (HDLC/SDLC)
    - LocalTalk (HDLC-based local area network protocol)
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART (1x clock mode)

  - Binary synchronous communication (BISYNC)
  - Totally transparent operation
- Serial peripheral interface (SPI) support for master or slave
- I^2C bus controller
- Time-slot assigner supports multiplexing of data from any of the SCCs and FCCs onto eight time-division multiplexed (TDM) interfaces. The time-slot assigner supports the following TDM formats:
  - T1/CEPT lines
  - T3/E3
  - Pulse code modulation (PCM) highway interface
  - ISDN primary rate
  - Motorola interchip digital link (IDL)
  - General circuit interface (GCI)
- User-defined interfaces
- Eight independent baud rate generators (BRGs)
- Four general-purpose 16-bit timers or two 32-bit timers
- General-purpose parallel ports—16 parallel I/O lines with interrupt capability

• DDR memory controller
- Programmable timing supporting DDR SDRAM
- 64-bit data interface, up to 333-MHz data rate
- Four banks of memory, each up to 1 Gbyte
- DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
- Full ECC support
- Page mode support (up to 16 simultaneous open pages)
- Contiguous or discontiguous memory mapping
- Read-modify-write support for atomic increment, decrement, set, and clear
- Sleep mode support for self refresh SDRAM
- Supports auto refreshing
- On-the-fly power management using CKE
- Registered DIMM support
- Fast memory access via JTAG port
- 2.5-V SSTL2 compatible I/O

• Local bus controller
- Multiplexed 32-bit address and data operating up to 166 MHz
- Eight chip selects support eight external slaves
- Up to eight-beat burst transfers
- 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- General purpose chip select machine (GPCM)

- Three user programmable machines (UPM)
- Dedicated single data rate SDRAM controller
- Parity support
- Boot chip select with programmable bus width (8-, 16-, or 32-bit)
- SDRAM machine

• Three-speed (10/100/1000) Ethernet controllers (TSEC)
  - Dual IEEE 802.3, 802.3u, 820.3x, 802.3z, 802.3 AC compliant controllers
  - Support for different Ethernet physical interfaces:
    - 10/100/1000 Mbps IEEE 802.3 GMII
    - 10/100 Mbps IEEE 802.3 MII
    - 10 Mbps IEEE 802.3 MII
    - 1000 Mbps IEEE 802.3z TBI
    - 10/100/1000 Mbps RGMII/RTBI
  - Full and half-duplex support
  - Buffer descriptors are backwards compatible with MPC8260 and MPC860T 10/100 programming models
  - Layer 2 acceleration
    - Eight unicast exact address matches
    - Up to sixteen 4-byte pattern matches
    - Accept or reject on address or pattern match
    - 256-entry hash for unicast and multicast
    - Direct queuing of four flows
    - Packet field extraction and insertion
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - 2-Kbyte internal transmit and receive FIFOs
  - MII management interface for control and status
  - Programmable CRC generation and checking

• RapidIO interface unit
  - 8-bit RapidIO I/O and messaging protocols
  - Source synchronous double data rate (DDR) interfaces
  - Supports small type systems (small domain, 8-bit device ID)
  - Supports four priority levels (ordering within a level)
  - Reordering across priority levels
  - Maximum data payload of 256 bytes per packet
  - Packet pacing support at the physical layer
  - CRC protection for packets

- Supports atomic increment, decrement, set, and clear
- LVDS signaling

- RapidIO compliant message unit
  - One inbound data message structure (inbox)
  - One outbound data message structure (outbox)
  - Supports chaining and direct modes in the outbox
  - Support of up to 16 packets per message
  - Support of up to 256 bytes per packet and up to 4 Kbytes of data per message
  - Supports one inbound doorbell message structure
- PCI/PCI-X functional unit
  - PCI 2.2 and PCI-X 1.0 compatible
  - 64- or 32-bit PCI support at 16 to 66 MHz
  - 64-bit PCI-X support up to 133 MHz
  - Host and agent mode support
  - 64-bit dual address cycle (DAC) support
  - PCI-X supports multiple split transactions
  - Supports PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses
  - Support posting of processor-to-PCI and PCI-to-memory writes
  - PCI 3.3-V compatible
  - Selectable hardware-enforced coherency
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both local and remote masters
  - Extended DMA operations (advanced chaining and stride capability)
  - Support for cascading descriptor chains
  - Extended chaining and direct modes
  - Scatter gathering
  - Unaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Supports transfers of packet data using packet buffer descriptors
  - Selectable hardware-enforced coherency (snoop/no-snoop)
  - Ability to start DMA from external 3-pin interface
  - Programmable chunk wire
  - Ability to launch DMA from single write transaction
  - Optimal 3-pin hardware handshake interface per channel

- OCeaN switch fabric
  - Four-port crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads up to 256 bytes
- Programmable interrupt controller (PIC)
  - Supports the OpenPIC architecture programming model
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Four global high resolution timers/counters can generate interrupts
  - Supports 32 other internal interrupt sources
  - Supports connection of external interrupt controller (for example, 8259)
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports fully nested interrupt delivery
  - Interrupts can be routed to external pin for external processing
  - Interrupts can be routed to the e500 core’s standard or critical interrupt inputs
  - Interrupt summary registers allow fast identification of interrupt source
  - Supports software-based reset of PIC
  - Supports software-based soft reset of entire chip
- I^2C controller
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - Software-programmable for 1 of 64 different serial clock frequencies
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Uses the I^2C interface to access serial ROM
  - Optionally loads configuration data at reset
  - Supports extended I^2C addressing mode
  - Can be used to initialize configuration registers and/or memory
  - Data integrity checked with preamble signature and CRC
- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 32-bit address space
  - Inbound and outbound ATMUs map to larger external address spaces
    - Three inbound windows plus a configuration translation on PCI/PCI-X
    - Four inbound windows plus default and configuration translation on RapidIO

    - Four outbound windows plus default translation for PCI
    - Eight outbound windows plus default translation for RapidIO
- System performance monitor
    - Support eight 32-bit counters that count the occurrence of selected events
    - Supports 64 reference events that can be counted on any of the 8 counters
    - Supports duration and quantity threshold counting
    - Burstiness feature that permits counting of burst events with a programmable time between bursts
- System access port
    - Uses JTAG interface and a TAP controller to access entire system memory map
    - Supports 32-bit accesses to configuration registers
    - Supports cache-line burst accesses to main memory
    - Supports large block (4-Kbyte) uploads and downloads
    - Supports continuous bit streaming of entire block for fast upload and download
- Power management
    - Fully static 1.2-V CMOS design with 3.3- and 2-V I/O
    - Supports power save modes: nap, doze, and sleep
    - Supports suspend power save mode
    - Supports dynamic power management
- IEEE 1149.1-compliant, JTAG boundary scan
- 783 FC-PBGA package
- Supports inverse muxing of ATM cells (IMA)

1.2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8560. The MPC8560 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

1.2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

1.2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings [1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.32	V	4
PLL supply voltage		AV_{DD}	–0.3 to 1.32	V	4
DDR DRAM I/O voltage		GV_{DD}	–0.3 to 3.63	V	2, 4
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	4
PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet,, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	3, 4
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	2, 5
	Local bus, RapidIO, 10/100 Ethernet, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	2, 5
	PCI/PCI-X	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	2, 6
Storage temperature range		T_{STG}	–55 to 150	°C	

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** V_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** V_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** OV_{DD}, LV_{DD}, and GV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2.0 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 3 and Figure 4.

1.2.1.2 Recommended Operating Conditions

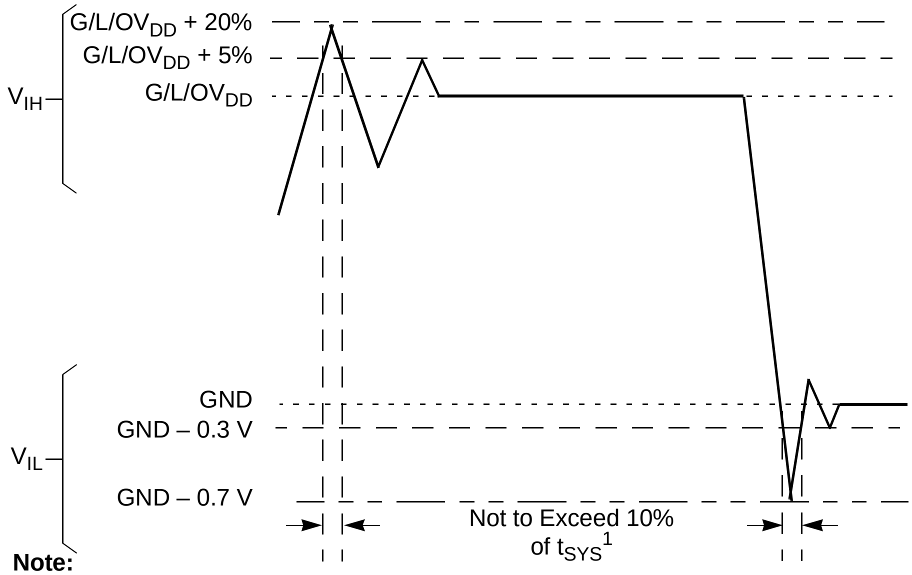
Table 2 provides the recommended operating conditions for the MPC8560. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD}	1.2 V ± 60 mV	V	
PLL supply voltage		AV_{DD}	1.2 V ± 60 mV	V	
DDR DRAM I/O voltage		GV_{DD}	2.5 V ± 125 mV	V	1
Three-speed Ethernet I/O voltage		LV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	1
PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	1
Input voltage	DDR DRAM signals	MV_{IN}	GND to GV_{DD}	V	
	DDR DRAM reference	MV_{REF}	GND to GV_{DD}	V	
	Three-speed Ethernet signals	LV_{IN}	GND to LV_{DD}	V	
	PCI/PCI-X, local bus,RapidIO, 10/100 Ethernet, DUART, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	
Die-junction temperature		T_j	0 to 105	°C	

Note:
1. **Caution:** OV_{DD}, LV_{DD}, and GV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2.0 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8560.



Note:

1. Note that t_{SYS} refers to the clock period associated with the SYSCLK signal.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

The MPC8560 core voltage must always be provided at nominal 1.2 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

Figure 3 and Figure 4 show the undershoot and overshoot voltage of the PCI interface of the MPC8560 for the 3.3- and 5-V signals, respectively.

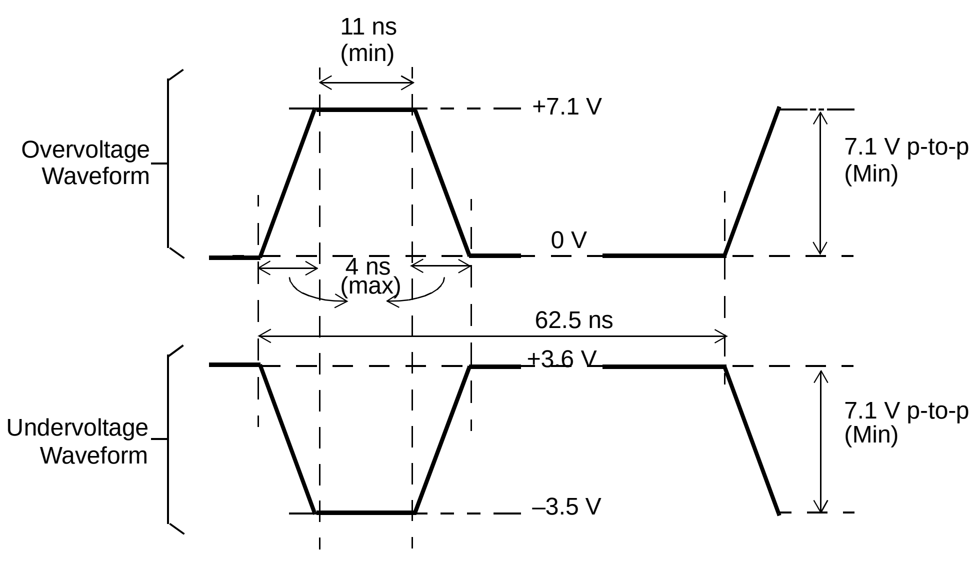


Figure 3. Maximum AC Waveforms for 3.3-V Signaling

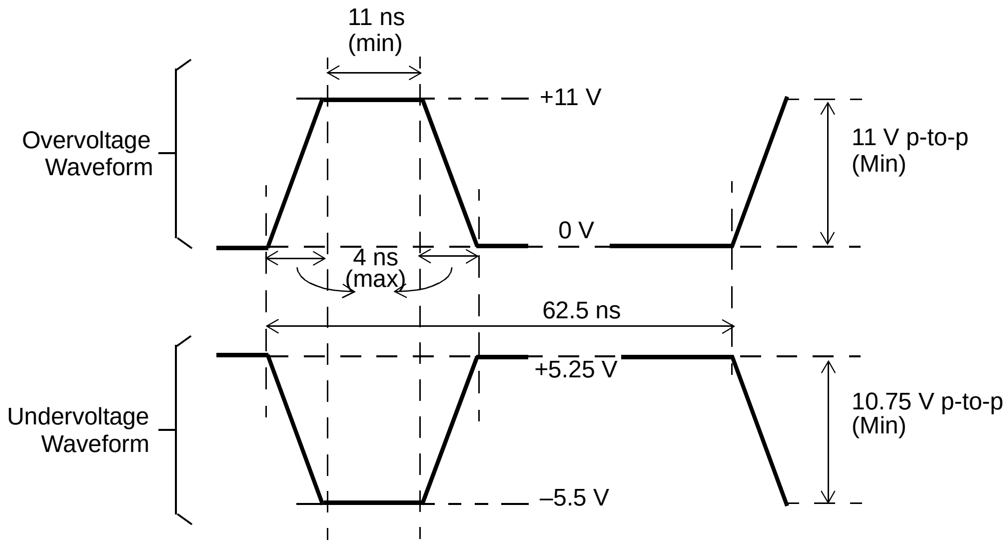


Figure 4. Maximum AC Waveforms for 5-V Signaling

1.3 Power Characteristics

The estimated typical power dissipation for the MPC8560 is 7 watts at 800 MHz.

1.4 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8560. Table 3 provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 3. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of HRESET	10	—	µs	
Minimum assertion time for SRESET	512	—	SYSCLKs	1
Input setup time for Power On Reset (POR) config inputs before the negation of HRESET	4	—	SYSCLKs	1
Input hold time for Power On Reset (POR) config inputs before the negation of HRESET	0	—	µs	
Minimum setup time for POR configs (other than PLL config) with respect to negation of HRESET	4	—	SYSCLKs	1
Minimum hold time for POR configs (including PLL config) with respect to negation of HRESET	2	—	SYSCLKs	1, 2
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of HRESET	—	5	SYSCLKs	1

Notes:
1. SYSCLK is identical to the PCI_CLK signal and is the primary clock input for the MPC8560. See the MPC8560 Reference Manual for more details.
3. The PLL config inputs have a 100 µs setup time wtih stable SYSCLK before HRESET negation.

1.5 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8560.

1.5.1 DDR SDRAM DC Electrical Characteristics

Table 4 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8560.

Table 4. DDR SDRAM DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} – 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	
Input low voltage	V_{IL}	–0.3	$MV_{REF} – 0.18$	V	
Output leakage current	I_{OZ}	–10	10	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–15.2	—	mA	
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

Table 5 provides the DDR capacitance.

Table 5. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, MSYNC_IN	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak to peak) = 0.2 V.

1.5.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

1.5.2.1 DDR SDRAM Input AC Timing Specifications

Table 6 provides the input AC timing specifications for the DDR SDRAM interface.

Table 6. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	
AC input high voltage	V_{IH}	MV_{REF} + 0.31	GV_{DD} + 0.3	V	
MDQS—MDQ/MECC input skew per byte	t_{DISKEW}	—	$0.25 \times t_{MCK} - 0.75$	ns	1

Note:

1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 <= n <= 7) or ECC (MECC[{0...7}] if n = 8).

Figure 5 shows the interface input timing for the DDR SDRAM.

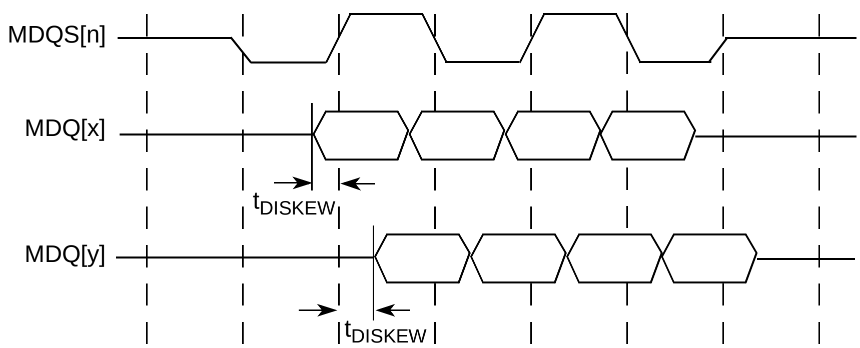


Figure 5. DDR SDRAM Input Timing Diagram

1.5.2.2 DDR SDRAM Output AC Timing Specifications

Table 7 and Table 8 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface.

Table 7. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing)	t_{MCK}	6	10	ns	2
MCK[n] skew to $\overline{\text{MCK}}$[n]	$t_{MCKSKEW1}$	—	150	ps	3
MCK[n] skew to MCK[m]	$t_{MCKSKEW2}$	—	150	ps	4
ADDR/CMD output valid	t_{DDKHOV}	—	3	ns	5
ADDR/CMD output invalid	t_{DDKHOX}	1	—	ns	5

Table 7. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
Write CMD to first MDQS capture edge	t_{DDSHMH}	t_{MCK} + 1.5	t_{MCK} + 4.0	ns	6
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}	0.25 × t_{MCK} – 0. 6	—	ns	7
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}	0.25 × t_{MCK} – 0.6	—	ns	7
MDQS preamble start	t_{DDSHMP}	0.75 × t_{MCK} + 1.5	0.75 × t_{MCK} + 4.0	ns	8
MDQS epilogue end	t_{DDSHME}	0.25 × t_{MCK} + 1.5	0.25 × t_{MCK} + 4.0	ns	8

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (OX or DX). For example, t_{DDKHOV} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (O) are valid (V) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. Maximum possible clock skew between a clock MCK[n] and its relative inverse clock $\overline{\text{MCK}}$[n]. Skew measured between complementary signals at GV_{DD}/2.
4. Maximum possible clock skew between a clock MCK[m] and a relative clock MCK[n]. Skew measured between complementary signals at GV_{DD}/2.
5. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$ and MDQ/MECC/MDM/MDQS.
6. Note that t_{DDSHMH} follows the symbol conventions described in note 1. For example, t_{DDSHMH} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) until the MDQS signal is valid (MH). t_{DDSHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. These controls allow the relationship between the synchronous clock control timing and the source-synchronous DQS domain to be modified by the user. See the MPC8560 Reference Manual for a description of the timing modifications enabled by the use of these bits.
7. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8560.
8. All outputs are referenced to the rising edge of MSYNC_IN (S) at the pins of the MPC8560. Note that t_{DDSHMP} follows the symbol conventions described in note 1. For example, t_{DDSHMP} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) for the duration of the MDQS signal precharge period (MP).

Table 8. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	V	1
V_{OUT}	0.5 × GV_{DD}	V	2

Notes:

1. Data input threshold measurement point.
2. Data output measurement point.

Figure 6 shows the DDR SDRAM output timing diagram.

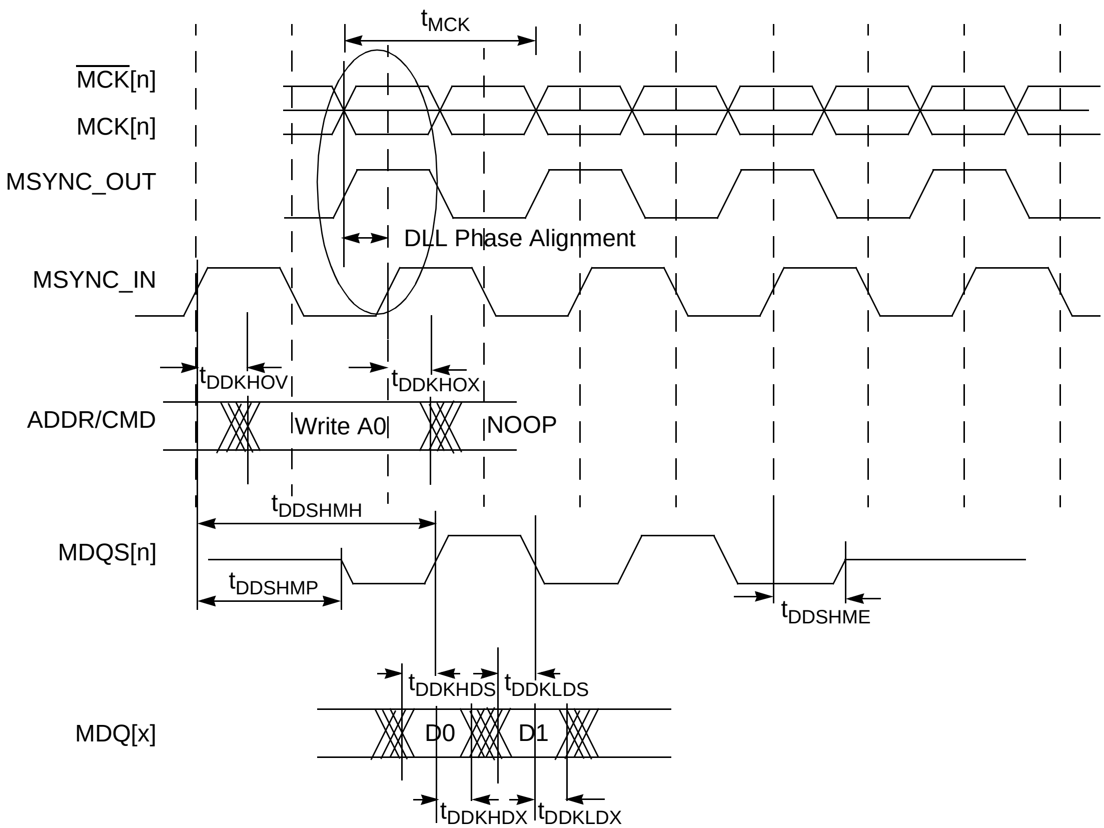


Figure 6. DDR SDRAM Output Timing Diagram

Table 9 provides approximate delay information that can be expected for the address and command signals of the DDR controller for various loadings. These numbers are the result of simulations for one topology. The delay numbers will strongly depend on the topology used. These delay numbers show the total delay for the address and command to arrive at the DRAM devices. The actual delay could be different than the delays seen in simulation, depending on the system topology. If a heavily loaded system is used, the DLL loop may need to be adjusted to meet setup requirements at the DRAM.

Table 9. Expected Delays for Address/Command

Load	Delay	Unit
4 devices (12 pF)	3.0	ns
9 devices (27 pF)	3.6	ns
36 devices (108 pF) + 40 pF compensation capacitor	5.0	ns
36 devices (108 pF) + 80 pF compensation capacitor	5.2	ns

1.6 Ethernet: Three-Speed, 10/100, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100, and MII management.

1.6.1 Three-Speed Ethernet Controller (TSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with the IEEE 802.3 standard. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 1.6.3, "Ethernet Management Interface Electrical Characteristics."

1.6.1.1 TSEC DC Electrical Characteristics

All GMII,MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 10 and Table 11. The potential applied to the input of a GMII,MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver's power supply (i.e., a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 10. GMII, MII, and TBI DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}	—		3.13	3.47	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.10	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—	—	1.70	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input high current	I_{IH}	LV_{DD} = Max	V_{IN} [1] = 2.1 V	—	40	μA
Input low current	I_{IL}	LV_{DD} = Max	V_{IN} [1] = 0.5 V	–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 11. RGMII and RTBI DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.70	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} =Min	–0.3	0.70	V
Input high current	I_{IH}	LV_{DD} = Max	V_{IN} [1] = 2.5 V	—	10	μA
Input low current	I_{IL}	LV_{DD} = Max	V_{IN} [1] = 0.4 V	–600	—	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1and Table 2.

1.6.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

1.6.2.1 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

1.6.2.1.1 GMII Transmit AC Timing Specifications

Table 12 provides the GMII transmit AC timing specifications.

Table 12. GMII Transmit AC Timing Specifications

At recommended operating conditions with GV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Input low voltage	V_{IL}	—	—	0.7	V
Input high voltage	V_{IH}	1.9	—	—	V
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	40	—	60	%
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise time, V_{IL}(min) to V_{IH}(max)	t_{GTXR}	—	—	1.0	ns
GTX_CLK data clock fall time, V_{IH}(max) to V_{IL}(min)	t_{GTXF}	—	—	1.0	ns
GTX_CLK125 clock period	t_{G125} [2]	—	8.0	—	ns

Table 12. GMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	—	50	—	%

Notes:
1. The symbols used for timing specifications herein follow the pattern $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol is used to represent the external GTX_CLK125 signal and does not follow the original symbol naming convention.

Figure 7 shows the GMII transmit AC timing diagram.

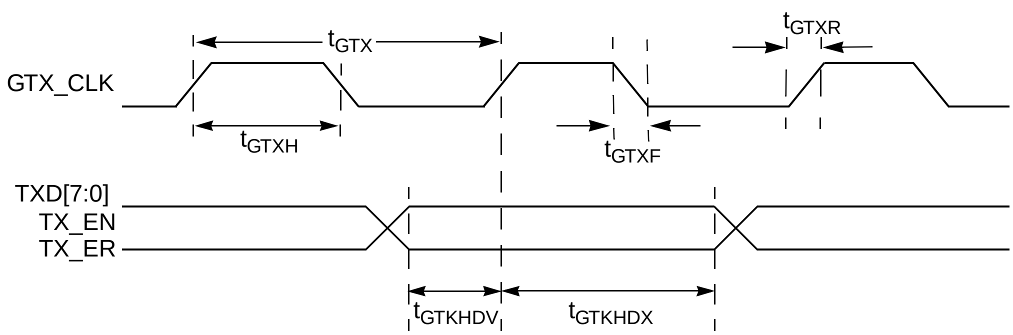


Figure 7. GMII Transmit AC Timing Diagram

1.6.2.1.2 GMII Receive AC Timing Specifications

Table 13 provides the GMII receive AC timing specifications.

Table 13. GMII Receive AC Timing Specifications

At recommended operating conditions with GV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Input low voltage	V_{IL}	—	—	0.7	V
Input high voltage	V_{IH}	1.9	—	—	V
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	ns
RXD[7:0], TX_DV, TX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], TX_DV, TX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise, V_{IL}(min) to V_{IH}(max)	t_{GRXR}	—	—	1.0	ns
RX_CLK clock fall time, V_{IH}(max) to V_{IL}(min)	t_{GRXF}	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 shows the GMII receive AC timing diagram.

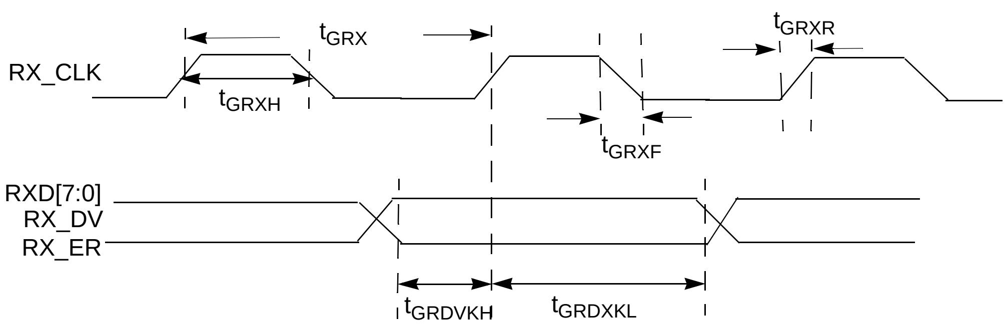


Figure 8. GMII Receive AC Timing Diagram

1.6.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

1.6.2.2.1 MII Transmit AC Timing Specifications

Table 14 provides the MII transmit AC timing specifications.

Table 14. MII Transmit AC Timing Specifications

At recommended operating conditions with GV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Input low voltage	V_{IL}	—	—	0.7	V
Input high voltage	V_{IH}	1.9	—	—	V
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_Clk to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X) . Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 9 shows the MII transmit AC timing diagram.

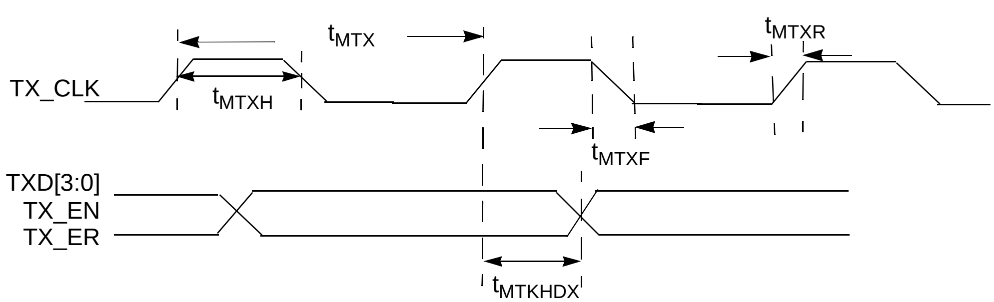


Figure 9. MII Transmit AC Timing Diagram

1.6.2.2.2 MII Receive AC Timing Specifications

Table 15 provides the MII receive AC timing specifications.

Table 15. MII Receive AC Timing Specifications

At recommended operating conditions with GV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Input low voltage	V_{IL}	—	—	0.7	V
Input high voltage	V_{IH}	1.9	—	—	V
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[7:0], TX_DV, TX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[7:0], TX_DV, TX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 shows the MII receive AC timing diagram.

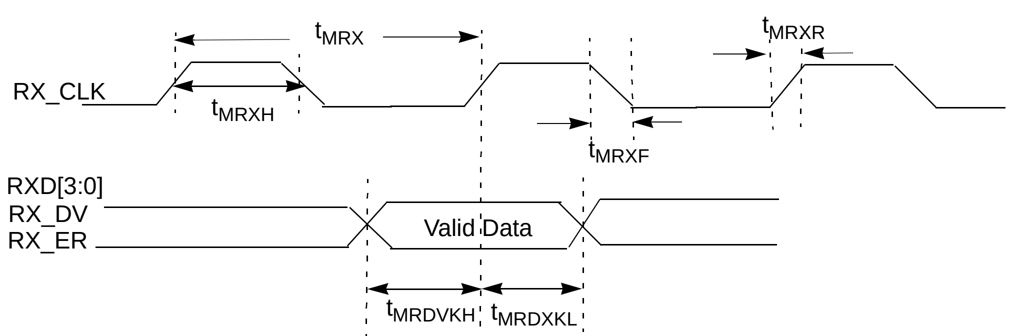


Figure 10. MII Receive AC Timing Diagram

1.6.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

1.6.2.3.1 TBI Transmit AC Timing Specifications

Table 16 provides the MII transmit AC timing specifications.

Table 16. TBI Transmit AC Timing Specifications

At recommended operating conditions with GV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	ns
GMII data TXD[7:0], TX_ER, TX_EN setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
GMII data TXD[7:0], TX_ER, TX_EN hold time from GTX_CLK going high	t_{TTKHDX}	0.0	—	—	ns
GMII data clock rise, V_{IL}(min) to V_{IH}(max)	t_{TTXR}	—	—	1.0	ns
GMII data clock fall time, V_{IH}(max) to V_{IL}(min)	t_{TTXF}	—	—	1.0	ns
GTX_CLK125 reference clock period	t_{G125} [2]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	—	50	—	ns

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention

Figure 11 shows the TBI transmit AC timing diagram.

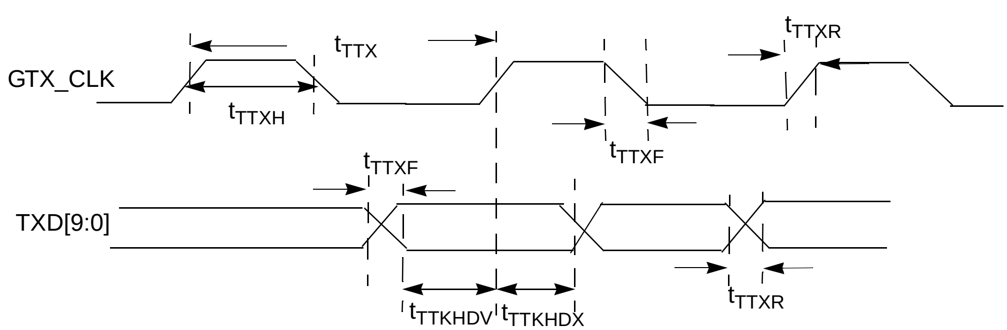


Figure 11. TBI Transmit AC Timing Diagram

1.6.2.3.2 TBI Receive AC Timing Specifications

Table 17 provides the TBI receive AC timing specifications.

Table 17. TBI Receive AC Timing Specifications

At recommended operating conditions with GV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
PMA_RX_CLK clock period	t_{TRX}		16.0		ns
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	ns
RXD[7:0], TX_DV, TX_ER setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RXD[7:0], TX_DV, TX_ER hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.5	—	—	ns
RX_CLK clock rise time V_{IL}(min) to V_{IH}(max)	t_{TRXR}	0.7	—	2.4	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{TRXF}	0.7	—	2.4	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).

Figure 12 shows the TBI receive AC timing diagram.

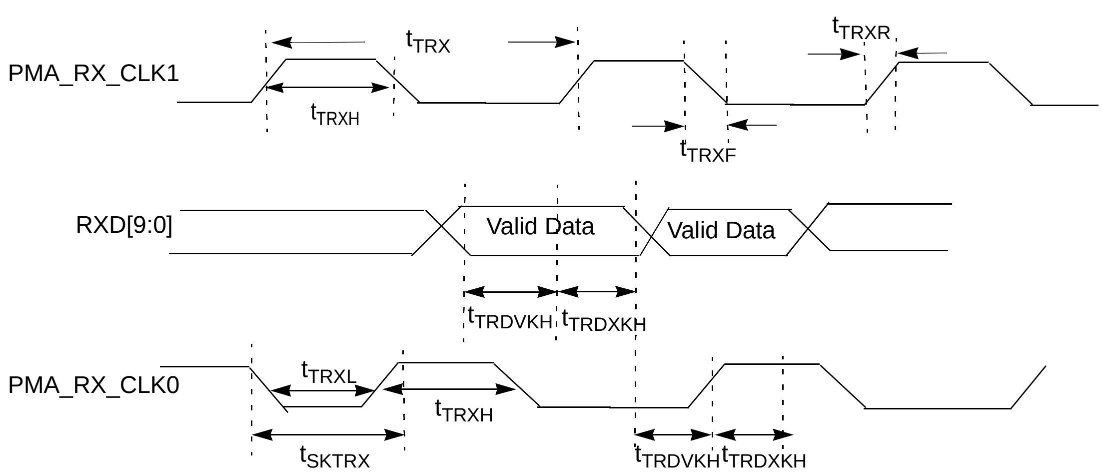


Figure 12. TBI Receive AC Timing Diagram

1.6.2.4 RGMII and RTBI AC Timing Specifications

Table 18 presents the RGMII and RTBI AC timing specifications.

Table 18. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–500	0	500	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12} [5]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	—	50	—	%

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.

Figure 13 shows the RBMII and RTBI AC timing and multiplexing diagrams.

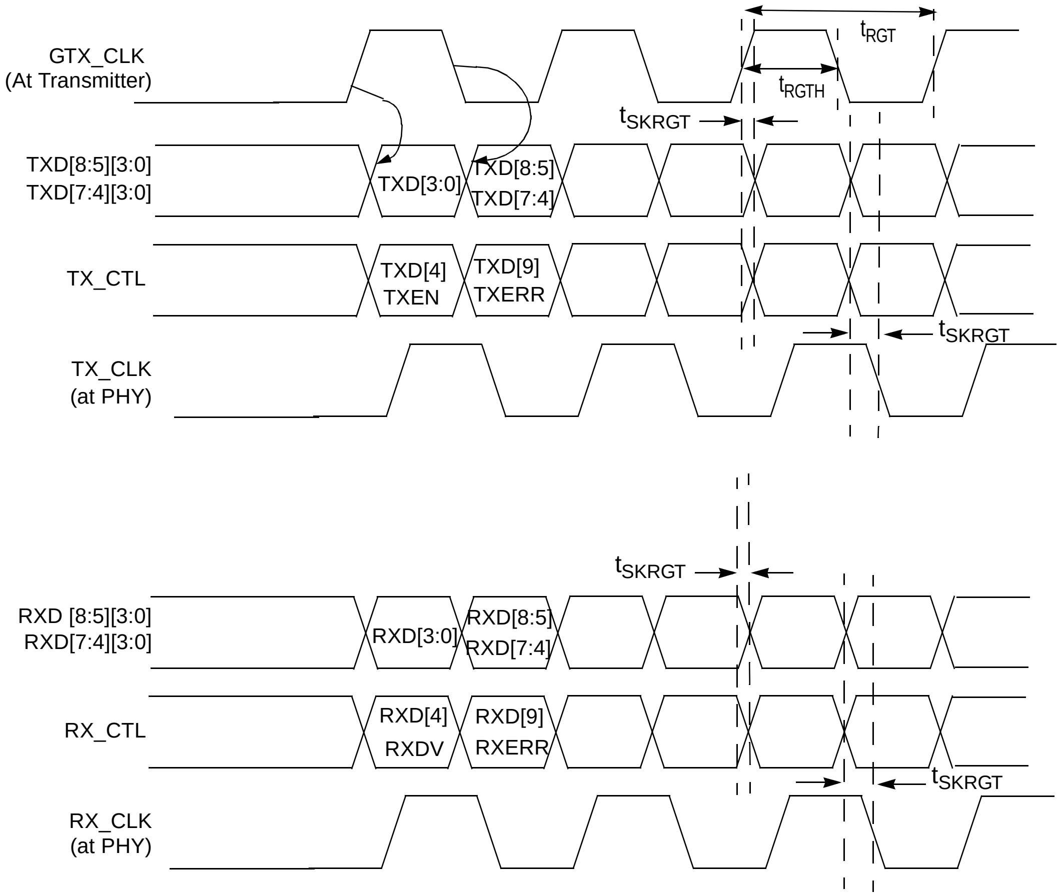


Figure 13. RGMII and RTBI AC Timing and Multiplexing Diagrams

1.6.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RBMII, TBI and RTBI are specified in Section 1.6.1, "Three-Speed Ethernet Controller (TSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

1.6.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 19.

Table 19. MII Management DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	LV_{DD}	—		3.13	3.47	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.10	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		1.70	—	V
Input low voltage	V_{IL}	—		—	0.90	V
Input high current	I_{IH}	LV_{DD} = Max	V_{IN} [1] = 2.1 V	—	40	μA
Input low current	I_{IL}	LV_{DD} = Max	V_{IN} = 0.5 V	–600	—	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

1.6.3.2 MII Management AC Electrical Specifications

Table 20 provides the MII management AC timing specificatons.

Table 20. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	2.5	—	12.5	MHz	2
MDC period	t_{MDC}	80	—	400	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO delay	t_{MDKHDX}	10	—	—	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	

Table 20. MII Management AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—	—	10	ns	

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{(first two letters of functional block)(signal)(state) (reference)(state)}$ for inputs and $t_{(first two letters of functional block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the system clock speed (i.e., for a system clock of 267 MHz, the delay is 70 ns and for a system clock of 333 MHz, the delay is 58 ns).
3. This parameter is dependent on the system clock speed (i.e., for a system clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz. For a system clock of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).

Figure 14 shows the MII management AC timing diagram.

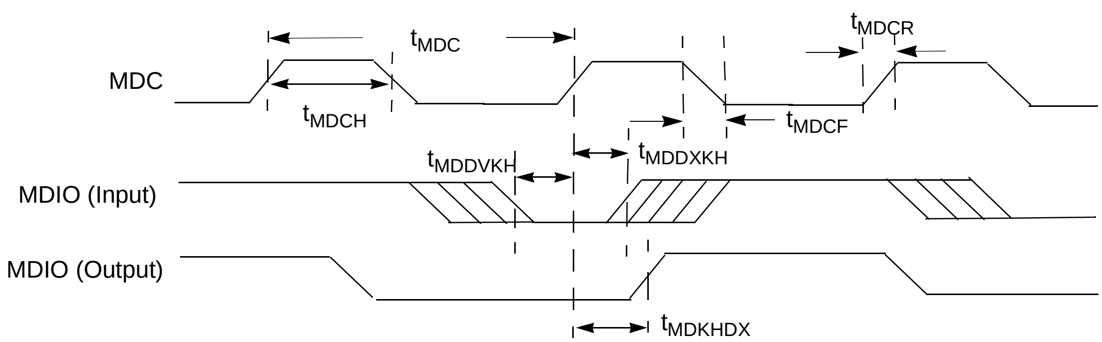


Figure 14. MII Management Interface Timing Diagram

1.7 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8560.

1.7.1 Local Bus DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the local bus interface.

Table 21. Local Bus DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
Input current	I_{IN}	V_{IN} [1] = 0 V or $V_{IN} = V_{DD}$	—	±5	μA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 μA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 μA	—	0.2	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

1.7.2 Local Bus AC Electrical Specifications

Table 22 describes the general timing parameters of the local bus interface of the MPC8560.

Table 22. Local Bus General Timing Parameters

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6.0	—	ns	2
DLL bypass mode only: local bus internal clock to LCLKO transition delay		t_{LBKHKT}	TBD	TBD	ns	2
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	1.5	—	ns	3, 4
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	1.0	—	ns	3, 4
TIMING RULE: input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1*}$	0	—	ns	
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	1.0	—	ns	3, 4
TIMING RULE: UPWAIT input hold from local bus clock		$t_{LBIXKH2*}$	0	—	ns	
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)		t_{LBOTOT}	1.0	—	ns	
TIMING RULE: LALE output transition to LAD[0:31] output transition (LATCH setup and hold time)		$t_{LBOTOT*}$	1.0	—	ns	

Table 22. Local Bus General Timing Parameters (continued)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output valid (except LAD/LDP and LALE)	LCS_B[3:4]=00	$t_{LBKHOV1}$	—	2.0	ns	5
	LCS_B[3:4]=11 (default)			3.5		
	LCS_B[3:4]=10			5.1		
	LCS_B[3:4]=01			5.8		
Local bus clock to data valid for LAD/LDP	LCS_B[3:4]=00	$t_{LBKHOV2}$	—	2.2	ns	5
	LCS_B[3:4]=11 (default)			3.7		3
	LCS_B[3:4]=10			5.3		
	LCS_B[3:4]=01			6.1		
Local bus clock to address valid for LAD	LCS_B[3:4]=00	$t_{LBKHOV3}$	—	2.3	ns	5
	LCS_B[3:4]=11 (default)			3.8		3
	LCS_B[3:4]=10			5.4		
	LCS_B[3:4]=01			6.2		
Output hold from local bus clock (except LAD/LDP and LALE)	LCS_B[3:4]=00	$t_{LBKHOX1}$	0.7	—	ns	5
	LCS_B[3:4]=11 (default)		1.6			3
	LCS_B[3:4]=10		2.5			
	LCS_B[3:4]=01		3.0			
Output hold from local bus clock for LAD/LDP	LCS_B[3:4]=00	$t_{LBKHOX2}$	0.7	—	ns	5
	LCS_B[3:4]=11 (default)		1.6			3
	LCS_B[3:4]=10		2.5			
	LCS_B[3:4]=01		3.0			
Output hold for LALE signal from local bus clock	LCS_B[3:4]=11 (default)	$t_{LBKHOX3}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	LCS_B[3:4]=00	$t_{LBKHOZ1}$	—	2.5	ns	5
	LCS_B[3:4]=11 (default)			3.8		6
	LCS_B[3:4]=10			5.4		
	LCS_B[3:4]=01			6.2		

Table 22. Local Bus General Timing Parameters (continued)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	LCS_B[3:4]=00	$t_{LBKHOZ2}$	—	2.5	ns	5
	LCS_B[3:4]=11 (default)			3.8		6
	LCS_B[3:4]=10			5.4		
	LCS_B[3:4]=01			6.2		

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for DLL enabled and internal local bus clock for DLL bypass mode.
3. All signals are measured from OV_{DD}/2 of the rising edge of LSYNC_IN for DLL enabled or Internal local bus clock for DLL bypass mode to 0.4 × OV_{DD} of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. **Caution**: This setting should **not** be used on Rev 1.X parts.
6. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 15 provides the AC test load for the local bus.

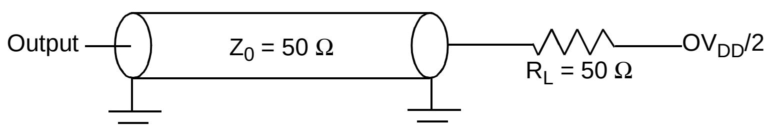


Figure 15. Local Bus C Test Load

Figure 16 to Figure 20 show the local bus signals.

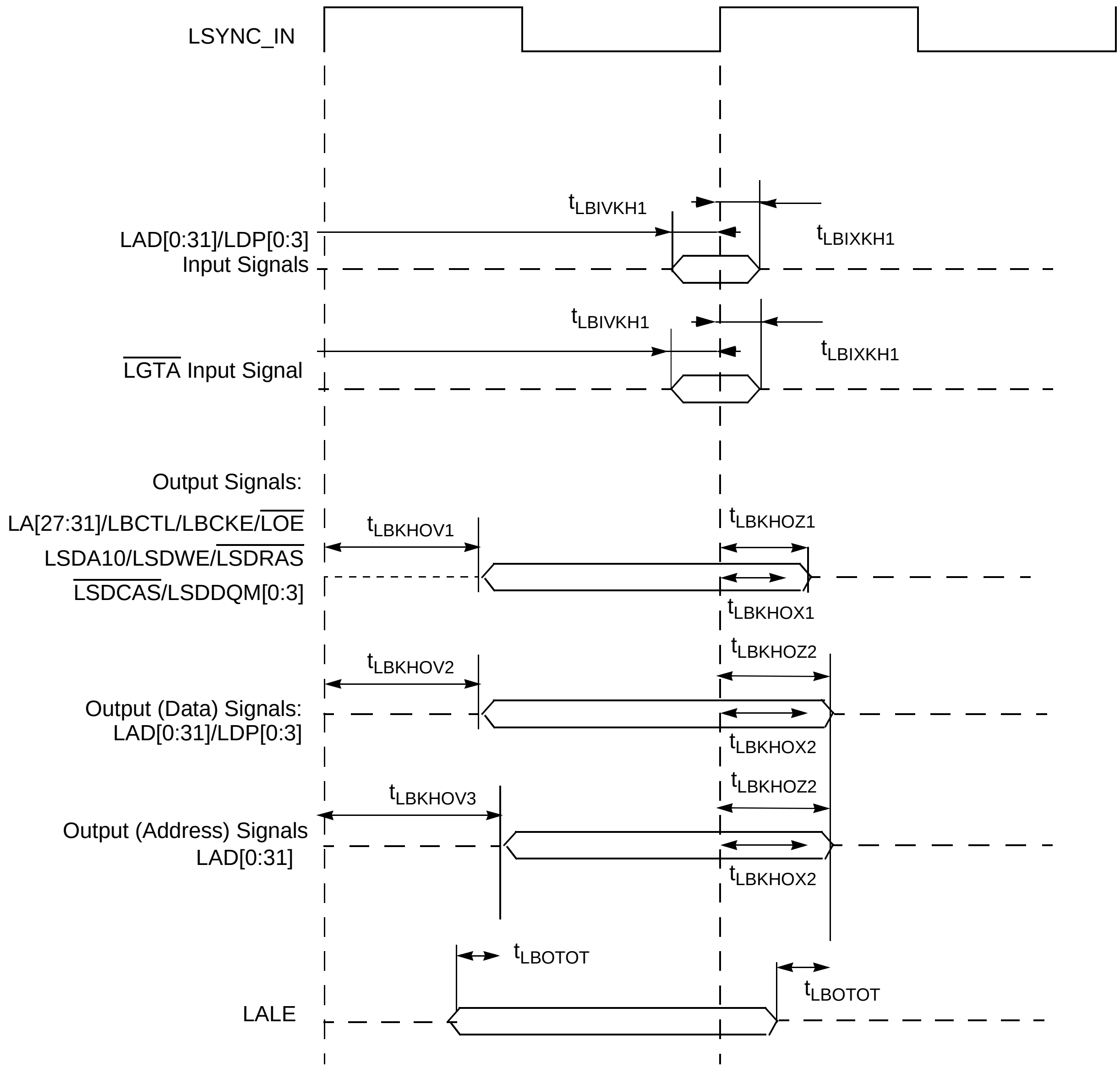


Figure 16. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

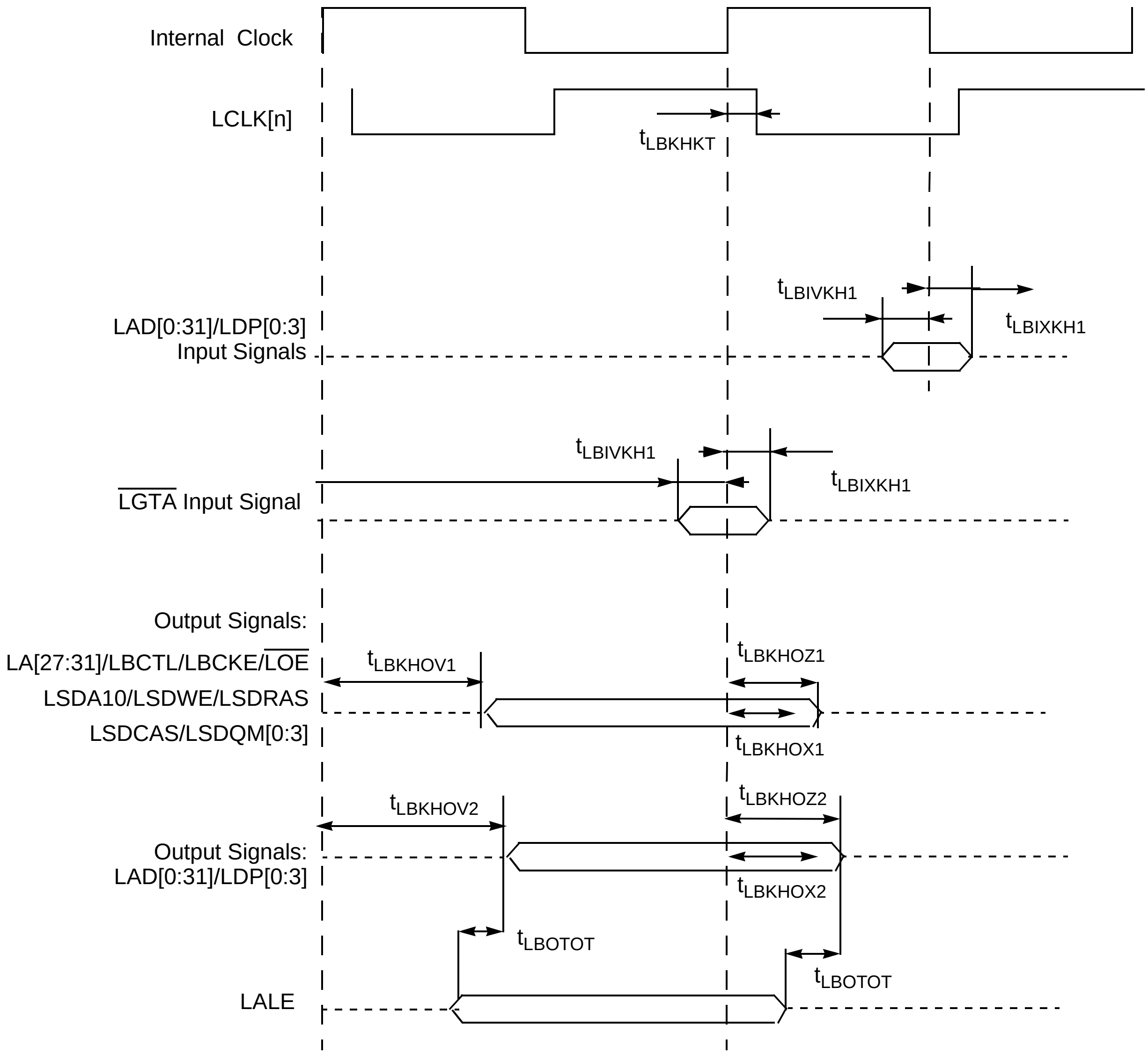


Figure 17. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)

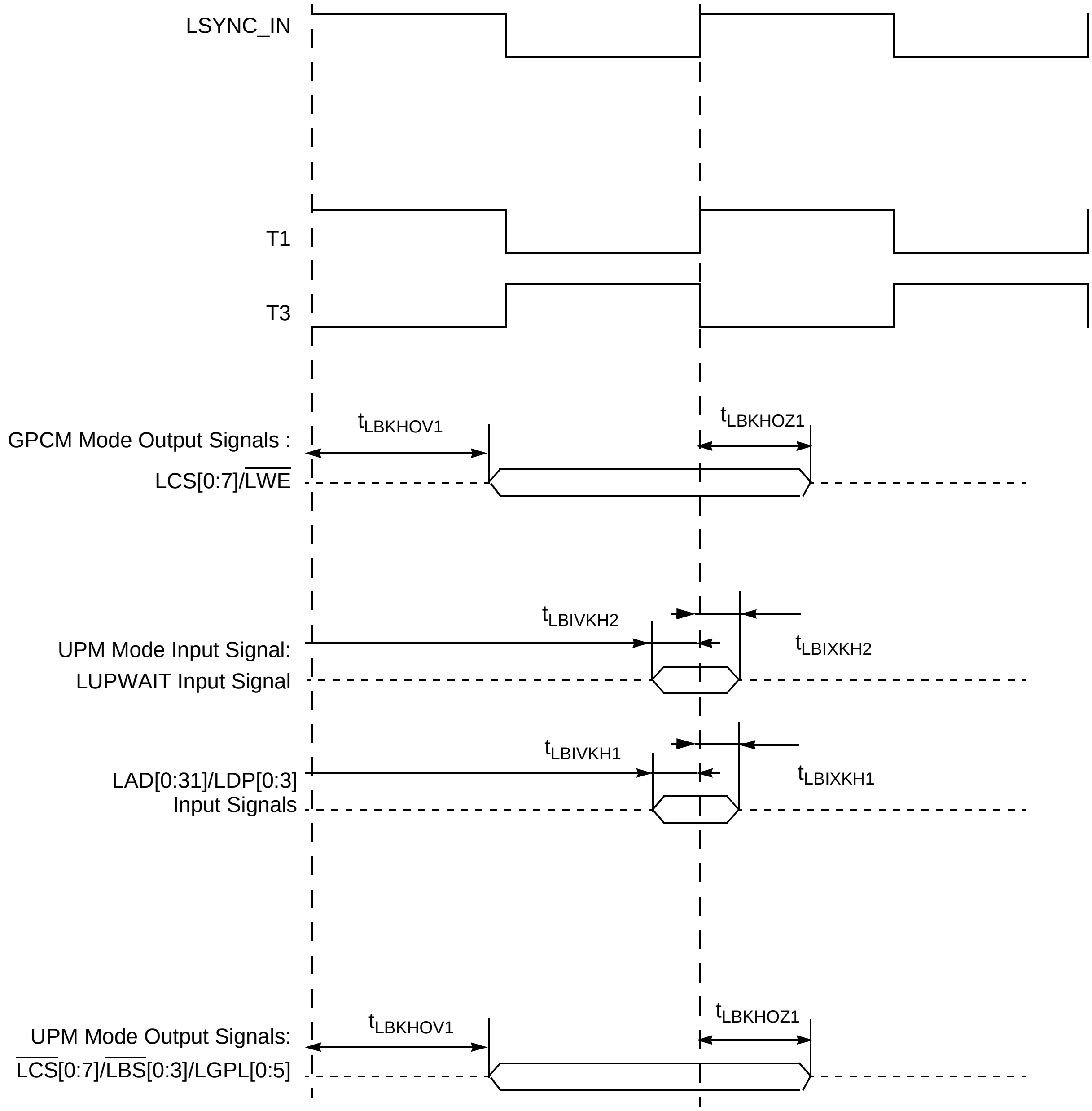


Figure 18. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

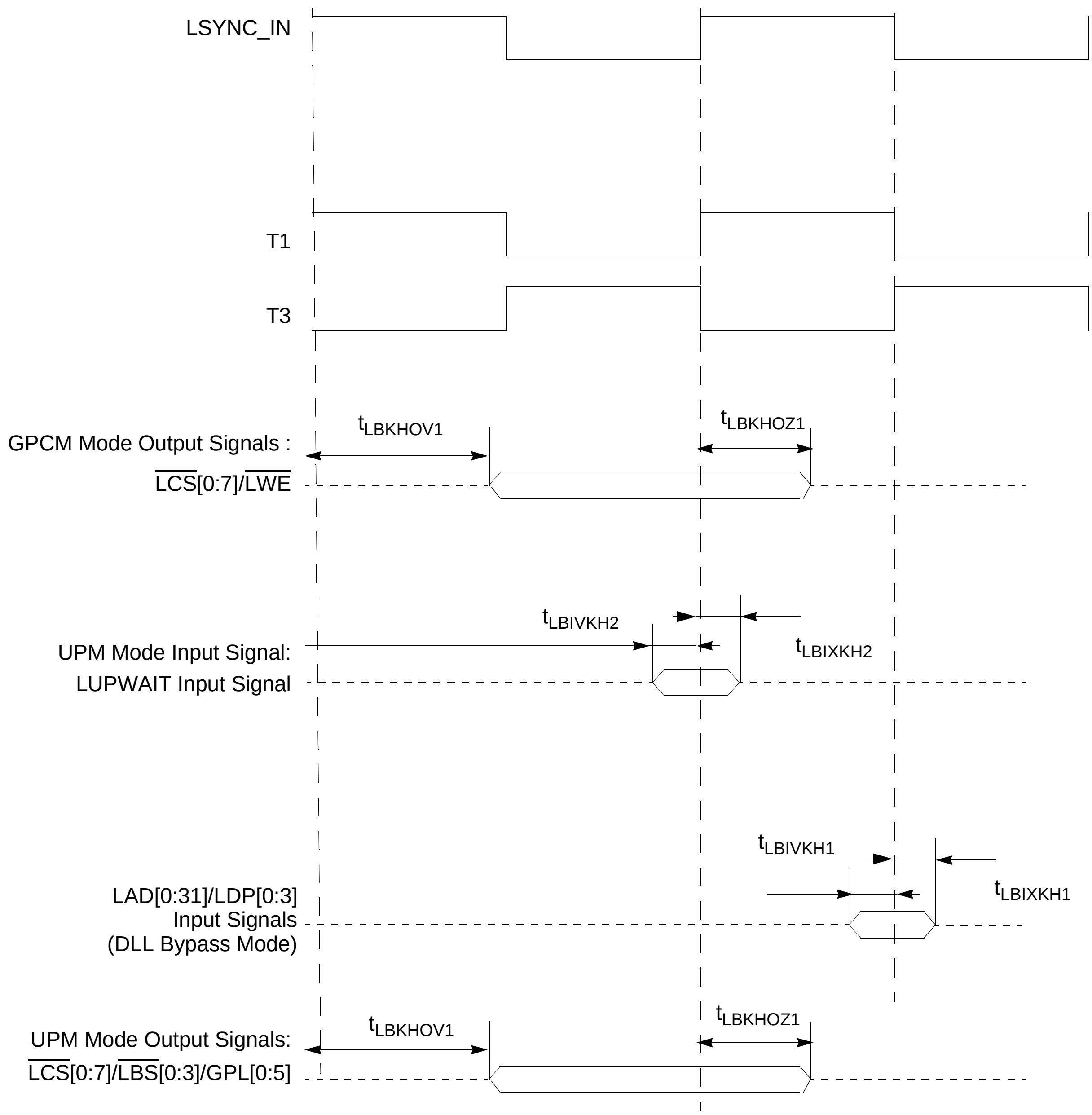


Figure 19. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

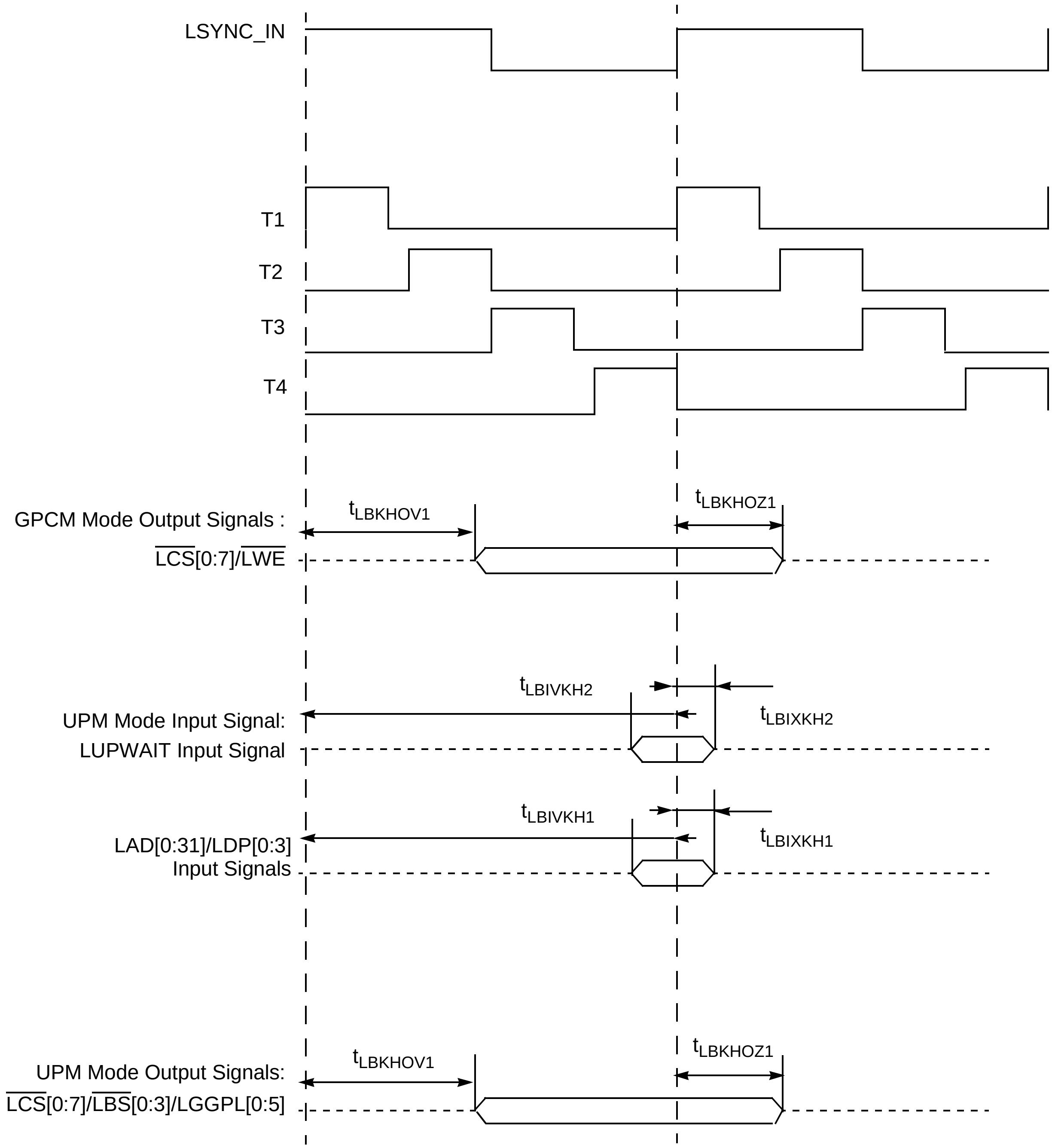


Figure 20. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Enabled)

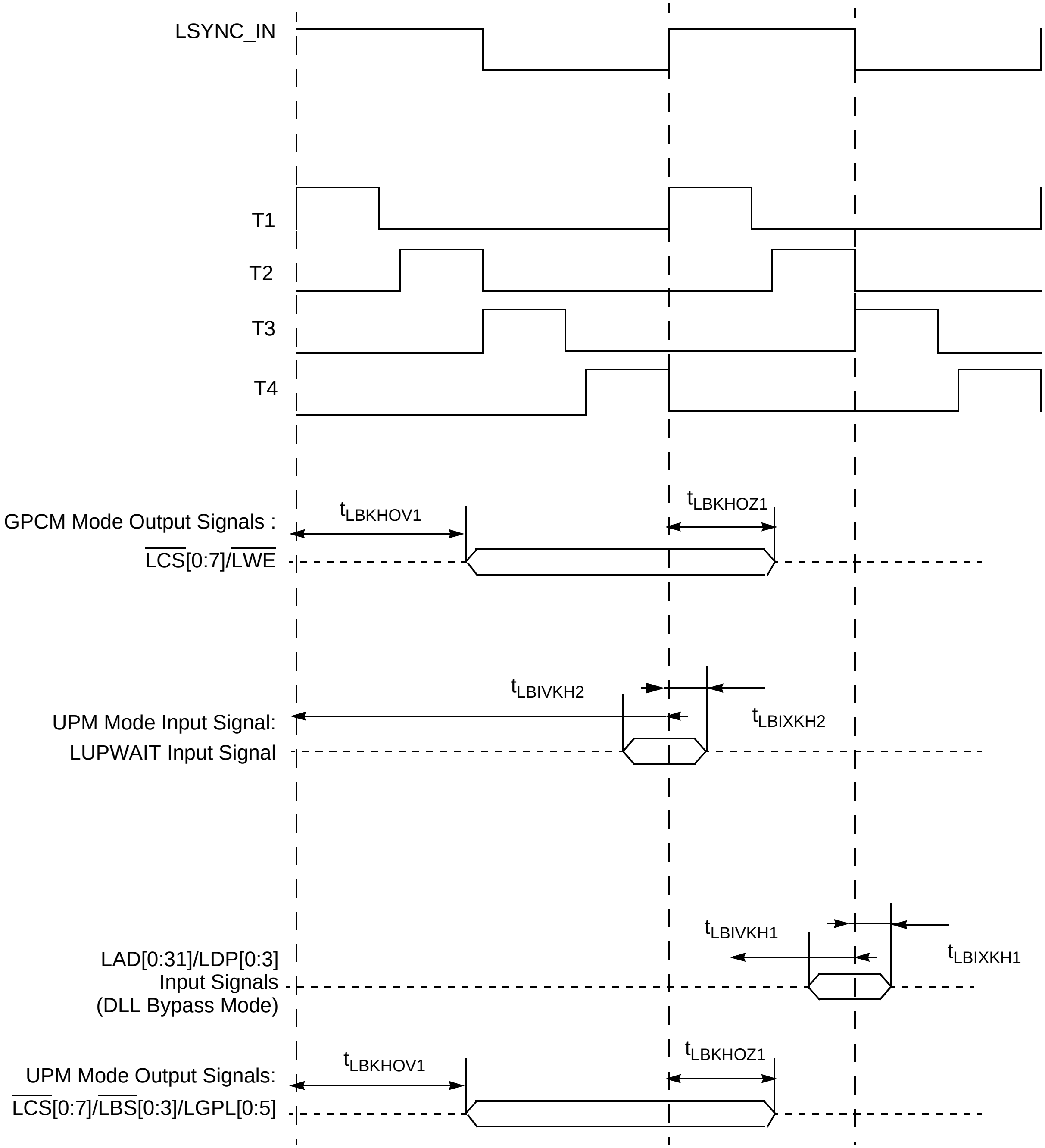


Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Bypass Mode)

1.8 CPM

This section describes the DC and AC electrical specifications for the CPM of the MPC8560.

1.8.1 CPM DC Electrical Characteristics

Table 23 provides the DC electrical characteristics for the MPC8560 CPM.

Table 23. CPM DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V	1
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1

Note: This specification applies to the following UTOPIA pins: PA[0–31], PB[4–31], PC[0–31], PD[4–31].

1.8.2 CPM AC Timing Specifications

Table 24 and Table 25 provide the CPM input and output AC timing specifications, respectively.

Table 24. CPM Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Typ [3]	Unit
FCC inputs—internal clock (NMSI) input setup time	t_{FIIVKH}	8	ns
FCC inputs—internal clock (NMSI) hold time	t_{FIIXKH}	0	ns
FCC inputs—external clock (NMSI) input setup time	t_{FEIVKH}	2.5	ns
FCC inputs—external clock (NMSI) hold time	t_{FEIXKH}b	2	ns
SCC/SMC/SPI/I2C inputs—internal clock (NMSI) input setup time	t_{NIIVKH}	16	ns
SCC/SMC/SPI/I2C inputs—internal clock (NMSI) input hold time	t_{NIIXKH}	0	ns
SCC/SMC/SPI/I2C inputs—external clock (NMSI) input setup time	t_{NEIVKH}	4	ns
SCC/SMC/SPI/I2C inputs—external clock (NMSI) input hold time	t_{NEIXKH}	2	ns
TDM inputs/SI—input setup time	t_{TDIVKH}	5	ns
TDM inputs/SI—hold time	t_{TDIXKH}	3	ns

Table 24. CPM Input AC Timing Specifications [1] (continued)

Characteristic	Symbol [2]	Typ [3]	Unit
COL width high (FCC)	t_{FCCH}	1.5	CLK

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{FIIVKH} symbolizes the FCC inputs internal timing (FI) with respect to the time the input signals (I) reaching the valid state (V) relative to the reference clock t_{FCC} (K) going to the high (H) state or setup time. And t_{TDIXKH} symbolizes the TDM timing (TD) with respect to the time the input signals (I) reach the invalid state (X) relative to the reference clock t_{FCC} (K) going to the high (H) state or hold time.
3. PIO and TIMER inputs and outputs are asynchronous to sysclk or any other externally visible clock. PIO/TIMER inputs are internally synchronized to the CPM internal clock. PIO/TIMER outputs should be treated as asynchronous.

Table 25. CPM Output AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
FCC outputs—internal clock (NMSI) delay	t_{FIKHOX}	1	5.5	ns
FCC outputs—external clock (NMSI) delay	t_{FEKHOX}	2	12	ns
SCC/SMC/SPI/I2C outputs—internal clock (NMSI) delay	t_{NIKHOX}	0.5	16	ns
SCC/SMC/SPI/I2C outputs—external clock (NMSI) delay	t_{NEKHOX}	2	16	ns
TDM outputs/SI delay	t_{TDKHOX}	3	12	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{FIKHOX} symbolizes the FCC inputs internal timing (FI) for the time t_{FCC} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 22 through Figure 27 represent the AC timing from Table 24 and Table 25. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 22 shows the FCC internal clock.

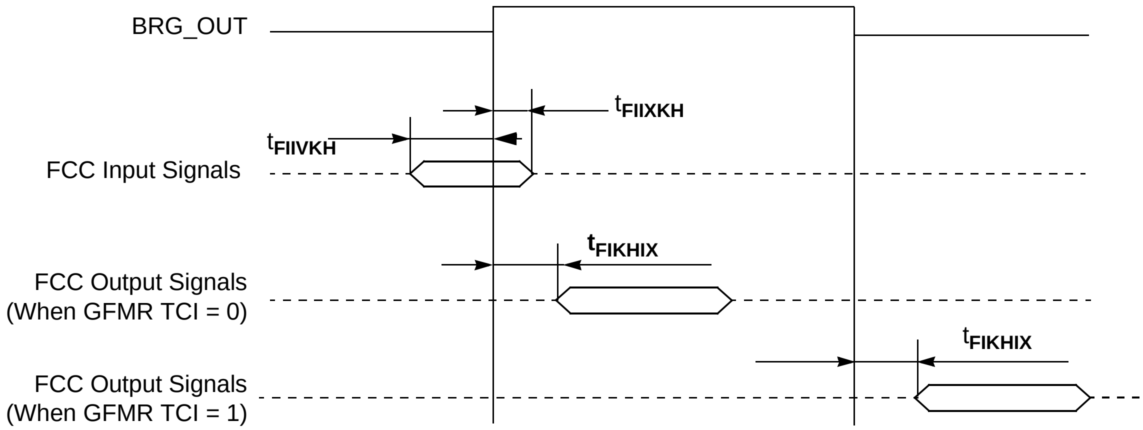


Figure 22. FCC Internal AC Timing Clock Diagram

Figure 23 shows the FCC external clock.

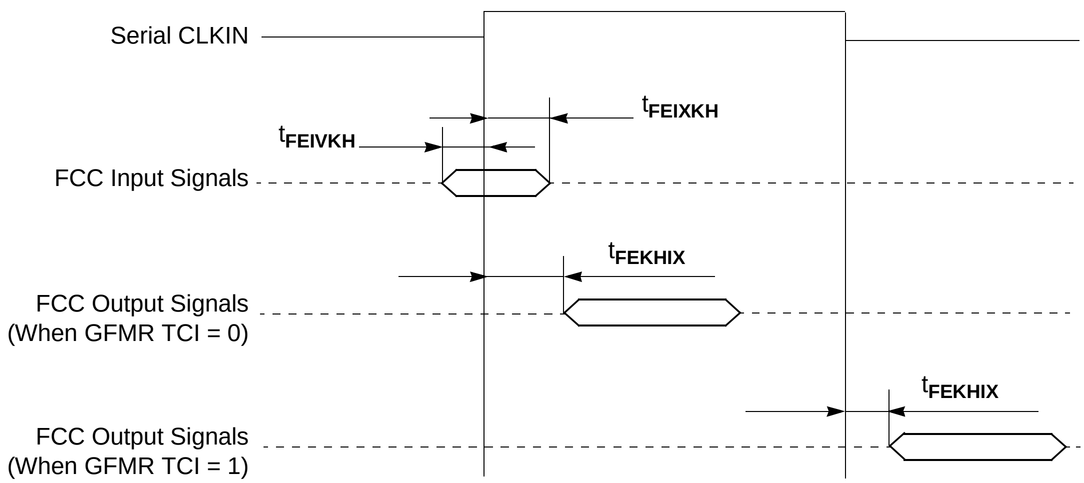


Figure 23. FCC External AC Timing Clock Diagram

Figure 24 shows Ethernet collision timing on FCCs.

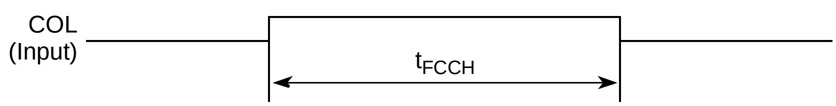
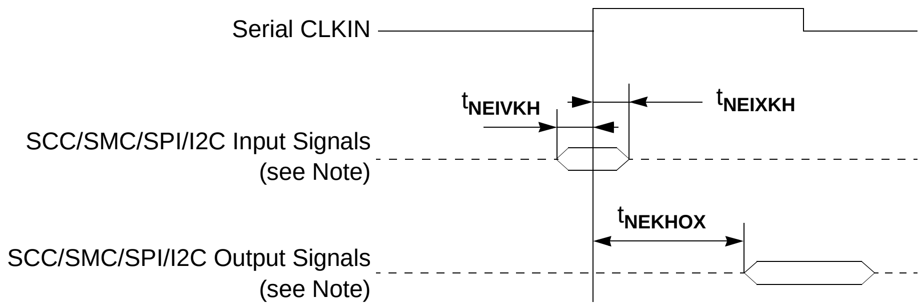


Figure 24. Ethernet Collision AC Timing Diagram (FCC)

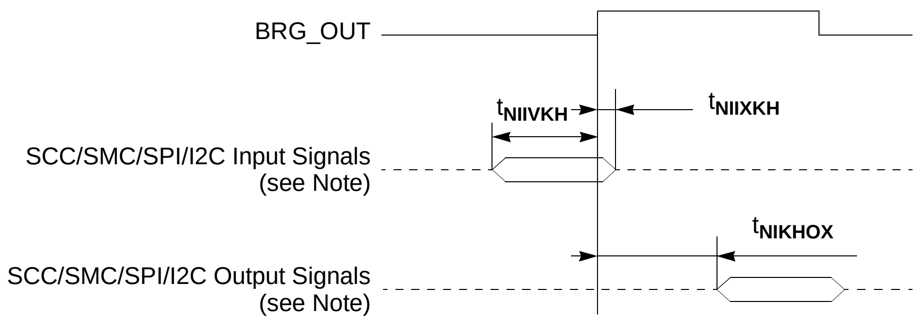
Figure 25 shows the SCC/SMC/SPI/I^{2}C external clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 25. SCC/SMC/SPI/I^{2}C AC Timing External Clock Diagram

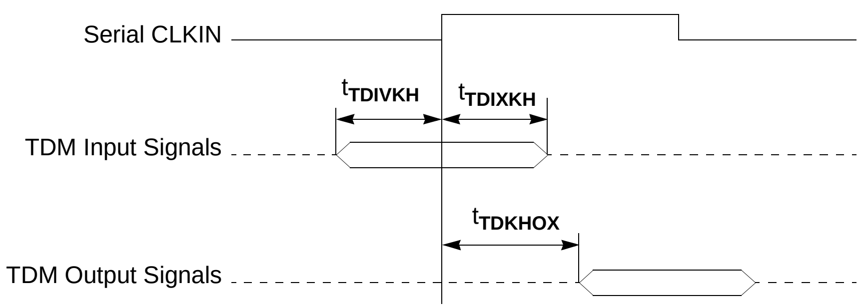
Figure 26 shows the SCC/SMC/SPI/I^{2}C internal clock.



Note: The clock edge is selectable on SCC and SPI.

Figure 26. SCC/SMC/SPI/I^{2}C AC Timing Internal Clock Diagram

Figure 27 shows TDM input and output signals.



Note: There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 27. TDM Signal AC Timing Diagram

1.9 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8560.

Table 26 provides the JTAG AC timing specifications as defined in Figure 29 through Figure 32.

Table 26. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 2)

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	 4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	 4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	 5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 TBD TBD	 TBD TBD	ns	 5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	 5, 6 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50–Ω load (see Figure 28). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

Figure 28 provides the AC test load for TDO and the boundary-scan outputs of the MPC8560.

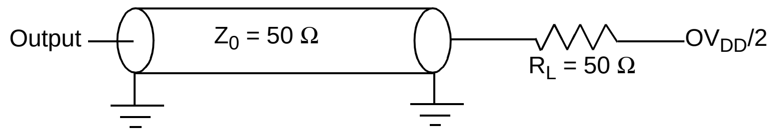


Figure 28. Alternate AC Test Load for the JTAG Interface

Figure 29 provides the JTAG clock input timing diagram.

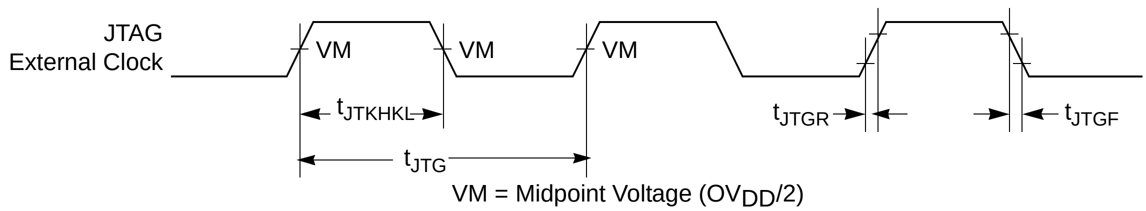


Figure 29. JTAG Clock Input Timing Diagram

Figure 30 provides the $\overline{\text{TRST}}$ timing diagram.

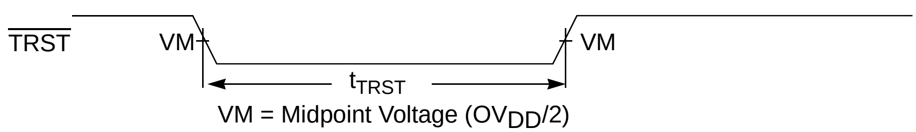


Figure 30. $\overline{\text{TRST}}$ Timing Diagram

Figure 31 provides the boundary-scan timing diagram.

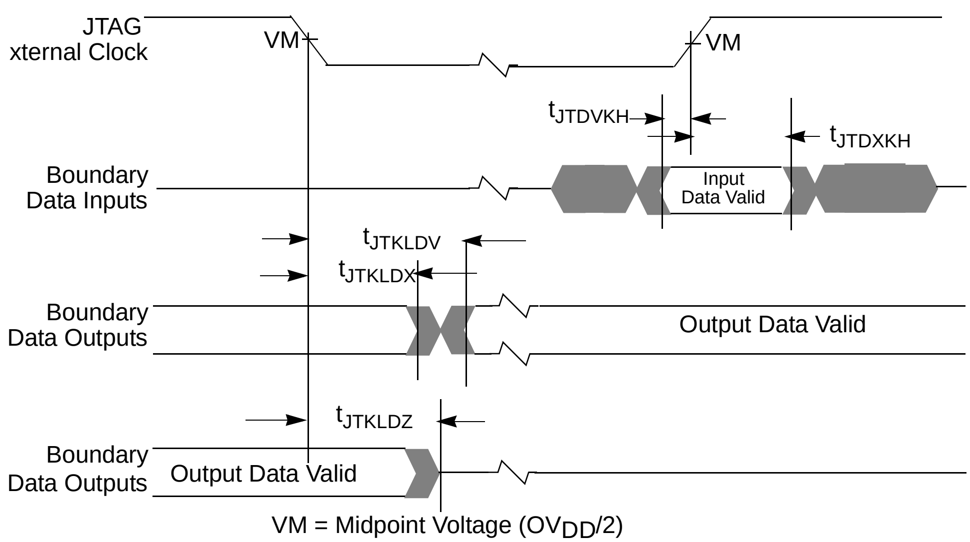


Figure 31. Boundary-Scan Timing Diagram

Figure 32 provides the test access port timing diagram.

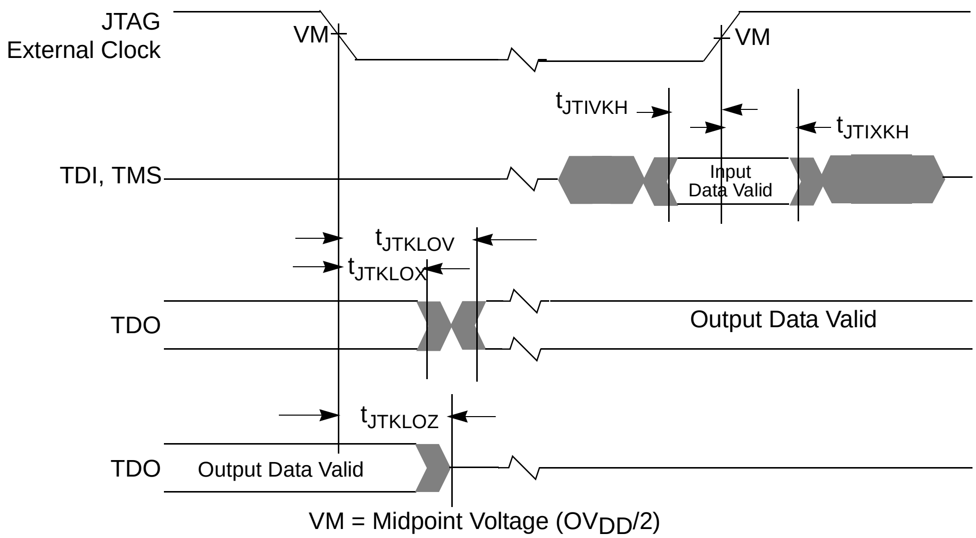


Figure 32. Test Access Port Timing Diagram

1.10 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interface of the MPC8560.

1.10.1 I^2C DC Electrical Characteristics

Table 27 provides the DC electrical characteristics for the I^2C interface of the MPC8560.

Table 27. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	OV_{DD}+ 0.3	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the MPC8560 Reference Manual for information on the digital filter used.
4. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

1.10.2 I^2C AC Electrical Specifications

Table 28 provides the AC timing parameters for the I^2C interface of the MPC8560.

Table 28. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 27).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0 [2]	 — 0.9 [3]	μs

Table 28. I^2C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 27).

Parameter	Symbol [1]	Min	Max	Unit
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1\ C_b$ [4]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	$20 + 0.1\ C_b$ [4]	300	ns
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^2C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^2C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8560 provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

Figure 33 shows the AC timing diagram for the I^2C bus.

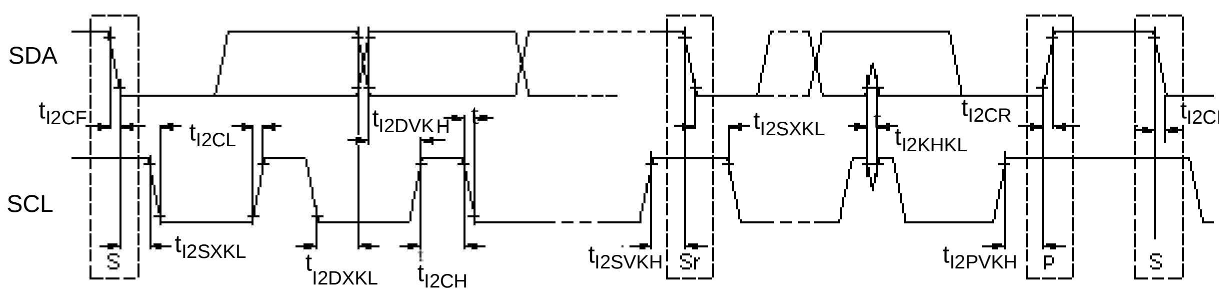


Figure 33. I^2C Bus AC Timing Diagram

1.11 PCI/PCI-X

This section describes the DC and AC electrical specifications for the PCI/PCI-X bus of the MPC8560.

1.11.1 PCI/PCI-X DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the PCI/PCI-X interface of the MPC8560.

Table 29. PCI/PCI-X DC Electrical Characteristics [1]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or $V_{OUT} \leq V_{OL}$ (max)	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}	V_{IN} [2] = 0 V or $V_{IN} = V_{DD}$	—	±5	μA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 μA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 μA	—	0.2	V

Notes:
1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

1.11.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus of the MPC8560. Table 30 provides the PCI AC timing specifications at 66 MHz.

Table 30. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	—	6.0	ns	2, 3
Output hold from SYSCLK	t_{PCKHOX}	2.0	—	ns	2
SYSCLK to output high impedence	t_{PCKHOZ}	—	14	ns	2, 4
Input setup to SYSCLK	t_{PCIVKH}	3.0	—	ns	2, 5
Input hold from SYSCLK	t_{PCIXKH}	0	—	ns	2, 5
$\overline{REQ64}$ to $\overline{HRESET}$ [9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	6, 7
$\overline{HRESET}$ to $\overline{REQ64}$ hold time	t_{PCRHRX}	0	50	ns	7

Table 30. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	8

Notes:
1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI/PCI-X timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI/PCI-X timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 1.14, “Clocking.”
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.

Figure 34 shows the PCI/PCI-X input AC timing conditions.

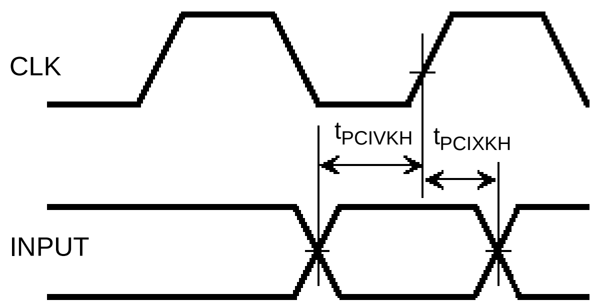


Figure 34. PCI-PCI-X Input AC Timing Measurement Conditions

Figure 35 shows the PCI/PCI-X output AC timing conditions.

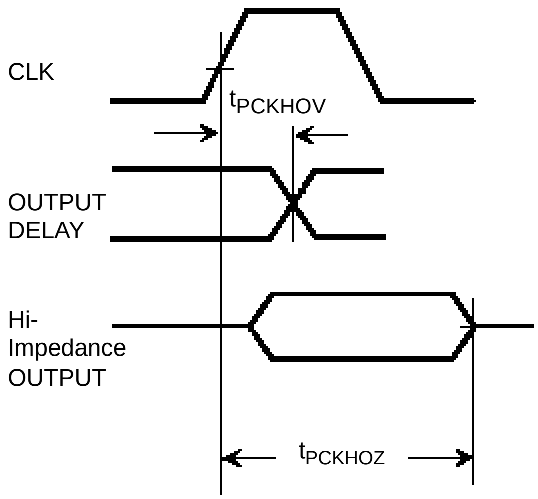


Figure 35. PCI-PCI-X Output AC Timing Measurement Condition

Table 31 provides the PCI-X AC timing specifications at 66 MHz.

Table 31. PCI-X AC Timing Specifications at 133 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	—	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t_{PCKHOX}	0.7	—	ns	1
SYSCLK to output high impedence	t_{PCKHOZ}	—	7	ns	1, 4, 8
Input setup time to SYSCLK	t_{PCIVKH}	1.2	—	ns	3, 5
Input hold time from SYSCLK	t_{PCIXKH}	0.5	—	ns	
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ setup time	t_{PCRVRH}	10	—	clocks	
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	9
PCI-X initialization pattern to $\overline{\text{HRESET}}$ setup time	t_{PCIVRH}	10	—	clocks	

Table 31. PCI-X AC Timing Specifications at 133 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ to PCI-X initialization pattern hold time	t_{PCRHIX}	0	50	ns	6

Notes:
1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.
2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
3. Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
6. Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.
7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
8. Device must meet this specification independent of how many outputs switch simultaneously.
9. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*

1.12 RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8560.

1.12.1 RapidIO DC Electrical Characteristics

RapidIO driver and receiver DC electrical characteristics are provided in Table 32 and Table 33, respectively.

Table 32. RapidIO 8/16 LP-LVDS Driver DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Characteristic	Symbol	Min	Max	Unit	Notes
Differential output high voltage	V_{OHD}	247	454	mV	1, 2
Differential output low voltage	V_{OLD}	–454	–247	mV	1, 2
Differential offset voltage	ΔV_{OSD}	—	50	mV	1,3
Output high common mode voltage	V_{OHCM}	1.125	1.375	V	1, 4
Output low common mode voltage	V_{OLCM}	1.125	1.375	V	1, 5
Common mode offset voltage	ΔV_{OSCM}	—	50	mV	1, 6
Differential termination	R_{TERM}	90	220	Ω	
Short circuit current (either output)	$\|I_{SS}\|$	—	24	mA	7
Bridged short circuit current	$\|I_{SB}\|$	—	12	mA	8

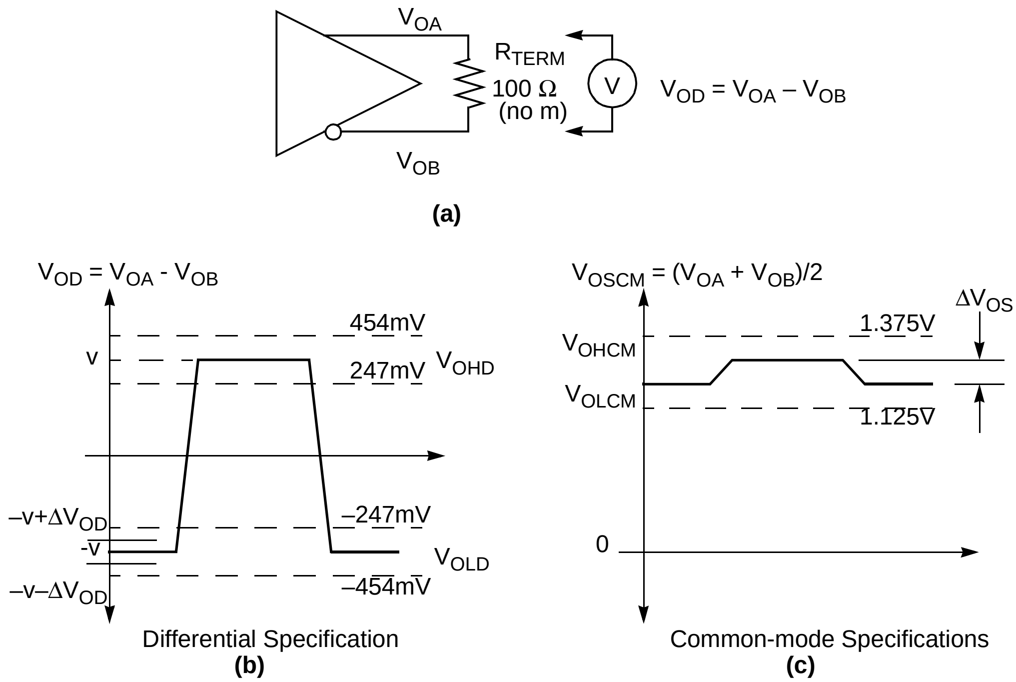
Notes:
1. Bridged 100-Ω load.
2. See Figure 36(a).
3. Differential offset voltage = $|V_{OHD}+V_{OLD}|$. See Figure 36(b).
4. $V_{OHCM} = (V_{OA} + V_{OB})/2$ when measuring V_{OHD}.
5. $V_{OLCM} = (V_{OA} + V_{OB})/2$ when measuring V_{OLD}.
6. Common mode offset $\Delta V_{OSCM} = |V_{OHCM} – V_{OLCM}|$. See Figure 36(c).
7. Outputs shorted to V_{DD} or GND.
8. Outputs shorted together.

Table 33. RapidIO 8/16 LP-LVDS Receiver DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit	Notes
Voltage at either input	V_I	0	2.4	V	
Differential input high voltage	V_{IHD}	100	600	mV	1
Differential input low voltage	V_{ILD}	–600	–100	mV	1
Common mode input range (referenced to receiver ground)	V_{ICM}	0.050	2.350	V	2
Input differential resistance	R_{IN}	90	110	Ω	

Notes:
1. Over the common mode range.
2. Limited by V_I. See Figure 43.

Figure 36 shows the DC driver signal levels.



Note: V_{OA} refers to voltage at output A; V_{OB} refers to voltage at output B.

Figure 36. DC Driver Signal Levels

1.12.2 RapidIO AC Electrical Specifications

This section contains the AC electrical specifications for a RapidIO 8/16 LP-LVDS device. The interface defined is a parallel differential low-power high-speed signal interface. Note that the source of the transmit clock on the RapidIO interface is dependent on the settings of the LGPL[0:1] signals at reset. Note that the default setting makes the core complex bus (CCB) clock the source of the transmit clock. See Chapter 4 of the Reference Manual for more details on reset configuration settings.

1.12.3 RapidIO Concepts and Definitions

This section specifies signals using differential voltages. Figure 37 shows how the signals are defined. The figure shows waveforms for either a transmitter output (TD and $\overline{TD}$) or a receiver input (RD and $\overline{RD}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- The transmitter output and receiver input signals TD, $\overline{TD}$, RD, and $\overline{RD}$ each have a peak-to-peak swing of A-B volts.
- The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} – V_{\overline{TD}}$.
- The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} – V_{\overline{RD}}$.
- The differential output signal of the transmitter, or input signal of the receiver, ranges from A – B volts to – (A – B) volts.
- The peak differential signal of the transmitter output, or receiver input, is A – B volts.

- The peak-to-peak differential signal of the transmitter output, or receiver input, is $2 \times (A - B)$ volts.

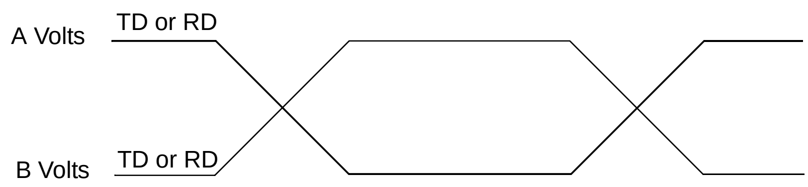


Figure 37. Differential Peak-to-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using numerical values, consider the case where a LVDS transmitter has a common mode voltage of 1.2 V and each signal has a swing that goes between 1.4 and 1.0 V. Using these values, the peak-to-peak voltage swing of the signals TD, $\overline{TD}$, RD, and $\overline{RD}$ is 400 mV. The differential signal ranges between 400 mV and –400 mV. The peak differential signal is 400 mV, and the peak-to-peak differential signal is 800 mV.

A timing edge is the zero-crossing of a differential signal. Each skew timing parameter on a parallel bus is synchronously measured on two signals relative to each other in the same cycle, such as data to data, data to clock, or clock to clock. A skew timing parameter may be relative to the edge of a signal or to the middle of two sequential edges.

Static skew represents the timing difference between signals that does not vary over time regardless of system activity or data pattern. Path length differences are a primary source of static skew.

Dynamic skew represents the amount of timing difference between signals that is dependent on the activity of other signals and varies over time. Crosstalk between signals is a source of dynamic skew.

Eye diagrams and compliance masks are a useful way to visualize and specify driver and receiver performance. This technique is used in several serial bus specifications. An example compliance mask is shown in Figure 38. The key difference in the application of this technique for a parallel bus is that the data is source synchronous to its bus clock while serial data is referenced to its embedded clock. Eye diagrams reveal the quality (cleanness, openness, goodness) of a driver output or receiver input. An advantage of using an eye diagram and a compliance mask is that it allows specifying the quality of a signal without requiring separate specifications for effects such as rise time, duty cycle distortion, data dependent dynamic skew, random dynamic skew, etc. This allows the individual semiconductor manufacturer maximum flexibility to trade off various performance criteria while keeping the system performance constant.

In using the eye pattern and compliance mask approach, the quality of the signal is specified by the compliance mask. The mask specifies the maximum permissible magnitude of the signal and the minimum permissible eye opening. The eye diagram for the signal under test is generated according to the specification. Compliance is determined by whether the compliance mask can be positioned over the eye diagram such that the eye pattern falls entirely within the unshaded portion of the mask.

Serial specifications have clock encoded with the data, but the LP-LVDS physical layer defined by RapidIO is a source synchronous parallel port so additional specifications to include effects that are not found in serial links are required. Specifications for the effect of bit to bit timing differences caused by static skew have been added and the eye diagrams specified are measured relative to the associated clock in order to include clock to data effects. With the transmit output (or receiver input) eye diagram, the user can determine if the transmitter output (or receiver input) is compliant with an oscilloscope with the appropriate software.

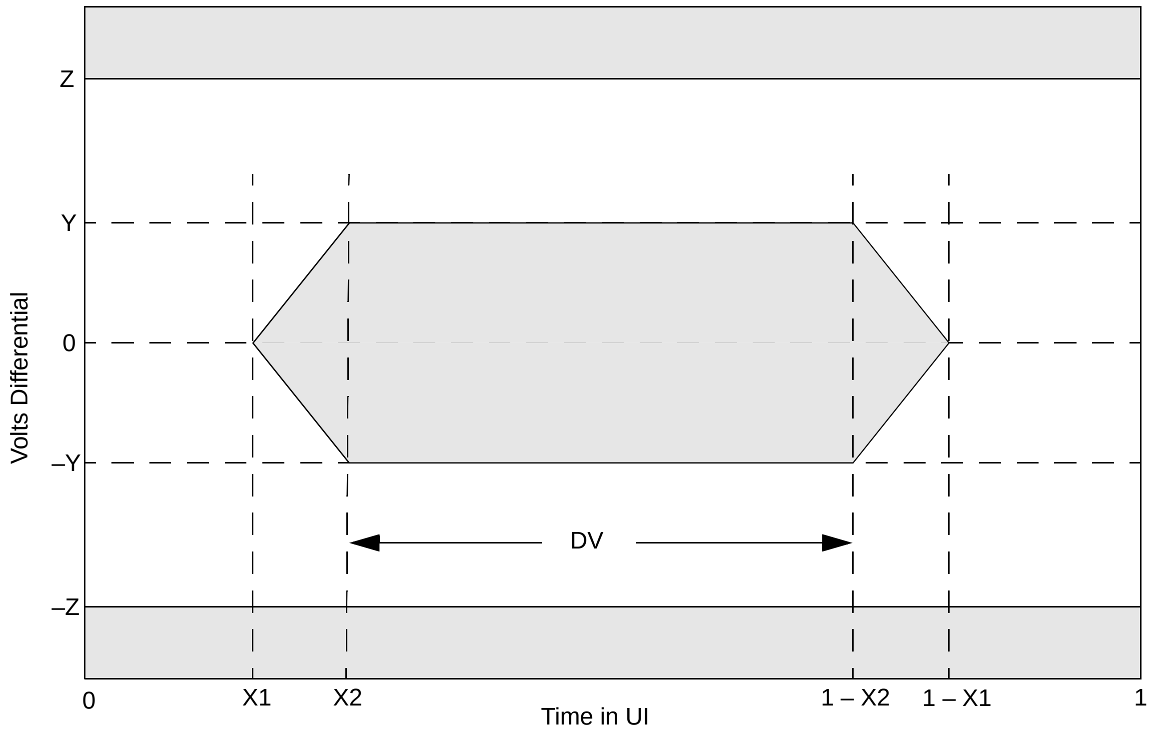


Figure 38. Example Compliance Mask

Y = minimum data valid amplitude

Z = maximum amplitude

1 UI = 1 unit interval = 1/baud rate

X1 = end of zero crossing region

X2 = beginning of data valid window

DV = data valid window = 1 – 2 × X2

The waveform of the signal under test must fall within the unshaded area of the mask to be compliant. Different masks are used for the driver output and the receiver input allowing each to be separately specified.

1.12.3.1 RapidIO Driver AC Timing Specifications

Driver AC timing specifications are provided in Table 34, Table 35, and Table 36. A driver shall comply with the specifications for each data rate/frequency for which operation of the driver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The output of a driver shall be connected to a 100 Ω, ±1%, differential (bridged) resistive load.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7]).

Table 34. RapidIO Driver AC Timing Specifications—500 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	1
Differential output low voltage	V_{OLD}	–540	–200	mV	1
Duty cycle	DC	48	52	%	2
V_{OD} rise time, 20%–80% of peak-to-peak differential signal swing	t_{FALL}	200	—	ps	3
V_{OD} fall time, 20%–80% of peak-to-peak differential signal swing	t_{RISE}	200	—	ps	
Data valid	DV	1260	—	ps	
Skew of any two data outputs	t_{DPAIR}	—	180	ps	4
Skew of single data outputs to associated clock	$t_{SKEW,PAIR}$	–180	180	ps	5

Notes:
1. See Figure 39.
2. Requires ±100 ppm long term frequency stability.
3. Measured at V_{OD} = 0 V.
4. Measured using the RapidIO transmit mask shown in Figure 39.
5. See Figure 44.

Table 35. RapidIO Driver AC Timing Specifications—750 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	1
Differential output low voltage	V_{OLD}	–540	–200	mV	1
Duty cycle	DC	48	52	%	2
V_{OD} rise time, 20%–80% of peak-to-peak differential signal swing	t_{FALL}	133	—	ps	3
V_{OD} fall time, 20%–80% of peak-to-peak differential signal swing	t_{RISE}	133	—	ps	
Data valid	DV	800	—	ps	
Skew of any two data outputs	t_{DPAIR}	—	133	ps	4
Skew of single data outputs to associated clock	$t_{SKEW,PAIR}$	–133	133	ps	5

Notes:
1. See Figure 39.
2. Requires ±100 ppm long term frequency stability.
3. Measured at V_{OD} = 0 V.
4. Measured using the RapidIO transmit mask shown in Figure 39.
5. See Figure 44.

Table 36. RapidIO Driver AC Timing Specifications—1 Gbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	1
Differential output low voltage	V_{OLD}	–540	–200	mV	1
Duty cycle	DC	48	52	%	2
V_{OD} rise time, 20%–80% of peak to peak differential signal swing	t_{FALL}	100	—	ps	3
V_{OD} fall time, 20%–80% of peak to peak differential signal swing	t_{RISE}	100	—	ps	
Data valid	DV	575	—	ps	
Skew of any two data outputs	t_{DPAIR}	—	100	ps	4
Skew of single data outputs to associated clock	$t_{SKEW,PAIR}$	–100	100	ps	5

Notes:
1. See Figure 39.
2. Requires ±100 ppm long term frequency stability.
3. Measured at V_{OD} = 0 V.
4. Measured using the RapidIO transmit mask shown in Figure 39.
5. See Figure 44.

The compliance of driver output signals TD[0:15] and TFRAME with their minimum data valid window (DV) specification shall be determined by generating an eye pattern for each of the data signals and comparing the eye pattern of each data signal with the RapidIO transmit mask shown in Figure 39. The value of X2 used to construct the mask shall be (1 – DV_{min})/2. A signal is compliant with the data valid window specification if the transmit mask can be positioned on the signal's eye pattern such that the eye pattern falls entirely within the unshaded portion of the mask.

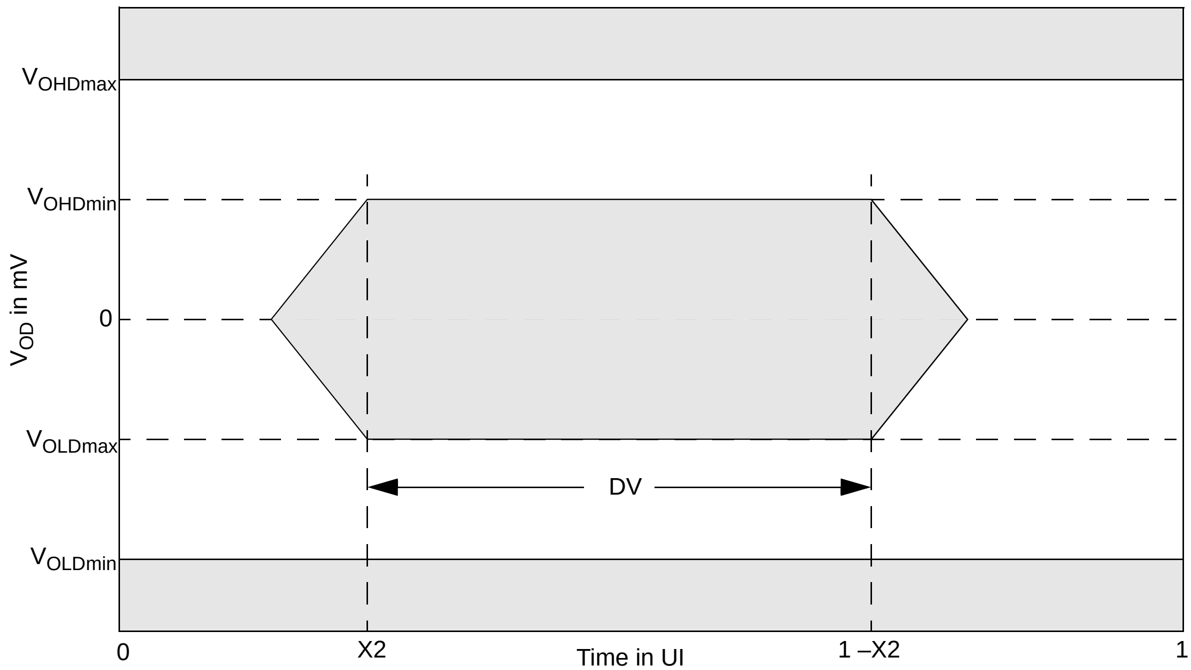


Figure 39. RapidIO Transmit Mask

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 40. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

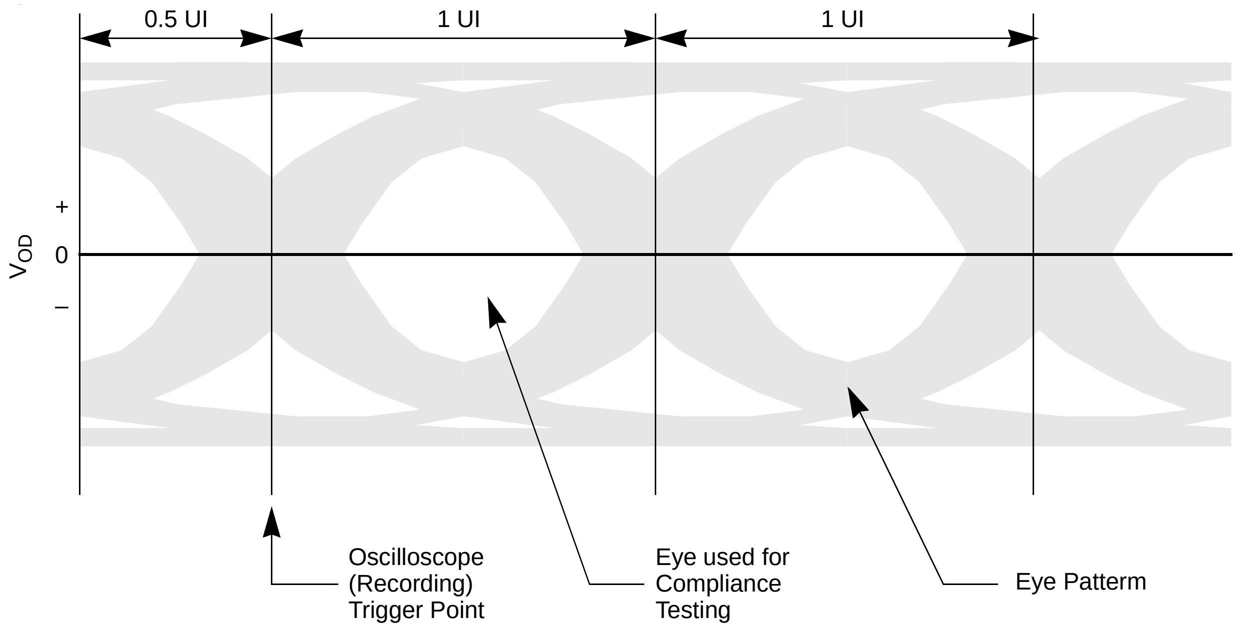


Figure 40. Example Driver Output Eye Pattern

1.12.3.2 RapidIO Receiver AC Timing Specifications

The RapidIO receiver AC timing specifications are provided in Table 37. A receiver shall comply with the specifications for each data rate/frequency for which operation of the receiver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The specifications apply over the receiver common mode and differential input voltage ranges.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7])

Table 37. RapidIO Receiver AC Timing Specifications—500 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1
Data valid	DV	1080		ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}		380	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–300	300	ps	4

Notes:
1. Measured at V_{ID} = 0 V.
2. Measured using the RapidIO receive mask shown in Figure 41.
3. See Figure 44.
4. See Figure 43, Figure 44.

Table 38. RapidIO Receiver AC Timing Specifications—750 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1
Data valid	DV	600		ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}		400	ps	3
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–267	267	ps	4

Notes:
1. Measured at V_{ID} = 0 V.
2. Measured using the RapidIO receive mask shown in Figure 41.
3. See Figure 44.
4. See Figure 43, Figure 44.

Table 39. RapidIO Receiver AC Timing Specifications—1 Gbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Duty cycle of the clock input	DC	47	53	%	1
Data valid	DV	425		ps	2
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}		300	ps	3

Table 39. RapidIO Receiver AC Timing Specifications—1 Gbps Data Rate (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	–200	200	ps	4

Notes:
1. Measured at V_{ID} = 0 V.
2. Measured using the RapidIO receive mask shown in Figure 41.
3. See Figure 44.
4. See Figure 43, Figure 44.

The compliance of receiver input signals RD[0:15] and RFRAME with their minimum data valid window (DV) specification shall be determined by generating an eye pattern for each of the data signals and comparing the eye pattern of each data signal with the RapidIO receive mask shown in Figure 41. The value of X2 used to construct the mask shall be $(1 – DV_{min})/2$. The ±100 mV minimum data valid and ±600 mV maximum input voltage values are from the DC specification. A signal is compliant with the data valid window specification if and only if the receive mask can be positioned on the signal's eye pattern such that the eye pattern falls entirely within the unshaded portion of the mask.

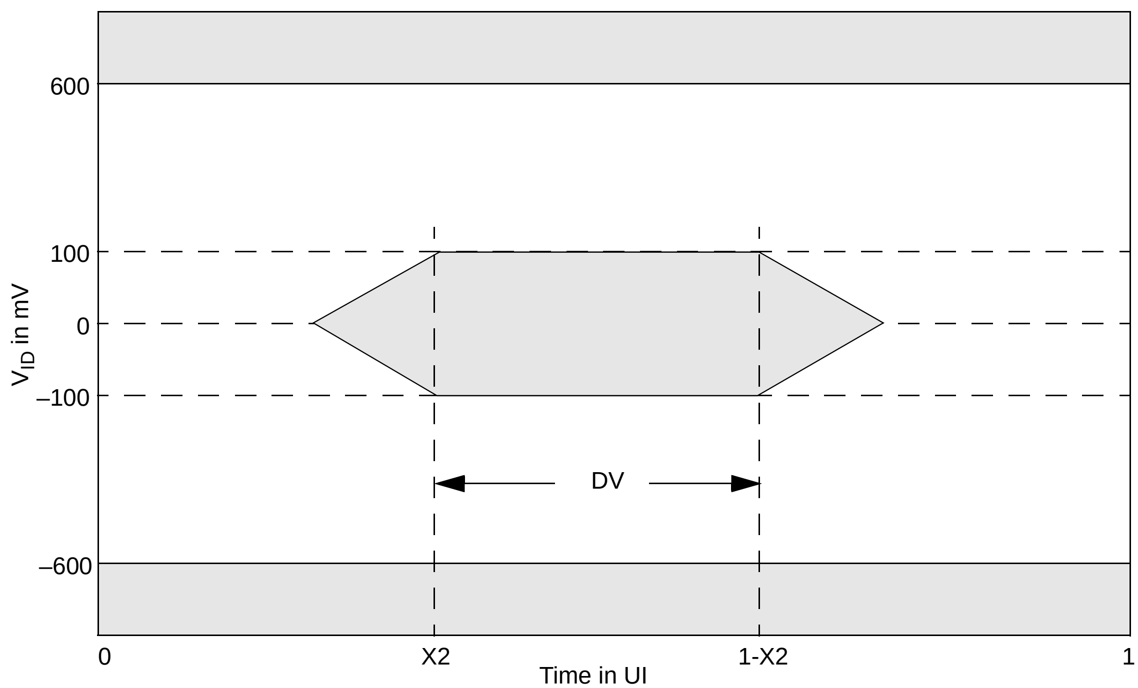


Figure 41. RapidIO Receive Mask

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO receive mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO receive mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 42. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

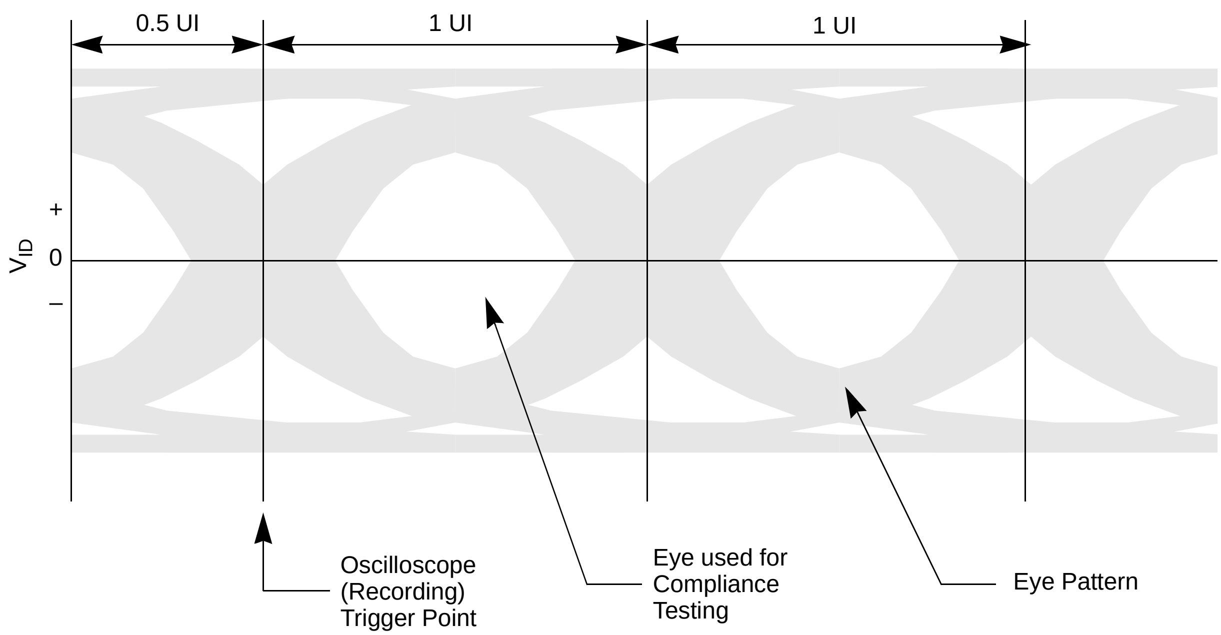


Figure 42. Example Receiver Input Eye Pattern

Figure 43 shows the definitions of the data to clock static skew parameter $t_{SKEW,PAIR}$ and thedata valid window parameter DV. The data and frame bits are those that are associated with the clock. The figure applies for all zero-crossings of the clock. All of the signals are differential signals. V_D represents V_{OD} for the transmitter and V_{ID} for the receiver. The center of the eye is defined as the midpoint of the region in which the magnitude of the signal voltage is greater than or equal to the minimum DV voltage.

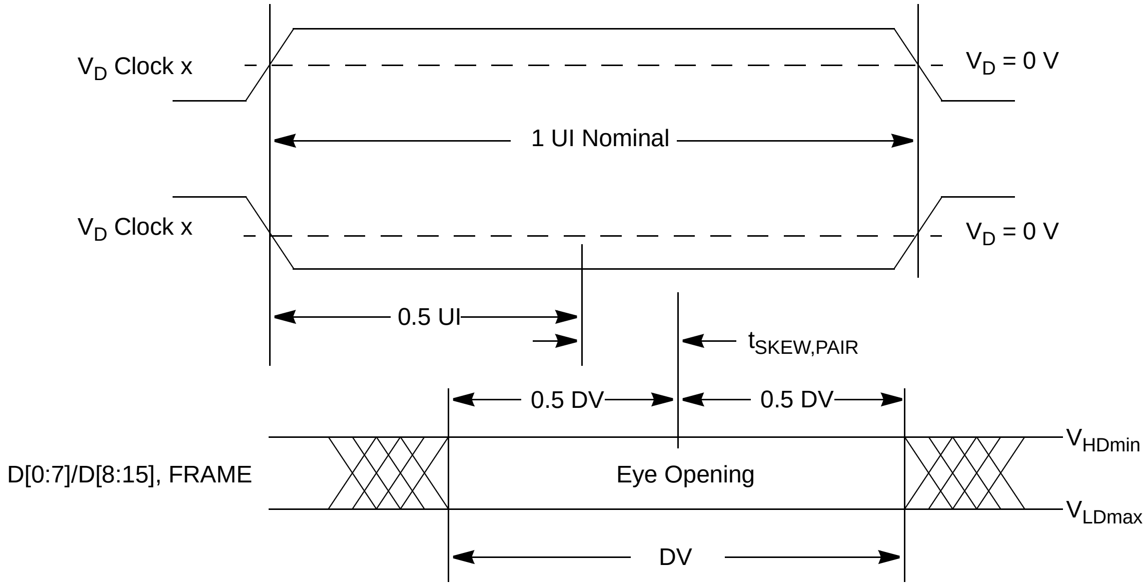


Figure 43. Data to Clock Skew

Figure 44 shows the definition of the data to data static skew parameter t_{DPAIR} and how the skew parameters are applied.

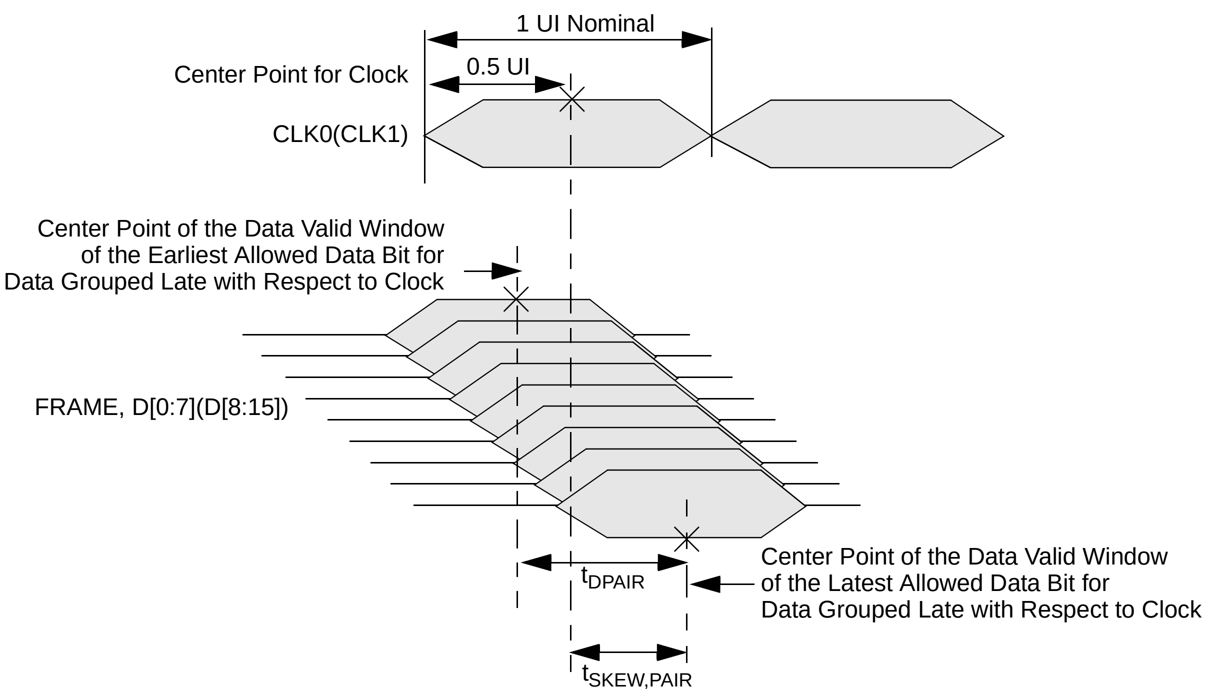


Figure 44. Static Skew Diagram

1.13 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

1.13.1 Package Parameters for the MPC8560 FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA).

Die size	12.2mm × 9.5 mm
Package outline	29 mm × 29 mm
Interconnects	783
Pitch	1 mm
Minimum module height	2.22 mm
Maximum module height	2.76 mm
Solder Balls	62 Sn/36 Pb/2 Ag
Ball diameter (typical)	0.5 mm

1.13.2 Mechanical Dimensions of the MPC8560 FC-PBGA

Figure 45 the mechanical dimensions and bottom surface nomenclature of the MPC8560, 783 FC-PBGA package.

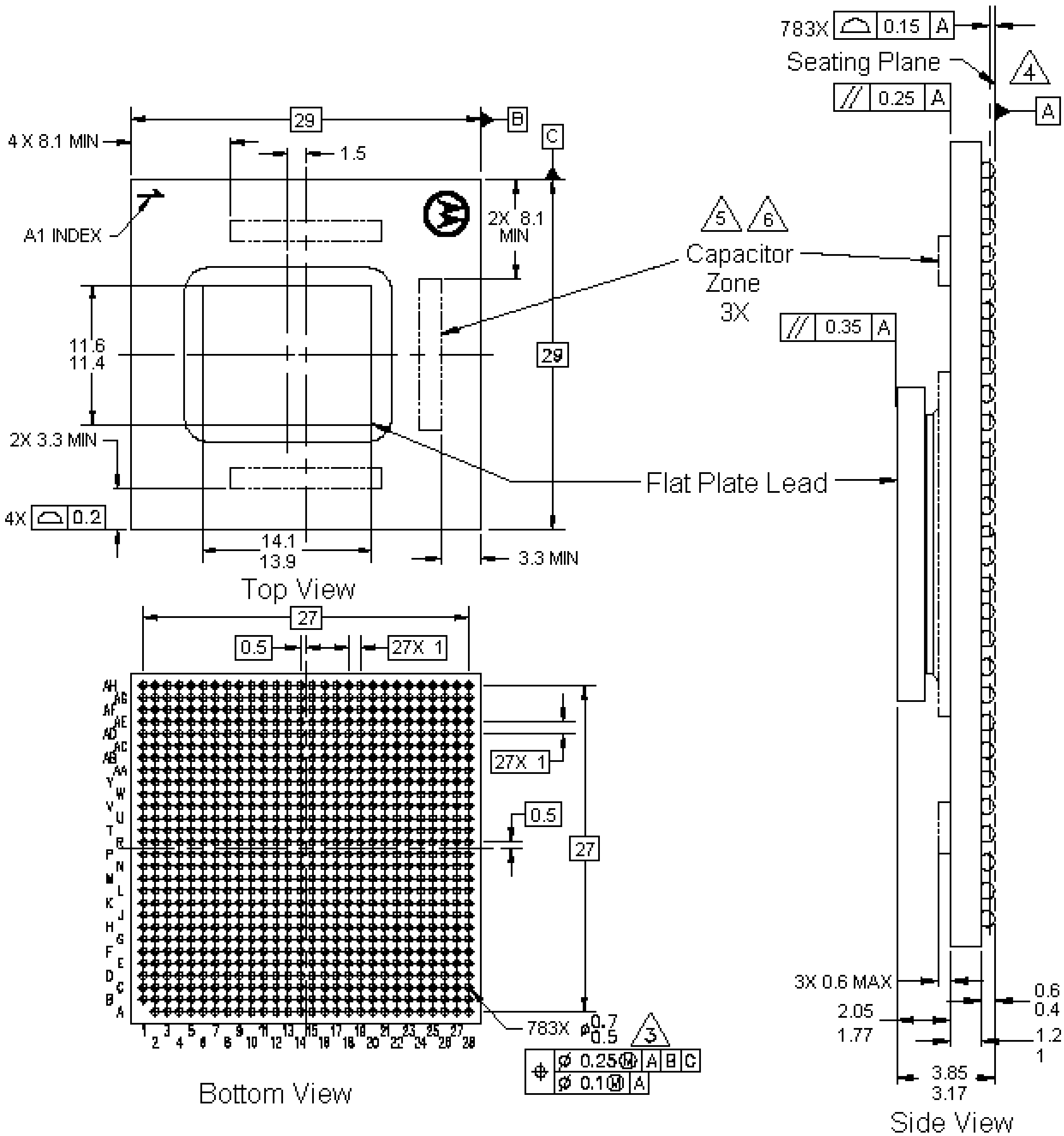


Figure 45. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8560 FC-PBGA

NOTES

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.

1.13.3 Pinout Listings

Table 40 provides the pin-out listing for the MPC8560, 783 FC-PBGA package.

Table 40. MPC8560 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI/PCI-X				
PCI_AD[63:0]	AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18, AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13	I/O	OV_{DD}	17
PCI_C_BE[7:0]	AG13, AH13, V14, W14, AH8, AB10, AD11, AC12	I/O	OV_{DD}	17
PCI_PAR	AA11	I/O	OV_{DD}	
PCI_PAR64	Y14	I/O	OV_{DD}	
PCI_FRAME	AC10	I/O	OV_{DD}	2
PCI_TRDY	AG10	I/O	OV_{DD}	2
PCI_IRDY	AD10	I/O	OV_{DD}	2
PCI_STOP	V11	I/O	OV_{DD}	2
PCI_DEVSEL	AH10	I/O	OV_{DD}	2
PCI_IDSEL	AA9	I	OV_{DD}	
PCI_REQ64	AE13	I/O	OV_{DD}	5, 10
PCI_ACK64	AD13	I/O	OV_{DD}	2
PCI_PERR	W11	I/O	OV_{DD}	2
PCI_SERR	Y11	I/O	OV_{DD}	2, 4
PCI_REQ0	AF5	I/O	OV_{DD}	
PCI_REQ[1:4]	AF3, AE4, AG4, AE5	I	OV_{DD}	
PCI_GNT0	AE6	I/O	OV_{DD}	
PCI_GNT[1:4]	AG5, AH5, AF6, AG6	O	OV_{DD}	5, 9

Table 40. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface				
MDQ[0:63]	M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12	I/O	GV_{DD}	
MECC[0:7]	N20, M20, L19, E19, C21, A21, G19, A19	I/O	GV_{DD}	
MDM[0:8]	L24, H28, F24, L21, E18, E16, G14, B13, M19	O	GV_{DD}	
MDQS[0:8]	L26, J25, D25, A22, H18, F16, F14, C13, C20	I/O	GV_{DD}	
MBA[0:1]	B18, B19	O	GV_{DD}	
MA[0:14]	N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13	O	GV_{DD}	
$\overline{\text{MWE}}$	D17	O	GV_{DD}	
$\overline{\text{MRAS}}$	F17	O	GV_{DD}	
$\overline{\text{MCAS}}$	J16	O	GV_{DD}	
$\overline{\text{MCS}}$[0:3]	H16, G16, J15, H15	O	GV_{DD}	
MCKE[0:1]	E26, E28	O	GV_{DD}	11
MCK[0:5]	J20, H25, A15, D20, F28, K14	O	GV_{DD}	
$\overline{\text{MCK}}$[0:5]	F20, G27, B15, E20, F27, L14	O	GV_{DD}	
MSYNC_IN	M28	I	GV_{DD}	
MSYNC_OUT	N28	O	GV_{DD}	
Local Bus Controller Interface				
LAD[0:31]	AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26	I/O	OV_{DD}	
LDP[0:3]	AA27, AA28, T26, P21	I/O	OV_{DD}	
LA[27]	U18	O	OV_{DD}	5, 9
LA[28:31]	T18, T19, T20, T21	O	OV_{DD}	5, 7, 9
$\overline{\text{LCS}}$[0:2]	Y27, Y28, W27	O	OV_{DD}	5, 9
$\overline{\text{LCS}}$[3:4]	W28, R27	O	OV_{DD}	9
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	R28	I/O	OV_{DD}	1

Table 40. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{LCS6}}$/$\overline{\text{DMA\_DACK2}}$	P27	O	OV_{DD}	1
$\overline{\text{LCS7}}$/$\overline{\text{DMA\_DDONE2}}$	P28	O	OV_{DD}	1
$\overline{\text{LWE}}$[0:1]/$\overline{\text{LBS}}$[0:1]	AB28, AB27	O	OV_{DD}	1, 9
$\overline{\text{LWE}}$[2:3]/$\overline{\text{LBS}}$[2:3]	T23, P24	O	OV_{DD}	1, 5, 9
LBCTL	V20	O	OV_{DD}	5, 9
LALE	V21	O	OV_{DD}	5, 8, 9
LGPL0/LSDA10	U19	O	OV_{DD}	5, 9
LGPL1/$\overline{\text{LSDWE}}$	U22	O	OV_{DD}	5, 9
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$	V28	O	OV_{DD}	5, 8, 9
LGPL3/$\overline{\text{LSDCAS}}$	V27	O	OV_{DD}	5, 9
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ LPBSE	V23	I/O	OV_{DD}	
LGPL5	V22	O	OV_{DD}	5, 9
LCKE	U23	O	OV_{DD}	
LCLK[0:2]	U27, U28, V18	O	OV_{DD}	
LSYNC_IN	T27	I	OV_{DD}	
LSYNC_OUT	T28	O	OV_{DD}	
DMA				
$\overline{\text{DMA\_DREQ}}$[0:1]	H5, G4	I	OV_{DD}	
$\overline{\text{DMA\_DACK}}$[0:1]	H6, G5	O	OV_{DD}	
$\overline{\text{DMA\_DDONE}}$[0:1]	H7, G6	O	OV_{DD}	
Programmable Interrupt Controller				
$\overline{\text{MCP}}$	AG17	I	OV_{DD}	
$\overline{\text{UDE}}$	AG16	I	OV_{DD}	
IRQ[0:7]	AA18, Y18, AB18, AG24, AA21, Y19, AA19, AG25	I	OV_{DD}	
IRQ8	AB20	I	OV_{DD}	9
IRQ9/$\overline{\text{DMA\_DREQ3}}$	Y20	I	OV_{DD}	1
IRQ10/$\overline{\text{DMA\_DACK3}}$	AF26	I/O	OV_{DD}	1
IRQ11/$\overline{\text{DMA\_DDONE3}}$	AH24	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	AB21	O	OV_{DD}	2, 4
Ethernet Management Interface				
EC_MDC	F1	O	LV_{DD}	5, 9
EC_MDIO	E1	I/O	LV_{DD}	

Table 40. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Gigabit Reference Clock				
EC_GTX_CLK125	E2	I	LV_{DD}	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_TXD[7:0]	A6, F7, D7, C7, B7, A7, G8, E8	O	LV_{DD}	5, 9
TSEC1_TX_EN	C8	O	LV_{DD}	11
TSEC1_TX_ER	B8	O	LV_{DD}	
TSEC1_TX_CLK	C6	I	LV_{DD}	
TSEC1_GTX_CLK	B6	O	LV_{DD}	5, 9
TSEC1_CRS	C3	I	LV_{DD}	
TSEC1_COL	G7	I	LV_{DD}	
TSEC1_RXD[7:0]	D4, B4, D3, D5, B5, A5, F6, E6	I	LV_{DD}	
TSEC1_RX_DV	D2	I	LV_{DD}	
TSEC1_RX_ER	E5	I	LV_{DD}	
TSEC1_RX_CLK	D6	I	LV_{DD}	
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_TXD[7:4]	B10, A10, J10, K11	O	LV_{DD}	5, 9
TSEC2_TXD[3:0]	J11, H11, G11, E11	O	LV_{DD}	
TSEC2_TX_EN	B11	O	LV_{DD}	11
TSEC2_TX_ER	D11	O	LV_{DD}	
TSEC2_TX_CLK	D10	I	LV_{DD}	
TSEC2_GTX_CLK	C10	O	LV_{DD}	5, 9
TSEC2_CRS	D9	I	LV_{DD}	
TSEC2_COL	F8	I	LV_{DD}	
TSEC2_RXD[7:0]	F9, E9, C9, B9, A9, H9, G10, F10	I	LV_{DD}	
TSEC2_RX_DV	H8	I	LV_{DD}	
TSEC2_RX_ER	A8	I	LV_{DD}	
TSEC2_RX_CLK	E10	I	LV_{DD}	
RapidIO Interface				
RIO_RCLK	Y25	I	OV_{DD}	
$\overline{\text{RIO\_RCLK}}$	Y24	I	OV_{DD}	
RIO_RD[0:7]	T25, U25, V25, W25, AA25, AB25, AC25, AD25	I	OV_{DD}	
$\overline{\text{RIO\_RD}}$[0:7]	T24, U24, V24, W24, AA24, AB24, AC24, AD24	I	OV_{DD}	

Table 40. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
RIO_RFRAME	AE27	I	OV_{DD}	
$\overline{\text{RIO\_RFRAME}}$	AE26	I	OV_{DD}	
RIO_TCLK	AC20	O	OV_{DD}	11
$\overline{\text{RIO\_TCLK}}$	AE21	O	OV_{DD}	11
RIO_TD[0:7]	AE18, AC18, AD19, AE20, AD21, AE22, AC22, AD23	O	OV_{DD}	
$\overline{\text{RIO\_TD}}$[0:7]	AD18, AE19, AC19, AD20, AC21, AD22, AE23, AC23	O	OV_{DD}	
RIO_TFRAME	AE24	O	OV_{DD}	
$\overline{\text{RIO\_TFRAME}}$	AE25	O	OV_{DD}	
RIO_TX_CLK_IN	AF24	I	OV_{DD}	
$\overline{\text{RIO\_TX\_CLK\_IN}}$	AF25	I	OV_{DD}	
I^2C interface				
IIC_SDA	AH23	I/O	OV_{DD}	2, 4
IIC_SCL	AH22	I/O	OV_{DD}	2, 4
System Control				
$\overline{\text{HRESET}}$	AH16	I	OV_{DD}	
$\overline{\text{HRESET\_REQ}}$	AG20	O	OV_{DD}	
$\overline{\text{SRESET}}$	AF20	I	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	M11	I	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	G1	O	OV_{DD}	2, 4
Debug				
TRIG_IN	N12	I	OV_{DD}	
TRIG_OUT	G2	I/O	OV_{DD}	5, 6, 9
MSRCID[0:1]	J9, G3	O	OV_{DD}	5, 6, 9
MSRCID[2:4]	F3, F5, F2	O	OV_{DD}	6
MDVAL	F4	O	OV_{DD}	6
Clock				
SYSCLK	AH21	I	OV_{DD}	
RTC	AB23	I	OV_{DD}	
CLK_OUT	AF22	O	OV_{DD}	11
JTAG				
TCK	AF21	I	OV_{DD}	
TDI	AG21	I	OV_{DD}	12

Table 40. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TDO	AF19	O	OV_{DD}	11
TMS	AF23	I	OV_{DD}	12
$\overline{TRST}$	AG23	I	OV_{DD}	12
DFT				
$\overline{LSSD\_MODE}$	AG19	I	OV_{DD}	2
L1_TSTCLK	AB22	I	OV_{DD}	2
L2_TSTCLK	AG22	I	OV_{DD}	2
TEST_SEL	AH20	I	OV_{DD}	3
Thermal Management				
THERM0	AG2	I/O	—	14
THERM1	AH3	I/O	—	14
Power Management				
ASLEEP	AG18			5, 9
Power and Ground Signals				
$AV_{DD}1$	AH19	Power for e500 PLL (1.2 V)	$AV_{DD}1$	
$AV_{DD}2$	AH18	Power for CCB PLL (1.2 V)	$AV_{DD}2$	
$AV_{DD}3$	AH17	Power for CPM PLL (1.2 V)	$AV_{DD}3$	
GND	A12, A17, B3, B14, B20, B26, B27, C2, C4, C11,C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7, AG26	—	—	
GV_{DD}	A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21	Power for DDR DRAM I/O Voltage (2.5 V)	GV_{DD}	

Table 40. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV_{DD}	A4, C5, E7, H10	Reference Voltage; Three-Speed Ethernet I/O (2.5 V, 3.3 V)	LV_{DD}	
MV_{REF}	N27	Reference Voltage Signal; DDR	MV_{REF}	
No Connects	AH26, AH27, AH28, AG28, AF28, AE28, AH1, AG1, AH2, B1, B2, A2, A3, AH25	—	—	16
OV_{DD}	D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4	PCI/PCI-X, RapidIO, 10/100 Ethernet, and other Standard (3.3 V)	OV_{DD}	
RESERVED	C1, T11, V11, AF1	—	—	15
SENSEVDD	L12	Power for Core (1.2 V)	V_{DD}	13
SENSEVSS	K12	—	—	13
V_{DD}	M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14	Power for Core (1.2 V)	V_{DD}	
CPM				
PA[0:31]	H1, H2, J1, J2, J3, J4, J5, J6, J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2	I/0	OV_{DD}	
PB[4:31]	M1, N1, N4, N5, N6, N7, N8, N9, N10, N11, P11, P10, P9, P8, P7, P6, P5, P4, P3, P2, P1, R1, R2, R3, R4, R5, R6, R7	I/0	OV_{DD}	
PC[0:31]	R8, R9, R10, R11, T9, T6, T5, T4, T1, U1, U2, U3, U4, U7, U8, U9, U10, V9, V6, V5, V4, V3, V2, V1, W1, W2, W3, W6, W7, W8, W9, Y9	I/0	OV_{DD}	

Table 40. MPC8560 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PD[4:31]	Y1, Y2, Y3, Y4, Y5, Y6, AA8, AA7, AA4, AA3, AA2, AA1, AB1, AB2, AB3, AB5, AB6, AC7, AC4, AC3, AC2, AC1, AD1, AD2, AD5, AD6, AE3, AE2	I/0	OV_{DD}	

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, LCS5/DMA_REQ2 is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as DMA_REQ2.
2. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.
3. This pin must always be pulled up to OV_{DD}.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the MPC8560 is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 1.14.2, "Platform/System PLL Ratio."
8. The value of LALE and LGPL2 at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 1.14.3, "e500 Core PLL Ratio."
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. Refer to the *PCI Specification*.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive resistor.
15. No connections should be made to these pins.
16. These pins are not connected for any functional use.
17. PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and PCI_C_BE[7:4]).

1.14 Clocking

This section describes the PLL configuration of the MPC8560. Note that the platform clock is identical to the CCB clock.

1.14.1 Clock Ranges

Table 41 provides the clocking specifications for the processor core and Table 42 provides the clocking specifications for the memory bus.

Table 41. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency				Unit	Notes
	667 MHz		833 MHz			
	Min	Max	Min	Max		
e500 core processor frequency	320	667	320	833	MHz	1, 2

Notes:
1. **Caution:** The CCB to SYSCLK) ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 1.14.2, "Platform/System PLL Ratio," and Section 1.14.3, "e500 Core PLL Ratio," for ratio settings.
2.)The minimum e500 core frequency is based on the minimum platform frequency of 160 MHz.

Table 42. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency				Unit	Notes
	667 MHz		833 MHz			
	Min	Max	Min	Max		
Memory bus frequency	80	133	80	166	MHz	1, 2

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 1.14.2, "Platform/System PLL Ratio," and Section 1.14.3, "e500 Core PLL Ratio," for ratio settings.
2.)The memory bus speed is half of the DDR data rate, hence half of the platform clock frequency.

1.14.2 Platform/System PLL Ratio

The platform clock is the clock that drives the L2 cache, the DDR SDRAM data rate, and the e500 core complex bus (CCB), and is also called the CCB clock. The values are determined by the binary value on LA[28:31] at power up, as shown in Table 43.

There is no default for this PLL ratio; these signals must be pulled to the desired values.

Table 43. CCB Clock Ratio

Binary Value of LA[28:31] Signals	Ratio Description
0000	16:1 ratio CCB clock: SYSCLK (PCI bus)
0001	Reserved
0010	2:1 ratio CCB clock: SYSCLK (PCI bus)
0011	3:1 ratio CCB clock: SYSCLK (PCI bus)
0100	4:1 ratio CCB clock: SYSCLK (PCI bus)
0101	5:1 ratio CCB clock: SYSCLK (PCI bus)
0110	6:1 ratio CCB clock: SYSCLK (PCI bus)
0111	Reserved
1000	8:1 ratio CCB clock: SYSCLK (PCI bus)
1001	9:1 ratio CCB clock: SYSCLK (PCI bus)
1010	10:1 ratio CCB clock: SYSCLK (PCI bus)
1011	Reserved
1100	12:1 ratio CCB clock: SYSCLK (PCI bus)
1101	Reserved
1110	Reserved
1111	Reserved

1.14.3 e500 Core PLL Ratio

Table 44 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LALE and LGPL2 at power up, as shown in Table 44.

Table 44. e500 Core to CCB Ratio

Binary Value of LALE, LGPL2 Signals	Ratio Description
00	2:1 e500 core:CCB
01	5:2 e500 core:CCB
10	3:1 e500 core:CCB
11	7:2 e500 core:CCB

1.14.4 Frequency Options

Table 45 shows the expected frequency values for the platform frequency when using a CCB to SYSCLK ratio in comparison to the memory bus speed.

Table 45. Frequency Options with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK [1]								
	17	**25**	**33**	**42**	**67**	**83**	**100**	**111**	**133**
	Platform/CCB Frequency								
2	33	50	67	83	133	167	200	222 [5]	267 [4]
3	50	75	100	125	200	250 [4]	300 [3]	333 [3]	
4	67	100	133	167	267 [4]	333 [3]			
5	83	125	167	208	333 [3]				
6	100	150	200	250 [4]					
8	133	200	267 [5]	333 [3]			Not available		
9	150	225 [5]	300 [4]	375 [2]					
10	167	250 [4]	333 [3]						
12	200	300 [3]							
16	267 [4]								

Notes:
1. Tthe CCB to SYSCLK ratios must be chosen according to the shading scheme for particular memory bus speeds.
2. The shading scheme for the cells are:
   - ☐ Available with memory bus speeds of 166 MHz and below.
   - (dark shading) Available only with memory bus speeds above 133 MHz.
   - (light shading) Available with memory bus speeds of 100 MHz and above.
3. Not available with e500 core to CCB ratios greater than 2.5:1.
4. Not available with e500 core to CCB ratios greater than 3:1.
5. Not available with e500 core to CCB ratios greater than 3.5:1.

1.15 Thermal

This section describes the thermal specifications of the MPC8560.

1.15.1 Thermal Characteristics

Table 46 provides the package thermal characteristics for the MPC8560.

Table 46. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient resistance (natural convection on 1S board)	θ_{JA}	32	°C/W	1,2
Junction-to-ambient resistance (natural convection on 2S2P board)	θ_{JMA}	21	°C/W	1,3
Junction-to-ambient resistance (forced airflow (200 ft/min) on 1S board)	θ_{JMA}	26	°C/W	1,3
Junction-to-ambient resistance (forced airflow (200 ft/min) on 2S2P board)	θ_{JMA}	17	°C/W	1,3
Die junction-to-board thermal resistance	θ_{JB}	12	°C/W	4
Junction-to-case thermal resistance	θ_{JC}	0.3	°C/W	5

Notes

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printe- circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface without thermal grease.

1.15.2 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 46. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

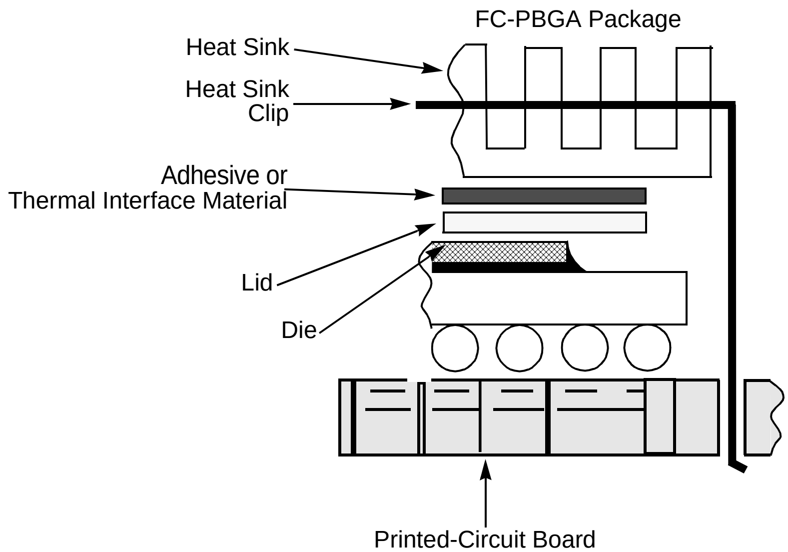


Figure 46. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the MPC8560. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MIE) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8560 to function in various environments.

1.15.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8540 thermal model is shown in Figure 47. Four volumes will used to represent this device. Two are modeled the foot print size of the package: Solder ball/air and substrate. The other two have the same size as the heat source: heat source and bump/underfill. The heat source layer is modeled as 10.5 × 13 × 1.8 mm using conductivity noted in Figure 47. The heat source is applied as a uniform source at the bottom of the volume. The bump/underfill layer is modeled as 10.5 × 13 × 0.069 mm (or as a collapsed volume) with orthotropic material properties: 0.6 W/(m × K) in the xy-plane direction and 1.6 W/(m × K) in the z-direction. The substrate layer is modeled as 29 × 29 × 1.14 mm using orthotropic material properties: 13.3 W/(m × K) in the xy-plane direction and 0.7 W/(m × K) in the z-direction. The solder ball/air layer is modeled as 29 × 29 × 0.33 mm (or as a collapsed volume) using orthotropic material properties: 0.034 W/(m × K) in the xy-plane direction and 0.33 W/(m × K) in the z-direction.

Conductivity	Value	Unit
Heat Source (10.5 × 13.2 × 1.8 mm)		
k_x	119	W/(m × K)
k_y	119	
k_z	49.5	
Bump/Underfill (10.5 × 13.2 × 0.069 mm)		
k_x	0.6	
k_y	0.6	
k_z	1.6	
Substrate (29 × 29 × 1.14 mm)		
k_x	13.3	
k_y	13.3	
k_z	0.7	
Solder Ball/Air (29 × 29 × 0.33mm)		
k_x	0.034	
k_y	0.034	
k_z	0.33	

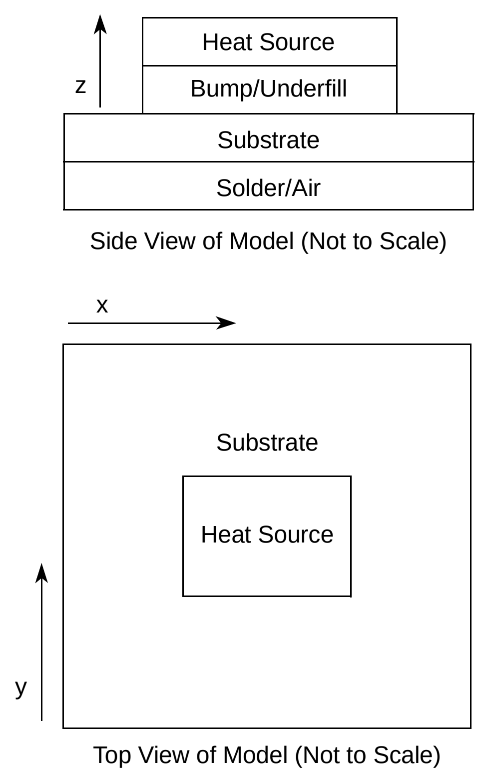


Figure 47. .MPC8560 Thermal Model

1.15.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 46, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 48 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

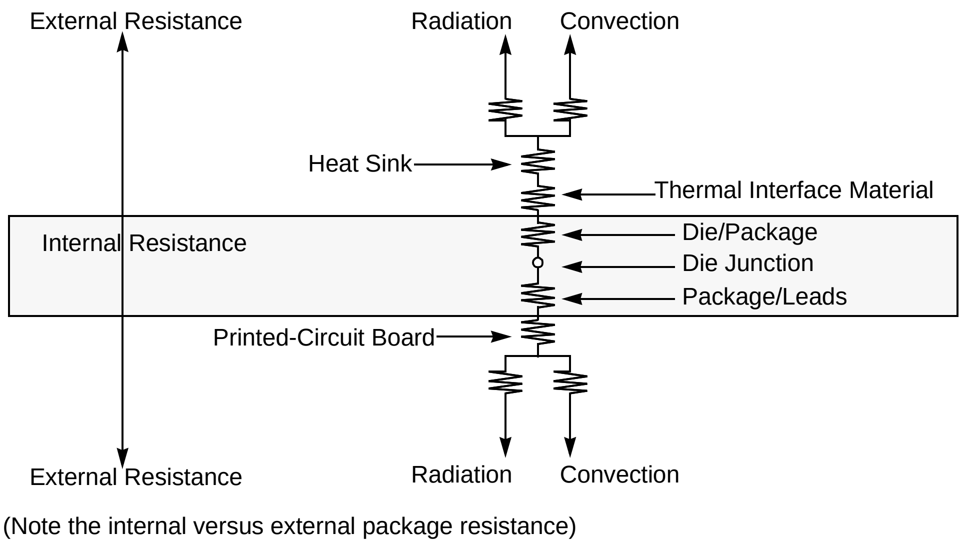


Figure 48. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

1.15.2.3 Adhesives and Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 49 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 46). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

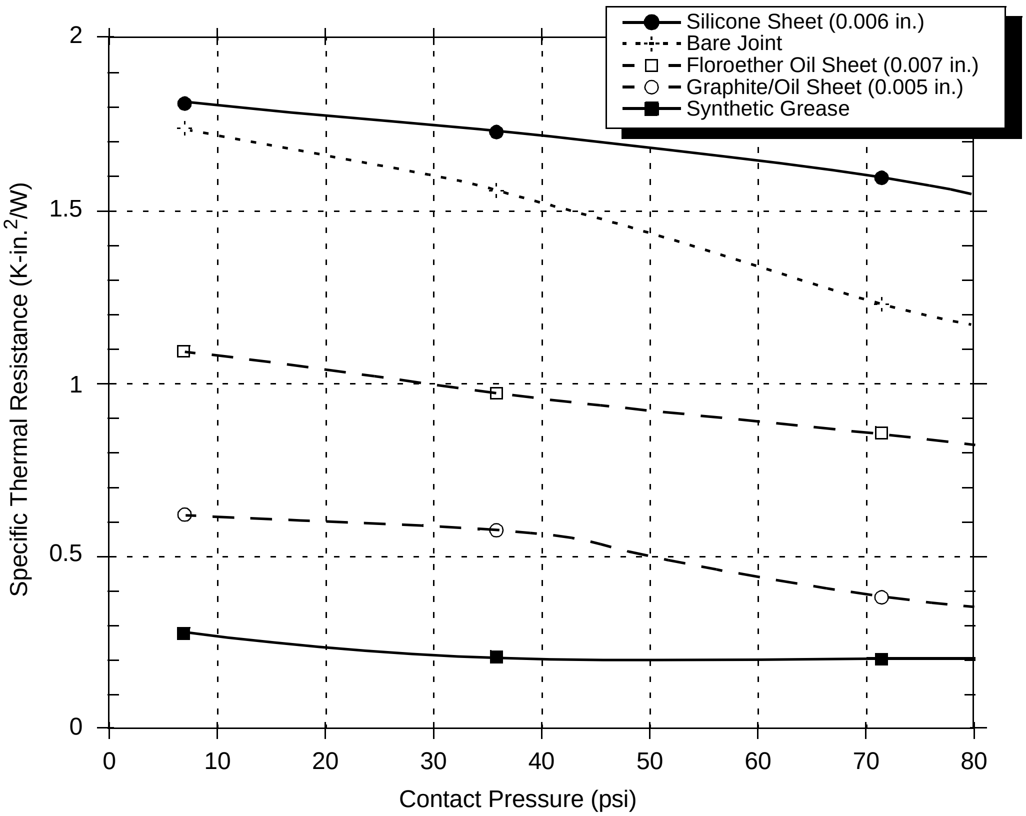


Figure 49. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

1.15.2.4 Heat Sink Selection Examples

The following section provides a heat sink selection example using one of the commercially available heat sinks.

1.15.2.4.1 Case 1

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_I + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

where

T_J is the die-junction temperature

T_I is the inlet cabinet ambient temperature

T_R is the air temperature rise within the computer cabinet

θ_{JC} is the junction-to-case thermal resistance

θ_{INT} is the adhesive or interface material thermal resistance

θ_{SA} is the heat sink base-to-ambient thermal resistance

P_D is the power dissipated by the device

During operation the die-junction temperatures (T_J) should be maintained within the range specified in Table 2. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30° to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5° to 10°C. The thermal resistance of some thermal interface material (θ_{INT}) may be about 1°C/W. Assuming a T_I of 30°C, a T_R of 5°C, a FC-PBGA package θ_{JC} = 0.3, and a power consumption (P_D) of 7.0 W, the following expression for T_J is obtained:

$$\text{Die-junction temperature: } T_J = 30°C + 5°C + (0.3°C/W + 1.0°C/W + \theta_{SA}) \times 7.0\ W$$

The heat sink-to-ambient thermal resistance (θ_{SA}) versus airflow velocity for a Thermalloy heat sink #2328B is shown in Figure 50.

Assuming an air velocity of 2 m/s, we have an effective θ_{SA+} of about 3.3°C/W, thus

$$T_J = 30°C + 5°C + (0.3°C/W + 1.0°C/W + 3.3°C/W) \times 7.0\ W,$$

resulting in a die-junction temperature of approximately 67°C which is well within the maximum operating temperature of the component.

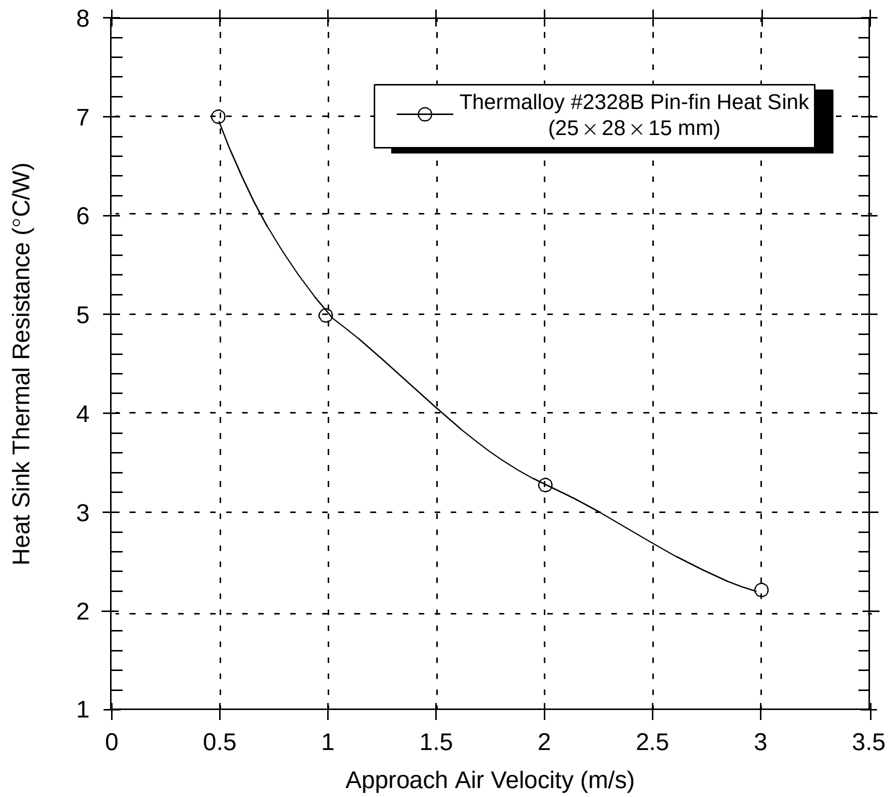


Figure 50. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

1.15.2.4.2 Case 2

Every system application has a little different conditions that the heat sink must meet. As an alternate example, assume that the air reaching the component is 85°C with an approach velocity of 1 m/s. For a maximum junction temperature of 105°C at 7 W, the thermal resistance of the heat sink and interface material must be less than 2.2°C/W. If the interface material is chosen to keep the interface thermal resistance less than 0.2°C/W, then the heat sink must be less than 2.0°C/W. If the heat sink is constrained by the board spacing in the compact PCI chassis to a height of 13 mm, then the heat sink will be approximately $75 \times 75 \times 13$mm. While the fin thickness should be minimized for improved flow through the heat sink, a 0.6-mm fin thickness is achievable with the less expensive extruded aluminum heat sinks. A thicker than normal base is needed because of the small heat source size, recommend 2 to 2.5 mm thick. A smaller heat sink ($60 \times 60 \times 13$ mm) can be build using a folded fin design. The heat sink can be much smaller if more height is allowed or if the air is ducted to the heat sink and higher pressure drops are acceptable. These heat sinks can be obtained from several vendors.

The spring mounting should be designed to apply the force only directly above the die. By localizing the force, rocking of the heat sink is minimized. One suggested mounting method attaches a plastic fence to the board to provide the structure on which the heat sink spring clips. The plastic fence also provides the opportunity to minimize the holes in the printed-circuit board and to locate them at the corners of the package. Figure 51 provides an exploded view of the plastic fence, heat sink, and spring clip.

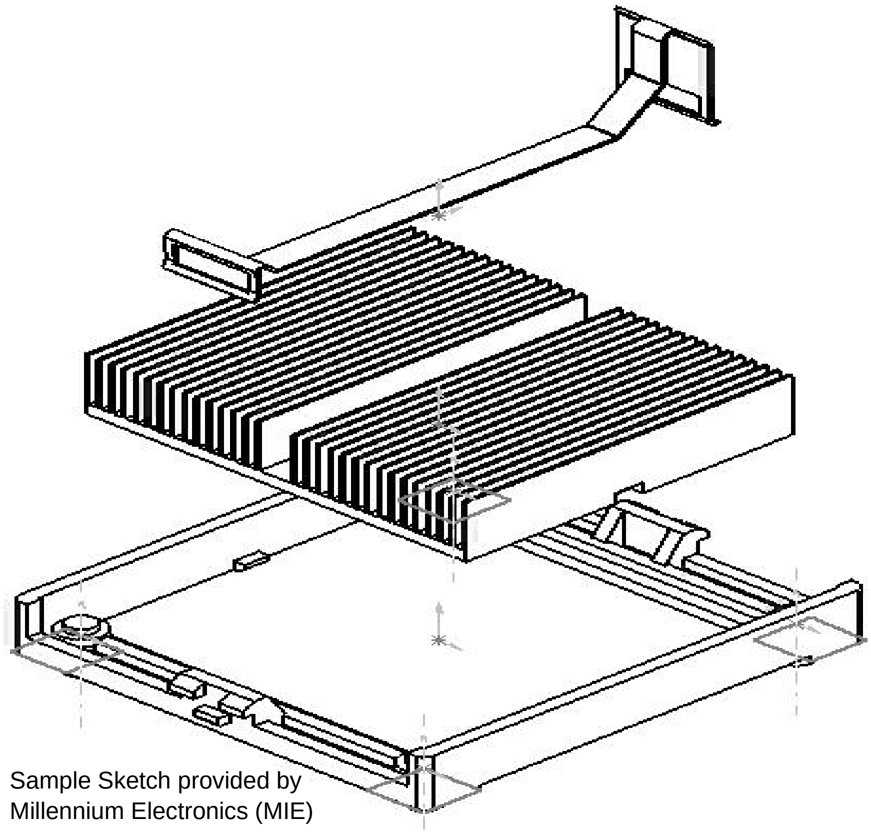


Figure 51. Exploded View of a Heat Sink Attachment using a Plastic Force

The die junction-to-ambient and the heat sink-to-ambient thermal resistances are common figure-of-merits used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-juntion temperature: airflow, board population (local heat flux of adjacent components), system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the boards, as well as, system-level designs.

1.16 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8560.

1.16.1 System Clocking

The MPC8560 includes three PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the Platform PLL Ratio configuration bits as described in Section 1.14.2, “Platform/System PLL Ratio.”
2. The e500 Core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL Ratio configuration bits as described in Section 1.14.3, “e500 Core PLL Ratio.”
3. The CPM PLL is slaved to the platform clock and is used to generate clocks used internally by the CPM block. The ratio between the CPM PLL and the platform clock is fixed and not under user control.

1.16.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AVDD1, AVDD2, and AVDD3, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide three independent filter circuits as illustrated in Figure 52, one to each of the three AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias.

Figure 52 shows the PLL power supply filter circuit.

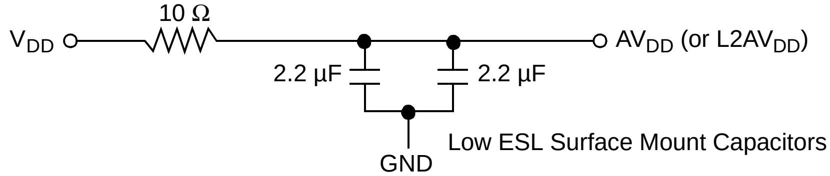


Figure 52. PLL Power Supply Filter Circuit

1.16.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8560 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8560 system, and the MPC8560 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pins of the MPC8560. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD} and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

1.16.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, GV_{DD}, or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the MPC8560.

1.16.5 Output Buffer DC Impedance

The MPC8560 drivers are characterized over process, voltage, and temperature. There are two driver types: a push-pull single-ended driver (open drain for I^2C) for all buses except RapidIO, and a current-steering differential driver for the RapidIO port.

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 53). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

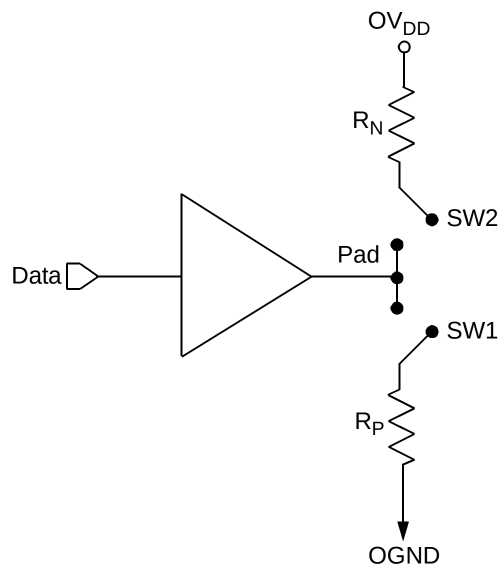


Figure 53. Driver Impedance Measurement

The output impedance of the RapidIO port drivers targets 200-Ω differential resistance. The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 47 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 47. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI/PCI-X	DDR DRAM	RapidIO	Symbol	Unit
R_N	43 Target	25 Target	20 Target	NA	Z_0	Ω
R_P	43 Target	25 Target	20 Target	NA	Z_0	Ω
Differential	NA	NA	NA	200 Target	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

1.16.6 Configuration Pin Muxing

The MPC8560 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform/system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

1.16.7 Pull-Up Resistor Requirements

The MPC8560 requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C pins and EPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 54. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

1.16.8 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. The MPC8560 requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert $\overline{\text{TRST}}$ during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

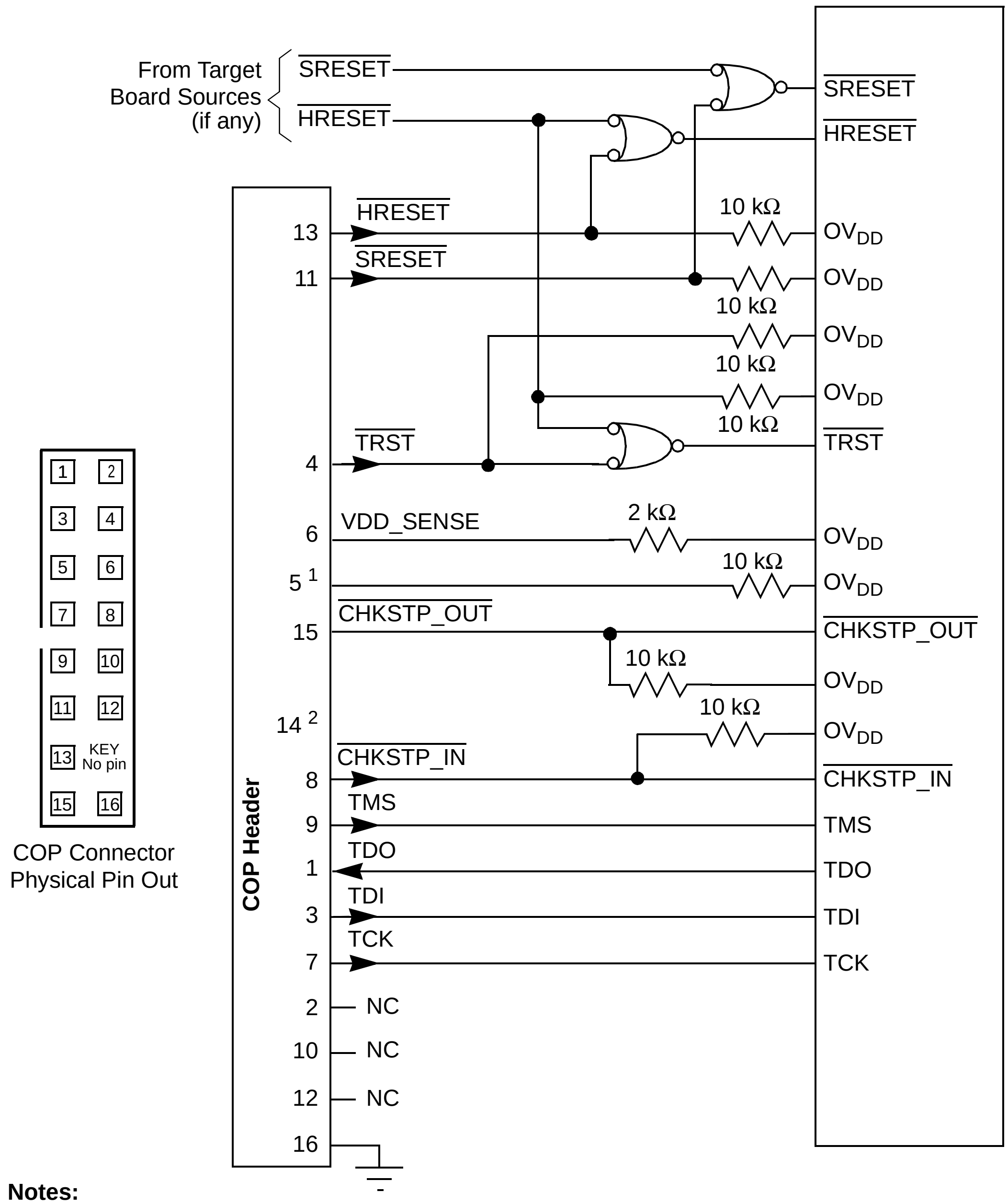
The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 54 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted.

The COP header shown Figure 54 in adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header).

There is no standardized way to number the COP header shown in Figure 54; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 54 is common to all known emulators.



Notes:

1. RUN/STOP, normally found on pin 5 of the COP header, is not implemented on the MPC8540. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.

Figure 54. JTAG Interface Connection

1.17 Document Revision History

Table 48 provides a revision history for this hardware specification.

Table 48. Document Revision History

Rev. No.	Substantive Change(s)
1	Original Customer Version.
1.1	Made updates throughout document. Secrion 1.6.1—Added symbols and note for the GTX_CLK125 timing parameters. Section 1.11.3—Updated pin list table: LGPL5/LSDAMUX to LGPL5, LA[27:29] and LA[30:31] to LA[27:31], TRST to $\overline{\text{TRST}}$, added GBE Clocking section and EC_GTX_CLK125 signal. Figure 50—Updated pin 2 connection information.

1.18 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 1.18.1, "Part Numbers Fully Addressed by this Document."

1.18.1 Part Numbers Fully Addressed by this Document

Table 49 provides the Motorola part numbering nomenclature for the MPC8560. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Motorola sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

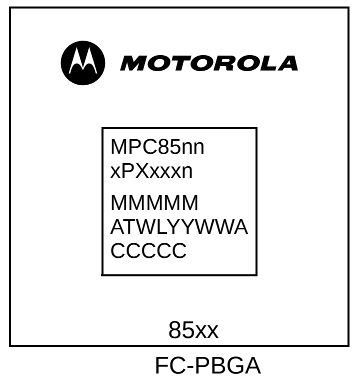
Table 49. Part Numbering Nomenclature

MPC	***nnnn***	***x***	***xx***	***nnn***	***xn***
Product Code	**Part Identifier**	**Temperature Range**	**Package** [1]	**Processor Frequency** [2]	**Revision Level**
MPC	8560	Blank = 0 to 105°C C= -40 to 105°C	PX = FC-PBGA	e500 core/ memory bus	Contact local Motorola sales office

Notes:
1. See Section 1.13, "Package and Pin Listings" for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

1.18.2 Part Marking

Parts are marked as the example shown in Figure 55.



Notes:

MMMMM is the 5-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 55. Part Marking for FC-PBGA Device

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