

MTX603 and MTX604™  
Release 1.0

# **MTX Series Motherboard Installation and Use**

MTXA/IH3

June 2000 Edition

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## Preface

This manual provides general information, hardware preparation and installation instructions, operating instructions, and a functional description of the MTX Embedded ATX family of motherboards. It also provides pinout information and a description of the initialization and diagnostic firmware - PPCBug.

Currently, the MTX is provided in the following configurations:

| Part Number   | Description   |
|---|---|
| <b>3-PCI-slot PowerPC ATX products</b>  |   |
| <b>MTX603-023</b>   | 200MHz MPC603e, three 32-bit PCI slots, Ethernet, Super I/O, EIDE, 512KB L2 cache, 4MB Flash, SCSI, sync serial, peripheral parallel port           |
| <b>MTX604-023</b>   | 300MHz MPC604e, three 32-bit PCI slots, Ethernet, Super I/O, EIDE, 512KB L2 cache, 4MB Flash, SCSI, sync serial, peripheral parallel port           |
| <b>MTX604-024</b>   | 300MHz MPC604e, three 32-bit PCI slots, Ethernet, Super I/O, EIDE   |
| <b>MTX604-030</b>   | Twin 300MHz MPC604e, three 32-bit PCI slots, Ethernet, Super I/O, EIDE, 512KB L2 cache, 4MB Flash   |
| <b>PowerPC ATX products with single 64-bit PCI slot and PMC</b>                                 |   |
| The PMC and 64-bit PCI slots on these products are not compatible with the standard ATX chassis |   |
| <b>MTX603-022</b>   | 200MHz MPC603e, one 64-bit PCI slot and two PMC sites, Ethernet, Super I/O, EIDE, 512KB L2 cache, 4MB Flash, SCSI, sync serial, peripheral parallel |
| <b>MTX604-022</b>   | 300MHz MPC604e, one 64-bit PCI slot and two PMC sites, Ethernet, Super I/O, EIDE, 512KB L2 cache, 4MB Flash, SCSI, sync serial, peripheral parallel |

## Summary of Changes

All references of “Glance chipset” have been changed to “Doubletake chipset”.

All references of “256KB L2 cache” have been changed to “512KB L2 cache”.

Figure 1-1 on page 1-2 has been corrected to reflect the following changes: 8M-256M DIMM Memory Socket, SCSI SYM53C875, and Ethernet DEC21143.

All references of Glance devices numbered “MCP2604GA” have been changed to reflect Doubletake devices numbered “MCP2605GA”. See [Cache Mode Control on page 1-8](#).

The motherboard no longer requires -12.0V and +12.0V power from an external source. See [System Considerations on page 1-18](#).

## Conventions Used in This Manual

The following typographical conventions are used in this document:

### **bold**

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

### *italic*

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

### `courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

### <Enter>, <Return> or <CR>

represents the carriage return or Enter key.

### **CTRL**

represents the Control key. Execute control characters by pressing the Ctrl key and the letter simultaneously, for example, **Ctrl-d**.

## Flammability

All Motorola PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

## EMI Caution



This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.

## Lithium Battery Caution

This product contains a lithium battery to power the clock and calendar circuitry.



Danger of explosion if battery is replaced incorrectly. Replace battery only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.



Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch denselben oder einen vom Hersteller empfohlenen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.



Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.

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Motorola Computer Group products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

EN55022 “Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment”; this product tested to Equipment Class B

EN50082-1:1997 “Electromagnetic Compatibility—Generic Immunity Standard, Part 1. Residential, Commercial and Light Industry”

System products also fulfill EN60950 (product safety) which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC/safety performance.

In accordance with European Community directives, a “Declaration of Conformity” has been made and is on file within the European Union. The “Declaration of Conformity” is available on request. Please contact your sales representative.

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## Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

### **Ground the Instrument.**

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

### **Do Not Operate in an Explosive Atmosphere.**

Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

### **Keep Away From Live Circuits Inside the Equipment.**

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

### **Use Caution When Exposing or Handling a CRT.**

Breakage of a Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, do not handle the CRT and avoid rough handling or jarring of the equipment. Handling of a CRT should be done only by qualified service personnel using approved safety mask and gloves.

### **Do Not Substitute Parts or Modify Equipment.**

Do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that all safety features are maintained.

### **Observe Warnings in Manual.**

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.



To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

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# Hardware Preparation and Installation

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# 1

## Introduction

This chapter provides general information, jumper settings, and hardware preparation and installation instructions for the MTX, the associated DIMMs, and the optional PMCs and PCI adapter card.

The MTX is a motherboard equipped with a PowerPC® Series microprocessor. The MTX603 series is equipped with a PowerPC 603® microprocessor, and the MTX604 has a PowerPC 604® microprocessor. There is also a dual PowerPC 604 model. A 512KB L2 cache (level 2 secondary cache memory) is available as an option on all versions.

The complete MTX consists of the motherboard plus:

- ❑ Up to four (minimum two) DIMM memory modules
- ❑ Optional PMC or PCI adapter cards

The block diagram in [Figure 1-1](#) illustrates the architecture of the MTX.

The following equipment is required to complete an MTX system:

- ❑ ATX chassis with power supply
- ❑ System console terminal
- ❑ Operating system (and/or application software)
- ❑ Disk drives (and/or other I/O) and controllers

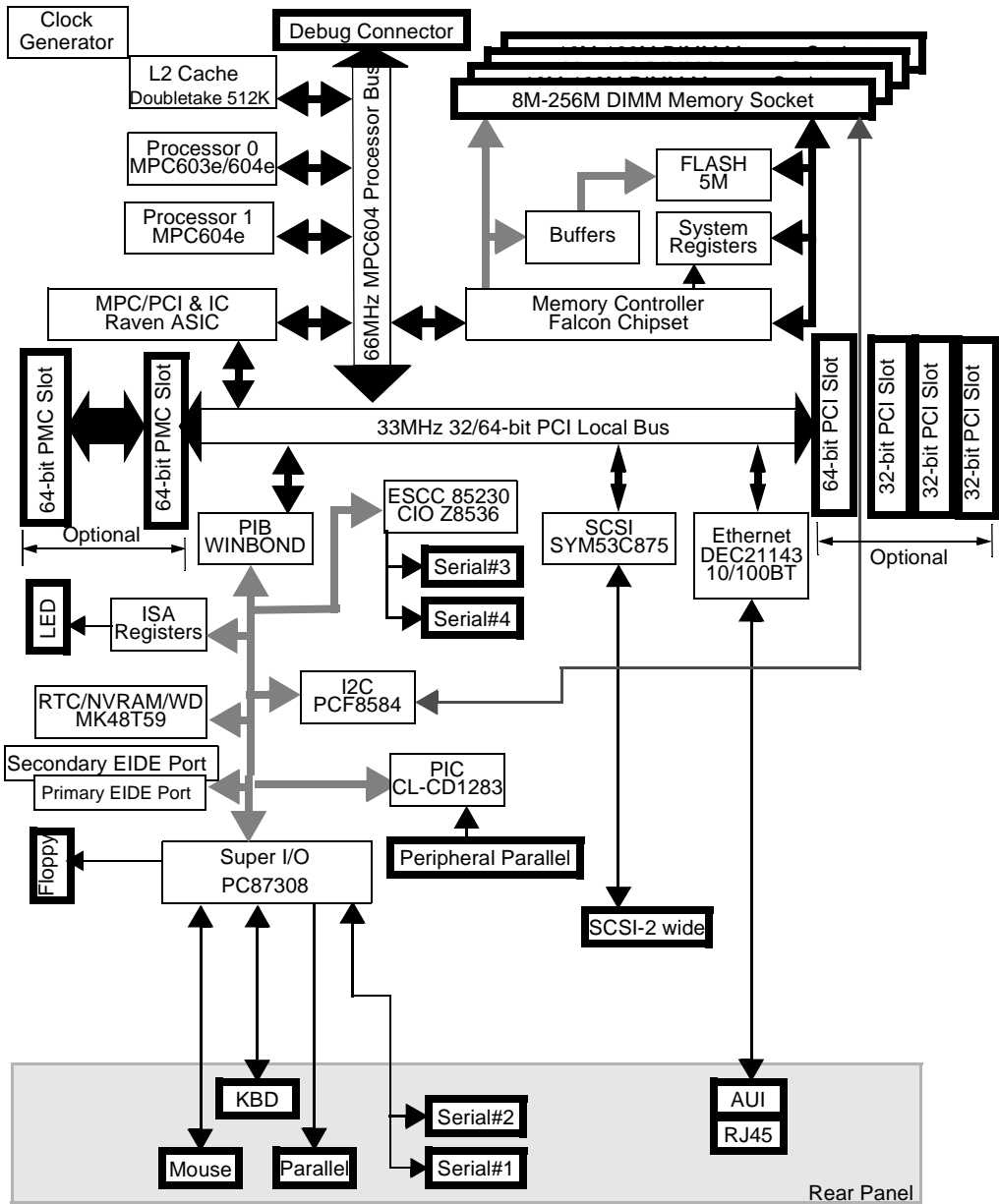


Figure 1-1. MTX Block Diagram

# Overview of Startup Procedure

The following table lists the things you will need to do before you can use this board and tells where to find the information you need to perform each step. Be sure to read this entire chapter, including all Caution and Warning notes, before you begin.

**Table 1-1. Startup Overview**

| What you need to do...   | Refer to Section Heading Titled...   |
|--|--|
| Unpack the hardware.   | <i>Unpacking Instructions</i> on page 1-3  |
| Configure the hardware by setting jumpers on the boards        | <i>MTX Motherboard Preparation</i> on page 1-4   |
| Ensure memory DIMMs are properly installed on the motherboard. | <i>DIMM Memory Installation</i> on page 1-11   |
| Install the MTX Motherboard in the chassis.                    | <i>MTX Motherboard Installation</i> on page 1-17   |
| Program the board as needed for your applications.             | <i>MTX Series Motherboard Programmer's Reference Guide</i> , listed in <i>Related Documentation</i> on page A-1. |

## Unpacking Instructions

**Note** If the shipping carton is damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.

Unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of equipment.



Avoid touching areas of integrated circuitry; static discharge can damage circuits.

## Hardware Configuration

To produce the desired configuration and ensure proper operation of the MTX, you may need to carry out certain hardware modifications before installing the motherboard.

The MTX provides software control over most options: by setting bits in control registers after installing the module in a system, you can modify its configuration. (The MTX control registers are described in the *MTX Series Single Board Computer Programmer's Reference Guide* as listed under [Related Documentation on page A-1.](#))

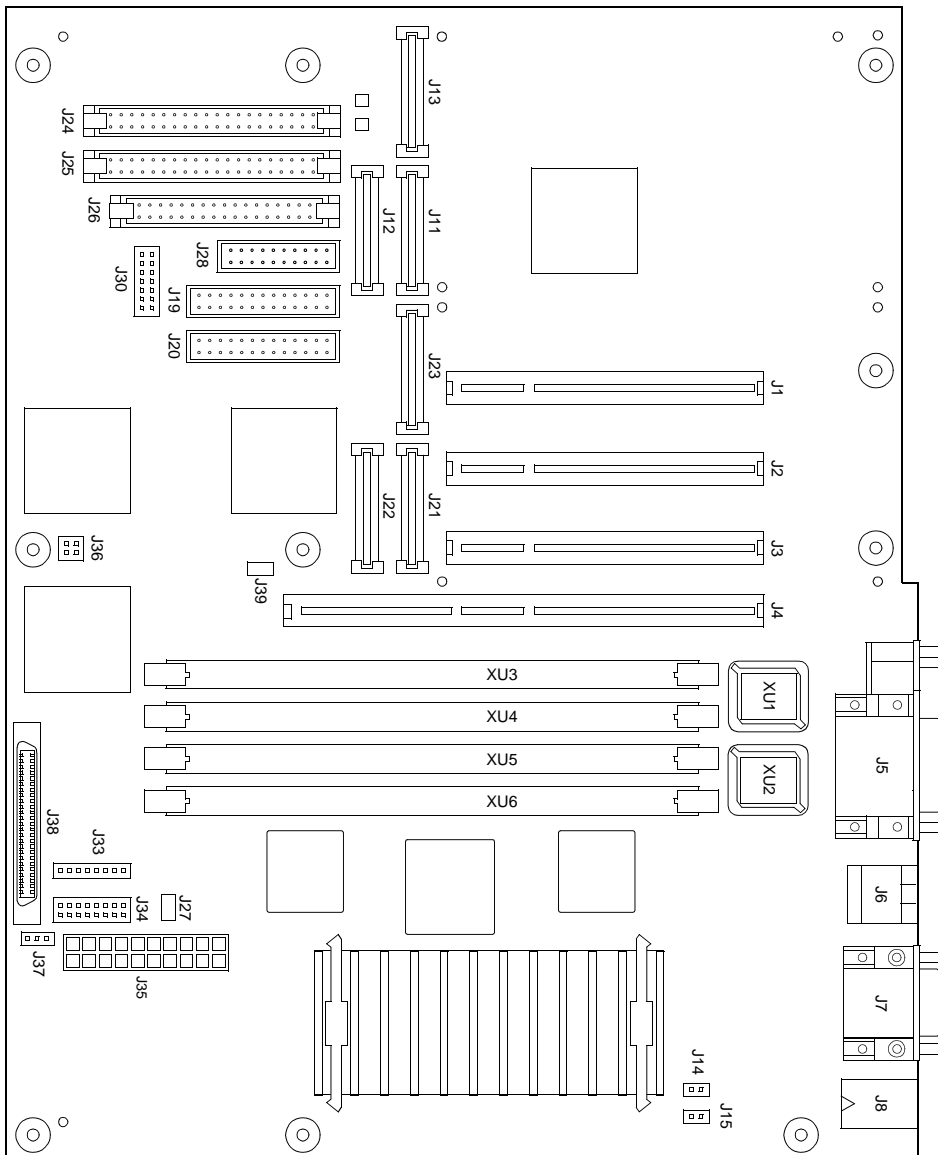
Some options, however, are not software-programmable. Such options are controlled through manual installation or removal of header jumpers.

## MTX Motherboard Preparation

Figure 1-2 illustrates the placement of the switches, jumper headers, connectors, and LED indicators on the MTX. [MTX Connector/Jumper Descriptions on page 1-6](#) lists the jumper and connector callouts and their associated function. Manually configured items on the base board include:

- ❑ Cache mode control (J15)
- ❑ Flash bank selection (J37)
- ❑ Power Control for ATX power supply (J27 and J39)
- ❑ Hardware/firmware disable of SCSI (J36)

The MTX is factory tested and shipped with the configurations described in the following sections. The MTX's required and factory-installed debug monitor, PPCBug, operates with those factory settings.



2077 9707

**Figure 1-2. MTX Switches, Headers, Connectors, Fuses, LEDs**

## Connector/Jumper Descriptions

The following table describes the MTX jumper functions and any specific mapping designations:

**Table 1-2. MTX Connector/Jumper Descriptions**

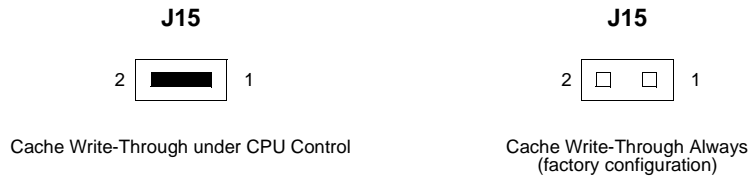
| Reference Designator | Function              | Comment               |
|----------------------|-----------------------|-----------------------|
| J1                   | 32-bit PCI slot 1B    | IDSEL = AD16          |
| J2                   | 32-bit PCI slot 2B    | IDSEL = AD17          |
| J3                   | 32-bit PCI slot 3B    | IDSEL = AD18          |
| J4                   | 64-bit PCI slot 3A    | IDSEL = AD18          |
| J5 Upper             | AUI                   |                       |
| J5 Lower             | Host Parallel         |                       |
| J6                   | 10/100 Base-T         |                       |
| J7 Upper             | COM2                  | Async DTE             |
| J7 Lower             | COM1                  | Async DTE             |
| J8 Upper             | Keyboard              |                       |
| J8 Lower             | Mouse                 |                       |
| J11                  | 64-bit PMC slot 1A    | IDSEL = AD16          |
| J12                  | 64-bit PMC slot 1A    |                       |
| J13                  | 64-bit PMC slot 1A    |                       |
| J15                  | L2 write-thru control | default = open        |
| J16                  | Debug                 | For factory use only  |
| J19                  | COM4                  | Port B Sync/async DTE |
| J20                  | COM3                  | Port A Sync/async DTE |
| J21                  | 64-bit PMC slot 2A    | IDSEL = AD17          |
| J22                  | 64-bit PMC slot 2A    |                       |
| J23                  | 64-bit PMC slot 2A    |                       |

**Table 1-2. MTX Connector/Jumper Descriptions (Continued)**

| <b>Reference Designator</b> | <b>Function</b>       | <b>Comment</b>                    |
|-----------------------------|-----------------------|-----------------------------------|
| J24                         | Primary EIDE          |                                   |
| J25                         | Secondary EIDE        |                                   |
| J26                         | Floppy                |                                   |
| J27                         | ATX Power Control     | Short to turn ATX power supply on |
| J28                         | 16-bit latched data   |                                   |
| J29                         | Peripheral Parallel   |                                   |
| J30                         | Front Panel Functions |                                   |
| J34                         | RISCWATCH             | Processor #1                      |
| J35                         | Power                 |                                   |
| J36                         | SCSI options          |                                   |
| J37                         | Flash Bank Select     |                                   |
| J38                         | SCSI                  |                                   |
| J39                         | ATX Soft Power        | Momentary Power Switch Input      |
| XU1                         | Flash Bank B          | Upper Byte                        |
| XU2                         | Flash Bank B          | Lower Byte                        |
| XU3                         | DIMM Bank B           | Upper 72-bits                     |
| XU4                         | DIMM Bank B           | Lower 72-bits                     |
| XU5                         | DIMM Bank A           | Upper 72-bits                     |
| XU6                         | DIMM Bank A           | Lower 72-bits                     |

## Cache Mode Control

The optional L2 cache functionality is provided via the Doubletake chipset. If populated, the Doubletake 512K look-aside cache option is implemented with two MCP2605GA (Doubletake) devices. Refer to the MCP2605GA Data Sheets and the *MTX Programmer's Guide* for additional information.



## Flash Bank Selection

The MTX motherboard contains two banks of FLASH memory. Bank A consists of two soldered-in 8-bit wide, 2 megabyte deep 3.3V FLASH SMT devices and appears as Flash Bank A (16 bits wide) to the Falcon chipset. A resistor select enables write protect for Bank A (default configuration is software write protect enabled), individual 64K byte blocks can be write protected by software. The entire Bank A memory can be write protected by removing the resistor jumper (R78) that supplies write power to the devices.

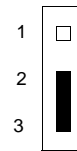
Bank B consists of two sockets for 8-bit wide +5.0 volt FLASH SMT devices and appears as Flash Bank B (16 bits wide) to the Falcon chipset. The bank B sockets support a maximum 512K byte FLASH in each socket.

Bank B contains the onboard debugger, PPCBug.

To enable Flash bank A, place a jumper across header J37 pins 1 and 2. To enable Flash bank B, place a jumper across header J37 pins 2 and 3.

**J37**

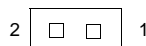
Flash Bank A Enabled  
(4MB, Soldered)

**J37**

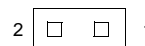
Flash Bank B Enabled (1MB, Sockets)  
(factory configuration)

## Power Control for ATX Power Supply

ATX power supplies have a logic level (+5.0V/GND) power control input (PS\_ON\_L). An ATX supply power is “ON” when this input is connected to logic ground. The MTX motherboard features both level and edge-sensitive control of this ATX power supply feature. A two pin header (J27) is provided for level control (short the pins to turn the supply on). A separate two-pin header (J39) controls the soft-power switch input to the Super I/O device. When there is a rising edge on the switch input, the Advanced Power Control section of the Super I/O device will toggle the state of the PS\_ON\_L input of the ATX power connector. The ATX power supply must provide 5VSB (+5 standby power) for the soft-power feature to be enabled.

**J27**

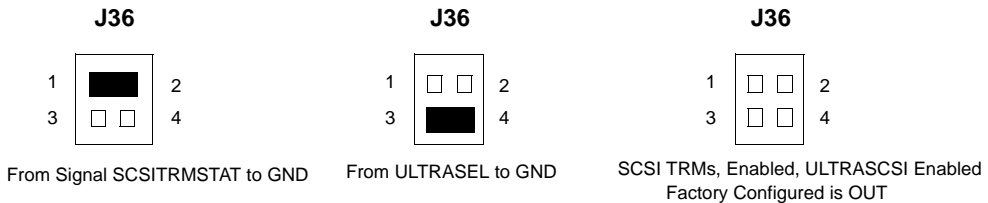
Power Off

**J39**

Connect Momentary Switch  
here to Control Power

## Hardware/Firmware Disable of SCSI Terminator

Jumper J36 is used to disable on-board SCSI terminators and to disable the firmware negotiation of UltraSCSI. To disable on-board SCSI terminators connect a jumper from J36-2 to J36-1. To disable firmware negotiation of UltraSCSI connect a jumper from J36-3 to J36-4.



## Remote Status and Control

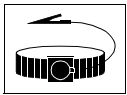
For factory test, the MTX front panel LEDs and switches are mounted on a removable mezzanine board. Removing the LED mezzanine makes the mezzanine connector (J30, a keyed double-row 14-pin connector) available for service as a remote status and control connector. In this application, J30 can be connected to a user-supplied external cable to carry the Reset and Abort signals and the LED lines to a control panel located apart from the MTX. Maximum cable length is 15 feet.

# Hardware Installation

The following sections discuss the placement of mezzanine or adapter cards on the MTX motherboard, the installation of the complete MTX assembly into an ATX chassis, and the system considerations relevant to the installation. Before installing the MTX, ensure that all header jumpers are configured as desired.

## ESD Precautions

### Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to ESD. After removing the component from the system or its protective wrapper, place the component flat on a grounded, static-free surface (and in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an unpainted metal part of the system chassis.

## DIMM Memory Installation

DIMM modules install into sockets XU3 through XU6 on the MTX motherboard. To upgrade or install a DIMM module, refer to [Figure 1-3](#) and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the motherboard.



Removing modules with power applied may result in damage to module components.



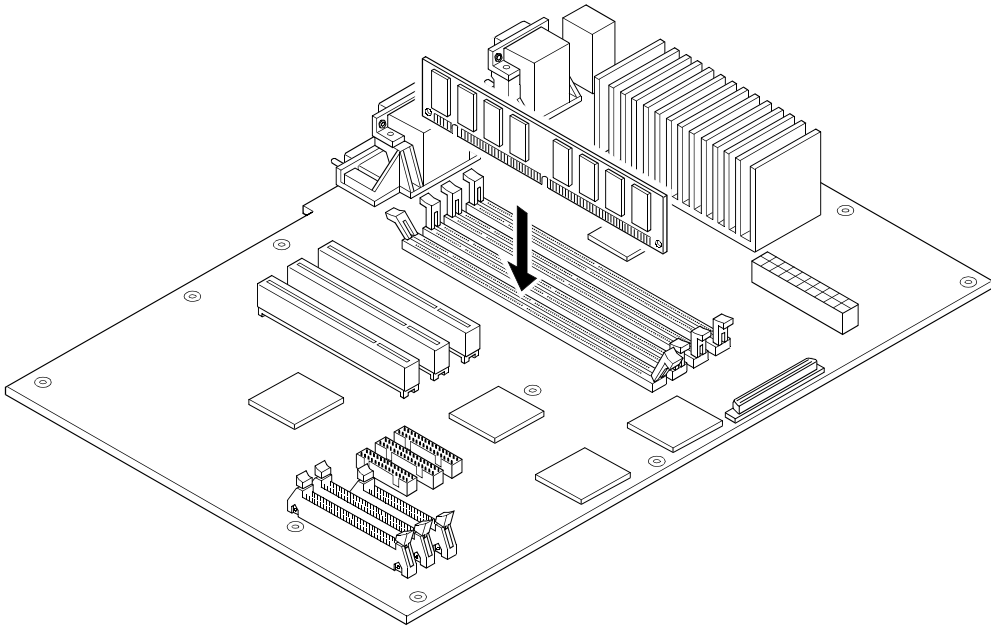
Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.



Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

3. Install the DIMM into XU3 through XU6 as needed, with pin 1 of the DIMM located at the rear of the motherboard (toward the external I/O connectors). Note that DIMMs must be installed in pairs, XU5 with XU6, or XU3 with XU4, and that at least one pair of DIMMs is required for MTX operation. Load Bank A (XU5, XU6) first.

**Note** 168 pin, 3.3V, unbuffered, serial presence detect, EDO or Fast Page DRAM DIMM's are required. Equivalent part numbers for some of the primary suppliers of this memory can be found in documents referenced on Motorola Computer Group's Web site at <http://www.motorola.com/computer/>



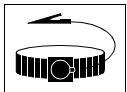
2078 9797

**Figure 1-3. DIMM Placement on MTX**

## PMC Module Installation (Optional)

PCI mezzanine card (PMC) modules mount to connectors J11, J12, and J13, or J21, J22 and J23 on the MTX motherboard. To install a PMC module, refer to [Figure 1-4](#) and proceed as follows:

### Use ESD

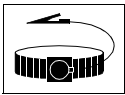


### Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or removing the Probe board. Electronic components such as disk drives, motherboards, and memory modules can be extremely sensitive to electrostatic discharge (ESD). After removing a component from a chassis or from its protective wrapper, place the

component flat on a grounded, static-free surface, and in the case of a board, component-side up. Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores). Wrap one end of the wrist grounding strap around your wrist.

**Use ESD****Wrist Strap**

Attach an ESD strap to your wrist. Attach the other end of the ESD strap to an electrical ground. (Note that the system chassis may not be grounded if it is unplugged.) The ESD strap must be secured to your wrist and to ground throughout the procedure.

1. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the motherboard.



Inserting or removing modules with power applied may result in damage to module components.

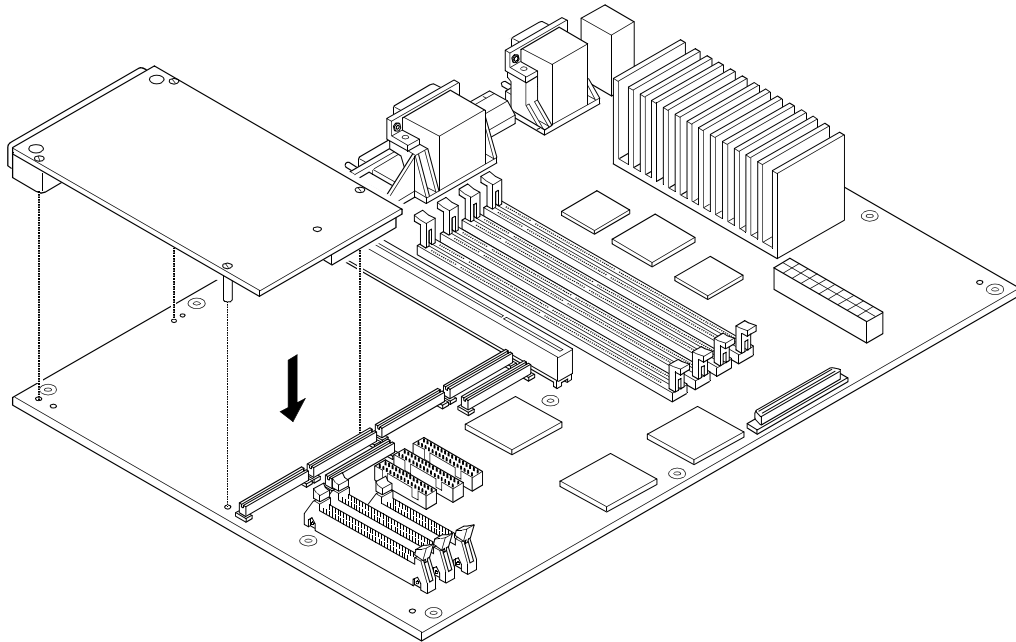
Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

2. Carefully remove the MTX from the chassis and lay it flat.



Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

3. Remove the PMC filler from the rear panel of the chassis.



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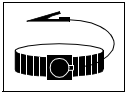
**Figure 1-4. PMC Module Placement on MTX**

4. Place the PMC module on top of the motherboard. The connectors on the underside of the PMC module should then connect smoothly with the corresponding connectors (either J11/J12/J13 or J21/J22/J23) on the MTX.
5. Insert the two short Phillips screws through the holes at the forward corners of the PMC module from the backside of the MTX motherboard, into the standoffs on the PMC module. Tighten the screws.
6. Reinstall the MTX assembly into the chassis.
7. Replace the chassis or system cover(s), reconnect the system to the AC or DC power source, and turn the equipment power on.

## PCI Adapter Installation (Optional)

PCI adapter boards mount to connectors J1 through J3 on the MTX motherboard. To install PCI adapters, refer to [Figure 1-5](#) and proceed as follows:

### Use ESD



**Wrist Strap**

Attach an ESD strap to your wrist. Attach the other end of the ESD strap to an electrical ground. (Note that the system chassis may not be grounded if it is unplugged.) The ESD strap must be secured to your wrist and to ground throughout the procedure.

1. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the motherboard.



**Caution**

Inserting or removing modules with power applied may result in damage to module components.



**Warning**

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

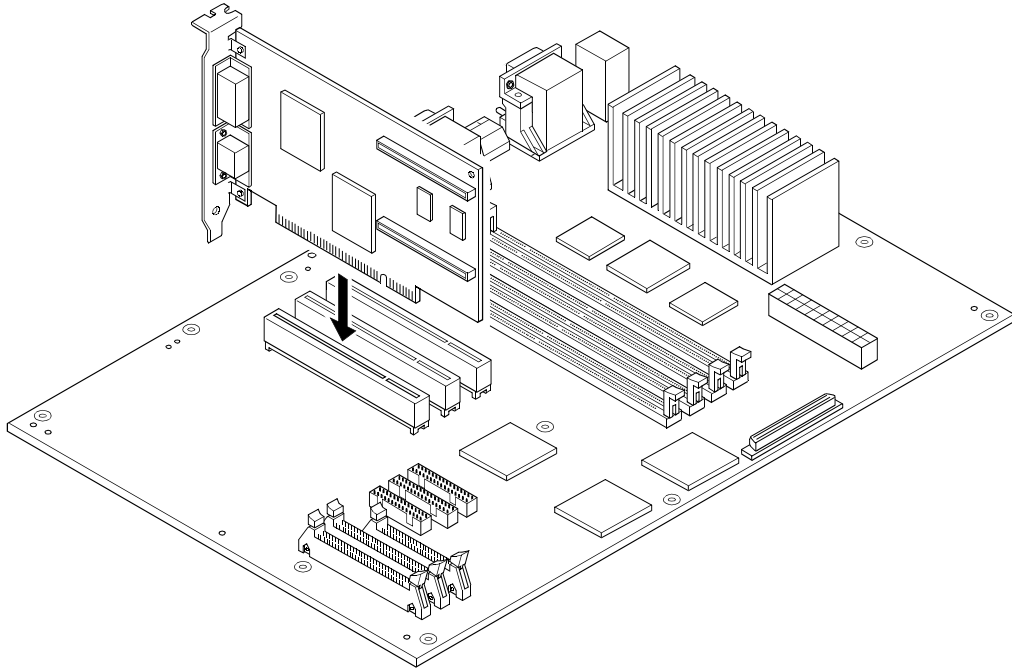
2. Remove the PCI filler from the chassis.



**Caution**

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

3. Install the PCI adapter card into slots J1 through J3.

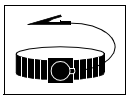


**Figure 1-5. PCI Adapter Card Placement on MTX**

## MTX Motherboard Installation

With PMC or PCI board(s) installed (if required) and headers properly configured, proceed as follows to install the MTX in the ATX chassis:

### Use ESD



### Wrist Strap

Attach an ESD strap to your wrist. Attach the other end of the ESD strap to an electrical ground. (Note that the system chassis may not be grounded if it is unplugged.) The ESD strap must be secured to your wrist and to ground throughout the procedure.

1. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary.



Inserting or removing modules with power applied may result in damage to module components.

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

2. Install standoffs provided with the chassis in locations aligning with the MTX motherboard mounting holes. Use as many screw-down metal standoffs as possible.



Avoid touching areas of integrated circuitry; static discharge can damage these circuits

3. Secure the MTX in the chassis with the screws provided.
4. Install jackposts on the rear panel COM2 and parallel port connectors.
5. Replace the chassis or system cover(s), making sure no cables are pinched. Cable the peripherals to the panel connectors, reconnect the system to the AC or DC power source, and turn the equipment power on.

## System Considerations

The MTX uses a 20-pin ATX compatible connector for power input. The motherboard requires +5.0V power from an external supply, and will generate +3.3V and PDXv-60Xe processor power (1.8 to 2.6 volts) from the +5.0V supply. The MTX routes +3.3V, +5.0V, and -5.0V to the PMC and PCI slots, and fused power is routed to other peripherals via polyswitches as described in the paragraph below.

The MTX board supplies +5.0V power to the mouse and keyboard via a 1.1 amp polyswitch, +5.0V (optional) to the SCSI termpower via a 1.1 amp polyswitch, +12.0V to the AUI port via a 1.1 amp polyswitch, and +5.0V to the Reset/Abort/LED connector (J30) via a 0.75 amp polyswitch.

## MTX Motherboard

Fused +5Vdc power is supplied to the motherboard's keyboard and mouse connectors through a polyswitch and to the 14-pin combined LED-mezzanine/remote-reset connector, J30.

The MTX motherboard supplies a SPEAKER\_OUT signal to the 14-pin combined LED-mezzanine/remote-reset connector, J30. When J30 is used as a remote reset connector with the LED mezzanine removed, the SPEAKER\_OUT signal can be cabled to an external speaker.

On the MTX motherboard, the standard serial DTE port (COM1) serves as the PPCBug debugger console port. The firmware console should be set up for initial power-up as follows:

- ❑ Eight bits per character
- ❑ One stop bit per character
- ❑ Parity disabled (no parity)
- ❑ Baud rate of 9600 baud

After power-up you can reconfigure the baud rate if you wish, using the PPCBug **PF** (Port Format) command via the command line interface. Whatever the baud rate, some type of hardware handshaking — either XON/OFF or via the RTS/CTS line — is desirable if the system supports it.



## Introduction

This chapter supplies information for use of the MTX motherboard in a system configuration. Here you will find the power-up procedure and descriptions of the switches and LEDs, memory maps, and software initialization.

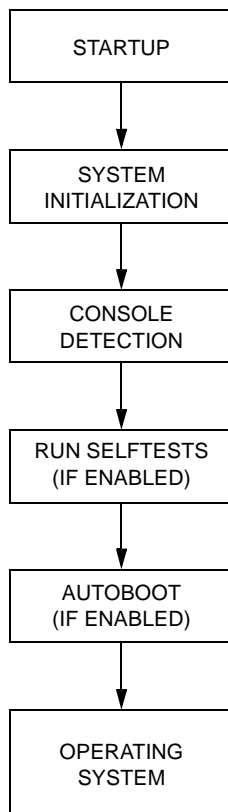
## Applying Power

After you have verified that all necessary hardware preparation has been done, that all connections have been made correctly, and that the installation is complete, you can power up the system. The MPU, hardware, and firmware initialization process is performed by the PowerPC™ PPCBug power-up or system reset. The firmware initializes the devices on the MTX module in preparation for booting the operating system.

The firmware is shipped from the factory with an appropriate set of defaults. In most cases there is no need to modify the firmware configuration before you boot the operating system.

The following flowchart shows the basic initialization process that takes place during PowerPC system startup.

For further information on PPCBug, refer to Chapter 6, *PPCBug on page 6-1*, or to the *PPCBug Firmware Package User's Manual*.



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**Figure 2-1. PPCBug System Startup**

## Front Panel Functions

The MTX has a 14-pin planar header for front panel functions including abort and reset switches, a speaker interface and LED drive. The header interfaces directly to the MEZLED board for diagnostic testing. The +5.0V power is supplied via a 0.75 amp polyfuse. The header provides the LED drive for seven functions: FAIL, CHKSTP, CPU, and PCI, SCSI, Ethernet, and EIDE:

- ❑ The STATLED# signal is active when either processor CHECKSTOP signal is active.
- ❑ The FAILED# signal is active when the firmware controlled BRDFAIL signal is active.
- ❑ The RUNLED# signal is active when the DBB# signal of the processor bus is active.
- ❑ The LANLED# signal is active when the Ethernet LED\_TX signal is active.
- ❑ The PCILED# signal is active when the IRDY# signal of the PCI bus is active.
- ❑ The SYSYLED# signal is active when the firmware controlled SCSIBSY# signal is active.
- ❑ The EIDELED# signal is active when an EIDE drive is connected and active.

All LED signals go active during a hardware reset (power-up or reset switch activated).

In addition, the MTX has two planar LEDs, the yellow FAIL LED is lit when the BRDFAIL signal line is active, and the green CPU LED is lit when the DBB# signal of processor bus is active.

Typical ATX chassis have front panel controls and indicators including a momentary power switch, a reset switch, a power LED, a disk activity LED, and a speaker. See the *MTX Motherboard Preparation on page 1-4* section for information on connecting chassis controls and indicators.

## Memory Maps

There are two points of view for memory maps:

- ❑ The mapping of all resources as viewed by the processor (MPU bus memory map)
- ❑ The mapping of onboard resources as viewed by PCI local bus masters (PCI bus memory map)

The following sections give a general description of the MTX memory organization from the above two points of view. Detailed memory maps can be found in the *MTX Series Motherboard Programmer's Reference Guide* (part number MTXA/PG).

### Processor Memory Map

The processor memory map configuration is under the control of the Raven bridge controller ASIC and the Falcon memory controller chip set. The Raven and Falcon devices adjust system mapping to suit a given application via programmable map decoder registers. At system power-up or reset, a default processor memory map takes over.

#### Default Processor Memory Map

The default processor memory map that is valid at power-up or reset remains in effect until reprogrammed for specific applications. [Table 2-1 on page 2-4](#) defines the entire default memory map (\$00000000 to \$FFFFFFFF).

**Table 2-1. Processor Default View of the Memory Map**

| Processor Address |           | Size           | Definition        | Notes |
|-------------------|-----------|----------------|-------------------|-------|
| Start             | End       |                |                   |       |
| 0000 0000         | 7FFF FFFF | 2GB            | Not Mapped        |       |
| 8000 0000         | 8001 FFFF | 128KB          | PCI/ISA I/O Space | 1     |
| 8002 0000         | FEF7 FFFF | 2GB-16MB-640KB | Not Mapped        |       |
| FEF8 0000         | FEF8 FFFF | 64K            | Falcon Registers  |       |

**Table 2-1. Processor Default View of the Memory Map (Continued)**

| Processor Address |           | Size | Definition            | Notes |
|-------------------|-----------|------|-----------------------|-------|
| Start             | End       |      |                       |       |
| FEF9 0000         | FEFE FFFF | 384K | Not Mapped            |       |
| FEFF 0000         | FEFF FFFF | 64K  | Raven Registers       |       |
| FF00 0000         | FFEF FFFF | 15M  | Not Mapped            |       |
| FFF0 0000         | FFFF FFFF | 1M   | ROM/FLASH Bank A or B | 2     |

**Notes** 1. Default map for PCI/ISA I/O space. Allows software to determine whether the system is PPC105-based or Falcon/Raven-based by examining either the PHB Device ID or the CPU Type register.

2. The first 1MB of ROM/Flash bank A (soldered 4MB Flash) appears in this range after a reset if the **rom\_b\_rv** control bit in the Falcon's ROM B Base/Size register is cleared. If the **rom\_b\_rv** control bit is set, this address range maps to ROM/Flash bank B (socketed 1MB ROM/Flash).

For detailed processor memory maps, including suggested PREP and CHRP compatible memory maps, refer to the *MTX Series Motherboard Programmer's Reference Guide* (part number MTXA/PG).

## PCI Local Bus Memory Map

The local PCI memory map is the PCI memory map as viewed by the MTX motherboard. After a reset, the Raven ASIC map decoders are in their default (off) state. Software must program the appropriate map decoders for a specific environment. For detailed PCI memory maps, including suggested PREP-compatible memory maps, refer to the *MTX Series Motherboard Programmer's Reference Guide* (part number MTXA/PG).

## L2 Cache

The optional L2 cache functionality is provided via the Doubletake chipset. If populated, the Doubletake 512K look-aside cache option is implemented with two MPC2605GA (Doubletake) devices. Refer to the MPC2605GA Data Sheets and the *MTX Series Motherboard Programmer's Reference Guide* (MTXA/PG) for additional information.

## System Clock Generator

The PPC60X processor and PCI clocks are generated and distributed by the PPC949 clock generator. Additional clocks are independently generated for the SCSI-1, SCSI-2, Ultra SCSI (SCSI-3), ISA bridge, synchronous serial ports, Super I/O chip and the LAN physical layer reference.

## PowerPC PPC Bus Arbitration

The PPC address bus is handled either by the Raven ASIC or by external logic. The data bus arbitration is the responsibility of each PPC bus master and follows the ownership ordering established on the address bus.

The PCI-initiated transactions will always have the highest priority over all external PPC bus requests. There can be up to three external PPC masters; two processors and the look-aside L2 Cache (in copy-back mode). With external PPC arbiter, the priority is as follows:

| <b>PPC Master</b> | <b>Priority</b> |
|-------------------|-----------------|
| L2 Cache          | Highest         |
| Raven             |                 |
| CPU0, CPU1        | Lowest          |

## PCI Host Bridge

The Raven ASIC provides the bridge function between the PPC60X bus and the onboard PCI Local Bus. It is a 64-bit PCI implementation for data transfers. Dual Address Cycle is not supported. The Raven supports various PowerPC processor external bus frequencies up to 66MHz and PCI frequencies up to 33MHz.

There are four programmable map decoders for each direction to provide flexible address mappings between the PPC and the PCI Local Bus. Refer to the *MTX Series Motherboard Programmer's Reference Guide* for additional information and programming details.

## PCI Arbitration

The PCI arbitration is performed by the PIB which supports six PCI external PCI masters. The PIB can also be a PCI master for ISA DMA functions. The arbitration assignments on the MTX are as follows:

**Table 2-2. Primary PCI Arbitration Assignments**

| PCI Bus Request | PCI Master(s)     |
|-----------------|-------------------|
| PIB Internal    | PIB               |
| PIB CPU Request | Raven Host Bridge |
| PIB Request 0   | PMC/PCI Slot 2    |
| PIB Request 1   | PMC/PCI Slot 1    |
| PIB Request 2   | Ethernet          |
| PIB Request 3   | SCSI              |
| PIB Request 4   | PCI Slot 3        |

Upon power-up, the PIB defaults to a “round-robin” arbitration mode. The relative priority of each request/grant pair can be customized via the PCI Priority Control Register 1. Refer to the W83C554 Data Book for additional details.

## Interrupt Handling

The Raven ASIC provides an MPIC Interrupt Controller to handle various interrupt sources. This MPIC supports up to two processors and 16 external interrupt sources. There are also six other interrupt sources inside the MPIC: two cross-processor interrupts and four timer interrupts. All ISA interrupts go through the 8259 pair in the PIB. The output of the PIB then goes through the MPIC in Raven.

Sources of interrupts may be any of the following:

- ❑ The Raven ASIC itself (four MPIC timer interrupts or transfer error interrupts)
- ❑ The Processor 0 (processor self-interrupts)
- ❑ The Processor 1 (processor self-interrupts on dual processor motherboard)
- ❑ Transfer Error Interrupt (from the Raven ASIC)
- ❑ The Falcon chip set (memory error interrupts)
- ❑ The PCI bus (interrupts from PCI devices)
- ❑ Two software interrupts
- ❑ The ISA bus (interrupts from ISA devices)

For details on interrupt handling, refer to the *MTX Series Motherboard Programmer's Reference Guide* (part number MTXA/PG).

## ISA DMA Channels

The PIB supports seven 8237 compatible DMA channels. ISA compatible type A, B, and F timing and scatter/gather capability is supported. For more information refer to the *MTX Series Motherboard Programmer's Reference Guide* (part number MTXA/PG).

## Sources of Reset

There are five potential sources of reset on the MTX. They are:

Power-On Reset

RESET Switch

Watchdog Timer Reset via the MK48T59 Timekeeper device

Port 92 Register via the PIB

I/O Reset via the Clock Divisor Register in the PIB

The following table shows which devices are affected by various reset sources:

**Table 2-3. MTX Device Reset Implications**

| Device Affected                        | Processor (s) | Raven ASIC | Falcon3 Chipset | PCI Devices | ISA Devices |
|--|---------------|------------|-----------------|-------------|-------------|
| Power-On                               | x             | x          | x               | x           | x           |
| Reset Switch                           | x             | x          | x               | x           | x           |
| Watchdog (MK48T59)                     | x             | x          | x               | x           | x           |
| Hot Reset (Port 92 Register)           | x             | x          | x               | x           | x           |
| PCI/ISA Reset (Clock Divisor Register) |               |            |                 | x           | x           |

## Soft Reset

Software can assert the SRESET# pin of any processor by programming the Processor Init Register of the RavenMPIC appropriately.

## Error Notification and Handling

The Raven and Falcon chipset can detect certain hardware errors and can be programmed to report these errors via the RavenMPIC interrupts or Machine Check Interrupt. Note that the TEA\* signal is not used at all by the MTX. The following table summarizes how the hardware errors are handled by the MTX:

**Table 2-4. Error Notification and Handling**

| Cause            | Action   |
|------------------|--|
| Single-bit ECC   | <i>Store:</i> Write corrected data to memory<br><i>Load:</i> Present corrected data to the PPC master<br>Generate interrupt via RavenMPIC if so enabled  |
| Double-bit ECC   | <i>Store:</i> Terminate the bus cycle normally without writing to DRAM<br><i>Load:</i> Present un-corrected data to the PPC master<br>Generate interrupt via RavenMPIC if so enabled<br>Generate Machine Check Interrupt to the Processor(s) if so enabled |
| PPC Bus Time Out | <i>Store:</i> Discard write data and terminate bus cycle normally<br><i>Load:</i> Present undefined data to the PPC master<br>Generate interrupt via RavenMPIC if so enabled<br>Generate Machine Check Interrupt to the Processor(s) if so enabled         |
| PCI Target Abort | <i>Store:</i> Discard write data and terminate bus cycle normally<br><i>Load:</i> Return all 1's and terminate bus cycle normally<br>Generate interrupt via RavenMPIC if so enabled<br>Generate Machine Check Interrupt to the Processor(s) if so enabled  |
| PCI Master Abort | <i>Store:</i> Discard write data and terminate bus cycle normally<br><i>Load:</i> Return all 1's and terminate bus cycle normally<br>Generate interrupt via RavenMPIC if so enabled<br>Generate Machine Check Interrupt to the Processor(s) if so enabled  |
| PERR# Detected   | Generate interrupt via RavenMPIC if so enabled<br>Generate Machine Check Interrupt to the Processor(s) if so enabled   |
| SERR# Detected   | Generate interrupt via RavenMPIC if so enabled<br>Generate Machine Check Interrupt to the Processor(s) if so enabled   |

## Endian Issues

The MTX supports both little-endian (e.g. NT) and big-endian software (e.g. AIX). The PowerPC is inherently big-endian, while the PCI bus is inherently little-endian. The following sections summarize how the MTX handles software and hardware differences in big- and little-endian operations. For further details on endian considerations, refer to the *MTX Series Motherboard Programmer's Reference Guide* (part number MTXA/PG).

### Processor/Memory Domain

The MTX processor can operate in both big-endian and little-endian mode. However, it always treats the external processor/memory bus as big-endian by performing *address rearrangement and reordering* when running in little-endian mode. The PPC registers in the Raven PCI bus bridge controller ASIC and the Falcon memory controller chip set, as well as DRAM, ROM/Flash, and system registers always appear as big-endian.

#### Role of the Raven ASIC

Because the PCI bus is little-endian, the Raven performs byte swapping in both directions (from PCI to memory and from the processor to PCI) to maintain address invariance while programmed to operate in big-endian mode with the processor and the memory subsystem.

In little-endian mode, the Raven *reverse-rearranges* the address for PCI-bound accesses and *rearranges* the address for memory-bound accesses (from PCI). In this case, no byte swapping is done.

## PCI Domain

The PCI bus is inherently little-endian. All devices connected directly to the PCI bus operate in little-endian mode, regardless of the mode of operation in the processor's domain.

### PCI and Ethernet

Ethernet is also byte-stream-oriented; the byte having the lowest address in memory is the first one to be transferred regardless of the endian mode. Since the Raven maintains address invariance in both little-endian and big-endian mode, no endian issues should arise for Ethernet data. Big-endian software must still take the byte-swapping effect into account when accessing the registers of the PCI/Ethernet device, however.

## Introduction

This chapter describes the MTX motherboard computer on a block diagram level. The *General Description* provides an overview of the MTX, followed by a detailed description of several blocks of circuitry.

Detailed descriptions of other MTX blocks, including programmable registers in the ASICs and peripheral chips, can be found in the *MTX Series Motherboard Programmer's Reference Guide* (part number MTXA/PG). Refer to it for a functional description of the MTX in greater depth.

## Features

The following table summarizes the features of the MTX single-board computers.

**Table 3-1. MTX Features**

| Feature           | Description   |
|-------------------|---|
| Microprocessor    | Supports BGA 60x processors: 603e, 603ev, and 604ev<br>Single/dual processor (604ev); Bus Clock Frequencies up to 66MHz |
| DRAM              | Two-way Interleaved, ECC protected, 256MB to 2GB on board (DIMMs).  |
| L2 cache memory   | Build option for 512KB Look-aside L2 Cache (Doubletake)   |
| Flash Memory      | 4MB (16-bit wide) plus sockets for 1MB (16-bit)   |
| Memory Controller | Falcon Chipset  |
| Real-time clock   | 8KB NVRAM with RTC and battery backup (SGS-Thomson M48T59)  |
| Status LEDs       | two: BFL, CPU   |
| Watchdog timer    | Provided in SGS-Thomson M48T59  |
| Form Factor       | ATX   |

**Table 3-1. MTX Features (Continued)**

| Feature            | Description  |
|--------------------|--|
| Interrupts         | Software interrupt handling via RavenMPIC (PCI-MPU bridge)   |
| Peripheral Support | Two 16550-compatible async serial ports<br>Two sync/async serial ports<br>One Host-mode Parallel Port<br>One Peripheral-mode Parallel Port<br>8-bit/16-bit single-ended SCSI interface<br>AUI/10BaseT/100BaseTX Ethernet interface<br>One PS/2 Keyboard and one PS/2 Mouse<br>One PS/2 Floppy Port<br>Two EIDE ports |
| PCI/PMC Expansion  | Build option for two 32/64-bit PMC slots with back-panel I/O<br>Build option for one 32/64-bit PCI Connector for horizontal PCI card via special riser<br>Build option for three 32-bit vertical PCI card slots with back panel I/O  |
| Switches           | RESET Switch support<br>ABORT Swtich support   |

## General Description

The MTX is a motherboard based on the PowerPlus architecture, including optional features for embedded applications. It consists of the MPC603e/PID7v-603e/PID9v-604e processor, the Raven PCI Bridge and Interrupt Controller, the ECC Memory Controller Falcon chipset, 5MB of Boot FLASH, ECC-protected DRAM, and a large set of I/O peripherals.

The MTX will support single 603ev, single 604e processors, or dual 604e processors. In the dual processor configuration, the internal operating frequencies of the 604e processors are independently configurable.

I/O peripheral interfaces present onboard include SCSI interface, a 10/100-BASE-T Ethernet interface, two 64-bit PMC and one 64-bit PCI slot, or three 32-bit PCI slots. Functions provided from the ISA bus include: two

EIDE ports, a host mode P1284 parallel port, a peripheral mode P1284 parallel port, two async serial ports, two sync/async serial ports, a real time clock, and counters/timers.

Rear panel connectors on the MTX include two 6-pin circular DIN connectors (one for the keyboard and one for the mouse interface), a 25-pin host mode parallel port connector, a RJ45 connector for 10 BaseT/100 BaseTx ethernet, and a 15-pin connector for the AUI interface.

The MTX can be populated with two IEEE1386.1 PCI Mezzanine Card Slots plus a 64-bit PCI slot, or with two 32-bit PCI slots plus a 64-bit PCI slot, or with three 32-bit PCI slots. The 32-bit PCI slots support ATX standard I/O spacing. All slots use rear panel I/O. The 64-bit PCI slot supports a horizontal PCI card via a customl riser card.

DRAM memory is added via DIMM sockets. The serial presence detect (SPD) feature of the DIMM DRAMs is supported via the I2C bus controller.

Some of the features not mentioned in Chapter 2, *Operating Instructions* on page 2-1, are described in the following sections of this chapter.

## Block Diagram

Refer to [Figure 1-1 on page 1-2](#) for copy of block diagram.

## MTX Processor

The MTX processor has BGA footprints that support MPC60x processors: 603e, PID7v-603e, and PID9v-604e. The maximum processor system bus speed is 66 MHz.

## Interrupt Controller (MPIC)

The Raven ASIC also provides an MPIC Interrupt Controller to handle various interrupts sources. The interrupt sources are: Four MPIC Timer Interrupts, Processor 0 self interrupt, the Memory Error Interrupt from the Falcon chipset, the Transfer Error Interrupt from the Raven ASIC, the

interrupts from all PCI devices, the two software interrupts, and the ISA interrupts. The ISA interrupts actually are handled as a single 8259 interrupt at INTO.

Refer to the *MTX Series Motherboard Programmer's Reference Guide (MTXA/PG)* for additional information and programming details.

## Boot FLASH

The MTX contains two banks of FLASH memory on the main board. Bank A consists of two soldered-in 8-bit wide, 2 megabyte deep 3.3V FLASH SMT devices and appears as FLASH Bank A (16 bits wide) to the Falcon chipset. A resistor select enables write protect for the entire 4M of Bank A, individual 64K byte block protection can be enabled by software.

Bank B consists of two sockets for 8-bit wide +5.0 volt FLASH SMT devices and appears as FLASH Bank B (16-bits wide) to the Falcon chipset. The Bank B sockets support a maximum 512K byte FLASH in each socket.

## ECC Memory

The MTX supports up to 2GB of ECC DIMM memory. The DRAM memory is controlled by the Falcon chipset which performs two-way interleaving and provides single-bit error correction and double-bit error detection. ECC is calculated over 72-bits. Refer to the *MTX Series Motherboard Programmer's Reference Guide* for additional information and programming details.

## L2 Cache

The optional L2 cache functionality is provided via the Doubletake chipset. If populated, the Doubletake 512K look-aside cache option is implemented with two MPC2605GA (Doubletake) devices. Refer to the MPC2605GA Data Sheets and the *MTX Series Motherboard Programming Reference Guide (MTXA/PG)* for additional information.

## Registers

The MTX contains the System Configuration Registers and ISA Registers specified by the *MTX Series Motherboard Programmer's Reference Guide*.

## SCSI Interface

The MTX provides support for SCSI-1, SCSI-2, and SCSI-3 standards. The MTX implements fast 8- or 16-bit transfers and UltraSCSI transfers. The standard SCSI SCLK is 40 MHz for SCSI-1, 2, and Ultra SCSI transfers (the SYM53C875A clock doubler is used for Ultra). In addition, an 80 MHz clock build option is provided.

## Ethernet Interface

The MTX provides an Ethernet transceiver interface via the DEC21143 device. The Ethernet interface is routed to rear panel connectors. Users may select either the AUI interface or the 10BaseT/100BaseTX interface.

Every board is assigned an Ethernet Station Address. Each board's Ethernet Station Address is displayed on a label attached to the PWB. In addition, the Ethernet address is stored in the configuration area of the NVRAM specified by the Boot ROM.

## PCI-ISA Bridge (PIB)

The MTX board uses the WINBOND 83C554 device to interface to ISA bus for many system resources. The 83C554 device, hereafter referred to as the PIB, provides the following features:

- ❑ PCI bus arbitration for: ISA DMA, the PHB, all onboard PCI devices, and the PMC and PCI Slots.
- ❑ ISA bus arbitration for DMA devices
- ❑ ISA Interrupt mapping for four PCI interrupts

- ❑ Functionality of two 82C59 Interrupt Controllers to support 14 ISA interrupts
- ❑ Edge/Level control for ISA interrupts
- ❑ Seven independently programmable DMA channels (functionality of two 82C37SA devices)
- ❑ One 16-bit Timer
- ❑ Three interval Counters/Timers (82C54 functionality)
- ❑ Primary and secondary EIDE port

The Super I/O, ESCC, CIO, I<sup>2</sup>C, and peripheral mode parallel devices connect to the ISA bus.

## **EIDE Ports**

The PIB provides the primary and secondary EIDE port controller. See the Winbond System I/O controller with PCI Arbiter data book for additional information.

## **PC87308 ISA Super IO Device (ISASIO)**

The MTX board uses the PC87308 ISASIO from National Semiconductor to provide: two async serial ports, a host mode parallel port, a PS/2 floppy disk interface, a PS/2 keyboard interface, and a PS/2 mouse interface. Each of the supported features are described in the following sub-sections.

### **Async Serial Ports**

These two ports are routed to rear panel. Firmware initializes the two serial ports as COM1 and COM2 with ISA IO base addresses of x3F8 and x2F8 respectively. This default configuration also assigns COM1 to IRQ4 and COM2 to IRQ3 of the PIB. The default configuration can be changed by programming the ISASIO device accordingly.

**Host Mode P1284/Printer Interface**

The host mode parallel I/O interface signals are routed to a 25-pin subminiature rear panel connector. Firmware initializes the parallel port as PPT1 with ISA IO base address of x3BC. This default configuration also assigns the parallel port to IRQ7 of the PIB. The default configuration can be changed by programming the ISASIO device accordingly.

**PS/2 Floppy Disk Interface**

The floppy port is configured for PS/2 compatibility. The floppy disk signals and power are routed to a 34-pin planar connector.

**Mouse and Keyboard**

The ISASIO provides a ROM-based Award BIOS for a Keyboard and Mouse interface. Two 6-pin circular DIN connectors are located on the rear panel of the MTX board for the Keyboard and the Mouse connections.

## Real-Time Clock and NVRAM and Watchdog Timer

The SGS-Thomson M48T59 IC is used by the MTX board to provide 8KB of non-volatile static RAM, a real-time clock, and a watchdog function. Refer to the MK48T59 Data Sheets for programming information. The M48T59 consists of two parts:

- ❑ A 28-pin 330mil SO device which contains the RTC, the oscillator, the power fail detection, the watchdog timer logic, 8KB of SRAM, and gold-plated sockets for the SNAPHAT battery
- ❑ A SNAPHAT battery that houses the crystal and the battery

The SNAPHAT battery package is mounted on top of the SO MT48T59 device after the completion of the surface mount process. The battery housing is keyed to prevent reverse insertion.

## Timers

Timers and counters on the MTX board are provided by the PIB and the Z8536.

### Interval Timers

The PIB has three built-in counters that are equivalent to those found in a 82C54 programmable interval timer. These counters are grouped into one timer unit, Timer 1, in the PIB. Each counter output has a specific function:

- ❑ Counter 0 is associated with IRQ0 and can be used for system timing functions, such as timer interrupt for a time-of-day
- ❑ Counter 1 is used to generate a refresh request signal for ISA memory (This timer is not used.)
- ❑ Counter 2 provides the tone for the Speaker output function on the PIB

These counters use the OSC clock input as their clock source. The MTX drives the OSC pin with a 14.31818 MHz clock source.

## 16-Bit Timers

There are four 16-bit timers on the MTX: One 16-bit timer is provided by the PIB and three 16-bit timers are provided by the Z8536 device. Refer to the W83C554 Data Book and the Z8536 Data Sheets for programming information on these timers.

## Z85230 ESCC

The two sync/async ports are implemented with the Z85230 ESCC. Since the Z85230 does not have all modem control lines, a Z8536 CIO is used to provide the missing modem lines.

A PAL device is used to perform decode for the Z85230 and the Z8536 for register accesses and pseudo interrupt acknowledge cycles in ISA I/O space. DMA support for the Z85230 is provided by the PIB.

The clock input to the Z85230 PCLK pin is a 10 MHz clock. The Z85230 supplies an interrupt vector during a pseudo interrupt acknowledge cycle. The vector is modified based upon the interrupt source within the Z85230.

## Z8536 CIO

The Z8536 CIO is used to provide the modem control lines not provided by the Z85230 ESCC. In addition, the Z8536 CIO has three independent 16-bit counters/timers. The clock input to the Z8536 PCLK pin is 5 MHz. Refer to the *MTX Series Motherboard Programmer's Reference Guide* for the pin assignments for the Z8536 port pins.

## Peripheral Mode P1284/Printer Interface

The peripheral mode printer interface is implemented using the Cirrus Logic CL-CD1283 IEEE 1284-Compatible Parallel Interface Controller. The peripheral mode parallel 1283C interface signals are routed to a 40-pin planar header.

## PCI Arbitration

PCI arbitration is performed by the PIB. The PCI request/arbitration assignments are as specified by the *MTX Series Motherboard Programmer's Reference Guide* (MTXA/PG).

## Interrupt Routing

Interrupts are routed to the PIB as specified by the *MTX Series Motherboard Programmer's Reference Guide* (MTXA/PG).

## ISA DMA Channels

There are seven DMA channels supports by the PIB. These DMA channels are assigned as specified by the *MTX Series Motherboard Programmer's Reference Guide* (MTXA/PG).

## Front Panel Functions

The MTX has a 14 pin planar header for front panel functions including abort and reset switches, speaker interface, and LED drive. The header interfaces directly to the MEZLED board for diagnostic testing. +5.0V power is supplied via a 0.75 amp polyfuse. The header provides the LED drive for seven functions: FAIL, CHKSTP, CPU, and PCI, SCSI, Ethernet, EIDE:

- ❑ The STATLED# signal is active when either processor CHECKSTOP signal is active
- ❑ The FAILED# signal is active when the firmware controlled BRDFAIL signal is active
- ❑ The RUNLED# signal is active when the DBB# signal of the processor bus is active
- ❑ The LANLED# signal is active when the Ethernet LED\_TX signal is active

- ❑ The PCILED# signal is active when the IRDY# signal of the PCI bus is active
- ❑ The SBSYLED# signal is active when the firmware controlled SCSIBSY# signal is active
- ❑ The EIDELED# signal is active when an EIDE drive is connected and active

All LED signals go active during a hardware reset (power-up or reset switch activated).

In addition, the MTX has two planar LEDs: the yellow FAIL LED is lit when the BRDFAIL signal line is active and the green CPU LED is lit when the DBB# signal of processor bus is active.

## MEZLED Module

During diagnostic testing, the MTX uses the same MEZLED module designed for the MVME1600-011 to provide the status LEDs and the switches for Reset and Abort functions. The MTX LED signals map to the MEZLED LEDs as follows:

- ❑ DS1 is lit when either processor CHECKSTOP signal is active.
- ❑ DS2 is lit when the firmware controlled BRDFAIL signal is active.
- ❑ DS3 is lit when the DBB# signal of processor bus is active.
- ❑ DS4 is lit when the IRDY# signal of the PCI bus is active.
- ❑ DS5 is lit when the firmware controlled SCSIBSY# signal is active.
- ❑ DS6 is lit when the Ethernet LED\_TX signal is active.

## RESET Switch

The RESET switch is located on the MEZLED module. When activated, the RESET switch will cause MTX to reset and HRESET# to be asserted to the Processor Module.

### ABORT Switch

The ABORT switch is located on the MEZLED module. The MTX board can be programmed to generate an interrupt to the processor via ISA interrupt IRQ8# when the ABORT switch is activated.

### Speaker Control

The MTX board routes the SPEAKER\_OUT signal to the front panel function connector. When the MEZLED module is not used, a 14-pin ribbon cable can be used to access the SPEAKER\_OUT signal to drive an external speaker for beep-tone function. This signal is driven by a NPN transistor device which is controlled by the SPKR output pin from the PIB. The SPKR output pin is an output from the PIB Counter 2 and is “ANDed” with Port 61h bit 1 of the PIB to provide Speaker Data Enable.

### PCI Mezzanine Card Slots

The MTX board supports two PMC slots. Three EIA-xxx connectors are located on the MTX board to interface to 32-bit/64-bit IEEE P1386.1 PMC to add any desirable function. This PMC slot supports:

- ❑ Mezzanine Type: PMC = PCI Mezzanine Card
- ❑ Mezzanine Size: S1B = Single width & standard depth (75mm x 150mm) with front panel
- ❑ PMC Connectors: J11, J12, and J13, (32/64-Bit PCI with rear I/O)
- ❑ Signalling Voltage:  $V_{io} = 5.0V$

### Power Supply

The MTX uses a 20-pin ATX compatible connector for power input. The motherboard requires +5.0V power from an external supply, and will generate +3.3V and PDXv-60Xe processor power (1.8 to 2.6 volts) from the +5.0V supply. The MTX routes +3.3V, +5.0V, and -5.0V to the PMC and PCI slots, and fused power is routed to other peripherals as described in the paragraph below, *Polyswitches*.

## Polyswitches

The MTX board supplies +5.0V power to the mouse and keyboard via a 1.1 amp polyswitch, +5.0 (optional) to the SCSI termpower via a 1.1 amp polyswitch, and +12.0V to the AUI port via a 1.1 amp polyswitch.



## MTX Series Connectors

This chapter summarizes the pin assignments for the following connectors, headers and sockets on the MTX board:

- ❑ Debug connector
- ❑ RISCwatch Header Pin Definitions
- ❑ GAL Programming Header Pin Definitions
- ❑ DRAM DIMM Socket Pin Definitions
- ❑ Seven Segment LED Header
- ❑ Front Panel Function Header
- ❑ Rear Panel Keyboard/Mouse Connectors
- ❑ PCI Mezzanine Card (PMC) Connectors
- ❑ 10BaseT/100BaseTx Connector
- ❑ AUI Connector
- ❑ IEEE P1284 Host Mode Parallel I/O Connector
- ❑ IEEE P1284 Peripheral Mode Parallel I/O Connector
- ❑ EIDE Connectors
- ❑ Floppy Disk Header
- ❑ Serial Port 1 and 2 Connectors
- ❑ Serial Port 3 and 4 Connectors
- ❑ Power Connector

## Debug Connector

A footprint for a Mictor connector is used to provide access to the 60x bus for debugging purposes. The following table shows the pin assignments for this connector.

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**Table 4-1. Debug Connector Pin Assignments**

| Pin | Signal |  | Pin | Signal  |
|-----|--------|--|-----|---------|
| 1   | PA0    |  | 2   | PA1     |
| 3   | PA2    |  | 4   | PA3     |
| 5   | PA4    |  | 6   | PA5     |
| 7   | PA6    |  | 8   | PA7     |
| 9   | PA8    |  | 10  | PA9     |
| 11  | PA10   |  | 12  | PA11    |
| 13  | PA12   |  | 14  | PA13    |
| 15  | PA14   |  | 16  | PA15    |
| 17  | PA16   |  | 18  | PA17    |
| 19  | PA18   |  | 20  | PA19    |
| 21  | PA20   |  | 22  | PA21    |
| 23  | PA22   |  | 24  | PA23    |
| 25  | PA24   |  | 26  | PA25    |
| 27  | PA26   |  | 28  | PA27    |
| 29  | PA28   |  | 30  | PA29    |
| 31  | PA30   |  | 32  | PA31    |
| 33  | APAR0  |  | 34  | APAR1   |
| 35  | APAR2  |  | 36  | APAR3   |
| 37  | APE_L  |  | 38  | RSRV0_L |
| 39  | PD0    |  | 40  | PD1     |
| 41  | PD2    |  | 42  | PD3     |
| 43  | PD4    |  | 44  | PD5     |
| 45  | PD6    |  | 46  | PD7     |

**Table 4-1. Debug Connector Pin Assignments (Continued)**

| <b>Pin</b> | <b>Signal</b> | <b>Pin</b> | <b>Signal</b> |
|------------|---------------|------------|---------------|
| 47         | PD8           | 48         | PD9           |
| 49         | PD10          | 50         | PD11          |
| 51         | PD12          | 52         | PD13          |
| 53         | PD14          | 54         | PD15          |
| 55         | PD16          | 56         | PD17          |
| 57         | PD18          | 58         | PD19          |
| 59         | PD20          | 60         | PD21          |
| 61         | PD22          | 62         | PD23          |
| 63         | PD24          | 64         | PD25          |
| 65         | PD26          | 66         | PD27          |
| 67         | PD28          | 68         | PD29          |
| 69         | PD30          | 70         | PD31          |
| 71         | PD32          | 72         | PD33          |
| 73         | PD34          | 74         | PD35          |
| 75         | PD36          | 76         | PD37          |
| 77         | PD38          | 78         | PD39          |
| 79         | PD40          | 80         | PD41          |
| 81         | PD42          | 82         | PD43          |
| 83         | PD44          | 84         | PD45          |
| 85         | PD46          | 86         | PD47          |
| 87         | PD48          | 88         | PD49          |
| 89         | PD50          | 90         | PD51          |
| 91         | PD52          | 92         | PD53          |
| 93         | PD54          | 94         | PD55          |
| 95         | PD56          | 96         | PD57          |
| 97         | PD58          | 98         | PD59          |
| 99         | PD60          | 100        | PD61          |
| 101        | PD62          | 102        | PD63          |
| 103        | DPAR0         | 104        | DPAR1         |

**Table 4-1. Debug Connector Pin Assignments (Continued)**

| <b>Pin</b> | <b>Signal</b> | <b>Pin</b> | <b>Signal</b> |
|------------|---------------|------------|---------------|
| 105        | DPAR2         | 106        | DPAR3         |
| 107        | DPAR4         | 108        | DPAR5         |
| 109        | DPAR6         | 110        | DPAR7         |
| 111        | NC            | 112        | NC            |
| 113        | DPE_L         | 114        | DBDIS_L       |
| 115        | TT0           | 116        | TSIZ0         |
| 117        | TT1           | 118        | TSIZ1         |
| 119        | TT2           | 120        | TSIZ2         |
| 121        | TT3           | 122        | TC0           |
| 123        | TT4           | 124        | TC1           |
| 125        | CI_L          | 126        | TC2           |
| 127        | WT_L          | 128        | CSE0          |
| 129        | GBL_L         | 130        | CSE1          |
| 131        | SHD_L         | 132        | DBWO_L        |
| 133        | AACK_L        | 134        | TS_L          |
| 135        | ARTRY_L       | 136        | XATS_L        |
| 137        | DRTRY_L       | 138        | TBST_L        |
| 139        | TA_L          | 140        | NC            |
| 141        | TEA_L         | 142        | NC            |
| 143        | NC            | 144        | DBG_L         |
| 145        | NC            | 146        | DBB_L         |
| 147        | NC            | 148        | ABB_L         |
| 149        | TCLK0         | 150        | MPUBG0_L      |
| 151        | NC            | 152        | MPUBR0_L      |
| 153        | MPUBR1_L      | 154        | IRQ0_L        |
| 155        | MPUBG1_L      | 156        | MCHK0_L       |
| 157        | IRQ1_L        | 158        | SMI_L         |
| 159        | MCHK1_L       | 160        | CKSTPI0_L     |
| 161        | L2BR_L        | 162        | CKSTPO0       |

**Table 4-1. Debug Connector Pin Assignments (Continued)**

| Pin | Signal    | Pin | Signal     |
|-----|-----------|-----|------------|
| 163 | L2BG_L    | 164 | HALTED0    |
| 165 | CLAIM_L   | 166 | TLBISYNC_L |
| 167 | NC        | 168 | TBEN0      |
| 169 | NC        | 170 | TBEN1      |
| 171 | NC        | 172 | DRVMOD0    |
| 173 | NC        | 174 | DRVMOD1    |
| 175 | NC        | 176 | NAPRUN0    |
| 177 | SRESET1_L | 178 | QREQ_L     |
| 179 | SRESET0_L | 180 | QACK_L     |
| 181 | HRESET_L  | 182 | CPU0TDO    |
| 183 | GND       | 184 | CPU0TDI    |
| 185 | MPUCLK    | 186 | CPU0TCK    |
| 187 | MPUCLK    | 188 | CPU0TMS    |
| 189 | MPUCLK    | 190 | CPU0TRST_L |

## RISCVATCH Header Pin Definitions

**Table 4-2. RISCwatch Header**

| Signal    | Pin | Pin | Signal    |
|-----------|-----|-----|-----------|
| CPUITDO   | 1   | 2   | NC        |
| CPUITDI   | 3   | 4   | CPU1RST_L |
| NC        | 5   | 6   | 1KPU_3.3V |
| CPUITCK   | 7   | 8   | NC        |
| CPUITMS   | 9   | 10  | NC        |
| SRESET1_L | 11  | 12  | NC        |
| ISABPWGD  | 13  | 14  | KEYPIN    |
| CKSTP01_L | 15  | 16  | GND       |

## GAL Programming Header Pin Definitions

**Table 4-3. GAL Programming Header Pin Definitions**

| Signal  | Pin |
|---------|-----|
| +5.0v   | 1   |
| ISPSDO  | 2   |
| ISPSDI  | 3   |
| ISPEN_L | 4   |
| KEY     | 5   |
| ISPMODE | 6   |
| GND     | 7   |
| ISPSCLK | 8   |

## DRAM DIMM Socket Pin Definitions

**Table 4-4. DRAM DIMM Socket Pin Definitions**

| Pin# | Front Side | Pin# | Front Side | Pin# | Rear Side | Pin# | Rear Side |
|------|------------|------|------------|------|-----------|------|-----------|
| 1    | Vss        | 43   | Vss        | 85   | Vss       | 127  | Vss       |
| 2    | DQ0        | 44   | OE2_L      | 86   | DQ32      | 128  | DU        |
| 3    | DQ1        | 45   | RAS2_L     | 87   | DQ33      | 129  | RAS3_L    |
| 4    | DQ2        | 46   | CAS2_L     | 88   | DQ34      | 130  | CAS6_L    |
| 5    | DQ3        | 47   | CAS3_L     | 89   | DQ35      | 131  | CAS7_L    |
| 6    | Vcc        | 48   | WE2_L      | 90   | Vcc       | 132  | DU        |
| 7    | DQ4        | 49   | Vcc        | 91   | DQ36      | 133  | Vcc       |
| 8    | DQ5        | 50   | NC         | 92   | DQ37      | 134  | NC        |
| 9    | DQ6        | 51   | NC         | 93   | DQ38      | 135  | NC        |
| 10   | DQ7        | 52   | CB2        | 94   | DQ39      | 136  | CB6       |
| 11   | DQ8        | 53   | CB3        | 95   | DQ40      | 137  | CB7       |
| 12   | Vss        | 54   | Vss        | 96   | Vss       | 138  | Vss       |
| 13   | DQ9        | 55   | DQ16       | 97   | DQ41      | 139  | DQ48      |
| 14   | DQ10       | 56   | DQ17       | 98   | DQ42      | 140  | DQ49      |
| 15   | DQ11       | 57   | DQ18       | 99   | DQ43      | 141  | DQ50      |

**Table 4-4. DRAM DIMM Socket Pin Definitions (Continued)**

| Pin# | Front Side | Pin# | Front Side | Pin# | Rear Side | Pin# | Rear Side |
|------|------------|------|------------|------|-----------|------|-----------|
| 16   | DQ12       | 58   | DQ19       | 100  | DQ44      | 142  | DQ51      |
| 17   | DQ13       | 59   | Vcc        | 101  | DQ45      | 143  | Vcc       |
| 18   | Vcc        | 60   | DQ20       | 102  | Vcc       | 144  | DQ52      |
| 19   | DQ14       | 61   | NC         | 103  | DQ46      | 145  | NC        |
| 20   | DQ15       | 62   | DU         | 104  | DQ47      | 146  | DU        |
| 21   | CB0        | 63   | NC         | 105  | CB4       | 147  | NC        |
| 22   | CB1        | 64   | Vss        | 106  | CB5       | 148  | Vss       |
| 23   | Vss        | 65   | DQ21       | 107  | Vss       | 149  | DQ53      |
| 24   | NC         | 66   | DQ22       | 108  | NC        | 150  | DQ54      |
| 25   | NC         | 67   | DQ23       | 109  | NC        | 151  | DQ55      |
| 26   | Vcc        | 68   | Vss        | 110  | Vcc       | 152  | Vss       |
| 27   | WE0_L      | 69   | DQ24       | 111  | DU        | 153  | DQ56      |
| 28   | CAS0_L     | 70   | DQ25       | 112  | CAS4_L    | 154  | DQ57      |
| 29   | CAS1_L     | 71   | DQ26       | 113  | CAS5_L    | 155  | DQ58      |
| 30   | RAS0_L     | 72   | DQ27       | 114  | RAS1_L    | 156  | DQ59      |
| 31   | OE0_L      | 73   | Vcc        | 115  | DU        | 157  | Vcc       |
| 32   | Vss        | 74   | DQ28       | 116  | Vss       | 158  | DQ60      |
| 33   | A0         | 75   | DQ29       | 117  | A1        | 159  | DQ61      |
| 34   | A2         | 76   | DQ30       | 118  | A3        | 160  | DQ62      |
| 35   | A4         | 77   | DQ31       | 119  | A5        | 161  | DQ63      |
| 36   | A6         | 78   | Vss        | 120  | A7        | 162  | Vss       |
| 37   | A8         | 79   | NC         | 121  | A9        | 163  | NC        |
| 38   | A10        | 80   | NC         | 122  | A11       | 164  | NC        |
| 39   | A12        | 81   | NC         | 123  | NC        | 165  | SA0       |
| 40   | Vcc        | 82   | SDA        | 124  | Vcc       | 166  | SA1       |
| 41   | Vcc        | 83   | SCL        | 125  | DU        | 167  | SA2       |
| 42   | DU         | 84   | Vcc        | 126  | DU        | 168  | Vcc       |

**Note** NC = no connect, DU = do not use

## Seven Segment LED Header

**Table 4-5. Seven Segment LED Header**

| Signal      | Pin | Pin | Signal      |
|-------------|-----|-----|-------------|
| +5_SSEG     | 1   | 2   | +5_SSEG     |
| LEDDISP(0)  | 3   | 4   | LEDDISP(1)  |
| LEDDISP(2)  | 5   | 6   | LEDDISP(3)  |
| LEDDISP(4)  | 7   | 8   | LEDDISP(5)  |
| LEDDISP(6)  | 9   | 10  | LEDDISP(7)  |
| LEDDISP(8)  | 11  | 12  | LEDDISP(9)  |
| LEDDISP(10) | 13  | 14  | LEDDISP(11) |
| LEDDISP(12) | 15  | 16  | LEDDISP(13) |
| LEDDISP(14) | 17  | 18  | LEDDISP(15) |
| LEDBLNK     | 19  | 20  | GND         |

## Front Panel Function Header

**Table 4-6. Front Panel Function Header**

| Signal     | Pin | Pin | Signal    |
|------------|-----|-----|-----------|
| GND        | 1   | 2   | RESETSW_L |
| NO CONNECT | 3   | 4   | ABPRTSW_L |
| PCILED_L   | 5   | 6   | FAILED_L  |
| NO CONNECT | 7   | 8   | STATLED_L |
| SBSYLED_L  | 9   | 10  | RUNLED_L  |
| EIDELED_L  | 11  | 12  | LANLED_L  |
| +5V_LED    | 13  | 14  | SPEAKER   |

## Rear Panel Keyboard/Mouse Connectors

The Keyboard and Mouse connectors are 6-pin circular DIN connectors, located on the rear panel of the MTX. The pin assignments for the Keyboard and Mouse connectors are as follows:

**Table 4-7. Keyboard Connector Pin Assignments**

|   |            |
|---|------------|
| 1 | KDATA      |
| 2 | No Connect |
| 3 | GND        |
| 4 | +5VF       |
| 5 | KCLK       |
| 6 | No Connect |

**Table 4-8. Mouse Connector Pin Assignments**

|   |            |
|---|------------|
| 1 | MDATA      |
| 2 | No Connect |
| 3 | GND        |
| 4 | +5VF       |
| 5 | MCLK       |
| 6 | No Connect |

## PCI Mezzanine Card (PMC) Connectors

There are two sets (three connectors for each set) of SMT connectors on the MTX that provide two 32/64-bit PCI interfaces for optional add-on PCI Mezzanine Cards (PMC). Connectors J11-J13 form PMC Slot 1 and connectors J21-J23 form PMC Slot 2. The pin assignments are as follows:

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**Table 4-9. PMC Connector J11/J21 Pin Assignments**

| J11 |                        |          |
|-----|------------------------|----------|
| 1   | TCK                    | -12V     |
| 3   | GND                    | INTA#    |
| 5   | INTB#                  | INTC#    |
| 7   | PMCPRSNT#              | +5V      |
| 9   | INTD#                  | Not Used |
| 11  | GND                    | Not Used |
| 13  | CLK                    | GND      |
| 15  | GND                    | PMCGNT#  |
| 17  | PMCREQ#                | +5V      |
| 19  | +5V (V <sub>io</sub> ) | AD31     |
| 21  | AD28                   | AD27     |
| 23  | AD25                   | GND      |
| 25  | GND                    | C/BE3#   |
| 27  | AD22                   | AD21     |
| 29  | AD19                   | +5V      |
| 31  | +5V (V <sub>io</sub> ) | AD17     |
| 33  | FRAME#                 | GND      |
| 35  | GND                    | IRDY#    |
| 37  | DEVSEL#                | +5V      |
| 39  | GND                    | LOCK#    |
| 41  | SDONE#                 | SBO#     |
| 43  | PAR                    | GND      |

**Table 4-9. PMC Connector J11/J21 Pin Assignments (Continued)**

|    |           |        |    |
|----|-----------|--------|----|
| 45 | +5V (Vio) | AD15   | 46 |
| 47 | AD12      | AD11   | 48 |
| 49 | AD09      | +5V    | 50 |
| 51 | GND       | C/BE0# | 52 |
| 53 | AD06      | AD05   | 54 |
| 55 | AD04      | GND    | 56 |
| 57 | +5V (Vio) | AD03   | 58 |
| 59 | AD02      | AD01   | 60 |
| 61 | AD00      | +5V    | 62 |
| 63 | GND       | REQ64# | 64 |

**Table 4-10. PMC Connector J12/J22 Pin Assignments**

| J12 |          |           |
|-----|----------|-----------|
| 1   | +12V     | TRST#     |
| 3   | TMS      | TDO       |
| 5   | TDI      | GND       |
| 7   | GND      | Not Used  |
| 9   | Not Used | Not Used  |
| 11  | Pull-up  | +3.3V     |
| 13  | RST#     | Pull-down |
| 15  | +3.3V    | Pull-down |
| 17  | Not Used | GND       |
| 19  | AD30     | AD29      |
| 21  | GND      | AD26      |
| 23  | AD24     | +3.3V     |
| 25  | IDSEL    | AD23      |
| 27  | +3.3V    | AD20      |
| 29  | AD18     | GND       |

**Table 4-10. PMC Connector J12/J22 Pin Assignments (Continued)**

|    |          |          |    |
|----|----------|----------|----|
| 31 | AD16     | C/BE2#   | 32 |
| 33 | GND      | Not Used | 34 |
| 35 | TDRY#    | +3.3V    | 36 |
| 37 | GND      | STOP#    | 38 |
| 39 | PERR#    | GND      | 40 |
| 41 | +3.3V    | SERR#    | 42 |
| 43 | C/BE1#   | GND      | 44 |
| 45 | AD14     | AD13     | 46 |
| 47 | GND      | AD10     | 48 |
| 49 | AD08     | +3.3V    | 50 |
| 51 | AD07     | Not Used | 52 |
| 53 | +3.3V    | Not Used | 54 |
| 55 | Not Used | GND      | 56 |
| 57 | Not Used | Not Used | 58 |
| 59 | GND      | Not Used | 60 |
| 61 | ACK64#   | +3.3V    | 62 |
| 63 | GND      | Not Used | 64 |

**Table 4-11. PMC Connector J13/J23 Pin Assignments**

| J13 |           |        |    |
|-----|-----------|--------|----|
| 1   | Reserved  | GND    | 2  |
| 3   | GND       | C/BE7# | 4  |
| 5   | C/BE6#    | C/BE5# | 6  |
| 7   | C/BE4#    | GND    | 8  |
| 9   | +5V (Vio) | PAR64  | 10 |
| 11  | AD63      | AD62   | 12 |
| 13  | AD61      | GND    | 14 |
| 15  | GND       | AD60   | 16 |

**Table 4-11. PMC Connector J13/J23 Pin Assignments (Continued)**

|    |           |          |    |
|----|-----------|----------|----|
| 17 | AD59      | AD58     | 18 |
| 19 | AD57      | GND      | 20 |
| 21 | +5V (Vio) | AD56     | 22 |
| 23 | AD55      | AD54     | 24 |
| 25 | AD53      | GND      | 26 |
| 27 | GND       | AD52     | 28 |
| 29 | AD51      | AD50     | 30 |
| 31 | AD49      | GND      | 32 |
| 33 | GND       | AD48     | 34 |
| 35 | AD47      | AD46     | 36 |
| 37 | AD45      | GND      | 38 |
| 39 | +5V (Vio) | AD44     | 40 |
| 41 | AD43      | AD42     | 42 |
| 43 | AD41      | GND      | 44 |
| 45 | GND       | AD40     | 46 |
| 47 | AD39      | AD38     | 48 |
| 49 | AD37      | GND      | 50 |
| 51 | GND       | AD36     | 52 |
| 53 | AD35      | AD34     | 54 |
| 55 | AD33      | GND      | 56 |
| 57 | +5V (Vio) | AD32     | 58 |
| 59 | Reserved  | Reserved | 60 |
| 61 | Reserved  | GND      | 62 |
| 63 | GND       | Reserved | 64 |

## 10BaseT/100BaseTx Connector

The 10BaseT/100BaseTx Connector is an RJ45 connector located on the rear panel of the Transition Module. The pin assignments for this connector are as follows:

**Table 4-12. 10/100BaseT Connector Pin Assignments**

|   |                         |
|---|-------------------------|
| 1 | TD+                     |
| 2 | TD-                     |
| 3 | RD+                     |
| 4 | Common Mode Termination |
| 5 | Common Mode Termination |
| 6 | RD-                     |
| 7 | Common Mode Termination |
| 8 | Common Mode Termination |

## AUI Connector

The AUI Connector is a 15-pin connector located on the rear panel. The pin assignments for this connector are as follows:

**Table 4-13. AUI Connector Pin Assignments**

|    |            |
|----|------------|
| 1  | GND        |
| 2  | C+         |
| 3  | T+         |
| 4  | GND        |
| 5  | R+         |
| 6  | GND        |
| 7  | No Connect |
| 8  | GND        |
| 9  | C-         |
| 10 | T-         |
| 11 | GND        |

**Table 4-13. AUI Connector Pin Assignments (Continued)**

|    |       |
|----|-------|
| 12 | R-    |
| 13 | GND   |
| 14 | +12VF |
| 15 | GND   |

## IEEE P1284 Host Mode Parallel I/O Connector

The host mode parallel I/O connector is a standard IEEE P1284A 25-pin connector located on the rear panel of the ATX motherboard. The pin assignments for this connector are as follows:

**Table 4-14. Host Mode Parallel I/O Connector Pin Assignments**

|    |             |             |    |
|----|-------------|-------------|----|
| 1  | STROBE_L    | AUTOFDXT_L  | 14 |
| 2  | DATA_1      | FAULT_L     | 15 |
| 3  | DATA_2      | INIT_L      | 16 |
| 4  | DATA_3      | SELECT_IN_L | 17 |
| 5  | DATA_4      | GND         | 18 |
| 6  | DATA_5      | GND         | 19 |
| 7  | DATA_6      | GND         | 20 |
| 8  | DATA_7      | GND         | 21 |
| 9  | DATA_8      | GND         | 22 |
| 10 | ACK_L       | GND         | 23 |
| 11 | BUSY        | GND         | 24 |
| 12 | PAPER_EMPTY | GND         | 25 |
| 13 | SELECT_L    |             |    |

## IEEE P1284 Peripheral Mode Parallel I/O Connector

The peripheral mode parallel I/O connector is a 40-pin planar header designed for ribbon cable connection to a 1284-C connector.

**Table 4-15. Peripheral Mode Parallel I/O Connector Pin Assignments**

|    |            |            |    |
|----|------------|------------|----|
| 1  | PtrBusy    | GND        | 2  |
| 3  | Xflag      | GND        | 4  |
| 5  | PtrClk     | GND        | 6  |
| 7  | nDataAvail | GND        | 8  |
| 9  | AckDataReq | GND        | 10 |
| 11 | Data_1     | GND        | 12 |
| 13 | Data_2     | GND        | 14 |
| 15 | Data_3     | GND        | 16 |
| 17 | Data_4     | GND        | 18 |
| 19 | Data_5     | GND        | 20 |
| 21 | Data_6     | GND        | 22 |
| 23 | Data_7     | GND        | 24 |
| 25 | Data_8     | GND        | 26 |
| 27 | nInit      | GND        | 28 |
| 29 | HostClk    | GND        | 30 |
| 31 | A_1284     | GND        | 32 |
| 33 | HostBusy   | GND        | 34 |
| 35 | No Connect | +5.0VPP    | 36 |
| 37 | No Connect | No Connect | 38 |
| 39 | No Connect | No Connect | 40 |

## EIDE Connectors

The 40-pin planar headers provide the interface to the primary and secondary EIDE ports. The pinouts for the ports are below:

**Table 4-16. Primary EIDE Connector Pin Assignments**

|    |          |            |    |
|----|----------|------------|----|
| 1  | PCIRST_L | GND        | 2  |
| 3  | DATA_7   | DATA_8     | 4  |
| 5  | DATA_6   | DATA_9     | 6  |
| 7  | DATA_5   | DATA_10    | 8  |
| 9  | DATA_4   | DATA_11    | 10 |
| 11 | DATA_3   | DATA_12    | 12 |
| 13 | DATA_2   | DATA_13    | 14 |
| 15 | DATA_1   | DATA_14    | 16 |
| 17 | DATA_0   | DATA_15    | 18 |
| 19 | GND      | No Connect | 20 |
| 21 | DRQA     | GND        | 22 |
| 23 | IOWA_L   | GND        | 24 |
| 25 | IORA_L   | GND        | 26 |
| 27 | CHRDY    | No Connect | 28 |
| 29 | DAKA_L   | GND        | 30 |
| 31 | IRQA     | IOCS16_L   | 32 |
| 33 | DA1      | No Connect | 34 |
| 35 | DA0      | DA2        | 36 |
| 37 | CS0_L    | CS1_L      | 38 |
| 39 | LEDA_L   | GND        | 40 |

**Table 4-17. Secondary EIDE Connector Pin Assignments**

|   |          |         |   |
|---|----------|---------|---|
| 1 | PCIRST_L | GND     | 2 |
| 3 | DATA_7   | DATA_8  | 4 |
| 5 | DATA_6   | DATA_9  | 6 |
| 7 | DATA_5   | DATA_10 | 8 |

**Table 4-17. Secondary EIDE Connector Pin Assignments (Continued)**

|    |        |            |    |
|----|--------|------------|----|
| 9  | DATA_4 | DATA_11    | 10 |
| 11 | DATA_3 | DATA_12    | 12 |
| 13 | DATA_2 | DATA_13    | 14 |
| 15 | DATA_1 | DATA_14    | 16 |
| 17 | DATA_0 | DATA_15    | 18 |
| 19 | GND    | No Connect | 20 |
| 21 | DRQB   | GND        | 22 |
| 23 | IOWB_L | GND        | 24 |
| 25 | IORB_L | GND        | 26 |
| 27 | CHRDY  | No Connect | 28 |
| 29 | DAKB_L | GND        | 30 |
| 31 | IRQB   | IOCS16_L   | 32 |
| 33 | DA1    | No Connect | 34 |
| 35 | DA0    | DA2        | 36 |
| 37 | CS0_L  | CS1_L      | 38 |
| 39 | LEDB_L | GND        | 40 |

## Floppy Disk Header

**Table 4-18. Floppy Disk Header Pin Assignments**

| Signal | Pin | Pin | Signal     |
|--------|-----|-----|------------|
| GND    | 1   | 2   | F_MSEN1    |
| GND    | 3   | 4   | F_DENSEL   |
| GND    | 5   | 6   | F_MENS0    |
| GND    | 7   | 8   | F_INDEX_L  |
| GND    | 9   | 10  | F_MTR0_L   |
| GND    | 11  | 12  | F_DR1_L    |
| GND    | 13  | 14  | F_DR0_L    |
| GND    | 15  | 16  | F_MTR1_L   |
| GND    | 17  | 18  | F_DIR_L    |
| GND    | 19  | 20  | F_STEP_L   |
| GND    | 21  | 22  | F_WDATA_L  |
| GND    | 23  | 24  | F_WGATE_L  |
| GND    | 25  | 26  | F_TRK0_L   |
| GND    | 27  | 28  | F_WP_L     |
| GND    | 29  | 30  | F_RDATA_L  |
| GND    | 31  | 32  | F_HDSEL_L  |
| GND    | 33  | 34  | F_DSKCHG_L |

## Serial Port 1 and 2 Connectors

Planar headers provide the interface to Serial Ports 1 and 2. The pin assignments for these headers is as follows:

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**Table 4-19. COM1 Header Pin Assignments**

|   |     |
|---|-----|
| 1 | DCD |
| 2 | RXD |
| 3 | TXD |
| 4 | DTR |
| 5 | GND |
| 6 | DSR |
| 7 | RTS |
| 8 | CTS |
| 9 | RI  |

**Table 4-20. COM2 Header Pin Assignments**

|   |     |
|---|-----|
| 1 | DCD |
| 2 | RXD |
| 3 | TXD |
| 4 | DTR |
| 5 | GND |
| 6 | DSR |
| 7 | RTS |
| 8 | CTS |
| 9 | RI  |

## Serial Ports 3 and 4 Headers

Two 25-pin planar headers provide the connection to serial ports 3 and 4. The pin assignments for the connectors are:

**Table 4-21. Pin Assignments for Serial Ports 3 and 4**

| Pin # | Signal Name |
|-------|-------------|
| 1     | No Connect  |
| 2     | No Connect  |
| 3     | TxD         |
| 4     | AUX CLK     |
| 5     | RxD         |
| 6     | No Connect  |
| 7     | RTS         |
| 8     | RX CLK      |
| 9     | CTS         |
| 10    | LL          |
| 11    | DSR         |
| 12    | No Connect  |
| 13    | GND         |
| 14    | DTR         |
| 15    | DCD         |
| 16    | RL          |
| 17    | No Connect  |
| 18    | RNG         |
| 19    | No Connect  |
| 20    | No Connect  |
| 21    | No Connect  |
| 22    | TX CLK      |

**Table 4-21. Pin Assignments for Serial Ports 3 and 4 (Continued)**

| Pin # | Signal Name |
|-------|-------------|
| 23    | No Connect  |
| 24    | TM          |
| 25    | No Connect  |

## Power Connector

The MTX power connector is a 20-pin connector compatible with the ATX specified Molex Part Number 39-29-9202. Pin assignments are as follows:

**Table 4-22. Pin Assignments for Power Connector**

| Pin # | Signal Name |
|-------|-------------|
| 1     | NC          |
| 2     | NC          |
| 3     | GND         |
| 4     | +5.0V       |
| 5     | GND         |
| 6     | +5.0V       |
| 7     | GND         |
| 8     | PW-OK       |
| 9     | NC          |
| 10    | +12.0V      |
| 11    | NC          |
| 12    | -12.0V      |
| 13    | GND         |
| 14    | PS-ON       |
| 15    | GND         |
| 16    | GND         |
| 17    | GND         |
| 18    | NC          |

**Table 4-22. Pin Assignments for Power Connector (Continued)**

| Pin # | Signal Name |
|-------|-------------|
| 19    | +5.0V       |
| 20    | +5.0V       |



## Overview

You can use the factory-installed debug monitor, PPCBug, to modify certain parameters contained in the PowerPC board's Non-Volatile RAM (NVRAM), also known as Battery Backed-up RAM (BBRAM).

- ❑ The Board Information Block in NVRAM contains various elements concerning operating parameters of the hardware. Use the PPCBug command **CNFG** to change those parameters.
- ❑ Use the PPCBug command **ENV** to change configured PPCBug parameters in NVRAM.

The **CNFG** and **ENV** commands are both described in the *PPCBug Firmware Package User's Manual* (part number PPCBUGA1/UM). Refer to that manual for general information about their use and capabilities.

The following paragraphs present additional information about **CNFG** and **ENV** that is specific to the PPCBug debugger, along with the parameters that can be configured with the **ENV** command.

## CNFG - Configure Board Information Block

Use this command to display and configure the Board Information Block, which is resident within the NVRAM. The board information block contains various elements detailing specific operational parameters of the PowerPC board. The board structure for the PowerPC board is as shown in the following example for an MTX:

```
Board (PWA) Serial Number      = "2717994      "  
Board Identifier               = "MTX-60X-0XX    "  
Artwork (PWA) Identifier      = "01-w3187F03B  "  
MPU Clock Speed               = "200          "  
Bus Clock Speed               = "067          "  
Ethernet Address              = 08003E25D0C5  
Local SCSI Identifier         = "07           "  
System Serial Number          = "1234567      "  
System Identifier             = "Motorola MTX603-001a"  
License Identifier            = "12345678     "
```

The parameters that are quoted are left-justified character (ASCII) strings padded with space characters, and the quotes (“”) are displayed to indicate the size of the string. Parameters that are not in quotes are considered data strings. Data strings are right-justified. The data strings are padded with zeroes if the length is not met.

The Board Information Block is factory-configured before shipment. There is no need to modify block parameters unless the NVRAM is corrupted.

Refer to the *Programmer's Reference Guide* (part number MTXA/PG) for the actual location and other information about the Board Information Block.

Refer to the *PPC Bug Firmware Package User's Manual* (part number PPCBUGA1/UM) for a description of **CNFG** and examples.

# ENV - Set Environment

Use the **ENV** command to interactively view and/or configure all PPCBug operational parameters that are kept in Non-Volatile RAM (NVRAM).

Refer to the *PPCBug Firmware Package User's Manual* for a description of the use of **ENV**.

Listed and described below are the parameters that you can configure using **ENV**. The default values shown were those in effect when this publication went to print.

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## Configuring the PPCBug Parameters

The parameters that can be configured using **ENV** are:

Bug or System environment [B/S] = B?

- B** Bug is the mode where no system type of support is displayed. However, system-related items are still available. (Default)
- S** System is the standard mode of operation and is the default mode if NVRAM should fail. System mode is defined in the *PPCBug Firmware Package User's Manual*.

Field Service Menu Enable [Y/N] = N?

- Y** Display the field service menu.
- N** Do not display the field service menu. (Default)

Probe System for Supported I/O Controllers [Y/N] = Y?

- Y** Access will be made to the appropriate system buses (e.g., VMEbus, local MPU bus) to determine the presence of supported controllers. (Default)
- N** Access will not be made to the VMEbus to determine the presence of supported controllers.

Auto-Initialize of NVRAM Header Enable [Y/N] = Y?

- Y** NVRAM (PReP partition) header space will be initialized automatically during board initialization, but only if the PReP partition fails a sanity check. (Default)
- N** NVRAM header space will not be initialized automatically during board initialization.

Network PReP-Boot Mode Enable [Y/N] = N?

- Y** Enable PReP-style network booting (same boot image from a network interface as from a mass storage device).
- N** Do not enable PReP-style network booting. (Default)

SCSI Bus Reset on Debugger Startup [Y/N] = N?

- Y** SCSI bus is reset on debugger setup.
- N** SCSI bus is not reset on debugger setup. (Default)

Primary SCSI Bus Negotiations Type [A/S/N] = A?

- A** Asynchronous SCSI bus negotiation. (Default)
- S** Synchronous SCSI bus negotiation.
- N** None.

Primary SCSI Data Bus Width [W/N] = N?

- W** Wide SCSI (16-bit bus).
- N** Narrow SCSI (8-bit bus). (Default)

NVRAM Bootlist (GEV.fw-boot-path) Boot Enable [Y/N] = N?

- Y** Give boot priority to devices defined in the *fw-boot-path* global environment variable (GEV).
- N** Do not give boot priority to devices listed in the *fw-boot-path* GEV. (Default)

**Note** When enabled, the GEV (Global Environment Variable) boot takes priority over all other boots, including Autoboot and Network Boot.

NVRAM Bootlist (GEV.fw-boot-path) Boot at power-up only [Y/N] = N?

- Y** Give boot priority to devices defined in the *fw-boot-path* GEV at power-up reset only.
- N** Give power-up boot priority to devices listed in the *fw-boot-path* GEV at any reset. (Default)

NVRAM Bootlist (GEV.fw-boot-path) Boot Abort Delay = 5?

The time in seconds that a boot from the NVRAM boot list will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

Auto Boot Enable [Y/N] = N?

- Y** The Autoboot function is enabled.
- N** The Autoboot function is disabled. (Default)

Auto Boot at power-up only [Y/N] = N?

- Y** Autoboot is attempted at power-up reset only.
- N** Autoboot is attempted at any reset. (Default)

Auto Boot Scan Enable [Y/N] = Y?

- Y** If Autoboot is enabled, the Autoboot process attempts to boot from devices specified in the scan list (e.g., FDISK/CDROM/TAPE/HDISK). (Default)
- N** If Autoboot is enabled, the Autoboot process uses the Controller LUN and Device LUN to boot.

Auto Boot Scan Device Type List = FDISK/CDROM/TAPE/HDISK?

This is the listing of boot devices displayed if the Autoboot Scan option is enabled. If you modify the list, follow the format shown above (uppercase letters, using forward slash as separator).

Auto Boot Controller LUN = 00?

Refer to the *PPC Bug Firmware Package User's Manual* for a listing of disk/tape controller modules currently supported by PPCBug. (Default = \$00)

Auto Boot Device LUN = 00?

Refer to the *PPC Bug Firmware Package User's Manual* for a listing of disk/tape devices currently supported by PPCBug. (Default = \$00)

Auto Boot Partition Number = 00?

Which disk "partition" is to be booted, as specified in the PowerPC Reference Platform (PRP) specification. If set to zero, the firmware will search the partitions in order (1, 2, 3, 4) until it finds the first "bootable" partition. That is, then, the partition that will be booted. Other acceptable values are 1, 2, 3, or 4. In these four cases, the partition specified will be booted without searching.

Auto Boot Abort Delay = 7?

The time in seconds that the Autoboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 7 seconds)

Auto Boot Default String [NULL for an empty string] =?

You may specify a string (filename) which is passed on to the code being booted. The maximum length of this string is 16 characters. (Default = null string)

ROM Boot Enable [Y/N] = N?

- Y** The ROMboot function is enabled.
- N** The ROMboot function is disabled. (Default)

ROM Boot at power-up only [Y/N] = Y?

- Y** ROMboot is attempted at power-up only. (Default)
- N** ROMboot is attempted at any reset.

ROM Boot Abort Delay = 5?

The time in seconds that the ROMboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

ROM Boot Direct Starting Address = FFF00000?

The first location tested when PPCBug searches for a ROMboot module. (Default = \$FFF00000)

ROM Boot Direct Ending Address = FFFFFFFC?

The last location tested when PPCBug searches for a ROMboot module. (Default = \$FFFFFFFC)

Network Auto Boot Enable [Y/N] = N?

**Y** The Network Auto Boot (NETboot) function is enabled.

**N** The NETboot function is disabled. (Default)

Network Auto Boot at power-up only [Y/N] = N?

**Y** NETboot is attempted at power-up reset only.

**N** NETboot is attempted at any reset. (Default)

Network Auto Boot Controller LUN = 00?

Refer to the *PPCBug Firmware Package User's Manual* for a listing of network controller modules currently supported by PPCBug. (Default = \$00)

Network Auto Boot Device LUN = 00?

Refer to the *PPCBug Firmware Package User's Manual* for a listing of network controller modules currently supported by PPCBug. (Default = \$00)

Network Auto Boot Abort Delay = 5?

The time in seconds that the NETboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

Network Auto Boot Configuration Parameters Offset (NVRAM) = 00001000?

The address where the network interface configuration parameters are to be saved/retained in NVRAM; these parameters are the necessary parameters to perform an unattended network boot. A typical offset might be \$1000, but this value is application-specific. (Default = \$00001000)



If you use the **NIOT** debugger command, these parameters need to be saved somewhere in the offset range \$00001000 through \$000016F7. The **NIOT** parameters do not exceed 128 bytes in size. The setting of this ENV pointer determines their location. If you have used the same space for your own program information or commands, they will be overwritten and lost.

You can relocate the network interface configuration parameters in this space by using the **ENV** command to change the Network Auto Boot Configuration Parameters Offset from its default of \$00001000 to the value you need to be clear of your data within NVRAM.

Memory Size Enable [Y/N] = Y?

- Y** Memory will be sized for Self Test diagnostics. (Default)
- N** Memory will not be sized for Self Test diagnostics.

Memory Size Starting Address = 00000000?

The default Starting Address is \$00000000.

Memory Size Ending Address = 02000000?

The default Ending Address is the calculated size of local memory. If the memory start is changed from \$00000000, this value will also need to be adjusted.

DRAM Speed in NANO Seconds = 60?

The default setting for this parameter will vary depending on the speed of the DRAM memory parts installed on the board. The default is set to the slowest speed found on the available banks of DRAM memory.

ROM First Access Length (0 - 31) = 10?

This is the value programmed into the MPC105 “ROMFAL” field (Memory Control Configuration Register 8: bits 23-27) to indicate the number of clock cycles used in accessing the ROM. The lowest allowable ROMFAL setting is \$00; the highest allowable is \$1F. The value to enter depends on processor speed; refer to your *Processor/Memory Mezzanine Module User’s Manual* (PM603/UM, listed in [Related Documentation on page A-1](#)) for appropriate values. The default value varies according to the system’s bus clock speed.

**Note** ROM First Access Length is not applicable to the MTX. The configured value is ignored by PPCBug.

ROM Next Access Length (0 - 15) = 0?

The value programmed into the MPC105 “ROMNAL” field (Memory Control Configuration Register 8: bits 28-31) to represent wait states in access time for nibble (or burst) mode ROM accesses. The lowest allowable ROMNAL setting is \$0; the highest allowable is \$F. The value to enter depends on processor speed; refer to your *Processor/Memory Mezzanine Module User’s Manual* (PM603/UM, listed in [Related Documentation on page A-1](#)) for appropriate values. The default value varies according to the system’s bus clock speed.

**Note** ROM Next Access Length is not applicable to the MTX. The configured value is ignored by PPCBug.

DRAM Parity Enable [On-Detection/Always/Never - O/A/N] = 0?

- O DRAM parity is enabled upon detection. (Default)
- A DRAM parity is always enabled.
- N DRAM parity is never enabled

**Note** This parameter (above) also applies to enabling ECC for DRAM.

L2 Cache Parity Enable [On-Detection/Always/Never - O/A/N] = O?

- O L2 Cache parity is enabled upon detection. (Default)
- A L2 Cache parity is always enabled.
- N L2 Cache parity is never enabled

PCI Interrupts Route Control Registers (PIRQ0/1/2/3) = 0A0B0E0F?

Initializes the PIRQx (PCI Interrupts) route control registers in the IBC (PCI/ISA bus bridge controller). The **ENV** parameter is a 32-bit value that is divided by 4 to yield the values for route control registers PIRQ0/1/2/3. The default is determined by system type. For details on PCI/ISA interrupt assignments and for suggested values to enter for this parameter, refer to the 8259 *Interrupts* section of Chapter 4 in the *MTX Programmer's Reference Guide*.

Serial Startup Code Master Enable [Y/N]=N?

The Serial Startup Codes can be displayed at key points in the initialization of the hardware devices. Should the debugger fail to come up to a prompt, the last code displayed will indicate how far the initialization sequence had progressed before stalling. The codes are enabled by an **ENV** parameter.

Serial Startup Code LF Enable [Y/N]=N?

A line feed can be inserted after each code is displayed to prevent it from being overwritten by the next code. This is also enabled by an **ENV** parameter.

A list of LED/serial codes is included in the section on MPU, Hardware, and Firmware Initialization in Chapter 1 of the *PPC Bug Firmware Package User's Manual, Part 1*.



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## PPCbug Overview

The PPCbug firmware is the layer of software just above the hardware. The firmware provides the proper initialization for the devices on the MTX motherboard upon power-up or reset.

This chapter describes the basics of PPCbug and its architecture, describes the monitor (interactive command portion of the firmware) in detail, and gives information on actually using the PPCbug debugger and the special commands. A complete list of PPCbug commands appears at the end of the chapter.

The chapter [CNFG and ENV Commands on page 5-1](#) contains information about the CNFG and ENV commands, system calls, and other advanced user topics.

For full user information about PPCbug, refer to the *PPCbug Firmware Package User's Manual* and the *PPC1Bug Diagnostics Manual*, listed in Appendix A, [Related Documentation on page A-1](#).

## PPCbug Basics

The PowerPC debug firmware, PPCbug, is a powerful evaluation and debugging tool for systems built around the Motorola PowerPC microcomputers. Facilities are available for loading and executing user programs under complete operator control for system evaluation.

PPCbug provides a high degree of functionality, user friendliness, portability, and ease of maintenance.

It achieves good portability and comprehensibility because it was written entirely in the C programming language, except where necessary to use assembler functions.

PPCBug includes commands for:

- ❑ Display and modification of memory
- ❑ Breakpoint and tracing capabilities
- ❑ A powerful assembler and disassembler useful for patching programs
- ❑ A self-test at power-up feature which verifies the integrity of the system

PPCBug consists of three parts:

- ❑ A command-driven, user-interactive *software debugger*, described in the *PPCBug Firmware Package User's Manual*. It is hereafter referred to as “the debugger” or “PPCBug”.
- ❑ A command-driven *diagnostics package* for the MTX hardware, hereafter referred to as “the diagnostics.” The diagnostics package is described in the *PPC1Bug Diagnostics Manual*.
- ❑ A *user interface* or *debug/diagnostics monitor* that accepts commands from the system console terminal.

When using PPCBug, you operate out of either the *debugger directory* or the *diagnostic directory*.

- ❑ If you are in the debugger directory, the debugger prompt `PPC1-Bug>` is displayed and you have all of the debugger commands at your disposal.
- ❑ If you are in the diagnostic directory, the diagnostic prompt `PPC1-Diag>` is displayed and you have all of the diagnostic commands at your disposal as well as all of the debugger commands.

Use the **SD** command to switch back and forth between these directories.

Because PPCBug is command-driven, it performs its various operations in response to user commands entered at the keyboard. When you enter a command, PPCBug executes the command and the prompt reappears.

However, if you enter a command that causes execution of user target code (for example, **GO**), then control may or may not return to PPCBug, depending on the outcome of the user program.

## Memory Requirements

PPCBug requires a maximum of 768KB of read/write memory (DRAM). The debugger allocates this space from the top of memory. For example, a system containing 64MB (\$04000000) of read/write memory will place the PPCBug memory page at locations \$03F80000 to \$03FFFFFF.

## PPCBug Implementation

PPCBug is written largely in the C programming language which provides benefits of portability and maintainability. Where necessary, assembly language has been used in the form of separately compiled program modules containing only assembler code. No mixed-language modules are used.

Physically, PPCBug is contained in two socketed 32-pin PLCC Flash devices that together provide 1MB of storage. The executable code is checksummed at every power-on or reset firmware entry and the result, which includes a precalculated checksum contained in the Flash devices, is verified against the expected checksum.

## MPU, Hardware, and Firmware Initialization

The debugger performs the MPU, hardware, and firmware initialization process. This process occurs each time the MTX is reset or powered up. The steps below are a high-level outline; not all of the detailed steps are listed.

1. Sets MPU.MSR to known value.
2. Invalidates the MPU's data/instruction caches.
3. Clears all segment registers of the MPU.

4. Clears all block address translation registers of the MPU.
5. For the dual processor only, catch one CPU of a dual CPU and place it in a waiting loop.
6. Initializes the MPU-bus-to-PCI-bus bridge device.
7. Initializes the PCI-bus-to-ISA-bus bridge device.
8. Calculate the external bus clock speed of the MPU.
9. Delays for 750 milliseconds.
10. Determines the CPU board type.
11. Sizes the local read/write memory (i.e., DRAM).
12. Initializes the read/write memory controller.
13. Sets base address of memory to \$00000000
14. Retrieves the speed of read/write memory from NVRAM.
15. Initializes the read/write memory controller with the speed of read/write memory.
16. Retrieves the speed of read only memory (Flash) from NVRAM.
17. Initializes the read only memory controller with the speed of read only memory.
18. Enables the MPU's instruction cache.
19. Copies the MPU's exception vector table from \$FFF00000 to \$00000000.
20. Initializes the Super I/O resources' base addresses.
21. Verifies MPU type.
22. Enables the super-scalar feature of the MPU (boards with MPC604 type chips only).
23. Initializes the Keyboard Controller Super I/O.

24. Determines the debugger's console/host ports and initializes the appropriate devices (PC16550/GD54xx/Z85C230).
25. Displays the debugger's copyright message.
26. Displays any hardware initialization errors that may have occurred.
27. Checksums the debugger object and displays a warning message if the checksum failed to verify.
28. Displays the amount of local read/write memory found.
29. Verifies the configuration data that is resident in NVRAM and displays a warning message if the verification failed.
30. Calculates and displays the MPU clock speed, verifies that the MPU clock speed matches the configuration data, and displays a warning message if the verification fails.
31. Displays the BUS clock speed, verifies that the BUS clock speed matches the configuration data, and displays a warning message if the verification fails.
32. Displays any Keyboard Controller initialization error that occurs.
33. Probes PCI bus for supported network devices.
34. Probes PCI bus for supported mass storage devices.
35. Initializes the memory/IO addresses for the supported PCI bus devices.
36. Executes Self-Test, if so configured. (Default is no Self-Test.)
37. Extinguishes the board fail LED, if there are no self-test failures or initialization/configuration errors.
38. Executes the configured boot routine: either ROMboot, Autoboot, or Network Autoboot.
39. Executes the user interface (prompt the <PPC1-Bug> OR <PPC1-Diag> prompt).

## Using PPCBug

PPCbug is command-driven; it performs its various operations in response to commands that you enter at the keyboard. When the `PPC1-Bug` prompt appears on the screen, the debugger is ready to accept debugger commands. When the `PPC1-Diag` prompt appears on the screen, the debugger is ready to accept diagnostics commands. To switch from one mode to the other, enter **SD**.

What you key in is stored in an internal buffer. Execution begins only after you press the **Return** or **Enter** key. This allows you to correct entry errors, if necessary, with the control characters described in the *PPCbug Firmware Package User's Manual*, Chapter 1.

After the debugger executes the command, the prompt reappears. However, if the command causes execution of user target code (for example, **GO**), then control may or may not return to the debugger depending on what the user program does. For example, if a breakpoint has been specified, then control returns to the debugger when the breakpoint is encountered during execution of the user program. Alternately, the user program could return to the debugger by means of the System Call Handler routine **RETURN** (described in the *PPCbug Firmware Package User's Manual*, Chapter 5). For more about this, refer to the **GD**, **GO**, and **GT** command descriptions in the *PPCbug Firmware Package User's Manual*, Chapter 3.

A debugger command is made up of the following parts:

- ❑ The command name, either uppercase or lowercase (for example, **MD** or **md**).
- ❑ Any required arguments, as specified by command.
- ❑ At least one space before the first argument. Precede all other arguments with either a space or comma.
- ❑ One or more options. Precede an option or a string of options with a semicolon (;). If no option is entered, the command's default option conditions are used.

## Debugger Commands

The individual debugger commands are listed in the following table. The commands are described in detail in the *PPCBug Firmware Package User's Manual*, Chapter 2.

**Note** You can list all the available debugger commands by entering the Help (**HE**) command alone. You can view the syntax for a particular command by entering **HE** and the command mnemonic, as listed below.

**Table 6-1. Debugger Commands**

| Command | Description                          |
|---------|--------------------------------------|
| AS      | One Line Assembler                   |
| BC      | Block of Memory Compare              |
| BF      | Block of Memory Fill                 |
| BI      | Block of Memory Initialize           |
| BM      | Block of Memory Move                 |
| BR      | Breakpoint Insert                    |
| NOBR    | Breakpoint Delete                    |
| BS      | Block of Memory Search               |
| BV      | Block of Memory Verify               |
| CM      | Concurrent Mode                      |
| NOCM    | No Concurrent Mode                   |
| CNFG    | Configure Board Information Block    |
| CS      | Checksum                             |
| CSAR    | PCI Configuration Space READ Access  |
| CSAW    | PCI Configuration Space WRITE Access |
| DC      | Data Conversion                      |
| DMA     | Block of Memory Move                 |
| DS      | One Line Disassembler                |
| DU      | Dump S-Records                       |
| ECHO    | Echo String                          |

**Table 6-1. Debugger Commands (Continued)**

| <b>Command</b> | <b>Description</b>                         |
|----------------|--|
| ENV            | Set Environment                            |
| FORK           | Fork Idle MPU at Address                   |
| FORKWR         | Fork Idle MPU with Registers               |
| GD             | Go Direct (Ignore Breakpoints)             |
| GEVBOOT        | Global Environment Variable Boot           |
| GEVDEL         | Global Environment Variable Delete         |
| GEVDUMP        | Global Environment Variable(s) Dump        |
| GEVEDIT        | Global Environment Variable Edit           |
| GEVINIT        | Global Environment Variable Initialization |
| GEVSHOW        | Global Environment Variable(s) Display     |
| GN             | Go to Next Instruction                     |
| GO             | Go Execute User Program                    |
| GT             | Go to Temporary Breakpoint                 |
| HE             | Help                                       |
| IDLE           | Idle Master MPU                            |
| IOC            | I/O Control for Disk                       |
| IOI            | I/O Inquiry                                |
| IOP            | I/O Physical (Direct Disk Access)          |
| IOT            | I/O Teach for Configuring Disk Controller  |
| IRD            | Idle MPU Register Display                  |
| IRM            | Idle MPU Register Modify                   |
| IRS            | Idle MPU Register Set                      |
| LO             | Load S-Records from Host                   |
| MA             | Macro Define/Display                       |
| NOMA           | Macro Delete                               |
| MAE            | Macro Edit                                 |
| MAL            | Enable Macro Listing                       |
| NOMAL          | Disable Macro Listing                      |
| MAR            | Load Macros                                |

**Table 6-1. Debugger Commands (Continued)**

| <b>Command</b> | <b>Description</b>                  |
|----------------|-------------------------------------|
| MAW            | Save Macros                         |
| MD, MDS        | Memory Display                      |
| MENU           | System Menu                         |
| MM             | Memory Modify                       |
| MMD            | Memory Map Diagnostic               |
| MS             | Memory Set                          |
| MW             | Memory Write                        |
| NAB            | Automatic Network Boot              |
| NAP            | Nap MPU                             |
| NBH            | Network Boot Operating System, Halt |
| NBO            | Network Boot Operating System       |
| NIOC           | Network I/O Control                 |
| NIOP           | Network I/O Physical                |
| NIOT           | Network I/O Teach (Configuration)   |
| NPING          | Network Ping                        |
| OF             | Offset Registers Display/Modify     |
| PA             | Printer Attach                      |
| NOPA           | Printer Detach                      |
| PBOOT          | Bootstrap Operating System          |
| PF             | Port Format                         |
| NOPF           | Port Detach                         |
| PFLASH         | Program FLASH Memory                |
| PS             | Put RTC into Power Save Mode        |
| RB             | ROMboot Enable                      |
| NORB           | ROMboot Disable                     |
| RD             | Register Display                    |
| REMOTE         | Remote                              |
| RESET          | Cold/Warm Reset                     |
| RL             | Read Loop                           |

**Table 6-1. Debugger Commands (Continued)**

| <b>Command</b> | <b>Description</b>              |
|----------------|---------------------------------|
| RM             | Register Modify                 |
| RS             | Register Set                    |
| RUN            | MPU Execution/Status            |
| SD             | Switch Directories              |
| SET            | Set Time and Date               |
| SROM           | SROM Examine/Modify             |
| SYM            | Symbol Table Attach             |
| NOSYM          | Symbol Table Detach             |
| SYMS           | Symbol Table Display/Search     |
| T              | Trace                           |
| TA             | Terminal Attach                 |
| TIME           | Display Time and Date           |
| TM             | Transparent Mode                |
| TT             | Trace to Temporary Breakpoint   |
| VE             | Verify S-Records Against Memory |
| VER            | Revision/Version Display        |
| WL             | Write Loop                      |



Although a command to allow the erasing and reprogramming of Flash memory is available to you, keep in mind that reprogramming any portion of Flash memory will erase everything currently contained in Flash, including the PPCBug debugger.

Bank B of Flash contains the PPCBug debugger.

## Diagnostic Tests

The PPCBug hardware diagnostics are intended for testing and troubleshooting the MTX module.

---

In order to use the diagnostics, you must switch to the diagnostic directory. You may switch between directories by using the **SD** (Switch Directories) command. You may view a list of the commands in the directory that you are currently in by using the **HE** (Help) command.

If you are in the debugger directory, the debugger prompt `<PPC1-Bug>` displays, and all of the debugger commands are available. Diagnostics commands cannot be entered at the `<PPC1-Bug>` prompt.

If you are in the diagnostic directory, the diagnostic prompt `<PPC1-Diag>` displays, and all of the debugger and diagnostic commands are available.

Note that not all tests are valid for the MTX. Using the **HE** command, you can list the diagnostic routines available in each test group. Refer to the *PPC1Bug Diagnostics Manual* for complete descriptions of the diagnostic routines and instructions on how to invoke them.

**Table 6-2. Diagnostic Test Groups**

| <b>Test Group</b> | <b>Description</b>                              | <b>PowerPC Board</b>  |
|-------------------|---|-----------------------|
| CL1283            | Parallel Interface (CL1283) Tests               | MTX                   |
| DEC               | DEC21x40 Ethernet Controller Tests              | All                   |
| EIDE              | IDE/EIDE Device Tests                           | MTX, MCP750           |
| ISABRDGE          | PCI/ISA Bridge Tests                            | All                   |
| KBD8730X          | PC8730x Keyboard/Mouse Tests                    | All                   |
| L2CACHE           | Level 2 Cache Tests                             | All                   |
| NCR               | NCR 53C8xx SCSI2 I/O Processor Tests            | All                   |
| PAR8730X          | Parallel Interface (PC8730x) Tests              | All                   |
| UART              | Serial Input/Output Tests                       | All                   |
| PCIBUS            | PCI/PMC Generic Tests                           | All                   |
| RAM               | Local RAM Tests                                 | All                   |
| RTC               | MK48Txx Timekeeping Tests                       | All                   |
| SCC               | Serial Communication Controller (Z85C230) Tests | All except MVME230x   |
| VGA54XX           | Video Diagnostics Tests*                        | MVME360x,<br>MVME460x |
| VME2              | VMEchip2 VME Interface ASIC Tests               | None                  |
| VME3              | VMEchip3 VME Interface ASIC Tests               | None                  |
| Z8536             | Z8536 Counter/Timer Tests                       | All except MVME230x   |

**Notes** You may enter command names in either uppercase or lowercase.

Some diagnostics depend on restart defaults that are set up only in a particular restart mode. Refer to the documentation on a particular diagnostic for the correct mode.

Test Sets marked with an asterisk (\*) are not available on the MTX.

## Motorola Computer Group Documents

The Motorola publications listed below are referenced in this manual. You can obtain paper or electronic copies of Motorola Computer Group publications by:

- ❑ Contacting your local Motorola sales office
- ❑ Visiting Motorola Computer Group's World Wide Web literature site, <http://www.motorola.com/computer/literature>

**Table A-1. Motorola Computer Group Documents**

| <b>Document Title</b>                                   | <b>Motorola Publication Number</b> |
|---|------------------------------------|
| MTX Series Motherboard Installation and Use*            | MTXA/IH                            |
| MTX Series Motherboard Programmer's Reference Guide*    | MTXA/PG                            |
| PPC Bug Firmware Package User's Manual (Parts 1 and 2)* | PPCBUGA1/UM<br>PPCBUGA2/UM         |
| PPC1Bug Diagnostics Manual*                             | PPCDIAA/UM                         |

To obtain the most up-to-date product information in PDF or HTML format, visit <http://www.motorola.com/computer/literature>.

## Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice

**Table A-2. Manufacturers' Documents**

| <b>Document Title and Source</b>   | <b>Publication Number</b> |
|--|---------------------------|
| PowerPC 603 <sup>®</sup> RISC Microprocessor Technical Summary<br>Literature Distribution Center for Motorola Semiconductor Products<br>Telephone: (800) 441-2447<br>FAX: (602) 994-6430 or (303) 675-2150<br>E-mail: ldcformotorola@hibbertco.com           | MPC603/D                  |
| PowerPC 603 <sup>®</sup> RISC Microprocessor User's Manual<br>Literature Distribution Center for Motorola Semiconductor Products<br>Telephone: (800) 441-2447<br>FAX: (602) 994-6430 or (303) 675-2150<br>E-mail: ldcformotorola@hibbertco.com               | MPC603UM/AD               |
| PowerPC 604 <sup>®</sup> RISC Microprocessor User's Manual<br>Literature Distribution Center for Motorola Semiconductor Products<br>Telephone: (800) 441-2447<br>FAX: (602) 994-6430 or (303) 675-2150<br>E-mail: ldcformotorola@hibbertco.com               | MPC604UM/AD               |
| PowerPC <sup>®</sup> Microprocessor Family: The Programming Environments<br>Literature Distribution Center for Motorola Semiconductor Products<br>Telephone: (800) 441-2447<br>FAX: (602) 994-6430 or (303) 675-2150<br>E-mail: ldcformotorola@hibbertco.com | MPCFPE/AD                 |
| MPC2605GA Integrated Secondary Cache for PowerPC<br>Literature Distribution Center for Motorola Semiconductor Products<br>Telephone: (800) 441-2447<br>FAX: (602) 994-6430 or (303) 675-2150<br>E-mail: ldcformotorola@hibbertco.com                         | MPC2605/D                 |
| MPC2605GA for PowerPC Fact Sheet   | MPC2605FACT/D             |

**Table A-2. Manufacturers' Documents (Continued)**

| Document Title and Source  | Publication Number |
|--|--------------------|
| DECchip 21140 PCI Fast Ethernet LAN Controller<br>Hardware Reference Manual<br>Digital Equipment Corporation<br>Maynard, Massachusetts<br>DECchip Information Line<br>Telephone (United States and Canada): 1-800-332-2717<br>TTY (United States only): 1-800-332-2515<br>Telephone (outside North America): +1-508-568-6868   | EC-QC0CA-TE        |
| PC87308VUL ( Super I/O <sup>TM</sup> Enhanced Sidewinder Lite) Floppy Disk<br>Controller,, Keyboard Controller, Real-Time Clock, Dual UARTs,<br>IEEE 1284 Parallel Port, and IDE Interface<br>National Semiconductor Corporation<br>Customer Support Center (or nearest Sales Office)<br>2900 Semiconductor Drive<br>P.O. Box 58090<br>Santa Clara, California 95052-8090<br>Telephone: 1-800-272-9959 | PC87308VUL         |
| MK48T59 CMOS 8K x 8 TIMEKEEPER <sup>TM</sup> SRAM Data Sheet<br>SGS-Thomson Microelectronics Group<br>Marketing Headquarters (or nearest Sales Office)<br>1000 East Bell Road<br>Phoenix, Arizona 85022<br>Telephone: (602) 867-6100   | M48T59             |

**Table A-2. Manufacturers' Documents (Continued)**

| <b>Document Title and Source</b>   | <b>Publication Number</b> |
|--|---------------------------|
| SYM 53CXX (was NCR 53C8XX) Family PCI-SCSI I/O Processors Programming Guide<br>Symbios Logic Inc.<br>1731 Technology Drive, Suite 600<br>San Jose, California 95110<br>Telephone: (408) 441-1080<br>Hotline: 1-800-334-5454  | J10931I                   |
| SCC (Serial Communications Controller) User's Manual (for Z85230 and other Zilog parts)<br>Zilog, Inc.<br>210 East Hacienda Ave., mail stop C1-0<br>Campbell, California 95008-6600<br>Telephone: (408) 370-8016<br>FAX: (408) 370-8056  | DC-8293-02                |
| Z8536 CIO Counter/Timer and Parallel I/O Unit Product Specification and User's Manual (in Z8000 <sup>®</sup> Family of Products Data Book)<br>Zilog, Inc.<br>210 East Hacienda Ave., mail stop C1-0<br>Campbell, California 95008-6600<br>Telephone: (408) 370-8016<br>FAX: (408) 370-8056 | DC-8319-00                |
| W83C554 Enhanced System I/O Controller with PCI Arbiter (PIB)<br>Winbond Electronics Corporation<br>Winbond Systems Laboratory<br>2730 Orchard Parkway<br>San Jose, CA 95134<br>Telephone: 1-408-943-6666<br>FAX: 1-408-943-6668   | W83C554                   |

## Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

**Table A-3. Related Specifications**

| Document Title and Source   | Publication Number |
|---|--------------------|
| ANSI Small Computer System Interface-2 (SCSI-2), Draft Document<br>Global Engineering Documents<br>15 Inverness Way East<br>Englewood, CO 80112-5704<br>Telephone: 1-800-854-7179<br>Telephone: (303) 792-2181                            | X3.131.1990        |
| IEEE - Common Mezzanine Card Specification (CMC)<br>Institute of Electrical and Electronics Engineers, Inc.<br>Publication and Sales Department<br>345 East 47th Street<br>New York, New York 10017-21633<br>Telephone: 1-800-678-4333    | P1386 Draft 2.0    |
| IEEE - PCI Mezzanine Card Specification (PMC)<br>Institute of Electrical and Electronics Engineers, Inc.<br>Publication and Sales Department<br>345 East 47th Street<br>New York, New York 10017-21633<br>Telephone: 1-800-678-4333       | P1386.1 Draft 2.0  |
| Bidirectional Parallel Port Interface Specification<br>Institute of Electrical and Electronics Engineers, Inc.<br>Publication and Sales Department<br>345 East 47th Street<br>New York, New York 10017-21633<br>Telephone: 1-800-678-4333 | IEEE Standard 1284 |

**Table A-3. Related Specifications (Continued)**

| <b>Document Title and Source</b>   | <b>Publication Number</b>   |
|--|-----------------------------|
| Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.1<br>PCI Special Interest Group<br>2575 NE Kathryn St #17<br>Hillsboro, OR 97124<br>Telephone: (800) 433-5177 (inside the U.S.)<br>or (503) 693-6232 (outside the U.S.)<br>FAX: (503) 693-8344   | PCI Local Bus Specification |
| PowerPC Reference Platform (PRP) Specification, Third Edition, Version 1.0, Volumes I and II<br>International Business Machines Corporation<br>Power Personal Systems Architecture<br>11400 Burnet Rd.<br>Austin, TX 78758-3493<br>Document/Specification Ordering<br>Telephone: 1-800-PowerPC<br>Telephone: 1-800-769-3772<br>Telephone: 708-296-9332 | MPR-PPC-RPU-02              |
| IEEE Standard for Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications<br>Institute of Electrical and Electronics Engineers, Inc.<br>Publication and Sales Department<br>345 East 47th Street<br>New York, New York 10017-21633<br>Telephone: 1-800-678-4333          | IEEE 802.3                  |

**Table A-3. Related Specifications (Continued)**

| Document Title and Source   | Publication Number         |
|---|----------------------------|
| Information Technology - Local and Metropolitan Networks - Part 3:<br>Carrier Sense Multiple Access with Collision Detection (CSMA/CD)<br>Access Method and Physical Layer Specifications<br>Global Engineering Documents<br>15 Inverness Way East<br>Englewood, CO 80112-5704<br>Telephone: 1-800-854-7179<br>Telephone: (303) 792-2181<br><i>(This document can also be obtained through the national standards body<br/>           of member countries.)</i> | ISO/IEC 8802-3             |
| Interface Between Data Terminal Equipment and Data Circuit-<br>Terminating Equipment Employing Serial Binary Data Interchange (EIA-<br>232-D)<br>Electronic Industries Association<br>Engineering Department<br>2001 Eye Street, N.W.<br>Washington, D.C. 20006   | ANSI/EIA-232-D<br>Standard |

## URLs

The following URLs (uniform resource locators) may provide helpful sources of additional information about this product, related services, and development tools. Please note that, while these URLs have been verified, they are subject to change without notice.

- ❑ Motorola Computer Group, <http://www.motorola.com/computer>
- ❑ Motorola Computer Group OEM Services, <http://www.motorola.com/computer/support>



## Specifications

[Table B-1](#) lists the Power Requirements for the MTX motherboard. Mechanical specifications conform to those of the current ATX form factor specification, revision 1.1: 12.0 in width x 9.6 in length x 1.25 in height (excluding PCI card). Subsequent sections detail cooling requirements, I/O Panel Dimensions, and EMC compliance.

Specifications for related components, peripherals and networks can be ordered from the sources listed in [Table A-3 on page A-5](#).

**Table B-1. MTX Power Requirements**

| Configuration         | Specifications All With +5V Power |
|-----------------------|-----------------------------------|
| 200MHz 603e           | 5.5A typical<br>7A maximum        |
| 200MHz PIDv-604e      | 6A typical<br>8A maximum          |
| Dual 200MHz PIDv-604e | 9A typical<br>12A maximum         |
| 300MHz 604r           | 6A typical<br>7.5A maximum        |
| Dual 300MHz 604r      | 7A typical<br>9A maximum          |

## Cooling Requirements

The Motorola MTX family of Single Board Computers is specified, designed, and tested to operate reliably with an incoming air temperature range from 0° to +55° C (0° to 131° F). Minimum airflow requirements

(across the heatsink) are 25 LFM for a single processor motherboard and 125 LFM for a dual processor motherboard. Temperature qualification was performed in a standard Motorola ATX chassis.

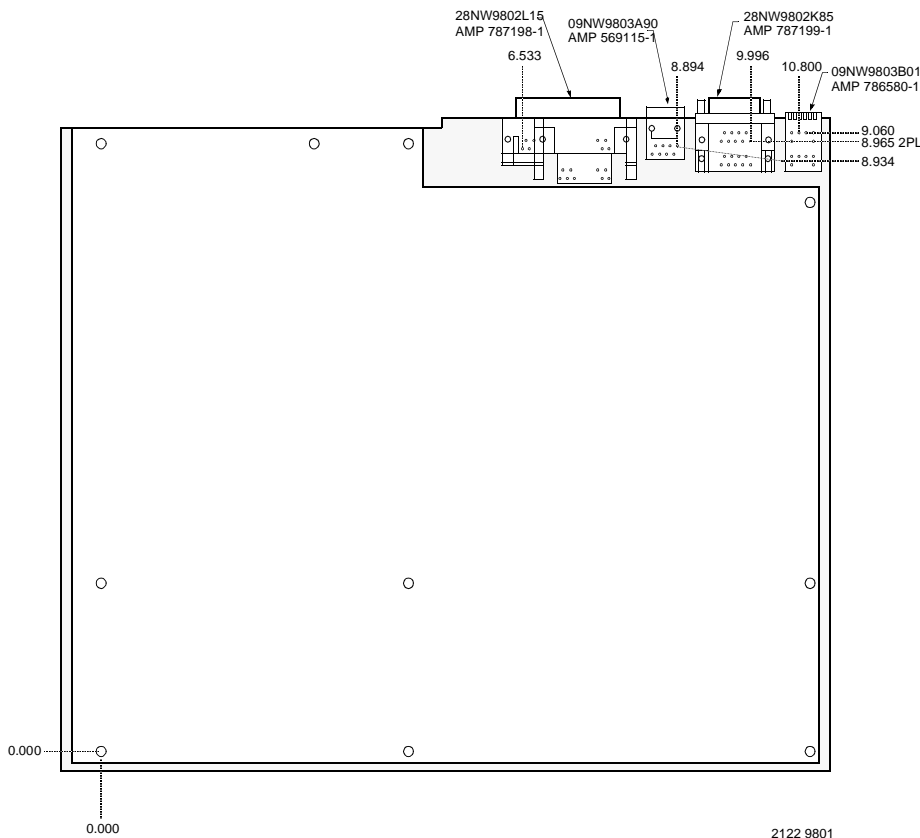
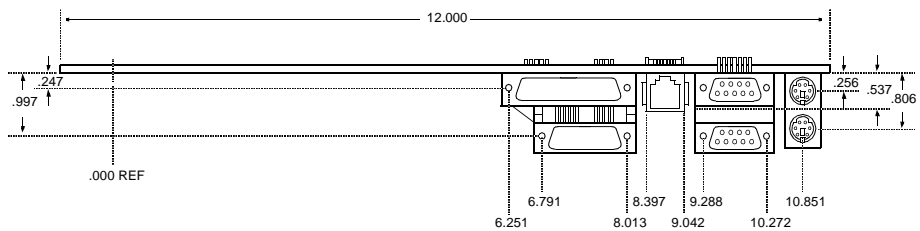
While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 10 CFM and 125 LFM (for dual processor), or 10 CFM and 25 LFM (for single processor) flowing across the heatsink. Less airflow is required to cool the motherboard in environments having lower maximum ambients. Under more favorable thermal conditions, it may be possible to operate the motherboard reliably at higher than 55° C with increased airflow. It is important to note that there are several factors, in addition to the rated CFM and/or LFM of the air mover, which determine the actual volume and speed of air flowing over a module.

## **Other Environmental Requirements**

The system meets all other standard environmental specifications including operating altitude up to 5,000 meters, humidity (NC) operating range of 10% to 80%, and a vibration tolerance of 2 Gs RMS, 20-2000 Hz Random.

## **I/O Panel Dimensions**

The following figure details the current I/O panel dimensions for this version of the MTX motherboard.



**Figure B-1. I/O Panel Dimensions**

## **EMC Compliance**

The MTX motherboard was tested in an EMC-compliant chassis and meets the requirements for EN55022 Class B equipment. Compliance was achieved under the following conditions:

- ❑ Shielded cables on all external I/O ports.
- ❑ Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.
- ❑ Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.
- ❑ Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented. Failure to do so could compromise the EMC compliance of the equipment containing the module.

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