MTX604-070™ MTX PCI Series Motherboard

Installation and Use

MTXPCIA/IH2

November 2000

Printed in the United States of America.

Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

Keep Away From Live Circuits Inside the Equipment.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

Use Caution When Exposing or Handling a CRT.

Breakage of a Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, do not handle the CRT and avoid rough handling or jarring of the equipment. Handling of a CRT should be done only by qualified service personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that all safety features are maintained.

Observe Warnings in Manual.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

Warning

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

Flammability

All Motorola PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

EMI Caution

Caution

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.

Lithium Battery Caution

This product contains a lithium battery to power the clock and calendar circuitry.

Caution

Danger of explosion if battery is replaced incorrectly. Replace battery only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Attention

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.

Vorsicht

Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch denselben oder einen vom Hersteller empfohlenen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

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Motorola Computer Group products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

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>
> EN50082-1:1997 “Electromagnetic Compatibility—Generic Immunity Standard, Part 1. Residential, Commercial and Light Industry”

System products also fulfill EN60950 (product safety) which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC/safety performance.

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About This Manual

This manual provides general information, hardware preparation, and installation instructions, a description of PPCBug firmware, and a functional description of the MTX604-070 family of Motherboards.

Summary of Changes

The following table show changes to this manual since its last publication.

Date	Changes	Replaces
October 2000	W83C554	W83C553
October 2000	603e	603r

Overview of Contents

This section gives you a brief description of each chapter and appendix in this manual.

Chapter 1, *Hardware Preparation and Installation*, describes hardware preparation and installation for the MTX604-070 motherboard.

Chapter 2, *Operating Instructions*, supplies information for use of the MTX604-070 motherboard in a system configuration.

Chapter 3, *Functional Description*, describes the MTX604-070 motherboard computer on a block diagram level.

Chapter 4, *Connector Pin Assignments*, summarizes the pin assignments for the connectors, headers, and sockets on the MTX board.

Chapter 5, *PPCBug*, describes the basics of PPCBug and its architecture, describes the monitor (interactive command portion of the firmware) in detail, and gives information on actually using the PPCBug debugger and the special commands.

Chapter 6, *CNFG and ENV Commands*, contains information about the **CNFG** and **ENV** commands. These two commands are used to change Bug Board Information and command parameters interactively.

Appendix A, *Specifications*, lists the power requirements for the MTX604-070 motherboard and subsequent sections detail cooling requirements and I/O Panel Dimensions.

Appendix B, *Related Documentation*, lists all documentation related to the MTX604-070.

Comments and Suggestions

Motorola welcomes and appreciates your comments on its documentation. We want to know what you think about our manuals and how we can make them better. Mail comments to:

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In all your correspondence, please list your name, position, and company. Be sure to include the title and part number of the manual and tell how you used it. Then tell us your feelings about its strengths and weaknesses and any recommendations for improvements.

Conventions Used in This Manual

The following typographical conventions are used in this document:

bold

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

italic

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

<**Enter**>, <**Return**> or <**CR**>

<**CR**> represents the carriage return or Enter key.

CTRL

represents the Control key. Execute control characters by pressing the Ctrl key and the letter simultaneously, for example, **Ctrl-d**.

Hardware Preparation and Installation

1

Introduction

The MTX604-070 is a motherboard equipped with PowerPC™ Series microprocessors. It consists of the MPC603e/PID9v-604e, the Raven PCI Bridge and Interrupt Controller, the ECC Memory Controller Falcon3 chipset, 9MB of Boot FLASH, ECC DRAM controller, and a large set of I/O peripherals. The MTX604-070 will support single or dual processors. In the dual processor configuration, the internal operating frequencies of the processors are independently configurable, allowing non-SMP board configurations. For example, a dual configuration with a 200 MHz 603ev and a 333 MHz 604e processor dual configuration is feasible, but would require custom firmware, test software, as well as other additional items. SMP operation is only supported in dual processor boards with 604e processors. A 256KB or 512KB L2 cache (level 2 secondary cache memory) is available as an option on all versions.

The complete MTX604-070 consists of the motherboard plus:

- ❏ Up to four (minimum two) DIMM memory modules
- ❏ Optional PCI adapter cards

The block diagram in Figure 1-1 illustrates the architecture of the MTX604-070.

The following equipment is required to complete an MTX604-070 system:

- ❏ ATX chassis with power supply
- ❏ System console terminal
- ❏ Operating system (and/or application software)
- ❏ Disk drives (and/or other I/O) and controllers

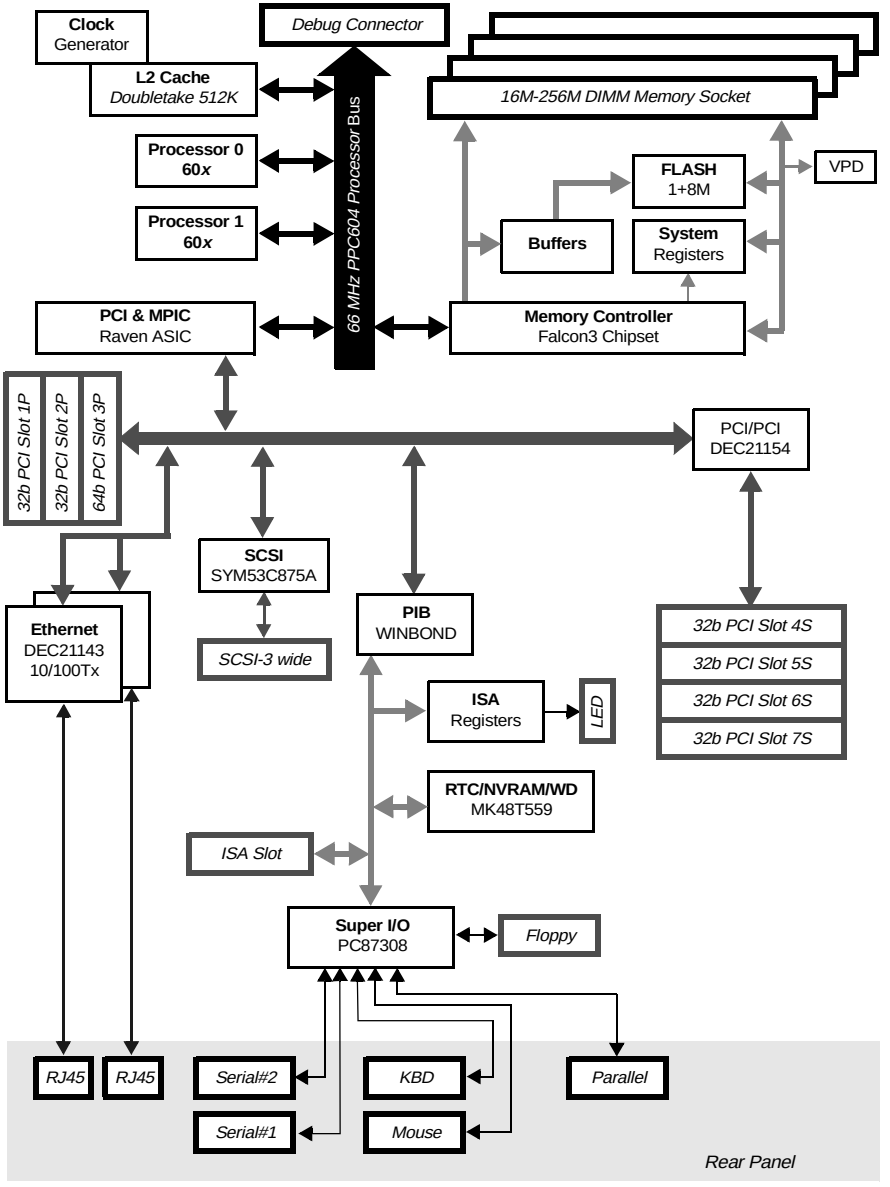


Figure 1-1. MTX604-070 Block Diagram

Overview of Startup Procedure

The following table lists the things you will need to do before you can use this board and tells where to find the information you need to perform each step. Be sure to read this entire chapter, including all Caution and Warning notes, before you begin.

Table 1-1. Startup Overview

What you need to do...	Refer to Section Heading Titled...
Unpack the hardware.	*Unpacking Instructions* on page 1-3
Configure the hardware by setting jumpers on the boards	*MTX604-070 Motherboard Preparation* on page 1-4
Ensure memory DIMMs are properly installed on the motherboard.	*DIMM Memory Installation* on page 1-12
Install the MTX604-070 Motherboard in the chassis.	*MTX604-070 Motherboard Installation* on page 1-16
Program the board as needed for your applications.	*MTX PCI Series Motherboard Programmer's Reference Guide*, listed in Appendix B, *Related Documentation*.

Unpacking Instructions

Note If the shipping carton is damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.

Unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of equipment.

Caution Avoid touching areas of integrated circuitry; static discharge can damage circuits.

Hardware Configuration

To produce the desired configuration and ensure proper operation of the MTX604-070, you may need to carry out certain hardware modifications before installing the motherboard.

The MTX604-070 provides software control over most options: by setting bits in control registers after installing the module in a system, you can modify its configuration. The MTX604-070 control registers are described in the *MTX PCI Series Motherboard Programmer's Reference Guide*, listed in Appendix B, *Related Documentation*.

Some options, however, are not software-programmable. Such options are controlled through manual installation or removal of header jumpers.

MTX604-070 Motherboard Preparation

Figure 1-2 illustrates the placement of the switches, jumper headers, connectors, and LED indicators on the MTX604-070. Table 1-2 lists the jumper and connector callouts and their associated function. Manually configured items on the base board include:

- Cache mode control (J5)
- Flash bank selection (J24)
- Power Control for ATX power supply (J19 and J20)
- Hardware/firmware disable of SCSI (J21)

The MTX604-070 is factory tested and shipped with the configurations described in the following sections. The MTX604-070's required and factory-installed debug monitor, PPCBug, operates with those factory settings.

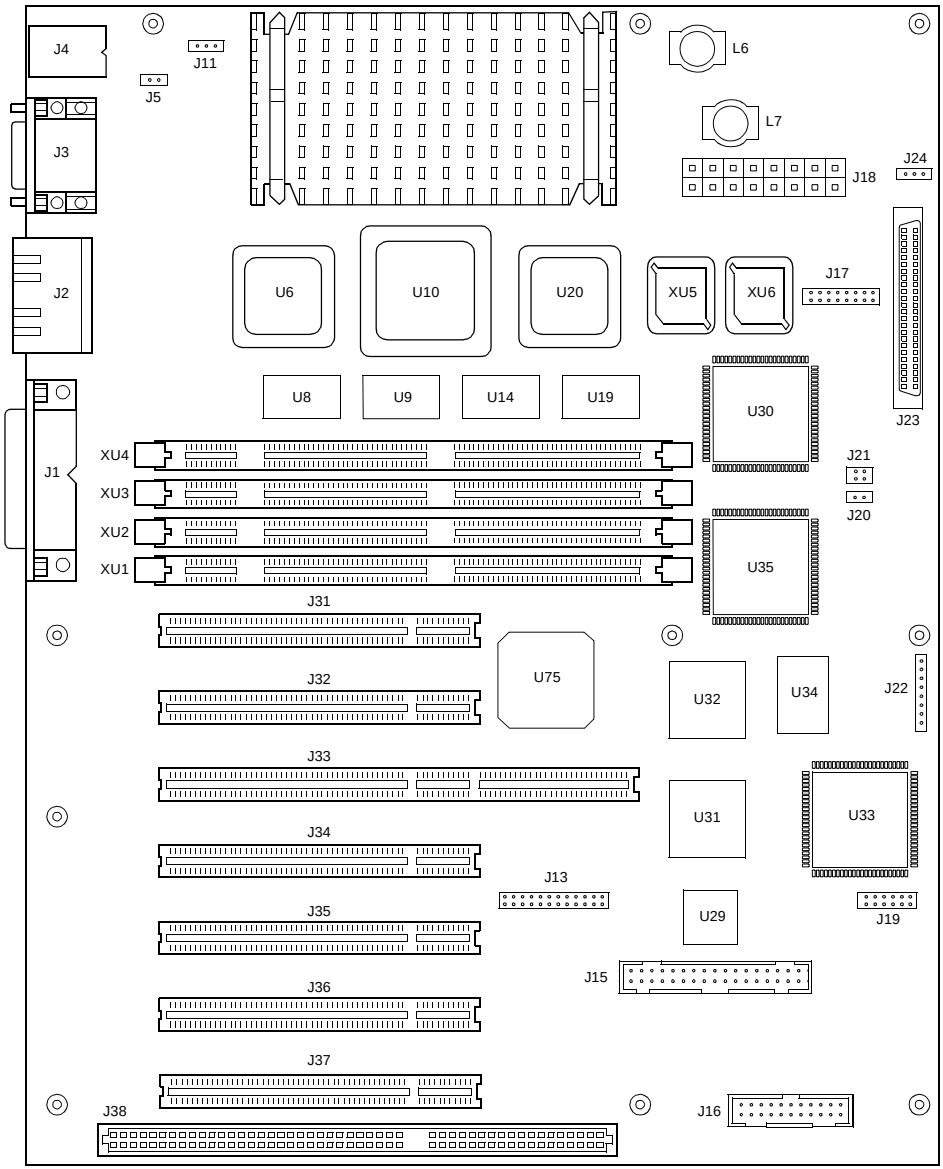


Figure 1-2. MTX604-070 Switches, Headers, Connectors, Fuses, LEDs

Connector/Jumper Descriptions

The following table describes the MTX604-070 jumper functions and any specific mapping designations:

Table 1-2. MTX604-070 Connector/Jumper Descriptions

Reference Designator	Function	Comment
J31	32-bit PCI slot 1P	IDSEL = AD16
J32	32-bit PCI slot 2P	IDSEL = AD17
J33	64-bit PCI slot 3P	IDSEL = AD18
J34	64-bit PCI slot 4S	Secondary bus IDSEL = SAD18
J35	32-bit PCI slot 5S	Secondary bus IDSEL = SAD19
J36	32-bit PCI slot 6S	Secondary bus IDSEL = SAD20
J37	32-bit PCI slot 7S	Secondary bus IDSEL = SAD21 (shared)
J38	ISA slot	(shared slot with J37)
J1	Host Parallel	
J2-A	10/100 Base-T	LAN1
J2-B	10/100 Base-T	LAN2
J3 Upper	COM2	Async DTE
J3 Lower	COM1	Async DTE
J4 Upper	Mouse	
J4 Lower	Keyboard	
J5	L2 write-thru control	default = open (write through always enabled)
J12	Debug	Processor bus access for prototyping
J13	LEDs and Switches	Status LEDs (except power status LED), and **RESET** and **ABORT** switch inputs
J15	Floppy	
J16	16-bit latched data	AIX LED code
J17	RISCWatch	Processor #0
J18	Power	
J19	Speaker & power status	

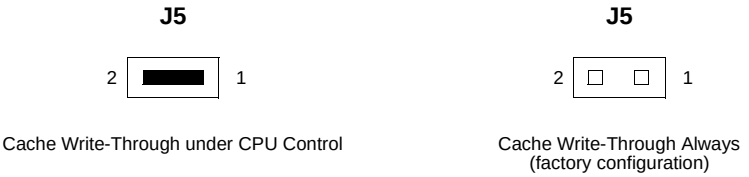
Table 1-2. MTX604-070 Connector/Jumper Descriptions (Continued)

Reference Designator	Function	Comment
J20	ATX LEVEL Power Control	short pins to turn ATX power supply on
J21	SCSI options	Jumper 1-2 to disable on-board SCSI bus terminator Jumper 3-4 to disable Ultra speed Default is no jumpers installed
J22	ISP GAL prog. port	For factory use only
J23	SCSI	
J24	Flash Bank Select	Jumper 2-3 to enable Bank B boot Jumper 1-2 (or no jumper at all) to enable Bank A boot
XU5	Flash Bank B	Upper Byte
XU6	Flash Bank B	Lower Byte
XU1	DIMM Bank B	Upper 72-bits
XU2	DIMM Bank B	Lower 72-bits
XU3	DIMM Bank A	Upper 72-bits
XU4	DIMM Bank A	Lower 72-bits

Cache Mode Control

The optional L2 cache functionality is provided via the Doubletake chipset. If populated, the Doubletake 256K or 512K look-aside cache option is implemented with one or two MCP2605ZP (Doubletake)

devices. Refer to the MPC2605ZP data sheets and the *MTX PCI Series Motherboard Programmer's Reference Guide,* listed in *Appendix B, Related Documentation*, for additional information.



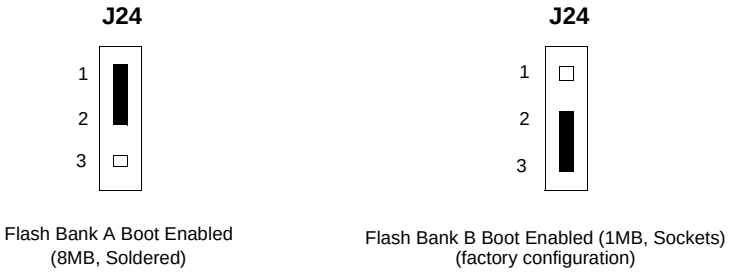
Flash Bank Selection

The MTX604-070 motherboard contains two banks of FLASH memory. Bank A consists of four soldered-in 16-bit wide, 2 megabytes or 1 megaword (16-bit words) deep 3.3V FLASH SMT devices and appears as FLASH Bank A (64 bits wide) to the Falcon chipset. Individual 64K byte blocks can be write protected by software. The entire Bank A memory can be write protected by removing four resistor jumpers (R138, R167, R184, R225) that supply write power to the devices. Additionally, software can write-enable/disable the entire Flash bank through control of the **rom_x_wc** bit of the Falcon's ROM Base/Size registers.

Bank B consists of two sockets for 8-bit wide +5.0 volt FLASH SMT devices and appears as FLASH Bank B (16 bits wide) to the Falcon chipset. The Bank B sockets support a maximum 512 K-byte FLASH in each socket.

Bank B contains the onboard debugger, PPCBug.

To enable a boot from Flash Bank A, place a jumper across pins 1 and 2 of header J24. To enable a boot from Flash Bank B, place a jumper across pins 2 and 3 of header J24.



Flash Bank A Boot Enabled (8MB, Soldered)

Flash Bank B Boot Enabled (1MB, Sockets) (factory configuration)

Power Control for ATX Power Supply

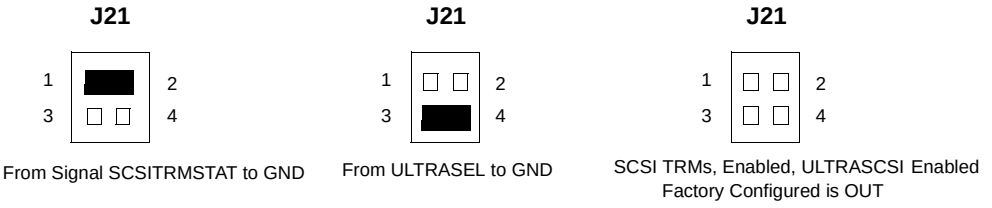
ATX power supplies have a logic level (+5.0V/GND) power control input (**PS_ON_L**). An ATX supply power is **ON** when this input is connected to logic ground. The MTX604-070 motherboard features both level and edge-sensitive control of this ATX power supply feature. A two pin header (J20) is provided for level control (short the pins to turn the supply on). A separate ten-pin header (J19) controls the soft-power switch input to the Super I/O device. When there is a rising edge on the switch input, the Advanced Power Control section of the Super I/O device will toggle the state of the **PS_ON_L** input of the ATX power connector. The ATX power supply must provide 5Vsb (+5 standby power) for the soft-power feature to be enabled.

Power On

Connect Momentary Switch here to Control Power

Hardware/Firmware Disable of SCSI

Jumper J21 is used to disable on-board SCSI terminators and to disable the firmware negotiation of UltraSCSI. To disable on-board SCSI terminators, connect a jumper from J21-2 to J21-1. To disable firmware negotiation of UltraSCSI, connect a jumper from J21-3 to J21-4.



Front Panel Functions

The MTX604-070 has two planar headers (J13 and J19) for front panel functions including abort and reset switches, speaker interface, and an LED drive. Refer to Chapter 4, *Connector Pin Assignments*, for specific pin assignments. The +5.0V power is supplied via a 0.75 amp polyfuse. The headers provide nine discrete LED functions. These functions are described below:

- The **STATLED#** signal is active when either processor **CHECKSTOP** signal is active.
- The **FAILLED#** signal is active when the firmware controlled **BRDFAIL** signal is active.
- The **RUNLED#** signal is active when the **DBB#** signal of the processor bus is active.
- The **LAN1LED#** signal is active when the Ethernet 1 Link signal is active.
- The **LAN2LED#** signal is active when the Ethernet 2 Link signal is active.
- The **PCI_IRDY_LED#** signal is active when the **IRDY#** signal of the Primary PCI bus is active.
- The **SPCI_IRDY_LED#** signal is active when the **IRDY#** signal of the Secondary PCI bus is active.

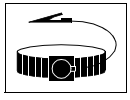
- The **PWRGOOD#** signal is active when the SMI interrupt is inactive. The SMI interrupt is used to signal impending power failure on some systems.
- The **SCSI_BUSY_LED#** signal is active when the software controlled **SCSI_BUSY#** signal is active.

In addition, the MTX604-070 has two planar LEDs, the yellow FAIL LED is lit when the **BRDFAIL** signal line is active, and the green CPU LED is lit when the **DBB#** signal of processor bus is active. There is also a separate 20 pin header that has ISA bus 16-bit latched data. This function can be used to display AIX debug codes on a separate seven segment LED drive board. The speaker control, reset switch, abort switch, and soft power switch input are described in Chapter 3, *Functional Description*, of this document.

Hardware Installation

The following sections discuss the placement of adapter cards on the MTX604-070 motherboard, the installation of the complete MTX604-070 assembly into an ATX chassis, and the system considerations relevant to the installation. Before installing the MTX604-070, ensure that all header jumpers are configured as desired.

ESD Precautions



Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to ESD. After removing the component from the system or its protective wrapper, place the component flat on a grounded, static-free surface (and in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an unpainted metal part of the system chassis.

DIMM Memory Installation

DIMM modules install into sockets XU1 through XU4 on the MTX604-070 motherboard. To upgrade or install a DIMM module, refer to Figure 1-3 and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the motherboard.

Caution

Removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

3. Install the DIMM into XU1 through XU4 as needed, with pin 1 of the DIMM located at the rear of the motherboard (toward the external I/O connectors). Note that DIMMs must be installed in pairs, XU3 with XU4, or XU1 with XU2, and that at least one pair of DIMMs is required for MTX604-070 operation. Load Bank A/C (XU3, XU4) first.

Note 168 pin, 3.3V, unbuffered, single or dual bank, serial presence detect, EDO or Fast Page DRAM DIMMs are required. Up to 256 MB may be installed per bank. Table 1-3 includes a list of suppliers and equivalent DIMM sizes that have been qualified for MTX604-070 boards.

Table 1-3. MTX Tested DIMM Memory Modules

Supplier	Size
Advantage Memory Corp	256MB
Crucial Technology	64MB
Crucial Technology	128MB
Hitachi	128MB
Micron (Crucial Technology)	16MB
Micron (Crucial Technology)	32MB
Micron (Crucial Technology)	64MB
Micron (Crucial Technology)	128MB
Samsung	16MB
Samsung	32MB
Simple	16MB
Simple	32MB
Simple	64MB
Viking	256MB
Motorola Computer Group	64MB

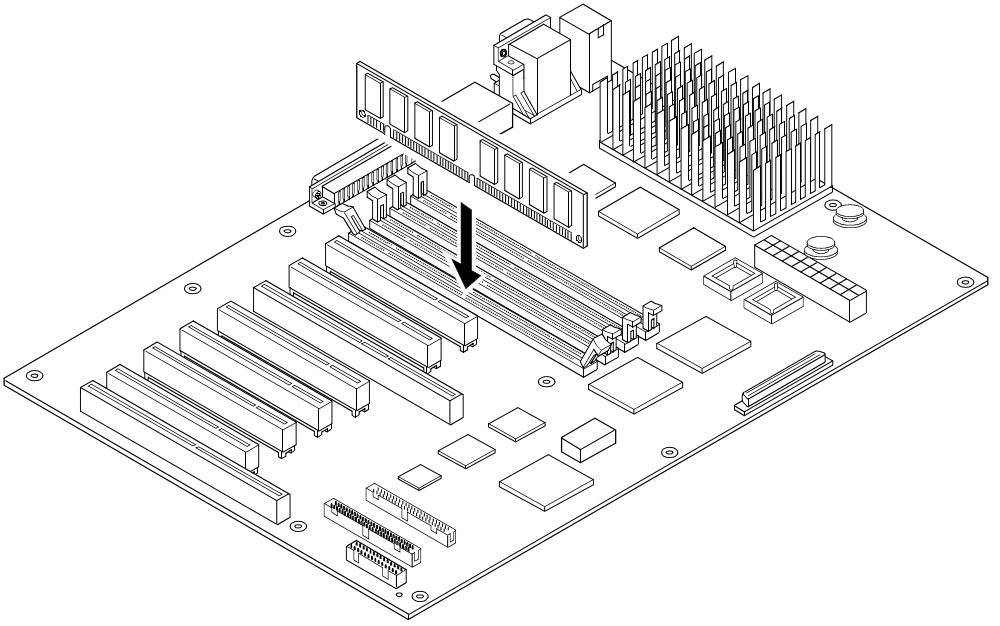


Figure 1-3. DIMM Placement on MTX604-070

PCI Adapter Installation (Optional)

PCI adapter boards mount to connectors J31 through J37 on the MTX604-070 motherboard. To install PCI adapters, refer to Figure 1-4 and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the motherboard.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Remove the PCI filler from the chassis.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

4. Install the PCI adapter card into slots J31 through J37.

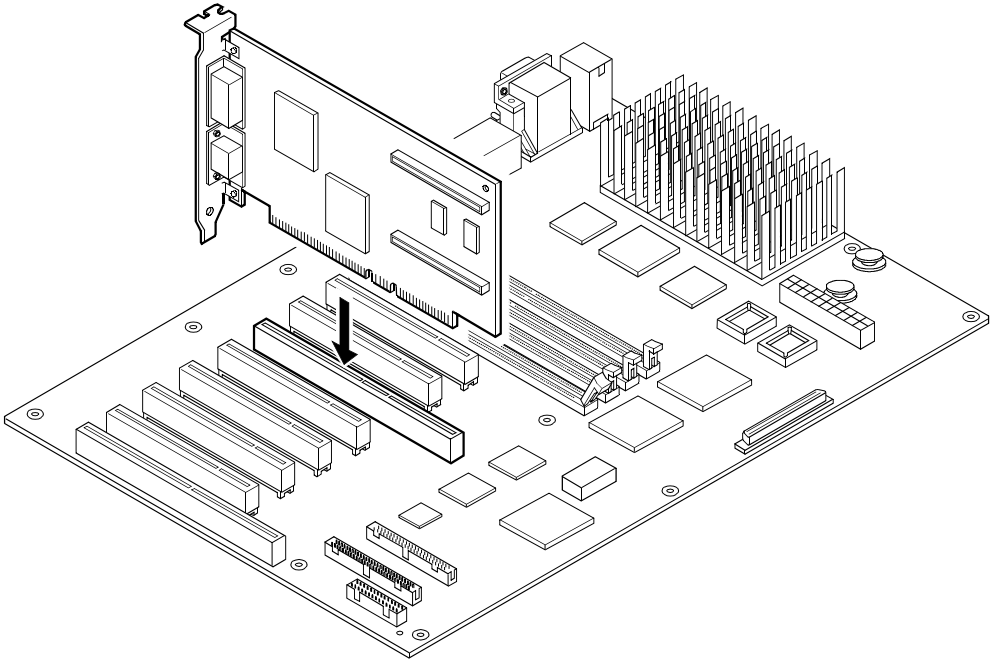


Figure 1-4. PCI Adapter Card Placement on MTX604-070

MTX604-070 Motherboard Installation

With PCI board(s) installed (if required) and headers properly configured, proceed as follows to install the MTX604-070 in the ATX chassis:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Install standoffs provided with the chassis in locations aligning with the MTX604-070 motherboard mounting holes. Use as many screw-down metal standoffs as possible.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits

4. Secure the MTX604-070 in the chassis with the screws provided.
5. Install jackposts on the rear panel COM2 and parallel port connectors.
6. Replace the chassis or system cover(s), making sure no cables are pinched. Cable the peripherals to the panel connectors, reconnect the system to the AC or DC power source, and turn the equipment power on.

System Considerations

The MTX604-070 uses a 20-pin ATX compatible connector for power input. In the default build configuration, the motherboard only requires +5.0V from the external ATX supply to operate, generating required secondary voltages (processor core voltage and +3.3V) from the +5.0V supply. As a build option, the +3.3V may be supplied from the external ATX supply. The PIDXv-60Xe processor power (1.8 to 2.6 Volts) comes from the +5.0V supply. The MTX604-070 routes +3.3V, +5.0V, +12.0V, -5.0V and -12.0V to the ISA and PCI slots, and fused power is routed to other peripherals via polyswitches as described in the paragraph below.

The MTX604-070 board supplies +5.0V power to the mouse and keyboard via a 1.1 amp polyswitch, +5.0V (optional) to the SCSI termpower via a 1.1 amp polyswitch, and +5.0V to the Reset/Abort/LED headers (J13 and J19) via a 0.75 amp polyswitch.

MTX604-070 Motherboard

Fused +5Vdc power is supplied to the motherboard's keyboard and mouse connectors through a 1.1 amp polyswitch and +5.0V power to the front panel header via a 0.75 amp polyswitch.

The MTX604-070 motherboard supplies a **SPEAKER_OUT** signal to front panel function header. This signal is driven by an NPN transistor device, which is controlled by the **SPKR** output pin from the PIB. The **SPKR** output pin is an output from the PIB Counter 2 and is ANDed with Port 61h bit 1 of the PIB to provide Speaker Data Enable.

On the MTX604-070 motherboard, the standard serial DTE port (COM1) serves as the PPCBug debugger console port. The firmware console should be set up for initial power-up as follows:

- Eight bits per character
- One stop bit per character
- Parity disabled (no parity)
- Baud rate of 9600 baud

After power-up you can reconfigure the baud rate if you wish, using the PPCBug **PF** (Port Format) command via the command line interface. Whatever the baud rate, some type of hardware handshaking—either **XON/OFF** or via the RTS/CTS line—is desirable if the system supports it.

Operating Instructions 2

Introduction

This chapter supplies information for use of the MTX604-070 motherboard in a system configuration. Here you will find the power-up procedure and descriptions of the switches and LEDs, memory maps, and software initialization.

Applying Power

After you have verified that all necessary hardware preparation has been done, that all connections have been made correctly, and that the installation is complete, you can power up the system. The MPU, hardware, and firmware initialization process is performed by the PowerPC™ PPCBug power-up or system reset. The firmware initializes the devices on the MTX604-070 module in preparation for booting the operating system.

The firmware is shipped from the factory with an appropriate set of defaults. In most cases there is no need to modify the firmware configuration before you boot the operating system.

The following flowchart shows the basic initialization process that takes place during PowerPC system startup.

For further information on PPCBug, refer to Chapter 5, *PPCBug*, or to the *PPCBug Firmware Package User's Manual*, listed in Appendix B, *Related Documentation*.

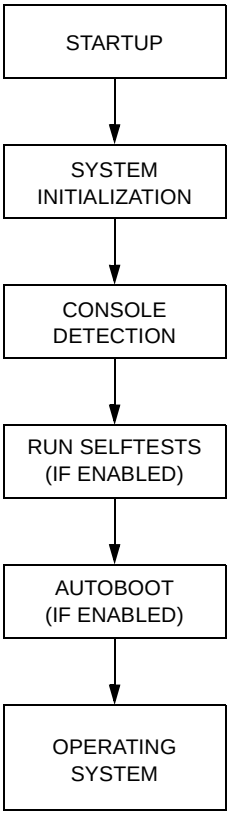


Figure 2-1. PPCBug System Startup

Front Panel Functions

The MTX604-070 has two planar headers for front panel functions including abort and reset switches, a speaker interface, and LED indicators.

Typical ATX chassis have front panel controls and indicators including a momentary power switch, a reset switch, a power LED, a disk activity LED, and a speaker. See *MTX604-070 Motherboard Preparation* on page 1-4 for information on connecting chassis controls and indicators.

Memory Maps

There are two points of view for memory maps:

- The mapping of all resources, as viewed by the processor (MPU bus memory map)
- The mapping of on-board resources as viewed by PCI local bus masters (PCI bus memory map)

The following sections give a general description of the MTX604-070 memory organization from the above two points of view. Detailed memory maps can be found in the *MTX PCI Series Motherboard Programmer's Reference Guide*, listed in Appendix B, *Related Documentation*.

Processor Memory Map

The processor memory map configuration is under the control of the Raven bridge controller ASIC and the Falcon memory controller chip set. The Raven and Falcon devices adjust system mapping to suit a given application via programmable map decoder registers. At system power-up or reset, a default processor memory map takes over.

Default Processor Memory Map

The default processor memory map that is valid at power-up or reset remains in effect until reprogrammed for specific applications. Table 2-1 defines the entire default memory map ($00000000 to $FFFFFFFF).

Table 2-1. Processor Default View of the Memory Map

Processor Address		Size	Definition	Notes
Start	End			
00000000	7FFFFFFF	2GB	Not Mapped	
80000000	8001FFFF	128KB	PCI/ISA I/O Space	1
80020000	FEF7FFFF	2GB-16MB-640KB	Not Mapped	
FF000000	FF7FFFFF	8MB	Flash Bank A	
FF800000	FF8FFFFF	1MB	Flash Bank B	

Table 2-1. Processor Default View of the Memory Map (Continued)

Processor Address		Size	Definition	Notes
Start	End			
FF900000	FFEFFFFF	6MB	Not Mapped	
FEF80000	FEF8FFFF	64KB	Falcon Registers	
FEF90000	FEFEFFFF	384KB	Not Mapped	
FEFF0000	FEFFFFFF	64KB	Raven Registers	
FFF00000	FFFFFFFF	1MB	ROM/Flash Bank A or Bank B	2

Notes

1. Default map for PCI/ISA I/O space. Allows software to determine whether the system is MPC105-based or Falcon/Raven-based by examining either the PHB Device ID or the CPU Type register.

2. The first 1MB of ROM/Flash Bank A (soldered 4MB Flash) appears in this range after a reset if the **rom_b_rv** control bit in the Falcon's ROM B Base/Size register is cleared. If the **rom_b_rv** control bit is set, this address range maps to ROM/Flash Bank B (socketed 1MB ROM/Flash).

For detailed processor memory maps, including suggested **PREP** and **CHRP** compatible memory maps, refer to the *MTX PCI Series Motherboard Programmer's Reference Guide*, listed in Appendix B, *Related Documentation*.

PCI Local Bus Memory Map

The local PCI memory map is the PCI memory map as viewed by the MTX604-070 motherboard. After a reset, the Raven ASIC map decoders are in the default (off) state. Software must program the appropriate map decoders for a specific environment. For detailed PCI memory maps, including suggested PREP-compatible memory maps, refer to the *MTX PCI Series Motherboard Programmer's Reference Guide*, listed in Appendix B, *Related Documentation*.

L2 Cache

The MTX604-070 motherboard uses a lookaside L2 cache structure that is implemented using the Doubletake integrated cache and controller. The MTX604-070 will support 0, 256KB or 512KB of L2 cache. The L2 cache can operate in copyback or writethru modes and supports system cache coherency through snooping. Refer to the *MTX PCI Series Motherboard Programmer's Reference Guide*, listed in Appendix B, *Related Documentation*, for additional information.

System Clock Generator

The system clocks for the processor, Raven/Falcon chipset (66 MHz) and each of the onboard PCI devices (33 MHz) are generated by a 66 MHz oscillator and distributed by the MPC949 clock buffer. Separate oscillators are provided as follows: 14.31818 MHz for the PIB internal timer; 20 MHz for the ethernet MAC interfaces; 25 MHz for the ethernet PHY devices; 24 MHz for the SuperI/O interface; and 40 MHz for the SCSI.

PPC Bus Arbitration

The arbitration control for the PPC bus is provided by a PLD. There are four potential PPC masters, PPC0, PPC1, Raven, and Doubletake, with Raven having the highest priority. See the following section titled *PCI Arbitration* for a description of arbitration control of PCI devices.

PCI Host Bridge

The Raven ASIC provides the bridge function between the CPU bus and the on-board PCI Local Bus. Raven is a PCI 2.1 compliant 64-bit PCI implementation for 32/64-bit data transfers. Dual Address Cycle is not supported. The Raven supports PowerPC processor external bus frequencies up to 66 MHz and PCI frequencies up to 33 MHz.

There are four programmable map decoders for each direction to provide flexible address mappings between the PPC/DRAM and the PCI Local Bus. Refer to the *MTX PCI Series Motherboard Programmer's Reference Guide* for additional information and programming details.

PCI Arbitration

There are ten potential primary PCI bus masters on the MTX604-070. One of these (the IDE interface) is not used, but its bus request and grant are internal to the PIB and are not reassignable to another device. The PIB arbiter can handle a total of eight masters. Six of the PIB levels are assigned directly to masters, the remaining two are assigned to an arbiter expansion circuit that expands them to four. The arbiter expansion uses rotating priority to provide fair arbitration between the two masters at each level. The PIB supports fixed, multi-level, and round-robin arbitration (round-robin is power-up default), see the Winbond W83C554 manual, listed in Appendix B, *Related Documentation*, for more information on the PIB arbiter options. The primary PCI bus arbitration assignments on MTX604-070 are as follows:

Table 2-2. Primary PCI Arbitration Assignments

PCI Bus Request	PCI Master(s)
PIB Internal	ISA bridge
PIB Internal	IDE
PIB CPU Request	Raven Host Bridge
PIB Request 0	PCI/PCI Bridge
PIB Request 1	SCSI
PIB Request 2	PCI Slot 1P
PIB Request 3	Expansion Arbiter Request A
PIB Request 4	Expansion Arbiter Request B
Arb. Exp. Request A1	PCI Slot 2P
Arb. Exp. Request A2	LAN 1
Arb. Exp. Request B1	PCI Slot 3P
Arb. Exp. Request B2	LAN 2

Interrupt Handling

The Raven ASIC provides an MPIC Interrupt Controller to handle various interrupt sources. This MPIC supports up to two processors and 16 external interrupt sources. There are also six other interrupt sources inside

the MPIC: two cross-processor interrupts and four timer interrupts. All ISA interrupts go through the 8259 pair in the PIB. The output of the PIB then goes through the MPIC in Raven.

Sources of interrupts may be any of the following:

- The Raven ASIC itself (four MPIC timer interrupts or transfer error interrupts)
- The Processor 0 (processor self-interrupts)
- The Processor 1 (processor self-interrupts on dual processor motherboard)
- Transfer Error Interrupt (from the Raven ASIC)
- The Falcon chip set (memory error interrupts)
- The PCI bus (interrupts from PCI devices)
- Power monitor interrupts
- Watchdog timer interrupt
- The ISA bus (interrupts from ISA devices)

The ISA interrupts are handled as a single 8259 interrupt from the PIB device.

For details on interrupt handling, refer to the *MTX PCI Series Motherboard Programmer's Reference Guide*, listed in Appendix B, *Related Documentation*.

ISA DMA Channels

The PIB supports seven 8237 compatible DMA channels. ISA compatible type A, B, and F timing and scatter/gather capability is supported.

Sources of Reset

There are five potential sources of reset on the MTX604-070. They are:

- Power-On Reset

- **RESET** Switch
- Watchdog Timer Reset via the MK48T559 Timekeeper device
- Port 92 Register via the PIB
- I/O Reset via the Clock Divisor Register in the PIB

The following table shows which devices are affected by various reset sources:

Table 2-3. MTX604-070 Device Reset Implications

Device Affected	Processor (s)	Raven ASIC	Falcon3 Chipset	PCI Devices	ISA Devices
Power-On	x	x	x	x	x
Reset Switch	x	x	x	x	x
Watchdog (MK48T559)	x	x	x	x	x
Hot Reset (Port 92 Register)	x	x	x	x	x
PCI/ISA Reset (Clock Divisor Register)				x	x

Soft Reset

Software can assert the **SRESET#** pin of any processor by programming the Processor Init Register of the RavenMPIC appropriately.

Error Notification and Handling

The Raven and Falcon3 chipset can detect certain hardware errors and can be programmed to report these errors via the RavenMPIC interrupts or Machine Check Interrupt.

Note The **TEA*** signal is not used at all by MTX604-070. The following table summarizes how the hardware errors are handled by MTX604-070:

Table 2-4. Error Notification and Handling

Cause	Action
Single-bit ECC	*Store*: Write corrected data to memory *Load*: Present corrected data to the MPC master Generate interrupt via RavenMPIC if so enabled
Double-bit ECC	*Store*: Terminate the bus cycle normally without writing to DRAM *Load*: Present un-corrected data to the MPC master Generate interrupt via RavenMPIC if so enabled Generate Machine Check Interrupt to the Processor(s) if so enabled
MPC Bus Time Out	*Store*: Discard write data and terminate bus cycle normally *Load*: Present undefined data to the MPC master Generate interrupt via RavenMPIC if so enabled Generate Machine Check Interrupt to the Processor(s) if so enabled
PCI Target Abort	*Store*: Discard write data and terminate bus cycle normally *Load*: Return all 1s and terminate bus cycle normally Generate interrupt via RavenMPIC if so enabled Generate Machine Check Interrupt to the Processor(s) if so enabled
PCI Master Abort	*Store*: Discard write data and terminate bus cycle normally *Load*: Return all 1s and terminate bus cycle normally Generate interrupt via RavenMPIC if so enabled Generate Machine Check Interrupt to the Processor(s) if so enabled
PERR# Detected	Generate interrupt via RavenMPIC if so enabled Generate Machine Check Interrupt to the Processor(s) if so enabled
SERR# Detected	Generate interrupt via RavenMPIC if so enabled Generate Machine Check Interrupt to the Processor(s) if so enabled

Endian Issues

The MTX604-070 supports both Little-Endian and Big-Endian software. The PowerPC is inherently Big-Endian, while the PCI bus is inherently Little-Endian. The following sections summarize how the MTX604-070 handles software and hardware differences in Big- and Little-Endian operations. For further details on Endian considerations, refer to the *MTX PCI Series Motherboard Programmer's Reference Guide*, listed in Appendix B, *Related Documentation*.

Processor/Memory Domain

The MTX604-070 processor can operate in both Big- and Little-Endian mode. However, it always treats the external processor/memory bus as Big-Endian by performing *address rearrangement* and *reordering* when running in Little-Endian mode. The PPC registers in the Raven PCI bus bridge controller ASIC and the Falcon memory controller chip set, as well as DRAM, ROM/Flash, and system registers, always appear as Big-Endian.

Role of the Raven ASIC

Because the PCI bus is Little-Endian, the Raven performs byte swapping in both directions (from PCI to memory and from the processor to PCI) to maintain address invariance while programmed to operate in Big-Endian mode with the processor and the memory subsystem.

In Little-Endian mode, the Raven *reverse-rearranges* the address for PCI-bound accesses and *rearranges* the address for memory-bound accesses (from PCI). In this case, no byte swapping is done.

PCI Domain

The PCI bus is inherently Little-Endian. All devices connected directly to the PCI bus operate in Little-Endian mode, regardless of the mode of operation in the processor's domain.

PCI and Ethernet

Ethernet is also byte-stream-oriented; the byte having the lowest address in memory is the first one to be transferred regardless of the endian mode. Since the Raven maintains address invariance in both Little-Endian and Big-Endian mode, no Endian issues should arise for Ethernet data. Big-endian software must still take the byte-swapping effect into account when accessing the registers of the PCI/Ethernet device, however.

Functional Description 3

Introduction

This chapter describes the MTX604-070 motherboard computer on a block diagram level. The *General Description* provides an overview of the MTX604-070, followed by a detailed description of several blocks of circuitry. Figure 3-1 shows a block diagram of the overall board architecture.

Detailed descriptions of other MTX604-070 blocks, including programmable registers in the ASICs and peripheral chips, can be found in the *MTX PCI Series Motherboard Programmer's Reference Guide*, listed in Appendix B, *Related Documentation*. Refer to it for a functional description of the MTX604-070 in greater depth.

Features

The following table summarizes the features of the MTX604-070 single-board computers.

Table 3-1. MTX604-070 Features

Feature	Description
Microprocessor	Supports BGA 60*x* processors: 603e, 604e Single/dual processor (604e); Bus Clock Frequencies up to 66 MHz
DRAM	Two-way Interleaved, ECC protected 32MB to 1GB on-board. Supports single or dual-bank DIMMs in four on-board connectors.
L2 cache memory	Build option for 256KB or 512KB Look-aside L2 Cache (Doubletake)
Flash Memory	8MB (64-bit wide) plus sockets for 1MB (16-bit)
Memory Controller	Falcon3 Chipset
Real-time clock	8KB NVRAM with RTC and battery backup (SGS-Thomson M48T559)
Status LEDs	two: BFL, CPU
Watchdog timer	Provided in SGS-Thomson M48T559 or Raven3

Table 3-1. MTX604-070 Features (Continued)

Feature	Description
Form Factor	ATX
Interrupts	Software interrupt handling via Raven (PCI-MPU bridge) and Legacy (Windbond)
Peripheral Support	Two 16550-compatible async serial ports One Host-mode Parallel Port 8-bit/16-bit single-ended SCSI interface Two 10 Base-T/100 Base-Tx Ethernet interfaces One PS/2 Keyboard and one PS/2 Mouse One PS/2 Floppy Port
PCI interface	32/64-bit Data, up to 33 MHz operation
PCI/ISA Expansion	Seven PCI slots (one shared), one ISA slot (shared)

General Description

The MTX604-070 is a motherboard based on the PowerPlus architecture, including optional features for embedded applications. It consists of the MPC603e/PID9v-604e processor, the Raven PCI Bridge and Interrupt Controller, the ECC Memory Controller Falcon3 chipset, 8 MB plus 1 MB of Boot FLASH, ECC-protected DRAM, and a large set of I/O peripherals.

The MTX604-070 will support single or dual processors. In the dual processor configuration, the internal operating frequencies of the processors are independently configurable, allowing non-SMP board configurations. For example, a dual configuration with a 200 MHz 603ev and a 300 MHz 604e processor dual configuration is feasible, but would require custom firmware, test software, and possibly other add-on items. SMP operation is only supported in dual processor boards with 604e processors.

I/O peripheral interfaces present onboard include SCSI interface, two 10 Base-T/100 Base-Tx Ethernet interfaces, one 64-bit PCI slot plus six 32-bit PCI slots (one slot shared with ISA function). Functions provided from the ISA bus include a host mode P1284 parallel port, two async serial ports, a real time clock, counters/timers, and one ISA slot (shared).

Rear panel connectors on the MTX604-070 include two 6-pin circular DIN connectors (one for the keyboard and one for the mouse), a 25-pin host mode parallel port connector, two RJ45 connectors for 10 Base-T/100 Base-Tx Ethernet, and two 9-pin D COM port connectors.

All PCI slots, as well as the ISA slot, use rear panel I/O on ATX spacing.

DRAM memory is added via DIMM sockets. The serial presence detect (SPD) feature of the DIMM DRAMs is supported via the Falcon3 I^2C bus controller.

Block Diagram

Figure 3-1 is a block diagram of the MTX604-070's overall architecture.

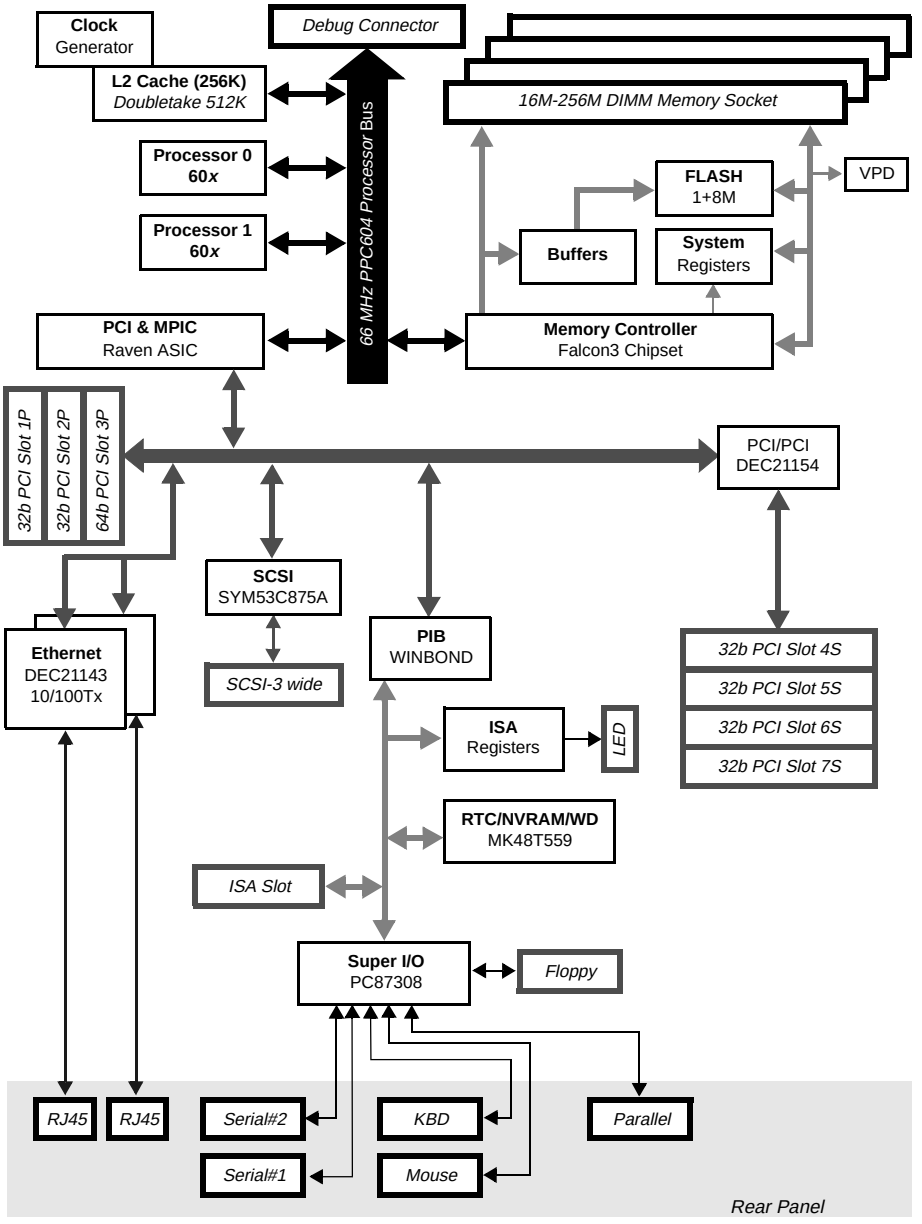


Figure 3-1. MTX604-070 Block Diagram

MTX604-070 Processor

The MTX604-070 processor has BGA footprints that support MPC60*x* processors: PID7v-603lc, and PID9v-604e. The maximum processor system bus speed is 66 MHz.

System Clock Generator

The MPC60*x* processor and PCI clocks are generated and distributed by the MPC949 clock generator. Additional clocks are independently generated for the SCSI, ISA bridge, Super I/O chip and the LAN.

Boot FLASH

The MTX604-070 contains two banks of FLASH memory on the main board. Bank A consists of four soldered-in 16-bit wide, 2 megabyte deep 3.3V FLASH SMT devices (Intel 28F160S3) and appears as FLASH Bank A, 64-bits wide to the Falcon3 chipset. A resistor select enables write protect for the entire 8M of Bank A, individual 64K byte block protection can be enabled by software. Additionally, software can write-enable/disable the entire Flash bank through control of this **rom_x_wc** bit of the Falcon ROM Base/Size registers.

Bank B consists of two sockets for 8-bit wide +5.0 volt FLASH SMT devices (typically AMD AM29F040-120JC) and appears as FLASH Bank B (16-bits wide) to the Falcon3 chipset. The Bank B sockets support a maximum 512 K-byte FLASH in each socket. Refer to Figure 3-2 for details.

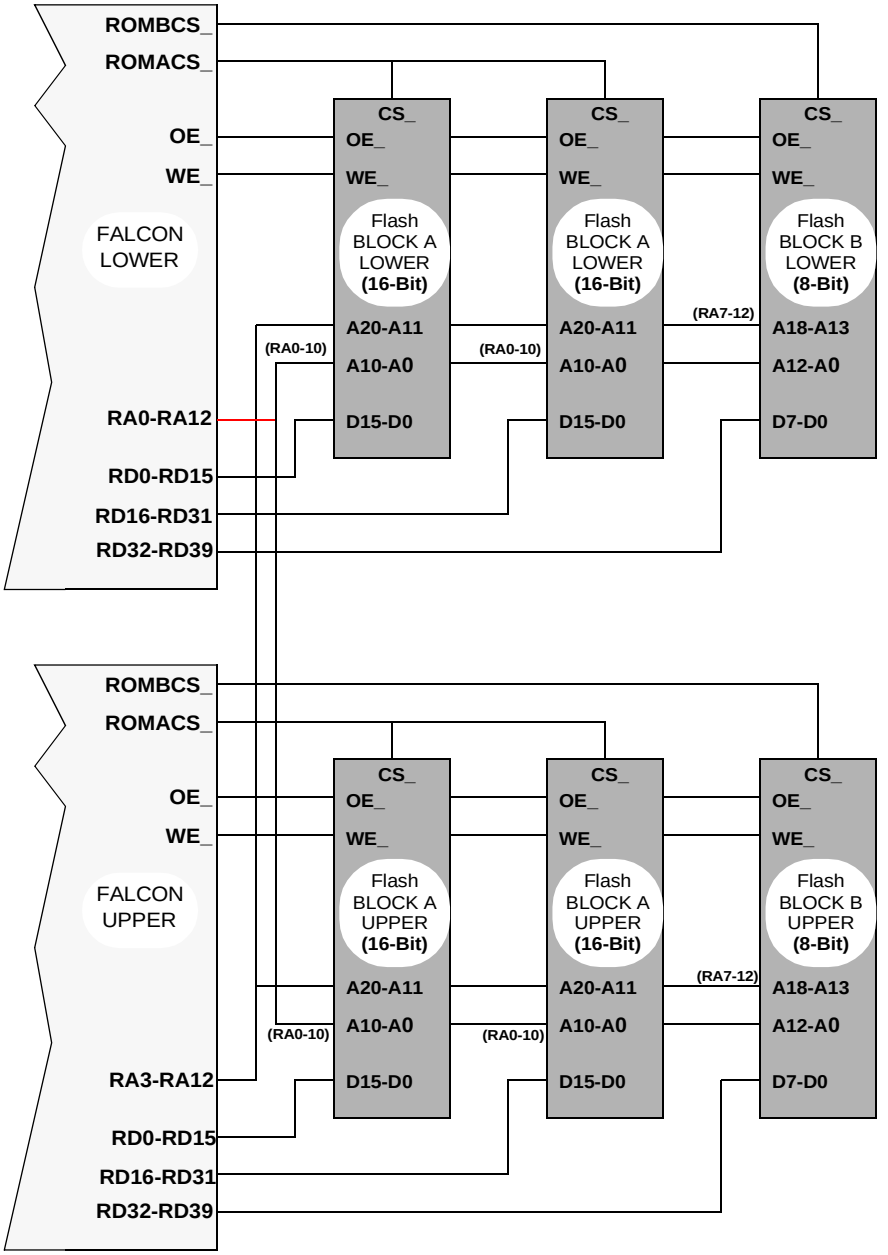


Figure 3-2. Falcon Upper/Lower Boot Flash Diagram

ECC Memory

The MTX604-070 supports up to 1GB of ECC DIMM memory. The DRAM memory is controlled by the Falcon3 chipset which performs two-way interleaving and provides single-bit error correction and double-bit error detection. ECC is calculated over 72-bits. DIMMs must be 168-pin, 3.3V, unbuffered, EDO or Fast-Page, with serial presence detect (SPD). Both single and dual-bank DIMMs are supported. Refer to the *MTX PCI Series Motherboard Programmer's Reference Guide*, listed in Appendix B, *Related Documentation*, for additional information and programming details.

L2 Cache

The optional L2 cache functionality is provided by the Doubletake chipset. The MTX604-070 may be populated with 256KB (one Doubletake device) or 512KB (two Doubletake devices) look-aside L2 cache. Refer to the MPC2605GA Data Sheets and the *MTX PCI Series Motherboard Programmer's Reference Guide* for additional information. Both are listed in Appendix B, *Related Documentation*.

PPC to PCI Host Bridge

The Raven ASIC provides the bridge function between the MPC60*x* bus and the PCI Local Bus. It is a 64-bit PCI implementation for data transfers. Dual Address Cycle is not supported. The Raven supports various PowerPC processor external bus frequencies up to 66 MHz and PCI frequencies up to 33 MHz.

There are four programmable map decoders for each direction to provide flexible address mappings between the MPC and the PCI Local Bus. Refer to the *MTX PCI Series Motherboard Programmer's Reference Guide* for additional information and programming details.

Interrupt Controller (MPIC)

The Raven ASIC also provides an MPIC Interrupt Controller to handle various interrupts sources. The interrupt sources are: four MPIC Timer Interrupts, Processor 0 self interrupt, the Memory Error Interrupt from the Falcon3 chipset, the Transfer Error Interrupt from the Raven ASIC, the interrupts from all PCI devices, the two software interrupts, and the ISA interrupts. The ISA interrupts are handled as a single 8259 interrupt at INT0.

Refer to the *MTX PCI Series Motherboard Programmer's Reference Guide*, listed in Appendix B, *Related Documentation*, for additional information and programming details.

SCSI Interface

The MTX604-070 provides support for SCSI-1, SCSI-2, and SCSI-3 standards. The MTX604-070 implements fast 8- or 16-bit transfers, and UltraSCSI transfers. The standard SCSI SCLK is 40 MHz for SCSI-1,2 and Ultra SCSI transfers (the SYM53C875A clock doubler is used for Ultra).

PCI-to-PCI Bridge Interface

The MTX604-070 uses a DEC21154 PCI-to-PCI bridge to support additional PCI slots. The bridge connects the 64-bit primary PCI (Raven) bus to the 32-bit secondary bus. This device is PCI 2.1 compliant. The 21154 provides read/write data buffering in both directions.

The device has an internal arbiter that implements a programmable 2-level rotating algorithm for all secondary PCI bus masters. The arbiter latency is typically one PCI clock. If the 21154 detects that an initiator has failed to assert **FRAME#** within 16 clock of the grant, the arbiter will deassert the grant. The arbiter parks the secondary bus at the last bus master by keeping the last grant asserted until a new bus request is asserted. All devices on the secondary PCI bus must support bus parking. After a reset, the 21154 parks the secondary PCI bus at itself until a new request is asserted. The 21154 supports error reporting on the primary PCI bus by implementing **PERR#** and **SERR#** signals on both primary and secondary busses, along

with status registers and an event disable register. For additional information, refer to the DEC21154 data sheet. The IDSEL assignments for all PCI buses is shown below.

Table 3-2. PCI IDSEL Assignments

Device	IDSEL
PIB	PAD11
SCSI	PAD12
Ethernet 1	PAD14
Slot 1P	PAD16
Slot 2P	PAD17
Slot 3P	PAD18
Ethernet 2	PAD19
PPB	PAD20
PHB	PAD30/31
Slot 4S	SAD18
Slot 5S	SAD19
Slot 6S	SAD20
Slot 7S	SAD21

Ethernet Interface

The MTX604-070 provides two Ethernet interfaces via the DEC21143 device and the Level One LXT970 MAU/PHY. Both Ethernet interfaces are routed to rear panel connectors. Users may select either the 10 Base-T or the 100 Base-Tx interface.

Every board will be assigned an Ethernet Station Address. The address is $08003E*xxxxxx* where *xxxxxx* is the unique number assigned to the board.

Note The Ethernet Station Address of boards manufactured after March 2000 is $0001AF*xxxxxx*.

Each board's Ethernet Station Address is displayed on a label attached to the PMC front-panel keep-out area. In addition, the Ethernet address is stored in the configuration area of the NVRAM specified by the Boot ROM and in the serial ROM attached to the 21143.

These bytes are stored in bytes 0x14 through 0x19 in the Ethernet SROM. The Ethernet information in the SROM is stored in DEC Version 3 format. For further information on this refer to the Digital Semiconductor 21x4x Serial ROM Format, Version 3.03 document.

Caution Use extreme caution when viewing the contents of the Ethernet SROM via the **PPCBUG SROM** command. If the contents are modified incorrectly this could cause the PPCBUG Firmware Ethernet Drivers to work incorrectly.

Note: When the board is shipped from the factory, it will contain the proper SROM data for the MTX604-070, which has 10 Base-T/100 Base-Tx Ethernet connections. There should not be a need to change the SROM contents.

For the pin assignments of the 10 Base-T/100 Base-Tx connector, refer to Table 4-10 on page 4-11.

PCI-ISA Bridge (PIB)

The MTX604-070 board uses the WINBOND 83C554 device to interface to the ISA bus for many system resources. The 83C554 device, hereafter referred to as the PIB, provides the following features:

- PCI bus arbitration for: ISA, DMA, the PHB, all onboard PCI devices, and the PCI slots
- ISA bus arbitration for DMA devices
- ISA Interrupt mapping for four PCI interrupts
- Functionality of two 82C59 Interrupt Controllers to support 14 ISA interrupts

- Edge/Level control for ISA interrupts
- Seven independently programmable DMA channels (functionality of two 82C37SA devices)
- One 16-bit Timer
- Three interval Counters/Timers (82C54 functionality)
- The Super I/O device and ISA expansion slot connect to the ISA bus

PC87308 ISA Super I/O Device

The MTX604-070 uses the PC87308 ISA SIO from National Semiconductor to provide: two async serial ports, a host-mode parallel port, a PS/2 floppy disk interface, a PS/2 keyboard interface, and a PS/2 mouse interface. Each of the supported features are described in the following sub-sections.

Async Serial Ports

These two ports are routed the rear panel. Firmware initializes the two serial ports as COM1 and COM2 with ISA I/O base addresses of x3F8 and x2F8 respectively. This default configuration also assigns COM1 to IRQ4 and COM2 to IRQ3 of the PIB. The default configuration can be changed by programming the ISA SIO device accordingly.

Host Mode P1284/Printer Interface

The host mode parallel I/O interface signals are routed to a 25-pin subminiature rear panel connector. Firmware initializes the parallel port as PPT1 with ISA IO base address of x3BC. This default configuration also assigns the parallel port to IRQ7 of the PIB. The default configuration can be changed by programming the ISA Super I/O device accordingly.

PS/2 Floppy Disk Interface

The floppy port is configured for PS/2 compatibility. The floppy disk signals and power are routed to a 34-pin planar connector.

Mouse and Keyboard

The ISA Super I/O provides a ROM-based Award BIOS for keyboard and mouse interface. Two 6-pin circular DIN connectors are located on the rear panel of the MTX604-070 board for the keyboard and the mouse connections.

Real-Time Clock & NVRAM & Watchdog Timer

The SGS-Thomson M48T559 provides 8 KB of non-volatile static RAM, a real-time clock, and a watchdog function. Refer to the M48T559 data sheets, listed in Appendix B, *Related Documentation*, for programming information. The M48T559 consists of two parts:

- A 28-pin 33-mil SOIC which contains the RTC, the oscillator, the power fail detection, the watchdog timer logic, 8 KB of SRAM, and gold-plated sockets for the SNAPHAT battery.
- A SNAPHAT battery that houses the battery and the crystal.

The SNAPHAT package is mounted on top of the SOIC MT48T559 device. Refer to the *MTX PCI Series Motherboard Programmer's Reference Guide* for configuration register definition.

The output of the watchdog timer is logically ORed onboard to provide a hard reset. The interrupt output generates an ISA interrupt. Refer to the *MTX PCI Series Motherboard Programmer's Reference Guide* for more details.

Timers

Timers and counters on the MTX604-070 board are provided by the Raven ASIC and the Winbond.

Raven Interval Timers

The Raven ASIC has four 32-bit tick timers. The timer input frequency is 66.67 MHz/8 = 8.33 MHz. Refer to the *MTX PCI Series Motherboard Programmer's Guide* for programming details.

PIB Interval Timers

The PIB has three built-in counters that are equivalent to those found in an 82C54 programmable interval timer. These counters are grouped into one timer unit, Timer 1, in the PIB. Each counter output has a specific function:

- Counter 0 is associated with IRQ0 and can be used for system timing functions, such as timer interrupt for a time-of-day.
- Counter 1 is used to generate a refresh request signal for ISA memory. This timer is not used.
- Counter 2 provides the tone for the Speaker output function on the PIB.

These counters use the OSC clock input as their clock source. The MTX604-070 drives the OSC pin with a 14.31818 MHz clock source.

Configuration and Status Registers

The MTX604-070 motherboard contains several registers used to provide configuration and status information about the board. These registers are implemented with discrete logic or in PLDs. Refer to the *MTX PCI Series Motherboard Programmer's Reference Guide*, listed in Appendix B, *Related Documentation*, for details on these registers.

Serial EEPROM

The MTX604-070 base board contains a 512 x 8 Serial EEPROM. The Serial EEPROM provides for vital product data storage of the board configuration information. The Serial EEPROM is accessed through the I^2C port in the upper Falcon memory controller chip.

PCI Arbitration

PCI arbitration is performed by the PIB and an arbiter expansion PLD. The PCI request/arbitration assignments are as specified in the *MTX PCI Series Motherboard Programmer's Reference Guide.*

Interrupt Routing

Interrupts are routed to the PIB and the Raven MPIC as specified in the *MTX PCI Series Motherboard Programmer's Reference Guide,* listed in Appendix B, *Related Documentation*.

ISA DMA Channels

There are seven DMA channels supported by the PIB. These DMA channels are assigned as specified in the *MTX PCI Series Motherboard Programmer's Reference Guide*.

Front Panel Functions

The MTX604-070 has two planar headers for front panel functions including abort and reset switches, speaker interface, and LED drive. The +5.0V to these headers power is supplied via a 0.75 amp polyfuse. The headers provide the LED drive for six functions: **FAIL**, **CHKSTP**, **CPU**, primary PCI activity, secondary PCI activity, **POWER GOOD**, and **LAN1** and **LAN2** links. These signals function in the following manner:

- The **STATLED#** signal is active when either processor **CHECKSTOP** signal is active.
- The **FAILLED#** signal is active when the firmware controlled **BRDFAIL** signal is active.
- The **RUNLED#** signal is active when the **DBB#** signal of the processor bus is active.
- The **LAN1LED#** signal is active when the Ethernet 1 Link signal is active.
- The **LAN2LED#** signal is active when the Ethernet 2 Link signal is active.
- The **PCI_IRDY_LED#** signal is active when the **IRDY#** signal of the Primary PCI bus is active.
- The **SPCI_IRDY_LED#** signal is active when the **IRDY#** signal of the Secondary PCI bus is active.

- The **PWRGOOD#** signal is active when the SMI interrupt is inactive. The SMI interrupt is used to signal impending power failure on some systems.
- The **SCSI_BUSY_LED#** signal is active when the software controlled **SCSI_BUSY#** signal is active.

In addition, the MTX604-070 has two planar LEDs, the yellow FAIL LED is lit when the **BRDFAIL** signal line is active, and the green CPU LED is lit when the **DBB#** signal of processor bus is active.

Speaker Control

The MTX604-070 motherboard routes the **SPEAKER_OUT** signal to a front panel function header. This signal is driven by a NPN transistor device that is controlled by the **SPKR** output pin from the PIB. The SPKR output pin is an output from the PIB Counter 2 and is ANDed with Port61h bit 1 of the PIB to provide Speaker Data Enable.

Reset Switch Input

A 300ms hard reset is applied to the MTX604-070 logic when the **RESETSW_L** signal (front panel function header) is connected to logic ground. See the *Connector/Jumper Descriptions* on page 1-6 for connector labeling and pin assignment information.

Abort Switch Input

The status (high/low) of this front panel function signal is reflected in an ISA register bit. See the *MTX PCI Series Motherboard Programmer's Reference Guide*, listed in Appendix B, *Related Documentation*, for more information. PPCBug uses this indication as a pushbutton abort request. See the *Connector/Jumper Descriptions* on page 1-6 for connector labeling and pin assignment information.

Soft Power Switch Input

ATX power supplies have a logic level (+5.0V) power control input (**PS_ON_L**). An ATX supply power is **ON** when this input is connected to logic ground. The MTX604-070 motherboard features both level and

edge-sensitive control of this ATX power supply feature. A two pin header is provided for level control (short the pins to turn the supply on), or the supply may be controlled from the soft power switch input on the front panel function header. When there is a transition on the **SPSW_L** signal, the Advanced Power Control section of the Super I/O device will toggle the state of the **ONCTL_L**, signal. **ONCTL_L** is connected to the **PS_ON** input of the ATX power connector. See the PC87308 (Super I/O) data sheet, listed in Appendix B, *Related Documentation*, for soft power control programming details.

PCI Card Slots

The MTX604-070 motherboard supports seven PCI slots. The slots support PCI adapters with the following characteristics:

- PCI size: Full length adapters are supported in slots 1-5
- PCI: Slot 3 has a 64-bit connector
- Signaling Voltage: VIO = 5.0V

Power Supply

The MTX604-070 uses a 20-pin ATX compatible connector for power input. An MTX system with PCI and ISA adapters requires +5.0V, -5.0V, -12.0V, and +12.0V (and optionally 3.3V) power from an external supply, and will generate PIDXv-60Xe processor power (1.8 to 2.5 volts) from the +5.0V supply. The motherboard itself only requires +5.0V in the default configuration. The MTX604-070 can be built (build option) to generate the 3.3V power from the +5.0V supply, or may be built to use the 3.3V from by the external supply. The MTX604-070 routes +3.3V, +5.0V, +12.0V, and -12.0V to the PCI slots and ISA slot (also -5.0V to the ISA slot), and fused power is routed to other peripherals as described in the paragraph below.

Polyswitches

The MTX604-070 board supplies +5.0V power to the mouse and keyboard via a 1.1 amp polyswitch, and +5.0V power to the front panel headers via a 0.75 amp polyswitch.

Connector Pin Assignments

4

MTX Series Connectors

This chapter summarizes the pin assignments for the following connectors, headers, and sockets on the MTX board:

- Debug connector
- RISCWatch Header
- GAL Programming Header
- DRAM DIMM Socket
- Seven Segment LED Header
- Status LEDs and Switches
- Speaker and Power Status
- Rear Panel Keyboard/Mouse Connectors
- 10 Base-T/100 Base-Tx Connectors
- IEEE P1284 Host Mode Parallel I/O Connector
- Floppy Disk Header
- Serial Port 1 and 2 Connectors
- Power Connector

Debug Connector (J12)

A footprint for a Mictor connector is used to provide access to the CPU bus for debugging purposes. The following table shows the pin assignments for this connector.

Table 4-1. Debug Connector Pin Assignments

Pin	Signal		Pin	Signal
1	PA0		2	PA1
3	PA2		4	PA3
5	PA4		6	PA5
7	PA6		8	PA7
11	PA10		12	PA11
13	PA12		14	PA13
15	PA14		16	PA15
17	PA16		18	PA17
19	PA18		20	PA19
21	PA20		22	PA21
23	PA22		24	PA23
25	PA24		26	PA25
27	PA26		28	PA27
29	PA28		30	PA29
31	PA30		32	PA31
33	APAR0		34	APAR1
35	APAR2		36	APAR3
37	APE_L		38	RSRV0_L
39	PD0		40	PD1
41	PD2		42	PD3
43	PD4		44	PD5
45	PD6		46	PD7
47	PD8		48	PD9
49	PD10		50	PD11
51	PD12		52	PD13
53	PD14		54	PD15
55	PD16		56	PD17
57	PD18		58	PD19

Table 4-1. Debug Connector Pin Assignments (Continued)

Pin	Signal		Pin	Signal
59	PD20		60	PD21
61	PD22		62	PD23
63	PD24		64	PD25
65	PD26		66	PD27
67	PD28		68	PD29
69	PD30		70	PD31
71	PD32		72	PD33
73	PD34		74	PD35
75	PD36		76	PD37
77	PD38		78	PD39
79	PD40		80	PD41
81	PD42		82	PD43
83	PD44		84	PD45
85	PD46		86	PD47
87	PD48		88	PD49
89	PD50		90	PD51
91	PD52		92	PD53
93	PD54		94	PD55
95	PD56		96	PD57
97	PD58		98	PD59
99	PD60		100	PD61
101	PD62		102	PD63
103	DPAR0		104	DPAR1
105	DPAR2		106	DPAR3
107	DPAR4		108	DPAR5
109	DPAR6		110	DPAR7
111	NC		112	NC
113	DPE_L		114	DBDIS_L
115	TT0		116	TSIZ0

Table 4-1. Debug Connector Pin Assignments (Continued)

Pin	Signal		Pin	Signal
117	TT1		118	TSIZ1
119	TT2		120	TSIZ2
121	TT3		122	TC0
123	TT4		124	TC1
125	CI_L		126	TC2
127	WT_L		128	CSE0
129	GBL_L		130	CSE1
131	SHD_L		132	DBWO_L
133	AACK_L		134	TS_L
135	ARTRY_L		136	XATS_L
137	DRTRY_L		138	TBST_L
139	TA_L		140	NC
141	TEA_L		142	NC
143	NC		144	DBG_L
145	NC		146	DBB_L
147	NC		148	ABB_L
149	TCLK0		150	MPUBG0_L
151	NC		152	MPUBR0_L
153	MPUBR1_L		154	IRQ0_L
155	MPUBG1_L		156	MCHK0_L
157	IRQ1_L		158	SMI_L
159	MCHK1_L		160	CKSTPI0_L
161	L2BR_L		162	CKSTPO0
163	L2BG_L		164	HALTED0
165	CLAIM_L		166	TLBISYNC_L
167	NC		168	TBEN0
169	NC		170	TBEN1
171	NC		172	DRVMOD0
173	NC		174	DRVMOD1

Table 4-1. Debug Connector Pin Assignments (Continued)

Pin	Signal		Pin	Signal
175	NC		176	NAPRUN0
177	SRESET1_L		178	QREQ_L
179	SRESET0_L		180	QACK_L
181	HRESET_L		182	CPU0TDO
183	GND		184	CPU0TDI
185	MPUCLK		186	CPU0TCK
187	MPUCLK		188	CPU0TMS
189	MPUCLK		190	CPU0TRST_L

RISCWatch Header Pin Definitions (J17)

Table 4-2. RISCWatch Header

Signal	Pin	Pin	Signal
CPU1TDO	1	2	NC
CPU1TDI	3	4	CPU1RST_L
NC	5	6	1KPU_3.3V
CPU1TCK	7	8	NC
CPU1TMS	9	10	NC
SRESET0_L	11	12	NC
RW0RESET_L	13	14	KEYPIN
CKSTPO0_L	15	16	GND

GAL Programming Header Pin Definitions (J22)

Table 4-3. GAL Programming Header Pin Definitions

Signal	Pin
+5.0v	1
ISPSDO	2
ISPSDI	3
ISPEN_L	4
KEY	5
ISPMODE	6
GND	7
ISPSCLK	8

DRAM DIMM Socket Pin Definitions (XU1-4)

Table 4-4. DRAM DIMM Socket Pin Definitions

Pin#	Front Side	Pin#	Front Side	Pin#	Rear Side	Pin#	Rear Side
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2_L	86	DQ32	128	DU
3	DQ1	45	RAS2_L	87	DQ33	129	RAS3_L
4	DQ2	46	CAS2_L	88	DQ34	130	CAS6_L
5	DQ3	47	CAS3_L	89	DQ35	131	CAS7_L
6	Vcc	48	WE2_L	90	Vcc	132	DU
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	DU	104	DQ47	146	DU
21	CB0	63	NC	105	CB4	147	NC
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE0_L	69	DQ24	111	DU	153	DQ56

Table 4-4. DRAM DIMM Socket Pin Definitions (Continued)

Pin#	Front Side	Pin#	Front Side	Pin#	Rear Side	Pin#	Rear Side
28	CAS0_L	70	DQ25	112	CAS4_L	154	DQ57
29	CAS1_L	71	DQ26	113	CAS5_L	155	DQ58
30	RAS0_L	72	DQ27	114	RAS1_L	156	DQ59
31	OE0_L	73	Vcc	115	DU	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	A11	164	NC
39	A12	81	NC	123	NC	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	DU	167	SA2
42	DU	84	Vcc	126	DU	168	Vcc

Note NC = no connect, DU = don’t use

Seven Segment LED Header (J16)

Table 4-5. Seven Segment LED Header

Signal	Pin	Pin	Signal
+5_SSEG	1	2	+5_SSEG
LEDDISP(0)	3	4	LEDDISP(1)
LEDDISP(2)	5	6	LEDDISP(3)
LEDDISP(4)	7	8	LEDDISP(5)
LEDDISP(6)	9	10	LEDDISP(7)

Table 4-5. Seven Segment LED Header (Continued)

Signal	Pin	Pin	Signal
LEDDISP(8)	11	12	LEDDISP(9)
LEDDISP(10)	13	14	LEDDISP(11)
LEDDISP(12)	15	16	LEDDISP(13)
LEDDISP(14)	17	18	LEDDISP(15)
LEDBLNK	19	20	GND

Status LEDs and Switches (J13)

Table 4-6. Status LEDs and Switches

Signal	Pin	Pin	Signal
+5PU1	1	2	LAN2_LNK_LED_L
+5PU2	3	4	PCI_IRDY_LED_L
+5PU3	5	6	FAIL_LED_L
+5PU4	7	8	STAT_LED_L
+5PU5	9	10	RUN_LED_L
+5PU6	11	12	LAN1_LNK_LED_L
+5PU7	13	14	NC
NC	15	16	+5 fused
GND	17	18	RESET_SW_L
GND	19	20	ABORT_SW_L
+5PU7	21	22	SPCI_IRDY
+5PU8	23	24	SCSI_BUSY_LED_L

Speaker and Power Status (J19)

Table 4-7. Speaker and Power Status

Signal	Pin	Pin	Signal
Power_LED +	1	2	Speaker +
Not Connected	3	4	NC
Power_LED -	5	6	NC
Not Connected	7	8	Speaker -
Soft Power Switch -	9	10	Soft Power Switch +

Rear Panel Keyboard/Mouse Connectors (J4 lower/J4 upper)

The keyboard and mouse connectors are 6-pin circular DIN connectors located on the rear panel of the MTX. The pin assignments for the

keyboard and mouse connectors are as follows:

Table 4-8. Keyboard Connector Pin Assignments

1	KDATA
2	No Connect
3	GND
4	+5VF
5	KCLK
6	No Connect

Table 4-9. Mouse Connector Pin Assignments

1	MDATA
2	No Connect
3	GND
4	+5VF
5	MCLK
6	No Connect

10 Base-T/100 Base-TxConnector (J2-A/J2-B)

The 10 Base-T/100 Base-Tx Connector is an RJ45 connector located on the rear panel I/O area. The pin assignments for this connector are as follows:

Table 4-10. 10 Base-T/100 Base-Tx Connector Pin Assignments

1	TD+
2	TD-
3	RD+
4	Common Mode Termination
5	Common Mode Termination
6	RD-

Table 4-10. 10 Base-T/100 Base-Tx Connector Pin Assignments (Continued)

7	Common Mode Termination
8	Common Mode Termination

IEEE P1284 Host Mode Parallel I/O Connector (J1)

The host mode parallel I/O connector is a standard IEEE P1284A 25-pin connector located on the rear panel of the ATX motherboard. The pin assignments for this connector are as follows:

Table 4-11. Host Mode Parallel I/O Connector Pin Assignments

1	STROBE_L	AUTOFDXT_L	14
2	DATA_1	FAULT_L	15
3	DATA_2	INIT_L	16
4	DATA_3	SELECT_IN_L	17
5	DATA_4	GND	18
6	DATA_5	GND	19
7	DATA_6	GND	20
8	DATA_7	GND	21
9	DATA_8	GND	22
10	ACK_L	GND	23
11	BUSY	GND	24
12	PAPER_EMPTY	GND	25
13	SELECT_L		

Floppy Disk Header (J15)

Table 4-12. Floppy Disk Header Pin Assignments

Signal	Pin	Pin	Signal
GND	1	2	F_MSEN1
GND	3	4	F_DENSEL
GND	5	6	F_MENS0
GND	7	8	F_INDEX_L
GND	9	10	F_MTR0_L
GND	11	12	F_DR1_L
GND	13	14	F_DR0_L
GND	15	16	F_MTR1_L
GND	17	18	F_DIR_L
GND	19	20	F_STEP_L
GND	21	22	F_WDATA_L
GND	23	24	F_WGATE_L
GND	25	26	F_TRK0_L
GND	27	28	F_WP_L
GND	29	30	F_RDATA_L
GND	31	32	F_HDSEL_L
GND	33	34	F_DSKCHG_L

Serial Port 1 and 2 Connectors (J3 upper/J3 lower)

Planar headers provide the interface to Serial Ports 1 and 2. The pin assignments for these headers is as follows:

Table 4-13. COM1 Header Pin Assignments

1	DCD
2	RXD
3	TXD
4	DTR

Table 4-13. COM1 Header Pin Assignments (Continued)

5	GND
6	DSR
7	RTS
8	CTS
9	RI

Table 4-14. COM2 Header Pin Assignments

1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

Power Connector (J18)

The MTX power connector is a 20-pin connector compatible with the ATX specified Molex Part Number 39-29-9202. Pin assignments are as follows:

Table 4-15. Pin Assignments for Power Connector

Pin #	Signal Name
1	NC
2	NC
3	GND
4	+5.0V
5	GND

Table 4-15. Pin Assignments for Power Connector (Continued)

Pin #	Signal Name
6	+5.0V
7	GND
8	PW-OK
9	NC
10	+12.0V
11	NC
12	-12.0V
13	GND
14	PS-ON
15	GND
16	GND
17	GND
18	NC
19	+5.0V
20	+5.0V

PPCBug Overview

The PPCBug firmware is the layer of software just above the hardware. The firmware provides the proper initialization for the devices on the MTX604-070 motherboard upon power-up or reset.

This chapter describes the basics of PPCBug and its architecture, describes the monitor (interactive command portion of the firmware) in detail, and gives information on actually using the PPCBug debugger and the special commands. A complete list of PPCBug commands appears at the end of the chapter.

Chapter 6, *CNFG and ENV Commands*, contains information about the CNFG and ENV commands. These two commands are used to change Bug Board Information and command parameters interactively.

For full user information about PPCbug, refer to the *PPCBug Firmware Package User's Manual* and the *PPCBug Diagnostics Manual*, listed in Appendix B, *Related Documentation*.

PPCBug Basics

The PowerPC debug firmware, PPCBug, is a powerful evaluation and debugging tool for systems built around the Motorola PowerPC microcomputers. Facilities are available for loading and executing user programs under complete operator control for system evaluation.

PPCBug provides a high degree of functionality, user friendliness, portability, and ease of maintenance.

It achieves good portability and comprehensibility because it was written entirely in the C programming language, except where necessary to use assembler functions.

PPCBug includes commands for:

- Display and modification of memory
- Breakpoint and tracing capabilities
- A powerful assembler and disassembler useful for patching programs
- A self-test at power-up feature which verifies the integrity of the system

PPCBug consists of three parts:

- A command-driven, user-interactive *software debugger*, described in the *PPCBug Firmware Package User's Manual,* listed in Appendix B, *Related Documentation*. It is hereafter referred to as "the debugger" or "PPCBug".
- A command-driven *diagnostics package* for the MTX hardware, hereafter referred to as "the diagnostics." The diagnostics package is described in the *PPCBug Diagnostics Manual.*
- A *user interface* or *debug/diagnostics monitor* that accepts commands from the system console terminal.

When using PPCBug, you operate out of either the *debugger directory* or the *diagnostic directory.*

- If you are in the debugger directory, the debugger prompt `PPC1-Bug>` is displayed and you have all of the debugger commands at your disposal.
- If you are in the diagnostic directory, the diagnostic prompt `PPC1-Diag>` is displayed and you have all of the diagnostic commands at your disposal as well as all of the debugger commands.

Use the **SD** command to switch back and forth between these directories.

Because PPCBug is command-driven, it performs its various operations in response to user commands entered at the keyboard. When you enter a command, PPCBug executes the command, and the prompt reappears. However, if you enter a command that causes execution of user target code (for example, **GO**), then control may or may not return to PPCBug, depending on the outcome of the user program.

Memory Requirements

PPCBug requires a maximum of 768KB of read/write memory (that is, DRAM). The debugger allocates this space from the top of memory. For example, a system containing 64MB ($04000000) of read/write memory will place the PPCBug memory page at locations $03F80000 to $03FFFFFF.

PPCBug Implementation

Physically, PPCBug is contained in two socketed 32-pin PLCC Flash devices that together provide 1MB of storage. The executable code is checksummed at every power-on or reset firmware entry, and the result, which includes a precalculated checksum contained in the Flash devices, is verified against the expected checksum.

MPU, Hardware, and Firmware Initialization

The debugger performs the MPU, hardware, and firmware initialization process. This process occurs each time the MTX604-070 is reset or powered up. The steps below are a high-level outline; not all of the detailed steps are listed.

1. Sets **MPU.MSR** to known value.
2. Invalidates the MPU's data/instruction caches.
3. Clears all segment registers of the MPU.
4. Clears all block address translation registers of the MPU.
5. For the dual processor only, catch one CPU of a dual CPU and place it in a waiting loop.
6. Initializes the MPU-bus-to-PCI-bus bridge device.
7. Initializes the PCI-bus-to-ISA-bus bridge device.
8. Calculate the external bus clock speed of the MPU.

9. Delays for 750 milliseconds.
10. Determines the CPU board type.
11. Sizes the local read/write memory (that is, DRAM).
12. Initializes the read/write memory controller.
13. Sets base address of memory to $00000000.
14. Retrieves the speed of read/write memory from NVRAM.
15. Initializes the read/write memory controller with the speed of read/write memory.
16. Retrieves the speed of read only memory (that is, Flash) from NVRAM.
17. Initializes the read only memory controller with the speed of read only memory.
18. Enables the MPU's instruction cache.
19. Copies the MPU's exception vector table from $FFF00000 to $00000000.
20. Initializes the Super I/O resources base addresses.
21. Verifies MPU type.
22. Enable the super-scalar feature of the MPU (boards with MPC604 type chips only).
23. Initialize the Keyboard Controller Super I/O.
24. Determines the debugger's console/host ports and initializes the appropriate devices (PC16550/GD54*xx*/Z85C230).
25. Displays the debugger's copyright message.
26. Displays any hardware initialization errors that may have occurred.
27. Checksums the debugger object and displays a warning message if the checksum failed to verify.
28. Displays the amount of local read/write memory found.

29. Verifies the configuration data that is resident in NVRAM and displays a warning message if the verification failed.
30. Calculates and displays the MPU clock speed, verifies that the MPU clock speed matches the configuration data, and displays a warning message if the verification fails.
31. Displays the BUS clock speed, verifies that the BUS clock speed matches the configuration data, and displays a warning message if the verification fails.
32. Displays any Keyboard Controller initialization error that occurs.
33. Probes PCI bus for supported network devices.
34. Probes PCI bus for supported mass storage devices.
35. Initializes the memory and I/O addresses for the supported PCI bus devices.
36. Executes Self-Test, if so configured. (Default is no Self-Test.)
37. Extinguishes the board fail LED, if there are no self-test failures or initialization/configuration errors.
38. Executes the configured boot routine, either ROMboot, Autoboot, or Network Autoboot.
39. Executes the user interface (that is, displays the `PPC1-Bug>` or `PPC1-Diag>` prompt).

Using PPCBug

PPCBug is command-driven; it performs its various operations in response to commands that you enter at the keyboard. When the `PPC1-Bug>` prompt appears on the screen, the debugger is ready to accept debugger commands. When the `PPC1-Diag>` prompt appears on the screen, the debugger is ready to accept diagnostics commands. To switch from one mode to the other, enter **SD**.

What you key in is stored in an internal buffer. Execution begins only after you press the **Return** or **Enter** key. This allows you to correct entry errors, if necessary, with the control characters described in Chapter 1 of the *PPCBug Firmware Package User's Manual*, listed in Appendix B, *Related Documentation*.

After the debugger executes the command, the prompt reappears. However, if the command causes execution of user target code (for example, **GO**) then control may or may not return to the debugger, depending on what the user program does. For example, if a breakpoint has been specified, then control returns to the debugger when the breakpoint is encountered during execution of the user program. Alternately, the user program could return to the debugger by means of the System Call Handler routine **RETURN** (described in Chapter 5 of the *PPCBug Firmware Package User's Manual*). For more about this, refer to the **GD**, **GO**, and **GT** command descriptions in Chapter 3 of the *PPCBug Firmware Package User's Manual.*

A debugger command is made up of the following parts:

- The command name, either uppercase or lowercase (for example, **MD** or **md**).
- Any required arguments, as specified by command.
- At least one space before the first argument. Precede all other arguments with either a space or comma.
- One or more options. Precede an option or a string of options with a semicolon (**;**). If no option is entered, the command's default option conditions are used.

Debugger Commands

The individual debugger commands are listed in the following table. The commands are described in detail in Chapter 2 of the *PPCBug Firmware Package User's Manual.*

Note You can list all the available debugger commands by entering the Help (**HE**) command alone. You can view the syntax for a particular command by entering **HE** and the command mnemonic, as listed below.

Table 5-1. Debugger Commands

Command	Description
AS	One Line Assembler
BC	Block of Memory Compare
BF	Block of Memory Fill
BI	Block of Memory Initialize
BM	Block of Memory Move
BR	Breakpoint Insert
NOBR	Breakpoint Delete
BS	Block of Memory Search
BV	Block of Memory Verify
CM	Concurrent Mode
NOCM	No Concurrent Mode
CNFG	Configure Board Information Block
CS	Checksum
CSAR	PCI Configuration Space READ Access
CSAW	PCI Configuration Space WRITE Access
DC	Data Conversion
DMA	Block of Memory Move
DS	One Line Disassembler
DU	Dump S-Records
ECHO	Echo String
ENV	Set Environment
FORK	Fork Idle MPU at Address
FORKWR	Fork Idle MPU with Registers
GD	Go Direct (Ignore Breakpoints)

Table 5-1. Debugger Commands (Continued)

Command	Description
GEVBOOT	Global Environment Variable Boot
GEVDEL	Global Environment Variable Delete
GEVDUMP	Global Environment Variable(s) Dump
GEVEDIT	Global Environment Variable Edit
GEVINIT	Global Environment Variable Initialization
GEVSHOW	Global Environment Variable(s) Display
GN	Go to Next Instruction
GO	Go Execute User Program
GT	Go to Temporary Breakpoint
HE	Help
IDLE	Idle Master MPU
IOC	I/O Control for Disk
IOI	I/O Inquiry
IOP	I/O Physical (Direct Disk Access)
IOT	I/O Teach for Configuring Disk Controller
IRD	Idle MPU Register Display
IRM	Idle MPU Register Modify
IRS	Idle MPU Register Set
LO	Load S-Records from Host
MA	Macro Define/Display
NOMA	Macro Delete
MAE	Macro Edit
MAL	Enable Macro Listing
NOMAL	Disable Macro Listing
MAR	Load Macros
MAW	Save Macros
MD, MDS	Memory Display
MENU	System Menu
MM	Memory Modify

Table 5-1. Debugger Commands (Continued)

Command	Description
MMD	Memory Map Diagnostic
MS	Memory Set
MW	Memory Write
NAB	Automatic Network Boot
NAP	Nap MPU
NBH	Network Boot Operating System, Halt
NBO	Network Boot Operating System
NIOC	Network I/O Control
NIOP	Network I/O Physical
NIOT	Network I/O Teach (Configuration)
NPING	Network Ping
OF	Offset Registers Display/Modify
PA	Printer Attach
NOPA	Printer Detach
PBOOT	Bootstrap Operating System
PF	Port Format
NOPF	Port Detach
PFLASH	Program FLASH Memory
PS	Put RTC into Power Save Mode
RB	ROMboot Enable
NORB	ROMboot Disable
RD	Register Display
REMOTE	Remote
RESET	Cold/Warm Reset
RL	Read Loop
RM	Register Modify
RS	Register Set
RUN	MPU Execution/Status
SD	Switch Directories

Table 5-1. Debugger Commands (Continued)

Command	Description
SET	Set Time and Date
SROM	SROM Examine/Modify
SYM	Symbol Table Attach
NOSYM	Symbol Table Detach
SYMS	Symbol Table Display/Search
T	Trace
TA	Terminal Attach
TIME	Display Time and Date
TM	Transparent Mode
TT	Trace to Temporary Breakpoint
VE	Verify S-Records Against Memory
VER	Revision/Version Display
WL	Write Loop

Caution

Although a command to allow the erasing and reprogramming of Flash memory is available to you, keep in mind that reprogramming any portion of the MTX604-070's Bank B Flash memory (Bank B) will erase everything currently contained in Bank B's Flash memory, including the PPCBug debugger. Reprogramming Bank A Flash Memory, erases the requested amount of bytes adjusted to a 256KB resolution.

Diagnostic Tests

The PPCBug hardware diagnostics are intended for testing and troubleshooting the MTX604-070 module.

In order to use the diagnostics, you must switch to the diagnostic directory. You may switch between directories by using the **SD** (Switch Directories) command. You may view a list of the commands in the directory that you are currently in by using the **HE** (Help) command.

If you are in the debugger directory, the debugger prompt `PPC1-Bug>` displays, and all of the debugger commands are available. Diagnostics commands cannot be entered at the `PPC1-Bug>` prompt.

If you are in the diagnostic directory, the diagnostic prompt `PPC1-Diag>` displays, and all of the debugger and diagnostic commands are available.

Note Not all tests are valid for the MTX604-070. Using the **HE** command, you can list the diagnostic routines available in each test group. Refer to the *PPCBug Diagnostics Manual,* listed in Appendix B, *Related Documentation*, for complete descriptions of the diagnostic routines and instructions on how to invoke them.

Table 5-2. Diagnostic Test Groups

Test Group	Description	Action
CL1283	Parallel Interface (CL1283) Tests	Bypass
DEC	DEC21*x*40 Ethernet Controller Tests	Executes tests
EIDE	IDE/EIDE Device Tests	Bypass
FALCON	Falcon Tests	Executes tests
ISABRDGE	PCI/ISA Bridge Tests	Executes tests
KBD8730X	PC8730x Keyboard/Mouse Tests	Executes tests
L2CACHE	Level 2 Cache Tests	Executes tests
NCR	NCR 53C8xx SCSI2 I/O Processor Tests	Executes tests
PAR8730X	Parallel Interface (PC8730x) Tests	Executes tests
PCIBUS	PCI/PMC Generic Tests	Executes tests
RAM	Local RAM Tests	Executes tests
RAVEN	Raven Tests	Executes tests
RTC	MK48Txx Timekeeping Tests	Executes tests
SCC	Serial Communication Controller (Z85C230) Tests	Bypass
UART	Serial Input/Output Tests	Executes tests

Table 5-2. Diagnostic Test Groups (Continued)

Test Group	Description	Action
VGA54XX	Video Diagnostics Tests	Bypass
VME2	VMEchip2 VME Interface ASIC Tests	Bypass
VME3	VMEchip3 VME Interface ASIC Tests	Bypass
Z8536	Z8536 Counter/Timer Tests	Bypass

Notes You may enter command names in either uppercase or lowercase.

Some diagnostics depend on restart defaults that are set up only in a particular restart mode. Refer to the documentation on a particular diagnostic for the correct mode.

Tests that do not apply to this particular board are automatically bypassed by the firmware.

CNFG and ENV Commands 6

Overview

You can use the factory-installed debug monitor, PPCBug, to modify certain parameters contained in the PowerPC board's Non-Volatile RAM (NVRAM), also known as Battery Backed-up RAM (BBRAM).

- The Board Information Block in NVRAM contains various elements concerning operating parameters of the hardware. Use the PPCBug command **CNFG** to change those parameters.
- Use the PPCBug command **ENV** to change configured PPCBug parameters in NVRAM.

The **CNFG** and **ENV** commands are both described in the *PPCBug Firmware Package User's Manual*, listed in Appendix B, *Related Documentation*. Refer to that manual for general information about their use and capabilities.

The following paragraphs present additional information about **CNFG** and **ENV** that is specific to the PPCBug debugger, along with the parameters that can be configured with the **ENV** command.

CNFG - Configure Board Information Block

Use this command to display and configure the Board Information Block, which is resident within the NVRAM. The board information block contains various elements detailing specific operational parameters of the PowerPC board. The board structure for the PowerPC board is as shown in the following example for an MTX:

```
Board (PWA) Serial Number   = "2717994             "
Board Identifier            = "MTX-60X-0XX         "
Artwork (PWA) Identifier    = "01-w3187F03B        "
MPU Clock Speed             = "200                 "
```

```
Bus Clock Speed             = “067                  ”
Ethernet Address            = “08003E25D0C5         ”
Local SCSI Identifier*      = “07                   ”
System Serial Number        = “1234567              ”
System Identifier           = “Motorola MTX603-001a ”
License Identifier          = “12345678             ”
```

The parameters that are quoted are left-justified character (ASCII) strings padded with space characters, and the quotes (“) are displayed to indicate the size of the string. Parameters that are not quoted are considered data strings, and data strings are right-justified. The data strings are padded with zeroes if the length is not met.

The Board Information Block is factory-configured before shipment. There is no need to modify block parameters unless the NVRAM is corrupted.

Refer to the *Programmer’s Reference Guide*, listed in Appendix B, *Related Documentation*, for the actual location and other information about the Board Information Block.

Refer to the *PPCBug Firmware Package User's Manual* for a description of **CNFG** and examples.

ENV - Set Environment

Use the **ENV** command to view and/or configure interactively all PPCBug operational parameters that are kept in Non-Volatile RAM (NVRAM).

Refer to the *PPCBug Firmware Package User's Manual* for a description of the use of **ENV**.

Listed and described below are the parameters that you can configure using **ENV**. The default values shown were those in effect when this publication went to print.

Configuring the PPCBug Parameters

The parameters that can be configured using **ENV** are:

```
Bug or System environment [B/S] = B?
```

B Bug is the mode where no system type of support is displayed. However, system-related items are still available. (Default)

S System is the standard mode of operation, and is the default mode if NVRAM should fail. System mode is defined in the *PPCBug Firmware Package User's Manual*, listed in Appendix B, *Related Documentation*.


```
Field Service Menu Enable [Y/N] = N?
```

Y Display the field service menu.

N Do not display the field service menu. (Default)

```
Probe System for Supported I/O Controllers [Y/N] = Y?
```

Y Accesses will be made to the appropriate system buses (for example, VMEbus, local MPU bus) to determine the presence of supported controllers. (Default)

N Accesses will not be made to the VMEbus to determine the presence of supported controllers.

```
Auto-Initialize of NVRAM Header Enable [Y/N] = Y?
```

Y NVRAM (PReP partition) header space will be initialized automatically during board initialization, but only if the PReP partition fails a sanity check. (Default)

N NVRAM header space will not be initialized automatically during board initialization.

```
Network PReP-Boot Mode Enable [Y/N] = N?
```

Y Enable PReP-style network booting (same boot image from a network interface as from a mass storage device).

N Do not enable PReP-style network booting. (Default)

```
SCSI Bus Reset on Debugger Startup [Y/N] = N?
```

Y SCSI bus is reset on debugger setup.

N SCSI bus is not reset on debugger setup. (Default)


```
Primary SCSI Bus Negotiations Type [A/S/N] = A?
```

A Asynchronous SCSI bus negotiation. (Default)

S Synchronous SCSI bus negotiation.

N None.

```
Primary SCSI Data Bus Width [W/N] = N?
```

W Wide SCSI (16-bit bus).

N Narrow SCSI (8-bit bus). (Default)

```
Secondary SCSI Identifier = 07?
```

If the board has a secondary SCSI controller, this number is the secondary SCSI ID or address. For the MTX604-070 all PCI add-on SCSI controllers/adaptors supported by PPCBug are set to the SCSI ID value entered here.

```
NVRAM Bootlist (GEV.fw-boot-path) Boot Enable [Y/N] = N?
```

Y Give boot priority to devices defined in the **fw-boot-path** global environment variable (GEV).

N Do not give boot priority to devices listed in the **fw-boot-path** GEV. (Default)

Note When enabled, the GEV (Global Environment Variable) boot takes priority over all other boots, including Autoboot and Network Boot.

```
NVRAM Bootlist (GEV.fw-boot-path) Boot at power-up only [Y/N] = N?
```

Y Give boot priority to devices defined in the **fw-boot-path** GEV at power-up reset only.

N Give power-up boot priority to devices listed in the **fw-boot-path** GEV at any reset. (Default)

```
NVRAM Bootlist (GEV.fw-boot-path) Boot Abort Delay = 5?
```

The time in seconds that a boot from the NVRAM boot list will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
Auto Boot Enable [Y/N]   = N?
```

Y The Autoboot function is enabled.

N The Autoboot function is disabled. (Default)

```
Auto Boot at power-up only [Y/N] = N?
```

Y Autoboot is attempted at power-up reset only.

N Autoboot is attempted at any reset. (Default)

```
Auto Boot Scan Enable [Y/N]   = Y?
```

Y If Autoboot is enabled, the Autoboot process attempts to boot from devices specified in the scan list (for example, FDISK/CDROM/TAPE/HDISK). (Default)

N If Autoboot is enabled, the Autoboot process uses the Controller LUN and Device LUN to boot.

```
Auto Boot Scan Device Type List = FDISK/CDROM/TAPE/HDISK?
```

This is the listing of boot devices displayed if the Autoboot Scan option is enabled. If you modify the list, follow the format shown above (uppercase letters, using forward slash as separator).

```
Auto Boot Controller LUN   = 00?
```

Refer to the *PPCBug Firmware Package User's Manual*, listed in Appendix B, *Related Documentation*, for a listing of disk/tape controller modules currently supported by PPCBug. (Default = $00)

```
Auto Boot Device LUN    = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of disk/tape devices currently supported by PPCBug. (Default = $00)


```
Auto Boot Partition Number = 00?
```

Which disk "partition" is to be booted, as specified in the PowerPC Reference Platform (PRP) specification. If set to zero, the firmware will search the partitions in order (1, 2, 3, 4) until it finds the first "bootable" partition. That is then the partition that will be booted. Other acceptable values are 1, 2, 3, or 4. In these four cases, the partition specified will be booted without searching.

```
Auto Boot Abort Delay = 7?
```

The time in seconds that the Autoboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 7 seconds)

```
Auto Boot Default String [NULL for an empty string] =?
```

You may specify a string (filename) which is passed on to the code being booted. The maximum length of this string is 16 characters. (Default = null string)

```
ROM Boot Enable [Y/N] = N?
```

Y	The ROMboot function is enabled.
N	The ROMboot function is disabled. (Default)

```
ROM Boot at power-up only [Y/N] = Y?
```

Y ROMboot is attempted at power-up only. (Default)

N ROMboot is attempted at any reset.

```
ROM Boot Abort Delay = 5?
```

The time in seconds that the ROMboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
ROM Boot Direct Starting Address = FFF00000?
```

The first location tested when PPCBug searches for a ROMboot module. (Default = $FFF00000)

```
ROM Boot Direct Ending Address = FFFFFFFC?
```

The last location tested when PPCBug searches for a ROMboot module. (Default = $FFFFFFFC)

```
Network Auto Boot Enable [Y/N] = N?
```

Y The Network Auto Boot (NETboot) function is enabled.

N The NETboot function is disabled. (Default)

```
Network Auto Boot at power-up only [Y/N] = N?
```

Y NETboot is attempted at power-up reset only.

N NETboot is attempted at any reset. (Default)

```
Network Auto Boot Controller LUN = 00?
```

Refer to the *PPCBug Firmware Package User's Manual*, listed in Appendix B, *Related Documentation*, for a listing of network controller modules currently supported by PPCBug. (Default = $00)

```
Network Auto Boot Device LUN = 00?
```

Refer to the *PPCBug Firmware Package User's Manual*, listed in Appendix B, *Related Documentation*, for a listing of network controller modules currently supported by PPCBug. (Default = $00)

```
Network Auto Boot Abort Delay = 5?
```

The time in seconds that the NETboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
Network Auto Boot Configuration Parameters Offset (NVRAM) =
00001000?
```


The address where the network interface configuration parameters are to be saved/retained in NVRAM; these parameters are the necessary parameters to perform an unattended network boot. A typical offset might be $1000, but this value is application-specific. (Default = $00001000)

Caution

If you use the **NIOT** debugger command, these parameters need to be saved somewhere in the offset range $00001000 through $000016F7. The **NIOT** parameters do not exceed 128 bytes in size. The setting of this ENV pointer determines their location. If you have used the same space for your own program information or commands, they will be overwritten and lost.

You can relocate the network interface configuration parameters in this space by using the **ENV** command to change the Network Auto Boot Configuration Parameters Offset from its default of $00001000 to the value you need to be clear of your data within NVRAM.

```
Memory Size Enable [Y/N] = Y?
```

Y Memory will be sized for Self Test diagnostics. (Default)

N Memory will not be sized for Self Test diagnostics.

```
Memory Size Starting Address = 00000000?
```

The default Starting Address is $00000000.

```
Memory Size Ending Address = 02000000?
```

The default Ending Address is the calculated size of local memory. If the memory start is changed from $00000000, this value will also need to be adjusted.

```
DRAM Speed in NANO Seconds = 60?
```

The default setting for this parameter will vary depending on the speed of the DRAM memory parts installed on the board. The default is set to the slowest speed found on the available banks of DRAM memory.


```
ROM First Access Length (0 - 31) = 10?
```

This is the value programmed into the MPC105 **ROMFAL** field (Memory Control Configuration Register 8: bits 23-27) to indicate the number of clock cycles used in accessing the ROM. The lowest allowable **ROMFAL** setting is $00; the highest allowable is $1F. The value to enter depends on processor speed; refer to your *Processor/Memory Mezzanine Module User's Manual* for appropriate values. The default value varies according to the system's bus clock speed.

Note ROM First Access Length is not applicable to the MTX604-070. The configured value is ignored by PPCBug.

```
ROM Next Access Length (0 - 15) = 0?
```

The value programmed into the MPC105 **ROMNAL** field (Memory Control Configuration Register 8: bits 28-31) to represent wait states in access time for nibble (or burst) mode ROM accesses. The lowest allowable **ROMNAL** setting is $0; the highest allowable is $F. The value to enter depends on processor speed; refer to your *Processor/Memory Mezzanine Module User's Manual*, listed in *Appendix B, Related Documentation*, for appropriate values. The default value varies according to the system's bus clock speed.

Note ROM Next Access Length is not applicable to the MTX604-070. The configured value is ignored by PPCBug.

```
DRAM Parity Enable [On-Detection/Always/Never - O/A/N] = 0?
```

O DRAM parity is enabled upon detection. (Default)

A DRAM parity is always enabled.

N DRAM parity is never enabled

Note This parameter (above) also applies to enabling ECC for DRAM.

```
L2 Cache Parity Enable [On-Detection/Always/Never - O/A/N] = O?
```

O L2 Cache parity is enabled upon detection. (Default)

A L2 Cache parity is always enabled.

N L2 Cache parity is never enabled

```
PCI Interrupts Route Control Registers (PIRQ0/1/2/3) = 0A0B0E0F?
```

Initializes the PIRQ*x* (PCI Interrupts) route control registers in the IBC (PCI/ISA bus bridge controller). The **ENV** parameter is a 32-bit value that is divided by 4 to yield the values for route control registers PIRQ0/1/2/3. The default is determined by system type. For details on PCI/ISA interrupt assignments and for suggested values to enter for this parameter, refer to the *8259 Interrupts* section of Chapter 4 in the *MTX PCI Series Motherboard Programmer's Reference Guide,* listed in Appendix B, *Related Documentation*.

```
Serial Startup Code Master Enable [Y/N]=N?
```

The Serial Startup Codes can be displayed at key points in the initialization of the hardware devices. Should the debugger fail to come up to a prompt, the last code displayed will indicate how far the initialization sequence had progressed before stalling. The codes are enabled by an **ENV** parameter.

```
Serial Startup Code LF Enable [Y/N]=N?
```

A line feed can be inserted after each code is displayed to prevent it from being overwritten by the next code. This is also enabled by an **ENV** parameter.

A list of LED/serial codes is included in the section on MPU, Hardware, and Firmware Initialization in Chapter 1 of the *PPCBug Firmware Package User's Manual, Part 1*, listed in Appendix B, *Related Documentation*.

Specifications

Table A-1 lists the Power Requirements for the MTX604-070 motherboard. Mechanical specifications conform to those of the current ATX form factor specification, revision 1.1, (12.0 in width x 9.6 in length x 1.25 in height (excluding PCI card). Subsequent sections detail cooling requirements and I/O Panel Dimensions.

Specifications for related components, peripherals and networks can be ordered from the sources listed in Appendix B, *Related Documentation*.

Table A-1. MTX604-070 Power Requirements

Configuration	Specifications All With +5V Power
200 MHz 603e	5.5A typical 7A maximum
333 MHz 604e	6.5A typical 8A maximum
Dual 333 MHz 604e	8A typical 10A maximum

Cooling Requirements

The Motorola MTX604-070 family of Single Board Computers is specified, designed, and tested to operate reliably with an incoming air temperature range from 0° to +55° C (0° to 131° F). Minimum airflow requirements (across the heatsink) are 25 LFM for a single processor motherboard and 125 LFM for a dual processor motherboard. Temperature qualification was performed in a standard Motorola ATX chassis.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 10 CFM

and 125 LFM (for dual processor), or 10 CFM and 25 LFM (for single processor) flowing across the heatsink. Less airflow is required to cool the motherboard in environments having lower maximum ambients. Under more favorable thermal conditions, it may be possible to operate the motherboard reliably at higher than 55° C with increased airflow. It is important to note that there are several factors, in addition to the rated CFM and/or LFM of the air mover, which determine the actual volume and speed of air flowing over a module.

Other Environmental Requirements

The system meets all other standard environmental specifications including operating altitude up to 5,000 meters, humidity (NC) operating range of 10% to 80%, and a vibration tolerance of 2 Gs RMS, 20-2000 Hz Random.

I/O Panel Dimensions

The following figure details the current I/O panel dimensions for this version of the MTX motherboard.

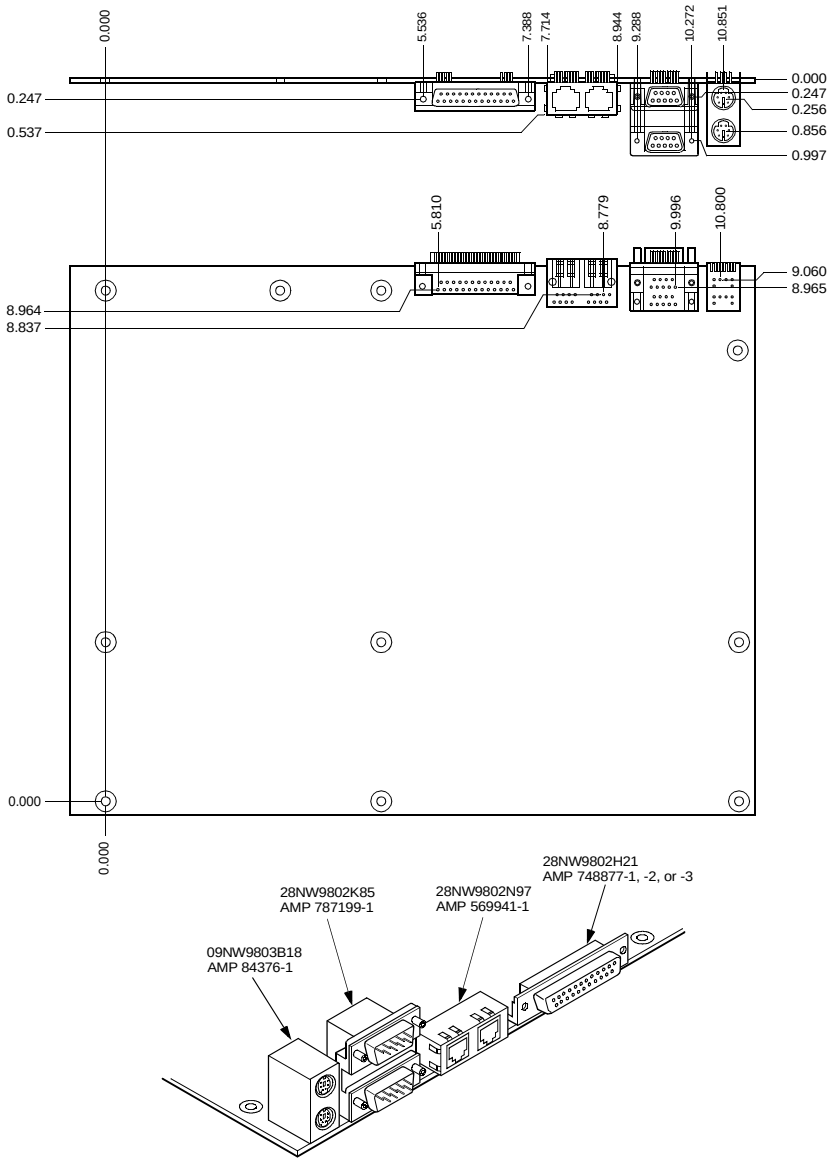


Figure 6-1. I/O Panel Dimensions

Related Documentation B

Motorola Computer Group Documents

The Motorola publications listed below are referenced in this manual. You can obtain paper or electronic copies of Motorola Computer Group publications by:

- Contacting your local Motorola sales office
- Visiting Motorola Computer Group's World Wide Web literature site, http://www.motorola.com/computer/literature

Table B-1. Motorola Computer Group Documents

Document Title	Publication Number
MTX PCI Series Motherboard Programmer's Reference Guide	MTXPCIA/PG
PPCBug Firmware Package User's Manual (Parts 1 and 2)	PPCBUGA1/UM PPCBUGA2/UM
PPCBug Diagnostics Manual	PPCDIAA/UM

- To obtain the most up-to-date product information in PDF or HTML format, visit http://www.motorola.com/computer/literature.

B

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-2. Manufacturers' Documents

Document Title and Source	Publication Number
PowerPC 603™ RISC Microprocessor Technical Summary Literature Distribution Center for Motorola Semiconductor Products Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com	MPC603/D
PowerPC 603™ RISC Microprocessor User's Manual Literature Distribution Center for Motorola Semiconductor Products Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com OR	MPC603UM/AD
IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPR603UMU-01

Table B-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
PowerPC 604™ RISC Microprocessor User's Manual Literature Distribution Center for Motorola Semiconductor Products Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPC604UM/AD MPR604UMU-01
PowerPC™ Microprocessor Family: The Programming Environments Literature Distribution Center for Motorola Semiconductor Products Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPCFPE/AD MPRPPCFPE-01

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Table B-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
MPC2605GA Integrated Secondary Cache for PowerPC Microprocessors Data Sheet Literature Distribution Center for Motorola Semiconductor Products Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com	MPC2605GA
DECchip 21143 PCI Fast Ethernet LAN Controller Hardware Reference Manual Digital Equipment Corporation Maynard, Massachusetts DECchip Information Line Telephone (United States and Canada): 1-800-332-2717 TTY (United States only): 1-800-332-2515 Telephone (outside North America): +1-508-568-6868	EC-QC0CA-TE
PC87308VUL (Super I/O™ Enhanced Sidewinder Lite) Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, IEEE 1284 Parallel Port, and IDE Interface National Semiconductor Corporation Customer Support Center (or nearest Sales Office) 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, California 95052-8090 Telephone: 1-800-272-9959	PC87308VUL
MK48T559 CMOS 8K x 8 TIMEKEEPER™ SRAM Data Sheet SGS-Thomson Microelectronics Group Marketing Headquarters (or nearest Sales Office) 1000 East Bell Road Phoenix, Arizona 85022 Telephone: (602) 867-6100	M48T559

Table B-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
SYM 53CXX (was NCR 53C8XX) Family PCI-SCSI I/O Processors Programming Guide Symbios Logic Inc. 1731 Technology Drive, Suite 600 San Jose, California 95110 Telephone: (408) 441-1080 Hotline: 1-800-334-5454	J10931I
W83C554 Enhanced System I/O Controller with PCI Arbiter (PIB) Winbond Electronics Corporation Winbond Systems Laboratory 2730 Orchard Parkway San Jose, CA 95134 Telephone: 1-408-943-6666 FAX: 1-408-943-6668	W83C554
DECchip 21554 PCI-to-PCI Bridge for Embedded Applications Data Sheet Digital Equipment Corporation Maynard, Massachusetts DECchip Information Line Telephone (United States and Canada): 1-800-332-2717 TTY (United States only): 1-800-332-2515 Telephone (outside North America): +1-508-568-6868	EC-R7BMA-TE

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Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-3. Related Specifications

Document Title and Source	Publication Number
ANSI Small Computer System Interface-2 (SCSI-2), Draft Document Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 Telephone: (303) 792-2181	X3.131.1990
Bidirectional Parallel Port Interface Specification Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE Standard 1284
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.1 PCI Special Interest Group 2575 NE Kathryn St #17 Hillsboro, OR 97124 Telephone: (800) 433-5177 (inside the U.S.) or (503) 693-6232 (outside the U.S.) FAX: (503) 693-8344	PCI Local Bus Specification

Table B-3. Related Specifications (Continued)

Document Title and Source	Publication Number
PowerPC™ Microprocessor Common Hardware Reference Platform: A System Architecture (CHRP), Version 1.0 Literature Distribution Center for Motorola Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com OR APDA, Apple Computer, Inc. P.O. Box 319 Buffalo, NY 14207 Telephone: (800) 282-2732 FAX: (716) 871-6511 OR IBM 1580 Route 52, Bldg. 504 Hopewell Junction, NY 12533-6531 Telephone: (800) PowerPC OR Morgan Kaufmann Publishers, Inc. 340 Pine Street, Sixth Floor San Francisco, CA 94104-3205, USA Telephone: (415) 392-2665 FAX: (415) 982-2665	TB338/D MPRPPCHRP-01 ISBN 1-55860-394-8
PowerPC Reference Platform (PRP) Specification, Third Edition, Version 1.0, Volumes I and II International Business Machines Corporation Power Personal Systems Architecture 11400 Burnet Rd. Austin, TX 78758-3493 Document/Specification Ordering Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 Telephone: 708-296-9332	MPR-PPC-RPU-02

Table B-3. Related Specifications (Continued)

Document Title and Source	Publication Number
IEEE Standard for Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE 802.3
Information Technology - Local and Metropolitan Networks - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 Telephone: (303) 792-2181 *(This document can also be obtained through the national standards body of member countries.)*	ISO/IEC 8802-3
Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange (EIA-232-D) Electronic Industries Association Engineering Department 2001 Eye Street, N.W. Washington, D.C. 20006	ANSI/EIA-232-D Standard

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