Trio64V+ Integrated Graphics/Video Accelerator

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- S3 Scenic Highway for direct interface to live video and MPEG-1 peripherals

S3 Trio64-compatible Mode Option

S3 Streams Processor Features

- Supports on-the-fly stretching and blending of primary RGB stream and RGB or YUV (video) secondary stream
- Each stream can have different color depths
- YUV data is color space converted

Advanced Playback Capabilities

- High-quality hardware-assisted video playback (up to 1024x768x16 bits/pixel)
- Support for India, Cinepak, and software-accelerated MPEG-1 video playback

Game and Presentation Effects.

- Hardware double-buffering support for high-quality tear-free playback
- 2-D scrolling and sprite plane support
- Color and chroma keying for overlaying of graphics onto video and video onto graphics
- Arithmetic blending of two pixel streams for fade-in/fade-out transition effects

S3 Scenic Highway Interface

- Philips SAA7110/SAA7111 video digitizers
- S3 Scenic/MX2 MPEG-1 audio/video decoder

High Non-Interlaced Screen Resolution Support

- 1280x1024x256 colors at 75 Hz refresh
- 1024x768x64K colors at 75 Hz refresh
- 800x600x16.7M colors at 75 Hz refresh

High-Performance Memory Interface

- 64-bit DRAM memory interface
- Supports 1-, 2-, or 4-MByte frame buffer
- Supports standard fast page mode and EDO DRAMs (60 MHz) and 1-cycle EDO DRAMs (50 MHz)

Supports CPUs with Big or Little Endian Byte Ordering

Industry-Standard Local Bus Support

- Glueless PCI bus support (fully compliant with Revision 2.0)
- Glueless VESA® VL-Bus support

Multimedia Support Hooks

- Glueless 16-bit VESA Advanced Feature Connector (VAFC)
- 8-bit bidirectional feature connector
- S3 Scenic Highway
- I^2C bus

Full Software Support

- Drivers for Windows® 3.11, Windows® NT, Windows® 95, OS/2® 2.1 and 3.0 (Warp™), SCO®UNIX®

Green PC/Monitor Plug and Play Support

- Full hardware and BIOS support for VESA Display Power Management Signaling (DPMS) monitor power savings modes
- DDC monitor communications support

Extensive Static/Dynamic Power Management

Industry-Standard 208-pin PQFP package

1.1 OVERVIEW

The S3® Trio64V+™ integrated graphics/video accelerator (hereinafter referred to as the Trio64V+) combines high-performance graphics and high-quality video acceleration features with the capability to directly interface to live video and MPEG-1 peripherals. It incorporates an enhanced version of the 64-bit graphics accelerator core and high-performance 135 MHz true-color RAMDAC that are found in S3's Trio64™ accelerator. All display applications that require high-quality video playback (from a CD-ROM or hard drive), or live video input capability, can take advantage of the Trio64V+'s new features. The Trio64V+ accelerates and enhances software MPEG-1/Indeo™ /Cinepak™ video playback by providing arbitrary scaling with high-quality linear interpolation and color space conversion (RGB to YUV). By performing these tasks in hardware and relieving the CPU of a substantial overhead, the Trio64V+ offers high-quality video playback with window sizes of up to 1024x768x16 bits/pixel at high frame rates. The Trio64V+ has an S3 Scenic Highway™ interface that provides a direct interface to MPEG-1 audio/video decoder devices and live video digitizers to attain full-motion video.

1.2 S3 STREAMS PROCESSOR

The S3 Streams Processor™ allows the mixing of three separate display streams. The primary stream can be RGB data of any color depth. The secondary stream can be RGB or YUV (video) data of any color depth. YUV data is color space converted to RGB. The third stream, the hardware cursor, overlays the other two streams.

Arithmetic blending of a primary graphics stream and secondary graphics/video enables dramatic transition effects for game applications. Color and chroma keying allow opaque or transparent overlays of one stream on the other. Hardware-assisted double buffering of both primary and secondary data streams is also provided to enable high-quality "tear-free" playback.

The Trio64V+ also enhances game acceleration, with support for a sprite plane where sprites are actually rendered into a sprite plane memory. Sprites can be overlaid onto the background without saving and restoring the background.

The Streams Processor is located in the pixel datapath between the display memory and the RAMDAC that drives the RGB signals to the monitor. One of the key advantages of this architecture is that it permits processing of pixel streams on the fly at display refresh rates. This eliminates the need to first write back processed (scaled or color-space-converted) data into the frame buffer before sending it to the RAMDAC. This saves memory storage and memory bandwidth.

The Streams Processor also enables simultaneous display of graphics and video of different color depths. For example, it is possible to display 24 bits/pixel-equivalent video on top of an 8-bit graphics background. This also saves memory bandwidth and storage capacity while permitting higher frame rates because of reduced bandwidth requirements.

In addition, if an opaque rectangular window of one stream is overlaid onto another background window of a second stream, it is not necessary

to fetch and refresh the hidden pixels. This provides additional memory bandwidth savings.

1.3 S3 SCENIC HIGHWAY

The S3 Scenic Highway™ interface directly connects to the S3 Scenic/MX2™ MPEG-1 audio/video decoder as well as video digitizers such as the Philips® 7110/7111. This provides easy implementation of MPEG-1 or digital video daughtercards that directly plug into the Scenic Highway connector or, alternately, ISA cards, where a ribbon cable is also necessary.

The Streams Processor and Scenic Highway are tightly coupled to provide optimal live video playback. The hardware automatically switches capture and display buffers without software intervention.

1.4 Trio64V+ CHANGES FROM THE Trio64

The Trio64V+ comes in two configurations, selectable by power-on strapping.

- Compatible Mode (compatibility with Trio64)
- Local Peripheral Bus (LPB) Mode

In compatible mode, the Trio64V+ can be installed in a Trio64 socket. Some software modifications are required to operate the chip. The pinout changes significantly for LPB mode. This means that compatible mode and LPB mode are not compatible. That is, a given design must be based one or the other. Once the chip is enabled in one mode, it must not be switched to the other.

This data book describes only how the Trio64V+ operates in LPB mode. In compatible mode, the physical and functional characteristics of the Trio64V+ are the same as described for the Trio64 in the *Trio32/Trio64 Graphics Accelerators Data Book* (DB014-A).

A major functional difference available in either mode is the S3 Streams Processor described earlier in this section. In addition to the Streams Processor, the following new features are provided in either compatible or LPB mode:

- All registers addresses relocatable for plug and play support
- Big and little endian addressing support (PowerPC™ /Intel®)
- 50 MHz single-cycle EDO memory support
- Power down input signal to power down the DAC RGB output
- Packed 24 bits/pixel (unaccelerated) mode
- Pass-through mode allowing decimation of 32-bit CPU writes to the frame buffer

The following new features are provided only in LPB mode:

- Bi-directional Scenic/MX2 Scenic Highway interface in either VL-Bus™ or PCI bus configuration
- In PCI configurations, input only or bi-directional CL-480 Scenic Highway interface
- In PCI configurations, 16-bit digitizer data Scenic Highway interface
- Serial Communications Port (I^2C and DDC2 monitor communications)
- Serial port can optionally be accessed via I/O ports E2 or E8 to allow use when the Trio64V+ is disabled
- 8-bit bi-directional (VL-Bus or PCI) or 16-bit VAFC (PCI bus) feature connector support that is not restricted to 1-MByte video modes as with the Trio64 and which requires no external glue logic
- Support for 4 MBytes of EDO memory in PCI configurations
- General Input/Output Port support via the LPB data bus

The following Trio64 features are not available in LPB mode:

- Genlocking
- Shared frame buffer support
- Direct decoding of the VL-Bus SA[31:23] lines. Two SAUP inputs provide indirect decoding via external logic
- 4 MBytes of fast page memory in VL-Bus configurations

Section 2: Mechanical Data

2.1 THERMAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
Thermal Resistance Θ_{JC}		5		°C/W
Thermal Resistance Θ_{JA} (Still Air)		24		°C/W
Junction Temperature			125	°C

2.2 MECHANICAL DIMENSIONS

The Trio64V+ comes in a 208-pin PQFP package. The mechanical dimensions are given in Figure 2-1.

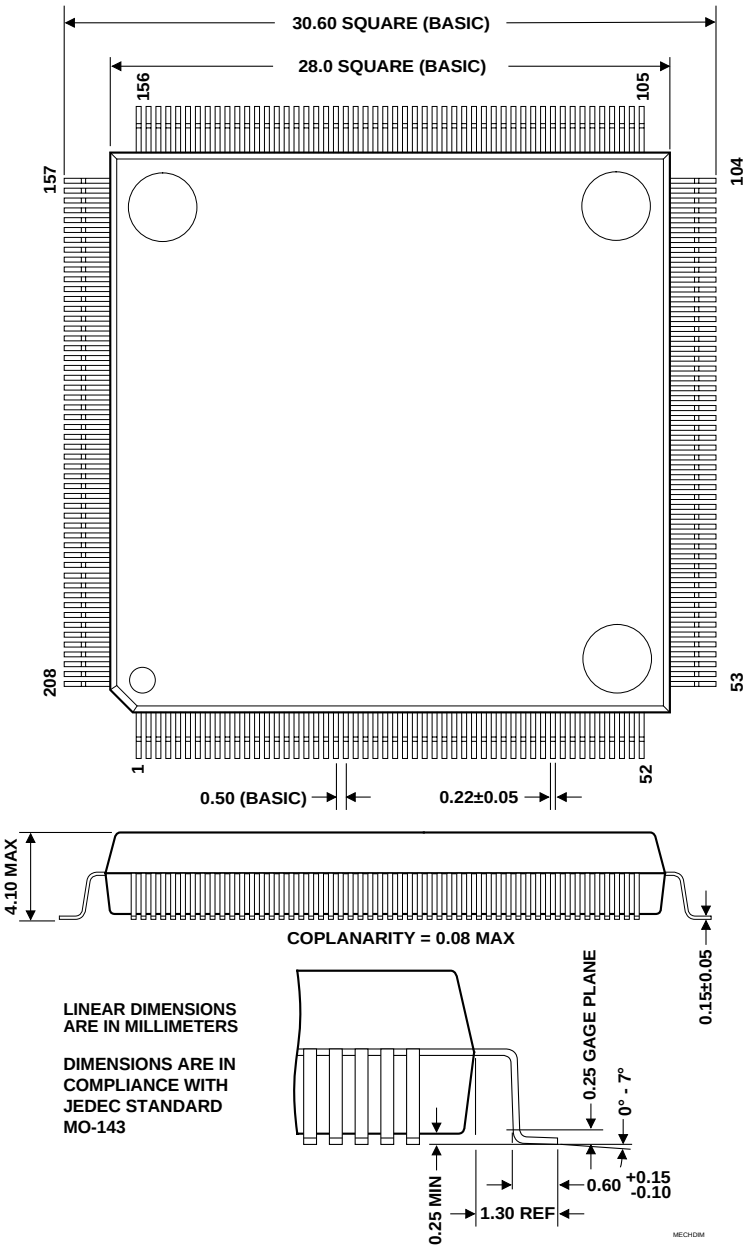


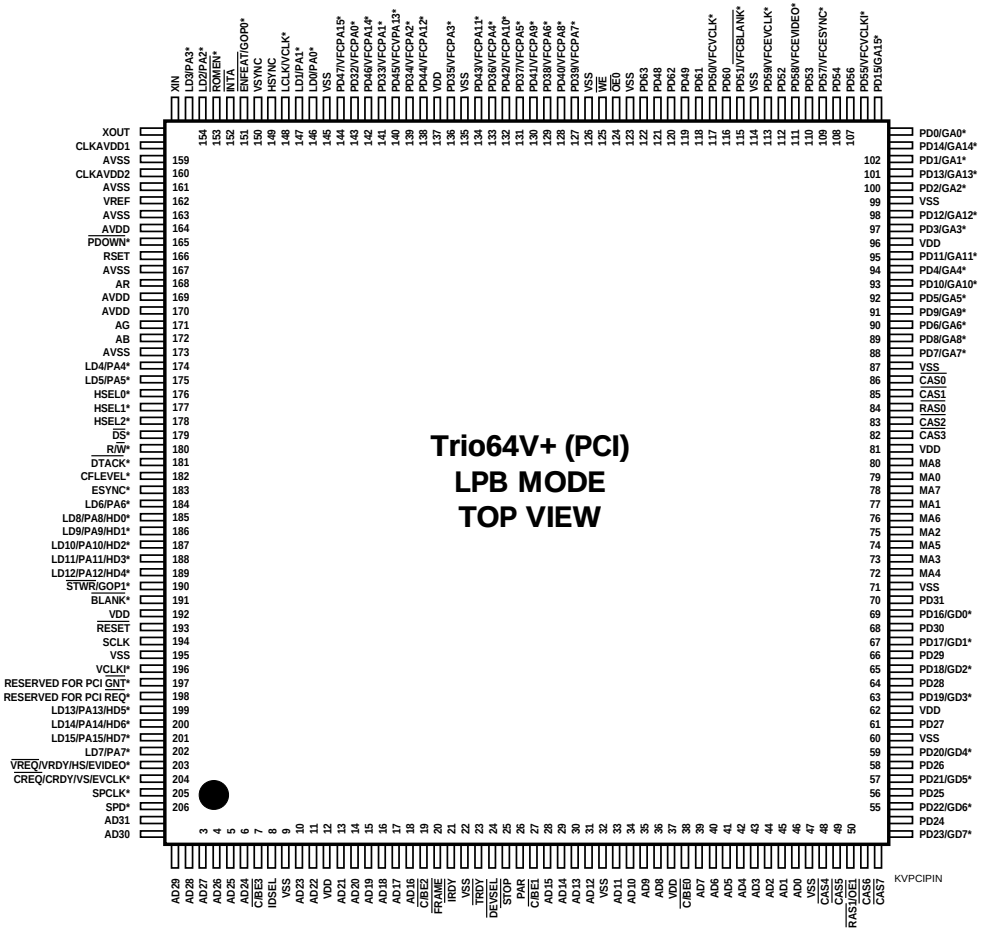
Figure 2-1. 208-pin PQFP Mechanical Dimensions

Section 3: Pins

3.1 PINOUT DIAGRAMS

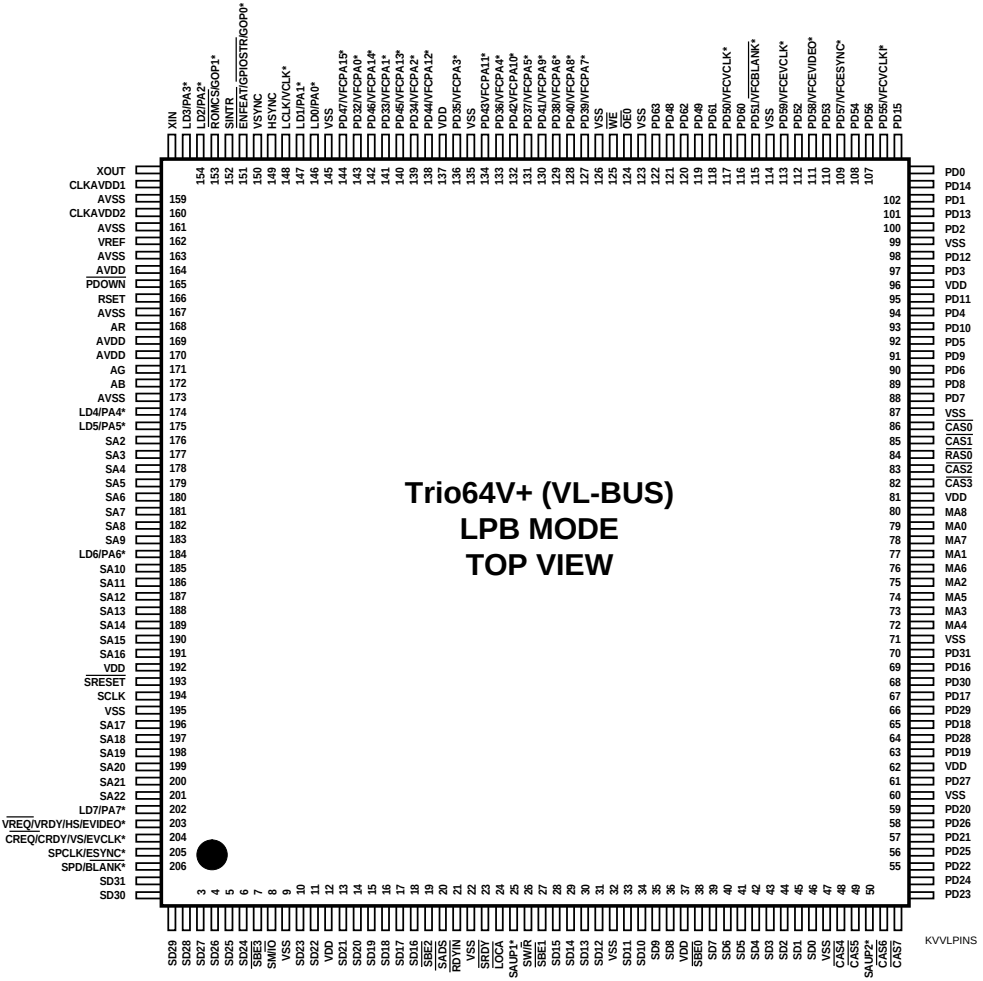
The Trio64V+ comes in a 208-pin PQFP package. It has two primary operating modes with significantly different pin definitions. These modes are selected according to the strapping of the PD24 pin at power-on reset.

If PD24 is strapped low at reset, the Trio64V+ powers up in Local Peripheral Bus (LPB) mode. This mode is not pin compatible with the Trio64 but offers additional functions. The pinout for this mode for a PCI configuration is shown in Figure 3-1. The pinout for this mode for a VL-Bus configuration is shown in Figure 3-2.



*** = Pin functions changed from Compatible Mode**

Figure 3-1. Trio64V+ PCI Bus Pinout - LPB Mode



*** = Pin functions changed from the definition for Compatible Mode**

Figure 3-2. Trio64V+ VL-Bus Pinout - LPB Mode

3.2 PIN DESCRIPTIONS

The following table provides a brief description of each pin on the Trio64V+ for its PCI bus and VL-Bus configurations in LPB mode. The following abbreviations are used for pin types.

I - Input signal
O - Output signal
B - Bidirectional signal

Some pins have multiple names. This either reflects the different functions performed by those pins depending on the bus configuration selected by power-on-strapping or multiplexed pins whose functions are selected via a register bit setting. The pin definitions and functions are given for each possible case.

Table 3-1. Pin Descriptions - LPB Mode

Symbol	Type	Pin Number(s)	Description
BUS INTERFACES			
Address and Data			
AD[31:0]	B	207-208, 1-6, 10-11, 13-18, 28-31, 33-36, 39-46	(PCI) Multiplexed Address/Data Bus. A bus transaction (cycle) consists of an address phase followed by one or more data phases.
SD[31:0]	B		(VL) System Data Bus.
SA[22:2]	I	201-196, 191-185, 183-176	(VL) System Address Bus Lines 22:2.
SAUP1 (VL)	I	25	(VL) Upper Address Decode 1. In conjunction with SAUP2 this input tells the Trio64V+ when to respond when its memory/register address space has been relocated above 4 MBytes. Specifically, SAUP1 = 0, SAUP2 = 1 - register/port address access SAUP1 = 1, SAUP2 = 0 - video memory access The other two combinations are ignored.
SAUP2 (VL)	I	50	(VL) Upper Address Decode 2. See definition for SAUP1.
C/BE[3:0]	I	7, 19, 27, 38	(PCI) Bus Command/Data Byte Enables. These signals carry the bus command during the address phase and the byte enables during the data phase.
SBE[3:0]			(VL) Data Byte Enables.
Bus Control			
SCLK	I	194	(PCI) PCI System Clock.
SCLK	I		(VL) CPU System Clock
INTA	O	152	(PCI) Interrupt Request.
SINTR			(VL) Interrupt Request.

Table 3-1. Pin Descriptions - LPB Mode (Continued)

Symbol	Type	Pin Number(s)	Description
IRDY ~~RDYIN~~	I	21	(PCI) Initiator Ready. A bus data phase is completed when both IRDY and TRDY are asserted on the same cycle. (VL) Local Bus Cycle End Acknowledge. The Trio64V+ holds read data valid on the system data bus until this input is asserted.
TRDY SRDY	O	23	(PCI) Target Ready. A bus data phase is completed when both IRDY and TRDY are asserted on the same cycle. (VL) Local Bus Cycle End.
DEVSEL LOCA	O	24	(PCI) Device Select. The Trio64V+ drives this signal active when it decodes its address as the target of the current access. (VL) Local Bus Access Cycle Indicator. This signal is output during local bus cycles to allow system logic chip sets to prevent concurrent EISA/ISA cycle generation.
IDSEL SM/IO	I I	8	(PCI) Initialization Device Select. This input is the chip select for PCI configuration register reads/writes. (VL) Memory/I/O Cycle Indicator. This signal is high for a memory cycle and low for an I/O cycle.
RESET SRESET	I	193	(PCI) System Reset. Asserting this signal forces the registers and state machines to a known state. (VL) System Reset.
FRAME SADS	I	20	(PCI) Cycle Frame. This signal is asserted by the bus master to indicate the beginning of a bus transaction. It is deasserted during the final data phase of a bus transaction. (VL) System Address Strobe.
PAR SW/R	O I	26	(PCI) Parity. The Trio64V+ asserts this signal to verify even parity during reads. (VL) Write/Read Cycle Indicator. This signal is high for a write and low for a read.

Table 3-1. Pin Descriptions - LPB Mode (Continued)

Symbol	Type	Pin Number(s)	Description
STOP	O	25	(PCI) Stop. The Trio64V+ asserts this signal to indicate a target disconnect.
SAUP1			(VL) Upper Address Decode 1. In conjunction with SAUP2 this input tells the Trio64V+ when to respond when its memory/register address space has been relocated above 4 MBytes. Specifically, SAUP1 = 0, SAUP2 = 1 - register/port address access SAUP1 = 1, SAUP2 = 0 - video memory access The other two combinations are ignored.
CLOCK CONTROL			
XIN	I	156	Reference Frequency Input. If an external crystal is used, it is connected between XOUT and this pin. A stable external frequency source can also be input via this pin. If PD11 is strapped low at power-on, this becomes the DCLK (dot clock) input, bypassing the internal oscillator. This is normally only used for test purposes.
XOUT	O	157	Crystal Output. If an external 14.318 MHz crystal is used, it is connected between XIN and this pin. This pin drives the crystal via an internal oscillator.
DISPLAY MEMORY INTERFACE			
Address and Data			
MA[8:0]	O	80, 78, 76, 74, 72, 73, 75, 77, 79	Memory Address Bus. The video memory row and column addresses are multiplexed on these lines.
PD[63:32]	B	122, 120, 118, 116, 113, 111, 109, 107, 106, 108, 110, 112, 115, 117, 119, 121, 144, 142, 140, 138, 134, 132, 130, 128, 127, 129, 131, 133, 136, 139, 141, 143	Display Memory Pixel Data Bus Lines 63:32. Certain of these pins are enabled for feature connector operation when bit 0 of SRD is set to 1 and bit 1 of SRD is cleared to 0.
PD[31:0]	B	70, 68, 66, 64, 61, 58, 56, 54, 53, 55, 57, 59, 63, 65, 67, 69, 105, 103, 101, 98, 95, 93, 91, 89, 88, 90, 92, 94, 97, 100, 102, 104	Display Memory Pixel Data Bus Lines 31:0. PD[28:0] are also used as the system configuration strapping bits, providing system configuration and setup information upon power-on or reset. After reset, the General Data Bus signals are multiplexed on 24 of these pins.

Table 3-1. Pin Descriptions - LPB Mode (Continued)

Symbol	Type	Pin Number(s)	Description
Memory Control			
RAS[1:0]	O	50, 84	Row Address Strobes. RAS1 is output on pin 50 when bit 6 of SRA is set to 1 for a PCI configuration. RAS1 is used to select the upper 2 MBytes of a 4-MByte memory configuration. It is not available for LPB VL-Bus configurations, limiting memory to 2 MBytes.
CAS[7:4]	O	52, 51, 49, 48	Column Address Strobe Lines 7:4]. These signals are not driven when the Trio64-compatible feature connector is enabled by setting bit 0 of SRD to 1 and bit 1 of SRD to 0. This prevents contention on the multiplexed PD lines.
CAS[3:0]	O	82, 83, 85, 86	Column Address Strobe Lines 3:0.
WE	O	125	Write Enable.
OE[1:0]	O	50, 124	Output Enable. OE1 is output on pin 50 when bit 2 of CR36 is cleared to 0 (EDO memory). If the feature connector is disabled (bit 0 of SRD cleared to 0), this output is the same as OE0 (for 64-bit PD bus operation). If the Trio64-compatible VAFC feature connector is enabled (bit 0 of SRD set to 1 and bit 1 of SRD cleared to 0), OE1 is held high (not asserted). This ensures that EDO memory data is not driven on the multiplexed PD lines when the Trio64-compatible feature connector is enabled. OE1 is never generated in fast page mode operation. Instead, if bit 6 of SRA is cleared to 0 (default), a second OE0 signal is output on pin 50. This allows the same board to use either fast page or EDO memory in 2-MByte designs with no additional hardware. OE1 is not available for LPB VL-Bus configurations. Memory designs requiring use of pin 50 as a memory control signal cannot be used.
VIDEO INTERFACE			
PDOWN	I	165	Power Down. Asserting this signal turns off the RGB analog output from the DACs.
VREF		162	Voltage Reference. This pin is tied to V_{SS} through a 0.1 µF capacitor.
RSET		166	Reference Resistor. This pin is tied to V_{SS} through an external resistor to control the full-scale current value.
AR	O	168	Analog Red. Analog red output to the monitor.
AG	O	171	Analog Green. Analog green output to the monitor.
AB	O	172	Analog Blue. Analog blue signal to the monitor.

Table 3-1. Pin Descriptions - LPB Mode (Continued)

Symbol	Type	Pin Number(s)	Description
ENFEAT	O	151	Enable Feature Connector. Setting SRD_0 to 1 drives this signal low when SR1C_1-0 are 00b. This also enables all feature connector operations.
BLANK VFCBLANK	B B	191, 206 115	Video Blank. The BLANK function is on pin 191 when LPB feature connector operation is enabled in PCI configurations. It is on pin 206 for LPB VL-Bus configurations. It is on pin 115 when Trio64-compatible VAFC operation is enabled and is called VFCBLANK. When ESYNC is high, BLANK is a feature connector output. When ESYNC is low, BLANK is a feature connector input that, when driven low, turns off the video output.
ESYNC VFCESYNC	I I	183, 205 109	External SYNC. The ESYNC function is on pin 183 when LPB feature connector operation is enabled in PCI configurations. It is on pin 205 for LPB VL-Bus configurations. It is on pin 109 when Trio64-compatible VAFC operation is enabled and is called VFCESYNC. When ESYNC is driven low, HSYNC, VSYNC and BLANK become inputs. When ESYNC is high, HSYNC, VSYNC and BLANK become outputs.
EVIDEO VFCEVIDEO	I I	203 111	External Video. The EVIDEO function is on pin 203 when LPB feature connector operation is enabled. It is on pin 111 when Trio64-compatible VAFC operation is enabled and is called VFCEVIDEO. When this input is asserted low, PA[15:0] (or VFCPA[15:0]) are inputs and are sampled by VCLKI. When this input is high, PA[15:0] (or VFCPA[15:0]) are outputs to the feature connector.
EVCLK VFCEVCLK	I	204 113	External VCLK. The EVCLK function is on pin 204 when LPB feature connector operation is enabled. It is on pin 113 when Trio64-compatible VAFC operation is enabled and is called VFCEVCLK. When this input is asserted low, VCLK is an input to the internal RAMDAC. When this input is high, VCLK is output to the feature connector.
VCLK	B	148	Video/Pixel Clock. The VCLK function is enabled on pin 148 when feature connector operation is enabled. When EVCLK (or VFCEVCLK) is high, this signal is an output to the feature connector. When EVCLK is low, this becomes an input used only for test purposes.
VCLKI	I	106	VCLK Input. The VCLKI function is enabled when LPB VAFC (16-bit) feature connector operation is enabled. Setting bit 1 of SRB to 1 causes VCLKI to be used to clock in feature connector pixel data to the internal RAMDAC.

Table 3-1. Pin Descriptions - LPB Mode (Continued)

Symbol	Type	Pin Number(s)	Description
HSYNC	B	149	Horizontal Sync. When ESYNC (or VFCESYNC) is high, this is the horizontal sync output. When ESYNC is low, this is an input from the feature connector.
VSYNC	B	150	Vertical Sync. When ESYNC (or VFCESYNC) is high, this is the vertical sync output. When ESYNC is low, this is an input from the feature connector.
PA[15:0]	B	201-199, 189-185, 202, 184, 175, 174, 155, 154, 147, 146	Pixel Address Lines [15:0]. The PA[15:0] function is enabled on the pins indicated for PCI configurations when LPB feature connector operation is enabled. Only PA[7:0] are enabled for VL-Bus configurations.
VFCPA[15:0]	B	144, 142, 140, 138, 134, 132, 130, 128, 127, 129, 131, 133, 136, 139, 141, 143	The PA function is on the pins indicated for VFCPA[15:0] when Trio64-compatible VAFC operation is enabled. When EVIDEO (or VFCEVIDEO) is high, PA signals are outputs to the feature connector. When EVIDEO is low, PA signals are inputs and are sampled by VCLKI if bit 1 of SRB is set to 1.
MISCELLANEOUS FUNCTIONS			
General Data, I/O and Serial Ports			
GA[15:0]	O	105, 103, 101, 98, 95, 93, 91, 89, 88, 90, 92, 94, 97, 100, 102, 104	(PCI) General Address Bus. These signals provide the address for BIOS ROM reads. They are multiplexed with PD signals. Programmers must ensure that the memory bus is inactive when reading the ROM.
GD[7:0]	I	53, 55, 57, 59, 63, 65, 67, 69	(PCI) General Data Bus. These signals carry data for BIOS ROM reads. They are multiplexed with PD signals. Programmers must ensure that the memory bus is inactive when reading the ROM.
ROMEN	O	153	(PCI) ROM Enable. This signal provides the chip output enable input for BIOS ROM reads.
ROMCS	O	153	(VL) ROM Chip Select. This signal provides the chip output enable for BIOS ROM reads. It is output when bits 1-0 of SR1C are any value except 11b.
GPIOSTR	O	151	(VL) General Input/Output Port Write Strobe. If SR1C_1-0 are 01b, this is asserted whenever a General Input Port access (CR55_2 is set to 1 and the 3C8H port is read) or a General Output Port access (write to CR5C) is made.
GOP[1:0]	O	190, 151	(PCI) General Output Port Bits 1-0. If SR1C_1 is set to 1, the value of CR5C_0 is output on pin 151 (GOP0) and the value of CR5C_1 is output on pin 190 (GOP1).
GOP[1:0]	O	153, 151	(VL) General Output Port Bits 1-0. If bit 1 of SR1C is set to 1, the value of CR5C_0 is output on pin 151 (GOP0). If SR1C_1-0 are 11b, the value of CR5C_1 is output on pin 153 (GOP1)

Table 3-1. Pin Descriptions - LPB Mode (Continued)

Symbol	Type	Pin Number(s)	Description
STWR	O	190	(PCI) Strobe Write. If SR1C_1 is cleared to 0, this signal is asserted whenever a write is made to CR5C. It is used to enable a General Output Port latch.
SPCLK	I/O	205	Serial Port Clock. This is the clock for serial data transfer, either for I^2C or DDC2 monitor data communications. As an output, it is programmed via MMFF20_0. As an input, its status is read via MMFF20_2. In either case the serial port must be enabled by setting MMFF20_4 to 1. PD[26:25] can be strapped to allow I/O (E2H or E8H) access to the Serial Port register while the Trio64V+ is disabled.
SPD	I/O	206	Serial Port Data. This is the data signal for serial data transfer, either for I^2C or DDC2 monitor data communications. As an output, it is programmed via MMFF20_1. As an input, its status is read via MMFF20_3. In either case the serial port must be enabled by setting MMFF20_4 to 1. PD[26:25] can be strapped to allow I/O (E2H or E8H) access to the Serial Port register while the Trio64V+ is disabled.
LOCAL PERIPHERAL BUS			
Scenic/MX2 Mode			
LD[7:0]	I/O	202, 184, 175, 174, 155, 154, 147. 146	LPB Data. This is the Scenic Highway data bus and carries compressed data to the Scenic/MX2 and video data from the Scenic/MX2.
LCLK	I	148	LPB Clock. This clock controls transactions between the Trio64V+ and Scenic Highway peripherals
VREQ/VRDY	O	203	Video Request/Ready. This signal is part of the the Scenic Highway data transfer protocol between the Trio64V+ and the Scenic/MX2.
CREQ/CRDY	I	204	Scenic/MX2 Request/Ready. This signal is part of the the Scenic Highway data transfer protocol between the Trio64V+ and the Scenic/MX2.
ENFEAT	O	151	Enable Feature Connector. This signal is connected to the Scenic/MX2 chip enable input such that the Scenic/MX2 is disabled when feature connector operation is enabled.

Table 3-1. Pin Descriptions - LPB Mode (Continued)

Symbol	Type	Pin Number(s)	Description
Video 8 in and Video 16 (PCI only) Modes			
LD[7:0]	I	202, 184, 175, 174, 155, 154, 147. 146	LPB Data Bus [7:0]. This is the Scenic Highway data bus and carries video data input.
LD[15:8]	I	201-199, 189-185	(PCI) LPB Data Bus [15:8]. Scenic Highway video data input for the upper data byte in Video 16 mode.
HS	I	203	HSYNC. HSYNC input signaling the transition from one line to the next.
VS	I	204	VSYNC. VSYNC input signaling the transition from one frame to the next.
HD[7:0]	O	201-199, 189-185	Host Data. CL-480 compressed data.
HSEL[2:0]	O	178-176	Host Select. These signals select one of five CL-480 host interface registers.
Video 8 In/Out Mode (CL-480) (PCI only)			
LD[7:0]	I	202, 184, 175, 174, 155, 154, 147. 146	LPB Data Bus [7:0]. This is the Scenic Highway data bus and carries video data input.
DS		179	Data Strobe. The Trio64V+ asserts this signal to select the CL-480 for a read or write operation.
R/W	O	180	Read/Write. The Trio64V+ drives this signal high to specify a CL-480 read cycle and low to specify a write cycle.
DTACK	I	181	Data Acknowledge. The CL-480 asserts this signal when it latches compressed data from the Trio64V+ or when it has placed video data on LD[7:0]. This is an open drain signal.
CFLEVEL	I	182	Compressed Data FIFO Level. When this signal is low, the CL-480 FIFO has room for at least 44 bytes of compressed data. This is an open drain signal.
POWER AND GROUND			
VDD	I	12, 37, 62, 81, 96, 137, 192	Digital power supply
AVDD	I	164, 169, 170	Analog power supply (RAMDAC)
CLKAVDD[1:2]	I	158, 160	Analog power supply (clock synthesizer) CLK1 = DCLK, CLK2 = MCKL
VSS	I	9, 22, 32, 47, 60, 71, 87, 99, 114, 123, 126, 135, 145, 195	Digital ground
AVSS	I	159, 161, 163, 167, 173	Analog ground

3.3 PIN LISTS

Table 3-2 lists all Trio64V+ pins alphabetically. The pin number(s) corresponding to each pin name are given in the appropriate bus interface type column. Table 3-3 lists all pins in numerical order. The corresponding pin name/pin number is given in the appropriate bus interface column.

Table 3-2. Alphabetical Pin Listing

	PIN(S)	
Name	**PCI**	**VL**
AB	172	172
AD[31:0]	207-208, 1-6, 10-11, 13-18, 28-31, 33-36,	
	39-46	
AG	171	171
AR	168	168
AVDD	164, 169, 170	164, 169, 170
AVSS	159, 161, 163, 167, 173	159, 161, 163, 167, 173
BLANK	191	206
CAS[3:0]	82, 83, 85, 86	82, 83, 85, 86
CAS[7:4]	52, 51, 49, 48	52, 51, 49, 48
C/BE[3:0]	7, 19, 27, 38	
CLKAVDD[1:2]	158, 160	158, 160
CREQ/CRDY	204	204
DEVSEL	24	
ENFEAT	151	151
ESYNC	183	205
EVCLK	204	204
EVIDEO	203	203
FRAME	20	
GA[15:0]	105, 103, 101, 98, 90, 92, 94, 97,	
	100, 102, 104	
GD[7:0]	53, 55, 57, 59, 63, 65, 67, 69	
GOP[1:0]	190, 151	153, 151
GPIOSTR		151
HD[7:0]	201-199, 189-185	
HS	203	203
HSYNC	149	149
IDSEL	8	
INTA	152	
IRDY	21	
LCLK	148	148
LD[7:0]	202, 184, 175, 174, 155, 154, 147, 146	202, 184, 175, 174, 155, 154, 147, 146
LD[15:8]	201-199, 189-185	
LOCA		24
MA[8:0]	80, 78, 76, 74, 72,73, 75, 77, 79	80, 78, 76, 74, 72, 73, 75, 77, 79

Table 3-2. Alphabetical Pin Listing (Continued)

	PIN(S)	
Name	**PCI**	**VL**
$\overline{OE0}$	124	124
$\overline{OE1}$	50	
PA[7:0]	202, 184, 175, 174, 155, 154, 147, 146	202, 184, 175, 174, 155, 154, 147, 146
PA[15:8]	201-199, 189-185, 134, 132, 130, 128,	
PAR	26	
PD[63:0]	122, 120, 118, 116, 113, 111, 109, 107,	122, 120, 118, 116, 113, 111, 109, 107,
	106, 108, 110, 112, 115, 117, 119, 121,	106, 108, 110, 112, 115, 117, 119, 121,
	144, 142, 140, 138, 134, 132, 130, 128,	144, 142, 140, 138, 134, 132, 130, 128,
	127, 129, 131, 133, 136, 139, 141, 143,	127, 129, 131, 133, 136, 139, 141, 143,
	70, 68, 66, 64, 61, 58, 56, 54, 53, 55,	70, 68, 66, 64, 61, 58, 56, 54, 53, 55,
	57, 59, 63, 65, 67, 69, 105, 103, 101,	57, 59, 63, 65, 67, 69, 105, 103, 101,
	98, 95, 93, 91, 89, 88, 90, 92, 94, 97	98, 95, 93, 91, 89, 88, 90, 92, 94, 97
	100, 102, 104	100, 102, 104
$\overline{PDOWN}$	165	165
$\overline{RAS0}$	50	50
$\overline{RAS1}$	84	
$\overline{RESET}$	193	
$\overline{RDYIN}$		21
$\overline{ROMEN}$	153	
$\overline{ROMCS}$		153
RSET	166	166
SA[22:2]		201-196, 191-185, 183-176
SA[31:23]		
$\overline{SADS}$		20
SAUP1		25
SAUP2		50
$\overline{SBE[3:0]}$		7, 19, 27, 38
SCLK	194	194
SD[31:0]		207-208, 1-6, 10-11, 13-18, 28-31, 33-36,
		39-46
SINTR		152
SM/$\overline{IO}$		8
SPCLK	205	205
SPD	206	206
$\overline{SRDY}$		23
SRESET		193
$\overline{STOP}$	25	
$\overline{STRD}$		
STWR		

Table 3-2. Alphabetical Pin Listing (Continued)

	PIN(S)	
Name	**PCI**	**VL**
$\overline{\text{STWR}}$	190	
SW/$\overline{\text{R}}$		26
$\overline{\text{TRDY}}$	23	
$\overline{\text{VFCBLANK}}$	115	115
VFCESYNC	109	109
VFCEVCLK	113	113
VFCEVIDEO	111	111
VFCPA[15:0]	144, 142, 140, 138, 134, 132, 130, 128,	144, 142, 140, 138, 134, 132, 130, 128,
	127, 129, 131, 133, 136, 139, 141, 143	127, 129, 131, 133, 136, 139, 141, 143
VFCVCLK	117	117
VFCVCLKI	106	106
VCLK	148	148
VCLKI	106	106
VDD	12, 37, 62, 81, 96,	12, 37, 62, 81, 96,
	137, 192	137, 192
$\overline{\text{VREQ}}$/VRDY	203	203
VREF	162	162
VS	204	204
VSS	9, 22, 32, 47, 60, 71, 87, 99, 114, 123,	9, 22, 32, 47, 60, 71, 87, 99, 114, 123,
	126, 135, 145	126, 135, 145
	195	195
VSYNC	150	150
$\overline{\text{WE}}$	125	125
XIN	156	156
XOUT	157	157

Table 3-3. Numerical Pin Listing

	PINS	
Number	**PCI**	**VL**
1	AD29	SD29
2	AD28	SD28
3	AD27	SD27
4	AD26	SD26
5	AD25	SD25
6	AD24	SD24
7	C/BE3	SBE3
8	IDSEL	SM/IO
9	**VSS**	**VSS**
10	AD23	SD23
11	AD22	SD22
12	**VDD**	**VDD**
13	AD21	SD21
14	AD20	SD20
15	AD19	SD19
16	AD18	SD18
17	AD17	SD17
18	AD16	SD16
19	C/BE2	SBE2
20	FRAME	SADS
21	IRDY	RDYIN
22	**VSS**	**VSS**
23	TRDY	SRDY
24	DEVSEL	LOCA
25	STOP	SAUP1
26	PAR	SW/R
27	C/BE1	SBE1
28	AD15	SD15
29	AD14	SD14
30	AD13	SD13
31	AD12	SD12
32	**VSS**	**VSS**
33	AD11	SD11
34	AD10	SD10
35	AD9	SD9
36	AD8	SD8
37	**VDD**	**VDD**
38	C/BE0	SBE0
39	AD7	SD7
40	AD6	SD6
41	AD5	SD5
42	AD4	SD4

Table 3-3. Numerical Pin Listing (Continued)

	PINS	
Number	**PCI**	**VL**
43	AD3	SD3
44	AD2	SD2
45	AD1	SD1
46	AD0	SD0
47	**VSS**	**VSS**
48	$\overline{\text{CAS4}}$	$\overline{\text{CAS4}}$
49	$\overline{\text{CAS5}}$	$\overline{\text{CAS5}}$
50	$\overline{\text{RAS1}}/\overline{\text{OE1}}$	SAUP2
51	$\overline{\text{CAS6}}$	$\overline{\text{CAS6}}$
52	$\overline{\text{CAS7}}$	$\overline{\text{CAS7}}$
53	PD23/GD7	PD23
54	PD24	PD24
55	PD22/GD6	PD22
56	PD25	PD25
57	PD21/GD5	PD21
58	PD26	PD26
59	PD20/GD4	PD20
60	**VSS**	**VSS**
61	PD27	PD27
62	**VDD**	**VDD**
63	PD19/GD3	PD19
64	PD28	PD28
65	PD18/GD2	PD18
66	PD29	PD29
67	PD17/GD1	PD17
68	PD30	PD30
69	PD16/GD0	PD16
70	PD31	PD31
71	**VSS**	**VSS**
72	MA4	MA4
73	MA3	MA3
74	MA5	MA5
75	MA2	MA2
76	MA6	MA6
77	MA1	MA1
78	MA7	MA7
79	MA0	MA0
80	MA8	MA8
81	**VDD**	**VDD**
82	$\overline{\text{CAS3}}$	$\overline{\text{CAS3}}$
83	$\overline{\text{CAS2}}$	$\overline{\text{CAS2}}$
84	$\overline{\text{RAS0}}$	$\overline{\text{RAS0}}$

Table 3-3. Numerical Pin Listing (Continued)

	PINS	
Number	**PCI**	**VL**
85	$\overline{CAS1}$	$\overline{CAS1}$
86	$\overline{CAS0}$	$\overline{CAS0}$
87	**VSS**	**VSS**
88	PD7/GA7	PD7
89	PD8/GA8	PD8
90	PD6/GA6	PD6
91	PD9/GA9	PD9
92	PD5/GA5	PD5
93	PD10/GA10	PD10
94	PD4/GA4	PD4
95	PD11/GA11	PD11
96	**VDD**	**VDD**
97	PD3/GA3	PD3
98	PD12/GA12	PD12
99	**VSS**	**VSS**
100	PD2/GA2	PD2
101	PD13/GA13	PD13
102	PD1/GA1	PD1
103	PD14/GA15	PD14
104	PD0/GA0	PD0
105	PD15/GA15	PD15
106	PD55/VFCVCLKI	PD55/VFCVCLKI
107	PD56	PD56
108	PD54	PD54
109	PD57/VFCESYNC	PD57/VFCESYNC
110	PD53	PD53
111	PD58/VFCEVIDEO	PD58/VFCEVIDEO
112	PD52	PD52
113	PD59/VFCEVCLK	PD59/VFCEVCLK
114	**VSS**	**VSS**
115	PD51/$\overline{VFCBLANK}$	PD51/$\overline{VFCBLANK}$
116	PD60	PD60
117	PD50/VFCVCLK	PD50/VFCVCLK
118	PD61	PD61
119	PD49	PD49
120	PD62	PD62
121	PD48	PD48
122	PD63	PD63
123	**VSS**	**VSS**
124	$\overline{OE0}$	$\overline{OE0}$
125	$\overline{WE}$	$\overline{WE}$
126	**VSS**	**VSS**

Table 3-3. Numerical Pin Listing (Continued)

	PINS	
Number	**PCI**	**VL**
127	PD39/VFCPA7	PD39/VFCPA7
128	PD40/VFCPA8	PD40/VFCPA8
129	PD38/VFCPA6	PD38/VFCPA6
130	PD41/VFCPA9	PD41/VFCPA9
131	PD37/VFCPA5	PD37/VFCPA5
132	PD42/VFCPA10	PD42/VFCPA10
133	PD36/VFCPA4	PD36/VFCPA4
134	PD43/VFCPA11	PD43/VFCPA11
135	**VSS**	**VSS**
136	PD35/VFCPA3	PD35/VFCPA3
137	**VDD**	**VDD**
138	PD44/VFCPA12	PD44/VFCPA12
139	PD34/VFCPA2	PD34/VFCPA2
140	PD45/VFCPA13	PD45/VFCPA13
141	PD33/VFCPA1	PD33/VFCPA1
142	PD46/VFCPA14	PD46/VFCPA14
143	PD32/VFCPA0	PD32/VFCPA0
144	PD47/VFCPA15	PD47/VFCPA15
145	**VSS**	**VSS**
146	LD0/PA0	LD0/PA0
147	LD1/PA1	LD1/PA1
148	LCLK/VCLK	LCLK/VCLK
149	HSYNC	HSYNC
150	VSYNC	VSYNC
151	$\overline{\text{ENFEAT}}$/GOP0	$\overline{\text{ENFEAT}}$/GPIOSTR/GOP0
152	$\overline{\text{INTA}}$	SINTR
153	$\overline{\text{ROMEN}}$	$\overline{\text{ROMCS}}$/GOP1
154	LD2/PA2	LD2/PA2
155	LD3/PA3	LD3/PA3
156	XIN	XIN
157	XOUT	XOUT
158	**CLKAVDD1**	**CLKAVDD1**
159	**AVSS**	**AVSS**
160	**CLKAVDD2**	**CLKAVDD2**
161	**AVSS**	**AVSS**
162	VREF	VREF
163	**AVSS**	**AVSS**
164	**AVDD**	**AVDD**
165	$\overline{\text{PDOWN}}$	$\overline{\text{PDOWN}}$
166	RSET	RSET
167	**AVSS**	**AVSS**
168	AR	AR

Table 3-3. Numerical Pin Listing (Continued)

	PINS	
Number	**PCI**	**VL**
169	**AVDD**	**AVDD**
170	**AVDD**	**AVDD**
171	AG	AG
172	AB	AB
173	**AVSS**	**AVSS**
174	LD4/PA4	LD4/PA4
175	LD5/PA5	LD5/PA5
176	N/C	SA2
177	N/C	SA3
178	N/C	SA4
179	N/C	SA5
180	N/C	SA6
181	N/C	SA7
182	N/C	SA8
183	ESYNC	SA9
184	LD6/PA6	LD6/PD6
185	LD8/PA8/HD0	SA10
186	LD9/PA9/HD1	SA11
187	LD10/PA10/HD2	SA12
188	LD11/PA11/HD3	SA13
189	LD12/PA12/HD4	SA14
190	$\overline{\text{STWR}}$/GOP1	SA15
191	$\overline{\text{BLANK}}$	SA16
192	**VDD**	**VDD**
193	$\overline{\text{RESET}}$	$\overline{\text{SRESET}}$
194	SCLK	SCLK
195	**VSS**	**VSS**
196	VCLKI	SA17
197	RESERVED ($\overline{\text{GNT}}$)	SA18
198	RESERVED ($\overline{\text{REQ}}$)	SA19
199	LD13/PA13/HD5	SA20
200	LD14/PA14/HD6	SA21
201	LD15/PA15/HD7	SA22
202	LD7/PA7	LD7/PA7
203	$\overline{\text{VREQ}}$/VRDY/HS/EVIDEO	$\overline{\text{VREQ}}$/VRDY/HS/EVIDEO
204	$\overline{\text{CREQ}}$/CRDY/VS/EVCLK	$\overline{\text{CREQ}}$/CRDY/VS/EVCLK
205	SPCLK	SPCLK/ESYNC
206	SPD	SPD/$\overline{\text{BLANK}}$
207	AD31	SD31
208	AD30	SD30

Section 4: Electrical Data

4.1 MAXIMUM RATINGS

Table 4-1. Absolute Maximum Ratings

Ambient temperature	0° C to 70° C
Storage temperature	-40° C to 125° C
DC Supply Voltage	-0.5V to 7.0V
I/O Pin Voltage with respect to V_{SS}	-0.5V to V_{DD}+0.5V

4.2 DC SPECIFICATIONS

Note: In all cases below, digital VDD = 5V ± 5% and the operating temperature is 0° C to 70° C.

Table 4-2. RAMDAC/Clock Synthesizer DC Specifications

Symbol	Parameter	Min	Typical	Max	Unit
AVDD	DAC supply voltage	4.75	5	5.25	V
AVDD (CLOCK)	PLL supply voltage	4.75	5	5.25	V
VREF	Internal voltage reference	1.2	1.35	1.5	V

Table 4-3. RAMDAC Characteristics

	Min	Typical	Max	Unit
Resolution Each DAC		8		bits
LSB Size		66		µA
Integral Linearity Error			± 1	LSB
Differential Linearity Error			± 1	LSB
Output Full-Scale Current	15.6	17.6	19.5	mA
DAC to DAC Mismatch			5%	
Power Supply Rejection Ratio			0.5	%/ % AVDD
Output Compliance	0.0		1.5	V
Output Capacitance			30	pF
Glitch Impulse		75		pV-Sec

Table 4-4. Digital DC Specifications (VDD = 5V ± 5%, Operating Temperature 0° C to 70° C)

Symbol	Parameter	Min	Max	Unit
V_{IL}	Input Low Voltage	-0.5	0.8	V
V_{IH}	Input High Voltage	2.4 (Note 1)	V_{DD} +0.5	V
V_{OL}	Output Low Voltage		V_{SS} + 0.4	V
V_{OH}	Output High Voltage	2.4		V
I_{OL1}	Output Low Current	8 (Note 2)		mA
I_{OH1}	Output High Current	-4		mA
I_{OL2}	Output Low Current	16 (Note 3)		mA
I_{OH2}	Output High Current	-8		mA
I_{OL3}	Output Low Current	24 (Note 4)		mA
I_{OH3}	Output High Current	-12		mA
I_{OZ}	Output Tri-state Current		1	µA
C_{IN}	Input Capacitance		5	pF
C_{OUT}	Output Capacitance		5	pF
I_{CC}	Power Supply Current		500 (Note 5)	mA

Notes for Table 4-4

1. The value for pins 25 ($\overline{\text{STOP}}$) and 26 (PAR) is 2.6V.
2. I_{OL1}, I_{OH1} for pins $\overline{\text{ROMEN}}$, $\overline{\text{INTA}}$, $\overline{\text{STRD}}$, $\overline{\text{STWR}}$, HSYNC, VSYNC, VCLK, $\overline{\text{BLANK}}$, $\overline{\text{ENFEAT}}$, MA[8:0], $\overline{\text{CAS[7:0]}}$, PD[63:0], AD[31:0], LD[7:0], HSEL, $\overline{\text{DS}}$, R/$\overline{\text{W}}$, $\overline{\text{DTACK}}$, $\overline{\text{VREQ}}$/VRDY, SPCLK, SPD
3. I_{OL2}, I_{OH2} for pins $\overline{\text{OE[1:0]}}$, $\overline{\text{WE}}$, $\overline{\text{RAS[1:0]}}$
4. I_{OL3}, I_{OH3} for pins PAR, $\overline{\text{STOP}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{TRDY}}$
5. I_{CC} measured for a resolution of 1024x768x8 with a 75 MHz DCLK and a 60 MHz MCLK at 25°C and 5V.
6. The pin names used in these notes are the primary ones for PCI configurations. An output signal multiplexed on one of these pins has the same drive level, as does a VL-Bus output for the same pin.

4.3 AC SPECIFICATIONS

Note: All AC timings are based on an 80 pF test load.

4.3.1 RAMDAC AC Specifications

Table 4-5. RAMDAC AC Specifications

Parameter	Typical	Max	Unit	Notes
DAC Output Delay	5		ns	1
DAC Output Rise/Fall Time	3		ns	2
DAC Output Settling Time	15		ns	
DAC-to-DAC Output Skew	2	5	ns	3

Notes for Table 4-5

1. Measured from the 50% point of VCLK to the 50% point of full scale transition
2. Measured from 10% to 90% full scale
3 With DAC outputs equally loaded

Table 4-6. RAMDAC Output Specifications

Description	I_{OUT} (mA)	V_{OUT} (V)	BLANK	Input Data
White	17.6 typical	0.66 typical	1	FFH
Data	Data	Data	1	Data
Data (sync)	Data	Data	1	Data
Black	0	0	1	00H
Black (sync)	0	0	1	00H
$\overline{BLANK}$	0	0	0	Don't Care

Note

1. Condition for V_{OUT} is a 75 Ohm doubly terminated load, RSET = 143 Ohms and use of internal VREF. A target V_{OUT} value of 714 mV requires RSET = 130 Ohms.

4.3.2 Clock Timing

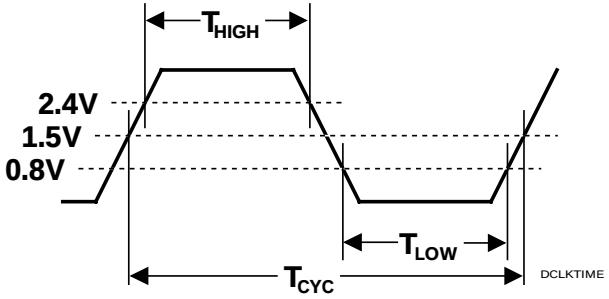


Figure 4-1. Clock Waveform Timing

Table 4-7. Clock Waveform Timing

Symbol	Parameter	Min	Max	Units	Notes
T_{CYC}	SCLK Cycle Time (VL-Bus)	20	125	ns	1
	SCLK Cycle Time (PCI)	30	125	ns	1
	LCLK Cycle Time	30	200	ns	
	MCLK Cycle Time	16.667	100	ns	
	DCLK Cycle Time (VGA Mode)	25	100	ns	1
	DCLK Cycle Time (Enhanced Mode)	12.5	100	ns	1, 2
T_{HIGH}	SCLK High Time (VL-Bus)	8	80	ns	
	SCLK High Time (PCI)	12	80	ns	
	LCLK High Time	12	160	ns	
T_{LOW}	SCLK Low Time (VL-Bus)	8	80	ns	
	SCLK Low Time (PCI)	12	80	ns	
	LCLK Low Time	12	160	ns	
	SCLK Slew Rate	1	4	V/ns	3
	LCLK Slew Rate	1	4	v/nS	3

Notes

1. $f_{DCLK} \geq 1/2\ f_{SCLK}$ to ensure valid writes to the PLLs.
2. For DCLK rates above 80 MHz, clock doubling is used. The maximum DCLK rate with clock doubling is 67.5 MHz.
3. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to peak portion of the clock waveform.

4.3.3 Input/Output Timing

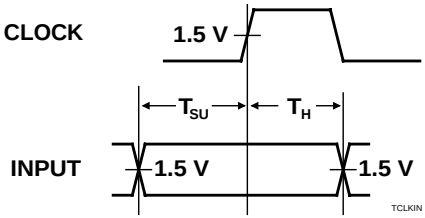


Figure 4-2. Input Timing

Table 4-8. SCLK-Referenced Input Timing

PCI Bus			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	AD[31:0], C/BE[3:0], FRAME, IRDY, IDSEL setup	7	ns
T_H	AD[31:0] hold	1	ns
T_H	C/BE[3:0], FRAME, IRDY, IDSEL hold	1	ns
VL-Bus			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	AD[31:2], BE[3:0], SM/IO, SW/R, SADS (address phase) setup	12	ns
T_H	AD[31:2], BE[3:0], SM/IO, SW/R, SADS (address phase) hold	1	ns
T_{SU}	AD[31:2], BE[3:0], D1, D0, SADS (data phase) setup	4	ns
T_H	AD[31:2], BE[3:0], D1, D0, SADS (data phase) hold	1	ns
T_{SU}	RDYIN setup	6	ns
T_H	RDYIN hold	1	ns
Miscellaneous			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	ROM data GD[7:0] setup (PCI)	5	ns
T_H	ROM data GD[7:0] hold (PCI)	7	ns
T_{SU}	General Input Port GD[7:0] setup	5	ns
T_H	General Input Port GD[7:0] hold	7	ns

Table 4-9. LCLK-Referenced Input Timing

Scenic/MX2 Interface			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	LD[7:0] setup	10	ns
T_H	LD[7:0] hold	9	ns
T_{SU}	$\overline{\text{CREQ}}$/CRDY	6	ns
T_H	$\overline{\text{CREQ}}$/CRDY	8	ns
CL-480/SAA7110 Interface			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	LD[7:0] setup (also LD[15:8] for 16-bit interface)	6	ns
T_H	LD[7:0] hold (also LD[15:8] for 16-bit interface)	8	ns
T_{SU}	HS setup	6	ns
T_H	HS hold	7	ns
T_{SU}	VS setup	6	ns
T_H	VS hold	7	ns

Table 4-10. MCLK-Referenced Input Timing

Symbol	**Parameter**	**Min**	**Units**
T_{SU}	PD[63:0] setup	0	ns
T_H	PD[63:0] hold	12.5/16 (Note 1)	ns

Note

1. The hold time is 12.5 ns for 1-cycle operation and 16 ns for 2-cycle operation.

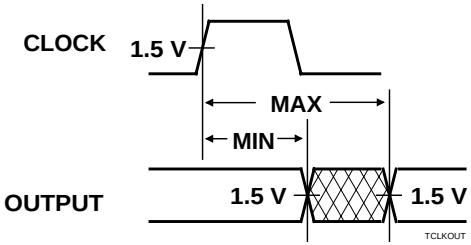


Figure 4-3. Output Timing

The minimum delay is the minimum time after the clock edge that the valid signal state from the previous cycle will begin transition to the next state (become invalid).

The maximum delay is the maximum time after the clock edge that the signal state is valid for the next cycle.

Table 4-11. SCLK-Referenced Output Timing

PCI Bus				
Parameter	**Min**	**Max**	**Units**	**Notes**
AD[31:0] valid delay	2	16	ns	1
$\overline{\text{DEVSEL}}$, PAR delay	2	11	ns	Medium $\overline{\text{DEVSEL}}$ timing used
$\overline{\text{STOP}}$ delay	2	11	ns	
$\overline{\text{TRDY}}$ delay	2	11	ns	
$\overline{\text{INTA}}$ delay	2	11	ns	
VL-Bus				
Parameter	**Min**	**Max**	**Units**	**Notes**
AD[31:2], D1, D0 valid delay	7	16	ns	
SINTR delay	5	30	ns	
$\overline{\text{SRDY}}$ delay	5	11	ns	
$\overline{\text{LOCA}}$ active delay	5	15	ns	
$\overline{\text{LOCA}}$ inactive delay	5	20	ns	
Miscellaneous				
Parameter	**Min**	**Max**	**Units**	**Notes**
$\overline{\text{STRD}}$ delay	3	15	ns	
$\overline{\text{ROMEN}}$ (PCI) delay	4	10		
ROM address valid delay (PCI)	5	30	ns	
AD[7:0] ROM data valid delay (PCI)	5	30	ns	

Note

1. Due to the timing for $\overline{\text{TRDY}}$ for read cycles, data is not sampled on the clock edge immediately following its becoming valid. This guarantees the PCI 2.0 specification time of 11 ns.

Table 4-12. LCLK-Referenced Output Timing

Scenic/MX2 Interface				
Parameter	**Min**	**Max**	**Units**	**Notes**
$\overline{VREQ}$/VRDY active delay	2	11	ns	7 ns typ
LD[7:0] valid delay	2	15	ns	8 ns typ
LD[7:0] tri-state from LCLK	7	15	ns	

Table 4-13. MCLK-Referenced Output Timing

Parameter	**Min**	**Max**	**Units**	**Notes**
PD[63:0] valid delay	2	7/11	ns	1
MA[8:0] valid delay	1.5	8	ns	
$\overline{CAS[7:0]}$ active delay	1	5.5	ns	
$\overline{CAS[7:0]}$ inactive delay	1	5.5	ns	
$\overline{RAS[1:0]}$ active delay	1	5	ns	
$\overline{RAS[1:0]}$ inactive delay	1	6.5	ns	
$\overline{OE[1:0]}$ active delay	1.5	4.5	ns	
$\overline{WE}$ active delay	1.5	4.5	ns	

Note

1. The maximum delay time is 7 ns for 1-cycle operation and 11 ns for 2-cycle operation.

Table 4-14. CL-480 Timings - Trio64V+ Driving Host Interface

CL-480 Interface			
Symbol	**Parameter**	**Min**	**Units**
	HD[7:0] (write), HSEL[2:0], R/$\overline{W}$ valid to DS low	LCLK T_{CYC}	ns
T_H	HD[7:0] (write), HSEL[2:0], R/$\overline{W}$ hold from DS low	LCLK T_{CYC}	ns
T_{SU}	HD[7:0] (read) setup to $\overline{DTACK}$ high	5	ns
T_H	HD[7:0] (read) hold from $\overline{DTACK}$ high	0	ns

Table 4-15. Feature Connector Timing - Output from Trio64V+ to Feature Connector

Symbol	**Parameter**	**Min**	**Units**	**Notes**
T_{SU}	PA[15:0], $\overline{BLANK}$ setup to VCLK rising	5	ns	
T_H	PA[15:0], $\overline{BLANK}$ hold from VCLK rising	5	ns	

Table 4-16. Feature Connector Timing - Output from Feature Connector to Trio64V+

Symbol	Parameter	Min	Max	Units	Notes
T_{SU}	PA[15:0], $\overline{BLANK}$ setup to VCLK or VCLKI rising	6		ns	1
T_H	PA[15:0], $\overline{BLANK}$ hold from VCLK or VCLKI rising	6		ns	1
	VCLK	25	40	ns	1
	VCLKI	27	40	ns	1, 2
	VCLK, VCLKI duty cycle	40	60	%	
	VCLK, VCLKI high time	10	25	ns	
	VCLK, VCLKI low time	10	25	ns	
	VCLK, VCLKI slew rate	1	4	V/ns	

Notes

1. Pixel data is clocked into the internal RAMDAC using VCLK for a pass-through feature connector and VCLKI for a VAFC configuration.
2. This corresponds to the VESA VAFC specification of a maximum clock of 37.5 MHz.

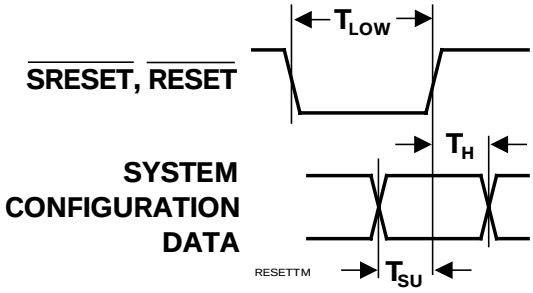


Figure 4-4. Reset Timing

Table 4-17. Reset Timing

Symbol	Parameter	Min	Units
T_{LOW}	$\overline{\text{SRESET}}$ (VL) or $\overline{\text{RESET}}$ (PCI) active pulse width	400	ns
T_{SU}	PD[28:0] setup to $\overline{\text{SRESET}}$ (VL) or $\overline{\text{RESET}}$ (PCI) inactive	20	ns
T_H	PD[28:0] hold from $\overline{\text{SRESET}}$ (VL) or $\overline{\text{RESET}}$ (PCI) inactive	10	ns

Section 5: Reset and Initialization

The reset signal ($\overline{\text{RESET}}$ for PCI, $\overline{\text{SRESET}}$ for VL-Bus) resets the internal state machines in the Trio64V+ and places all registers in their power-on default states. It also initiates several configuration actions, as described in this section.

The PD[28:0] pins are pulled high internally and can be individually pulled low through 10 KΩ resistors. These pull-ups and pull-downs do not affect normal operation of the pins as part of the pixel data bus, but they do force the pins to a definite state during reset. At the rising edge of the reset signal, this state is sampled and the data loaded into the CR36, CR37, CR68 and CR6F registers. The data is used for system configuration, such as system bus and memory parameter selection. The definitions of the PD[28:0] strapping bits at the rising edge of the reset signal are shown in Table 5-1.

Strapping bits 7-5 define the display memory size. However, the S3 BIOS determines this value directly and writes it to CR36_7-5 after reset. Therefore, systems using the S3 BIOS do not need to strap the PD[7:5] pins. Other pins may also not require strapping, depending on the design and bus type.

$\overline{\text{OE}}$[1:0] are driven high during reset. This prevents them from floating low and enabling incorrect data on the configuration strapping pins.

Table 5-1. Definition of PD[28:0] at the Rising Edge of the Reset Signal

CR Bits	PD Bits	Value	Function
	System Bus Select		
CR36_1-0	1-0	00	Reserved
		01	VL-Bus
		10	PCI local bus
		11	Reserved
	Memory Page Mode Select		
CR36_3-2	3-2	00	1-cycle extended data out (EDO) mode
		01	Reserved
		10	2-cycle Extended data out (EDO) mode
		11	Fast page mode
	Enable Video BIOS (VL-Bus only)		
CR36_4	4	0	Disable video BIOS accesses
		1	Enable video BIOS accesses
	Display Memory Size		
CR36_7-5	7-5	000	4 MBytes
		001	Reserved
		010	Reserved
		011	Reserved
		100	2 MBytes
		101	Reserved
		110	1 MByte
		111	Reserved
	Enable Trio64V+ (VL-Bus Only)		
CR37_0	8	0	Disable Trio64V+ except for video BIOS accesses
		1	Enable Trio64V+
CR37_1	9		Reserved
	Video BIOS Size (VL-Bus Only)		
CR37_2	10	0	64 KByte video BIOS
		1	32 KByte video BIOS
	Clock Select		
CR37_3	11	0	Use external DCLK on pin 156 and external MCLK on pin 151 (test purposes only)
		1	Use internal DCLK, MCLK
	RAMDAC Write Snooping		
CR37_4	12	0	Disable $\overline{\text{LOCA}}/\overline{\text{SRDY}}$ for RAMDAC writes
		1	Enable $\overline{\text{LOCA}}/\overline{\text{SRDY}}$ for RAMDAC writes

Table 5-1. Definition of PD[28:0] at the Rising Edge of the Reset Signal (Continued)

CR Bits	PD Bits	Value	Function
CR37_7-5	15-13		Reserved
	$\overline{\text{CAS}}$/$\overline{\text{OE}}$ Low Stretch		
CR68_1-0	17-16	00	approximately 6.5 ns stretch (nominal)
		01	approximately 5 ns stretch (nominal)
		10	approximately 3.5 ns stretch (nominal)
		11	No stretch
	$\overline{\text{RAS}}$ Low Timing Select		
CR68_2	18	0	4.5 MCLKs
		1	3.5 MCLKs
	$\overline{\text{RAS}}$ Pre-Charge Timing Select		
CR68_3	19	0	3.5 MCLKs
		1	2.5 MCLKs
	BIOS Area		
CR68_6-4	22-20		Reserved for use by the video BIOS
	Memory Data Bus Size		
CR68_7	23	0	Memory data bus is 32 bits
		1	Memory data bus is 32 bits (1 MByte) or 64 bits (2 or more MBytes)
		Operating Mode Select	
CR6F_0	24	0	LPB mode
		1	Trio64-compatible mode
	Serial Port I/O Address Select		
CR6F_1	25	0	The Serial Port register is mapped to I/O port 000E8H
		1	The Serial Port register is mapped to I/O port 000E2H
	Serial Port Address Type Select		
CR6F_2	26	0	The Serial Port register is mapped to the I/O port defined by PD25 or can be accessed at its MMIO address at offset FF20H.
		1	The Serial Port register is accessed at its MMIO address only (no I/O)
	$\overline{\text{WE}}$ Delay		
CR6F_4-3	28-27	00	3 units delay
		01	2 units delay
		10	1 unit delay
		11	no delay

Section 6: System Bus Interfaces

The Trio64V+ interfaces to either a PCI bus or a VESA local bus (VL-Bus). This section describes the connections and functional characteristics of these interfaces.

6.1 PCI BUS INTERFACE

The Trio64V+ provides a complete PCI interface. Power-on strapping bits 1-0 must be set to 10b to enable this interface. The pinout and other specifications are in complete conformance with Revision 2 of the the PCI specification. No glue logic is required.

6.1.1 PCI CONFIGURATION

The Vendor ID register (Index 00H) in the PCI Configuration space is hardwired to 5333H to specify S3 Incorporated as the vendor. The Device ID register is hardwired to 8811. The BIOS must use CR2F (= 4xH) to differentiate this chip from other Trio® family products.

Bits 10-9 of the Status register (Index 06H) are hardwired to 01b to specify medium DEVSEL timing. The Class Code register (Index 08H) is hardwired to 30000xxH to specify that the Trio64V+ is a VGA compatible device. Bits 3-0 of the Base Address 0 register (Index 10H) are hardwired to 00H. This indicates that the "prefetchable" bit is cleared to 0, the base register can be located anywhere in a 32-bit address space and the base register is located in memory space.

When the Trio64V+ powers up in a PCI configuration, it defaults to linear addressing and memory mapped I/O enabled at a relocatable base address of 7000 0000H. This allows the PCI system to reconfigure as required for plug and play.

6.1.2 PCI Bus Cycles

Figures 6-1 and 6-2 show the basic PCI read and write cycles respectively. Bit 1 of the PCI Command register (Index 04H) must be set to 1 to allow memory space access. Bit 0 of the PCI Command register must be set to 1 to allow I/O space access.

Figures 6-3 and 6-4 show two examples of PCI bus disconnection. These examples show cases where data is transferred after STOP is asserted. In example A, data is transferred after FRAME is deasserted because the master was not ready (IRDY deasserted on clock 2). In example B, data is transferred before FRAME is deasserted. See revision 2.0 or later of the *PCI Local Bus Specification* for a complete explanation of disconnects. Bit 7 of the CR66 register must be set to 1 to enable PCI disconnects. If bit 3 of CR66 is set to 1, an attempt to write data with the Command FIFO full or to read data with the Command FIFO not empty generates a PCI bus disconnect cycle.

The PCI configuration register space occupies 256 bytes. When a configuration read or write command is issued, the AD[7:0] lines contain the address of the register in this space to be accessed. Figures 6-5 and 6-6 show the configuration read and write cycles respectively. The Trio64V+ supports or returns 0 for the first 64 bytes of configuration space.

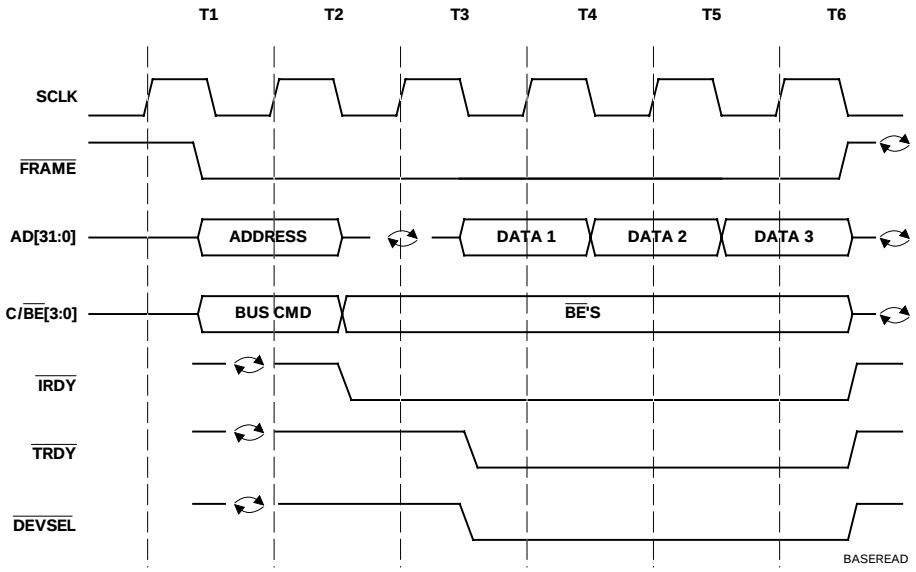


Figure 6-1. Basic PCI Read Cycle

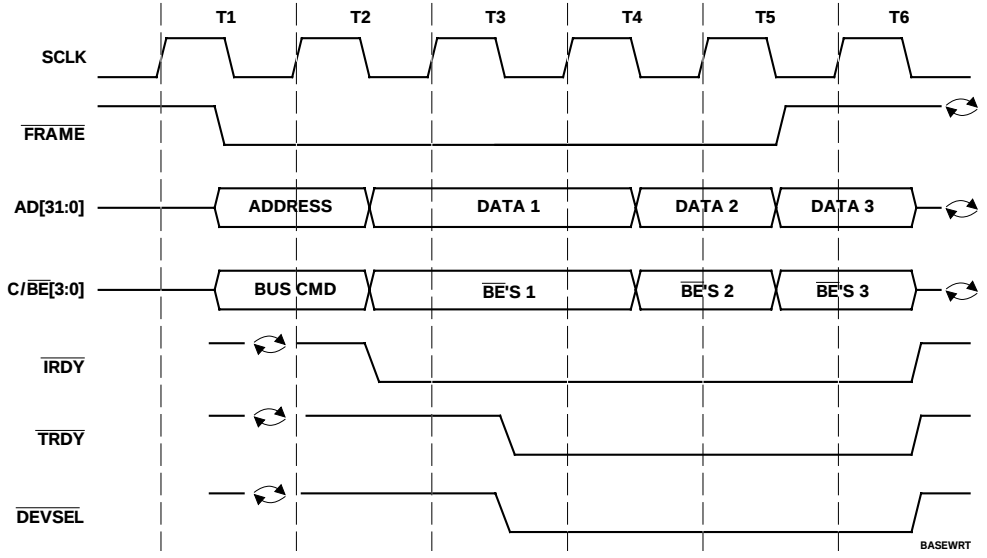


Figure 6-2. Basic PCI Write Cycle

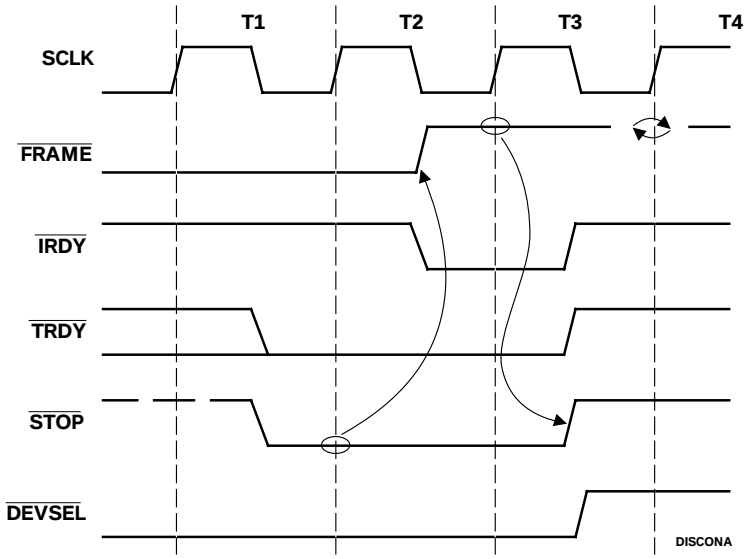


Figure 6-3. PCI Disconnect Example A

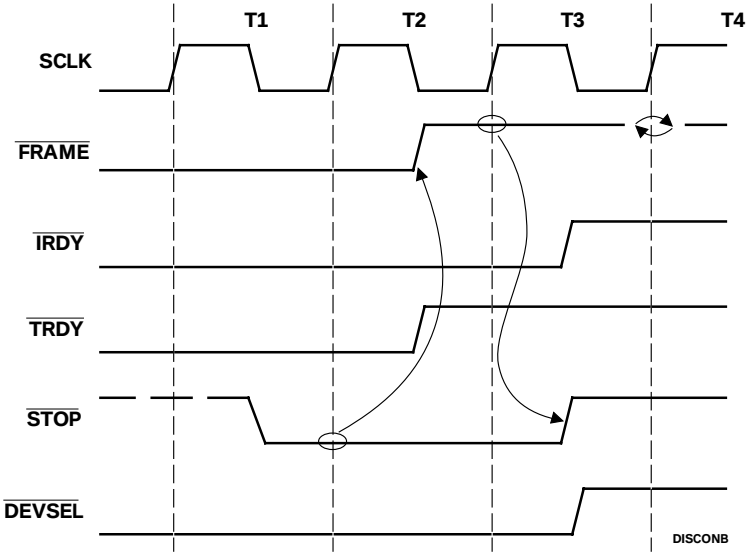


Figure 6-4. PCI Disconnect Example B

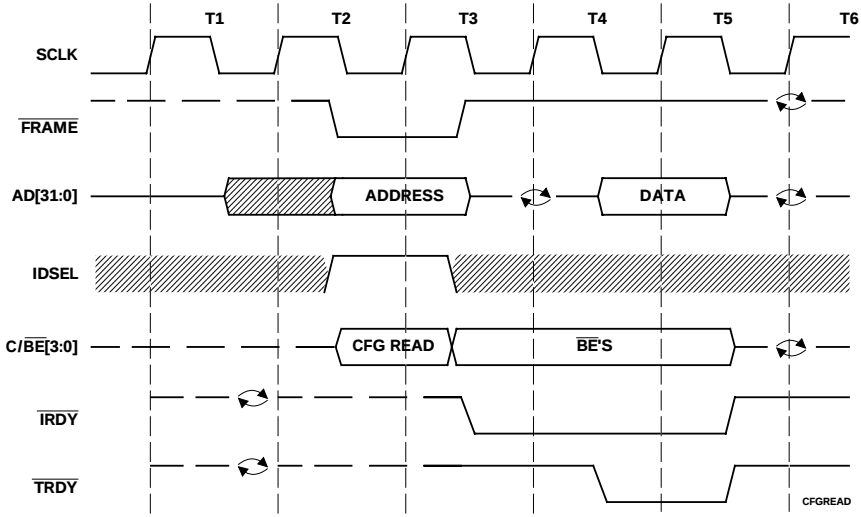


Figure 6-6. PCI Configuration Read Cycle

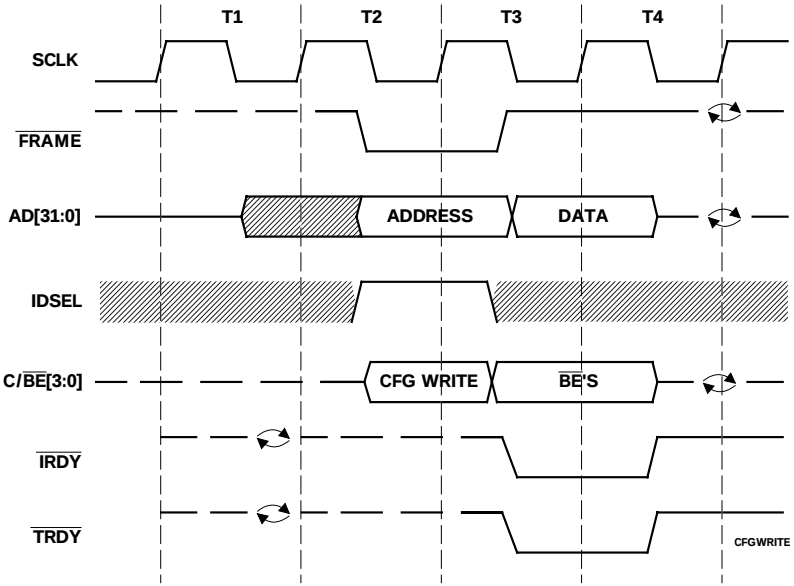


Figure 6-5. PCI Configuration Write Cycle

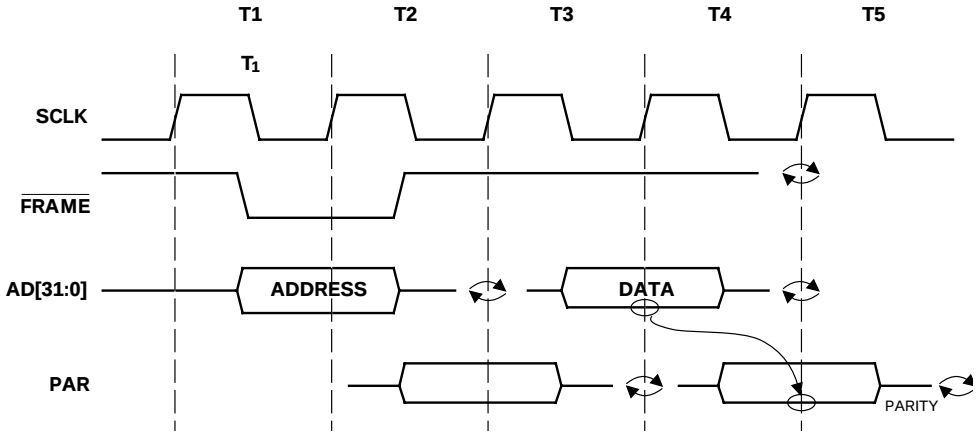


Figure 6-7. Read Parity Operation

The Trio64V+ drives even parity information onto the PAR line during read transactions. This operation is depicted in Figure 6-7.

6.2 VL-BUS INTERFACE

Power-on strapping bits 1-0 must be set to 01b to enable VL-Bus operation. Only SA[22:2] are directly decoded by the Trio64V+. Two inputs (SAUP1, SAUP2) are provided to allow decoding of the upper address lines for Trio64V+ address space accesses. The meanings of SAUP1 and SAUP2 are defined by the following truth table.

Table 6-1. VL-Bus Upper Address Decoding

SAUP2	SAUP1	EFFECT
0	0	Ignored
0	1	Decode Access to register/port address space
1	0	Decode Access to linear addressing address space (video memory)
1	1	Ignored

There are many ways to generate these inputs, depending on the system design.

6.2.1 VL-Bus Cycles

The basic VL-Bus read cycle is shown in Figure 6-8. The address is latched by the Trio64V+ on one of two rising SCLK edges as shown in Figure 6-8 and explained in Note 1.

The basic VL-Bus write cycle is shown in Figure 6-9. The single wait-state is the default configuration. This can be changed to 0 wait-states (SRDY asserted one cycle earlier) by clearing bit 4 of CR40 to 0. The address is latched at the end of T1. By default, write data is latched on the first rising SCLK edge after the assertion of RDYIN.

6.2.2 SRDY Generation

For a VL-Bus configuration, the Trio64V+ raises its SRDY output early in the T_1 cycle and then tri-states it. It then asserts SRDY to signal the end of the cycle. Some systems synchronize or otherwise delay this signal and then assert RDY to the processor. If this is done, this RDY signal should also be fed to the RDYIN input of the Trio64V+ (see Note 3 of Figure 6-9). The Trio64V+ holds read data active until RDYIN is asserted. If the SRDY signal is not intercepted, it should be fed to both the processor RDY input and the Trio64V+ RDYIN input.

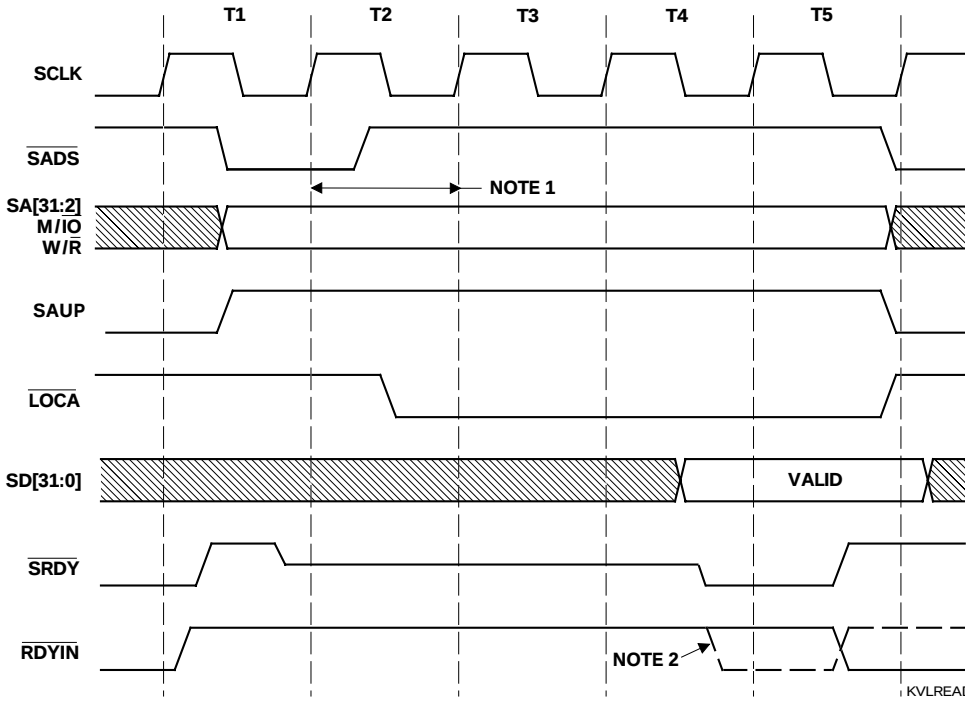


Figure 6-8. VL-Bus Read Cycle

Notes

1. For one decode wait state (bit 4 of CR40 set to 1), the address is latched on the first clock edge indicated here if bit 3 of CR58 is set to 1. If this bit is cleared to 0, the address is latched on the second clock edge indicated. The address is always latched on the first clock edge if bit 4 of CR40 is cleared to 0.
2. The system chip set can delay the $\overline{\text{RDYIN}}$ input by 1 or more cycles. This example assumes a 1 cycle delay, as indicated by the solid line. Note that read data is held valid an extra cycle.

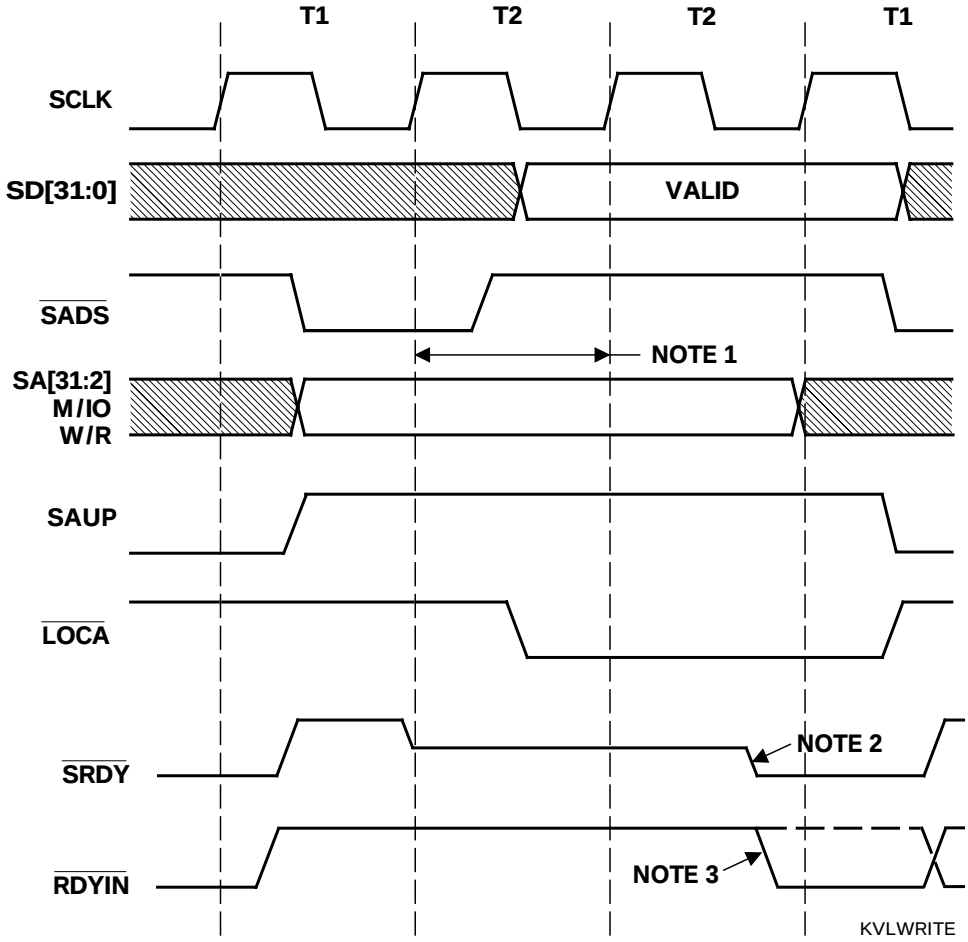


Figure 6-9. 1 Wait-state VL-Bus Write Cycle

Notes

1. For one decode wait state (bit 4 of CR40 set to 1), the address is latched on the first clock edge indicated here if bit 3 of CR58 is set to 1. If this bit is cleared to 0, the address is latched on the second clock edge indicated. The address is always latched on the first clock edge if bit 4 of CR40 is cleared to 0.
2. The wait-state is inserted by setting bit 4 of CR40 to 1 to delay $\overline{\text{SRDY}}$ assertion by 1 cycle from the assertion of $\overline{\text{SADS}}$. This is the default value.
3. Data is latched on the rising SCLK edge following assertion of $\overline{\text{RDYIN}}$.

Section 7: Display Memory

The Trio64V+ supports a DRAM-based video frame buffer. This section describes the various configurations supported, the functional timing for memory accesses and the operation of various register bits that affect memory timing and operation. It also describes how access to display memory is controlled to maximize graphics performance.

7.1 DISPLAY MEMORY CONFIGURATIONS

The Trio64V+ uses fast page mode or extended data out (EDO) DRAMs for its frame buffer, with support for single-cycle EDO operation. The type of DRAM used is specified via power-on strapping of PD[3:2]. All DRAMs can be configured as 256Kx4, 256Kx8 or 256Kx16. A Tech Note lists recommended DRAMs.

For loading reasons, a maximum of 8 DRAM chips can be used for the frame buffer. Table 7-1 shows the supported memory size/chip count configurations.

Table 7-1 Memory Size/Chip Count Configurations

	256Kx4	256Kx8	256Kx16
1 MB	8	4	2
2 MB		8	4
4 MB			8

Figure 7-1 shows 1- and 2-MByte configurations. The 1-MByte memory configuration is available for either a VL-Bus or PCI bus configuration. Either fast page or EDO (1-cycle or standard) memory can be used. The PD bus is 32 bits. This reduces performance and the number of video modes available as compared with 64-bit PD bus operation. Trio64-compatible VAFC feature connector operation can be enabled (SRD_1 = 0).

The configuration options for 2 MBytes of memory are complex, depending on memory type (fast page or EDO), system bus type (VL-Bus or PCI) and feature connector operation type (Trio64-compatible VAFC or LPB feature connector). With 2 MBytes of memory, 64-bit PD bus operation is available unless the Trio64-compatible VAFC feature connector is enabled (SRD_1 = 0). The signals for this feature connector are multiplexed on the upper PD lines. Therefore, 32-bit PD bus operation must be forced (CR68_7 = 0) before feature connector operation is enabled. (Note that this entire discussion applies only to Trio64-compatible VAFC feature connector operation and not LPB connector operation, which is selected by SRD_1 = 1.)

If only fast page memory is to be used, $\overline{OE0}$ can be connected to both the 1st and 2nd MByte. Pin 124 always outputs $\overline{OE0}$. Pin 50 also outputs $\overline{OE0}$ with fast page memory when SRA_6 = 0 for a PCI configuration. Figure 7-1 shows pin 50 connected to the 2nd MByte DRAMs' $\overline{OE}$ inputs. However, pin 124 could be connected to the $\overline{OE}$s (and must be for a VL-Bus configuration). In either case, forcing the PD bus to 32 bits turns off all control signal activity for the 2nd MByte so feature connector activation is allowed.

If EDO memory is to be used with a 2-MByte configuration, the 2nd MByte DRAM $\overline{OE}$ pins must be connected to pin 50 of the Trio64V+ if feature connector activation is required. In this case, pin 50 outputs $\overline{OE1}$ when SRA_6 = 0 for a PCI configuration. With EDO memory, 2 MBytes of memory and the feature connector enabled, $\overline{OE1}$ is held high throughout the memory cycle. This is required to turn off output from the EDO DRAMs in the 2nd MByte. The 1st MByte is still active because it is connected to the still-functioning $\overline{OE0}$.

Connecting pin 50 to the 2nd MByte DRAM $\overline{OE}$s works for both fast page and EDO DRAM in PCI configurations whether or not feature connector operation is to be enabled. It cannot be used for VL-bus configurations. In addition, this configuration cannot be upgraded to 4 MBytes.

If feature connector operation is never required, $\overline{OE0}$ (pin 124) can be used to drive both the 1st and 2nd MBytes of both fast page and EDO DRAM configurations. This configuration can be upgraded to 4 MBytes for PCI bus systems.

A 4-MByte configuration requires $\overline{RAS1}$ to select the 3rd and 4th MByte. The Trio64V+ outputs $\overline{RAS1}$ on pin 50 for PCI configurations when bit 6 of SRA is set to 1. $\overline{RAS1}$ is not available for VL-Bus configurations, limiting memory size to 2 MBytes. Figure 7-2 shows a 4-MByte configuration using $\overline{RAS1}$. The Trio64-compatible VAFC feature connector cannot be used with 4 MBytes of memory and must never be enabled for 4-MByte configurations.

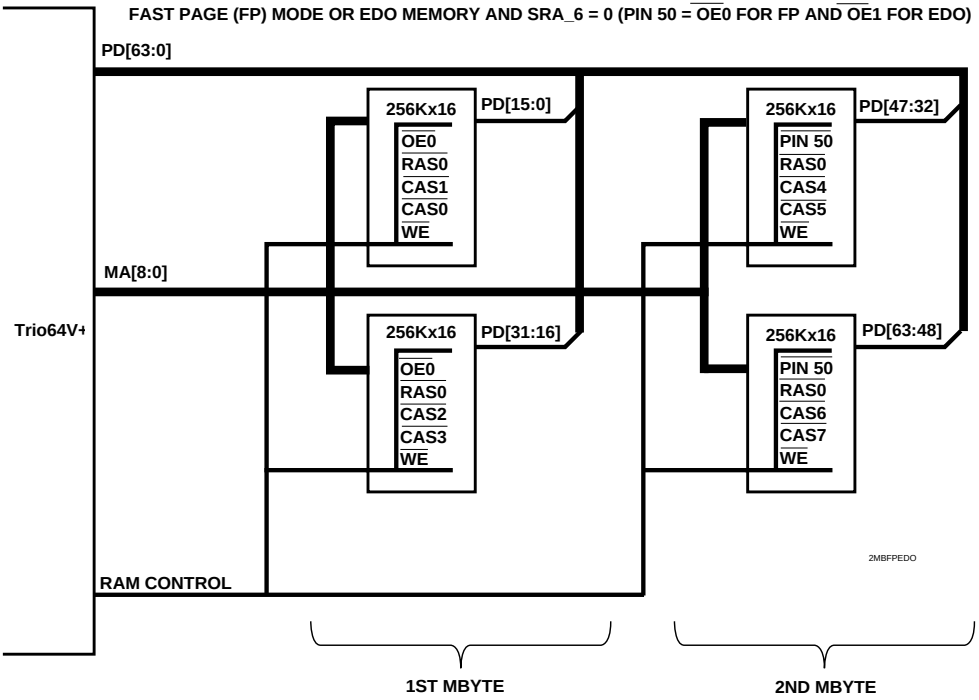


Figure 7-1. 1- or 2-MByte DRAM Configuration

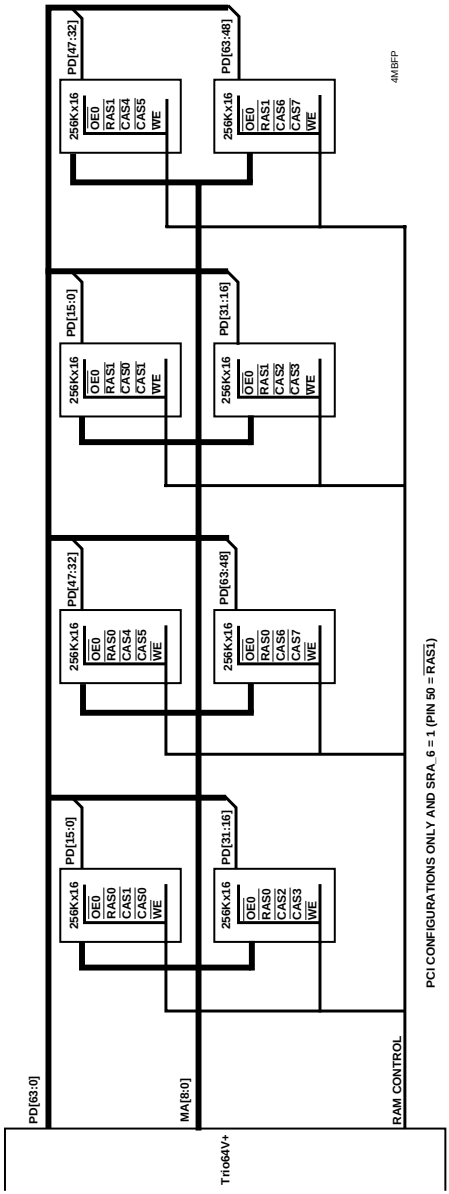


Figure 7-2. 4-MByte DRAM Configuration

7.2 DISPLAY MEMORY REFRESH

The Trio64V+ uses the standard $\overline{CAS}$ before $\overline{RAS}$ DRAM refresh method. The functional timing for this can be found in any standard DRAM data book.

The number of refresh cycles performed per horizontal line is determined by bit 6 of CR11. If bit 2 of CR3A is set to 1, the number of refresh cycles per horizontal line is determined by the setting of bits 1-0 of CR3A. Refreshes are performed during the horizontal blanking period.

7.3 DISPLAY MEMORY FUNCTIONAL TIMING

Figure 7-3 shows the functional timing for a fast page mode read cycle. This also shows how certain parameters for various control signals can be adjusted to meet the access time require-

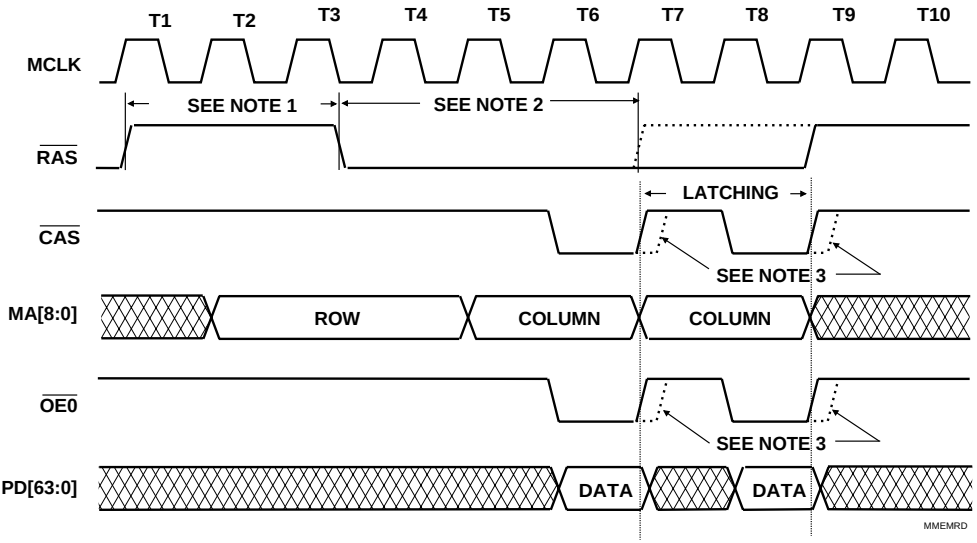


Figure 7-3. Fast Page Mode Read Cycle

Notes

1. The minimum $\overline{RAS}$ precharge time can be adjusted from 2.5 to 3.5 MCLKs via CR68_3, to 1.5 MCLKs via MM81EC_16, and reduced by 0.5 MCLK via CR58_7.
2. This figure shows a $\overline{RAS}$ low time for a single column access of 3.5 MCLKs. (The dashed line shows the $\overline{RAS}$ signal if the second page mode cycle were to be eliminated.) This $\overline{RAS}$ active time can be changed to 4.5 MCLKs via CR68_2 or to 2.5 MCLKs via MM81EC_15 and increased by 0.5 MCLK via CR58_7.
3. The $\overline{CAS}$ and $\overline{OE}$ active (low) times can be stretched via bits 1-0 of CR68.

ments of a variety of DRAMs. Bits 1-0 of CR68 allow the pulse widths of the CAS and OE signals to be adjusted. Bit 2 of CR68, bit 15 of MM81EC and bit 7 of CR58 allow adjustment of the RAS low time. Bit 3 of CR68, bit 16 of MM81EC and bit 7 of CR58 allow adjustment of the RAS precharge (high) time. The settings in CR68 can be made by power-on strapping of PD[23:16] at reset. All settings can be changed by programming after reset.

Figure 7-4 shows the functional timing for a fast page mode write cycle. The RAS and CAS signals can be adjusted as explained for the read cycle above. The WE can be delayed via bits 4-3 of CR6F.

Figure 7-5 shows the functional timing for a fast page mode read/modify/write cycle. This is a 1-wait state cycle.

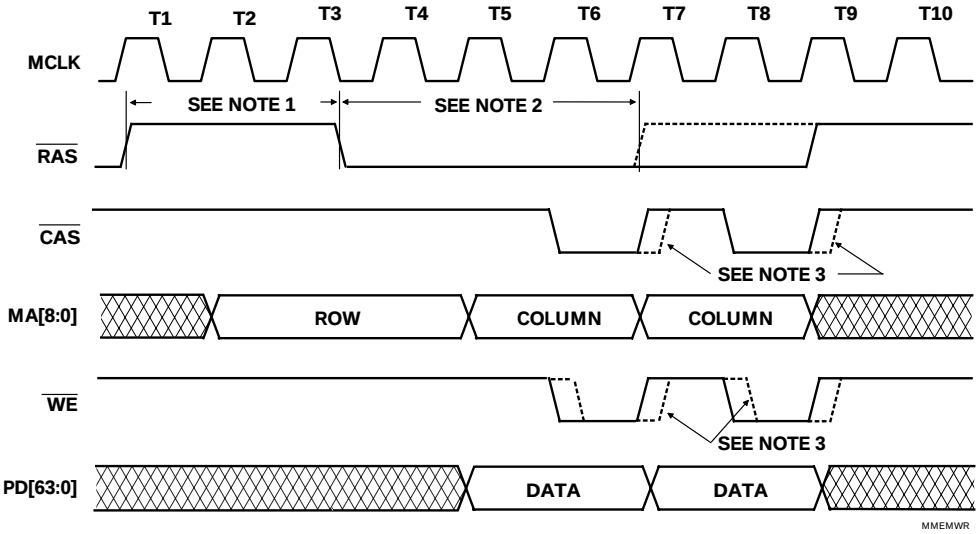


Figure 7-4. Fast Page Mode Write Cycle

Notes

1. The minimum RAS precharge time can be adjusted from 2.5 to 3.5 MCLKs via CR68_3, to 1.5 MCLKs via MM81EC_16, and reduced by 0.5 MCLK via CR58_7.
2. This figure shows a RAS low time for a single column access of 3.5 MCLKs. (The dashed line shows the RAS signal if the second page mode cycle were to be eliminated.) This RAS active time can be changed to 4.5 MCLKs via CR68_2 or to 2.5 MCLKs via MM81EC_15 and increased by 0.5 MCLK via CR58_7.
3. The CAS active (low) time can be stretched via bits 1-0 of CR68 and the WE active time delayed via bits 4-3 of CR6F.

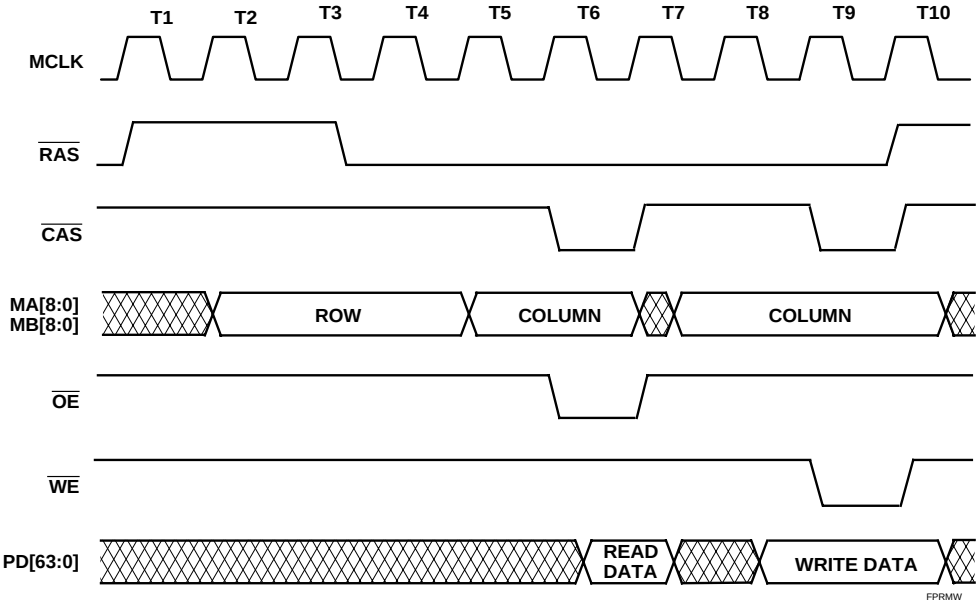


Figure 7-5. Fast Page Mode Read/Modify/Write Cycle

Figure 7-6 shows the functional timing for an Extended Data Out (EDO) mode read cycle. One difference between an EDO read cycle and a fast page mode read cycle is that EDO memory holds the data valid longer, allowing the data to be latched one cycle later (rising edges of T8 and T10). This allows the use of slower access time memory or a faster MCLK. Therefore, the last page access (or first for a single access) is one MCLK later. Note that $\overline{RAS}$, the last $\overline{CAS}$ and $\overline{OE}$ are all stretched one MCLK and $\overline{OE}$ is held low for the entire cycle instead of being pulsed as in a fast page mode cycle.

The timing adjustments for $\overline{RAS}$ and for $\overline{CAS}$/$\overline{OE}$/$\overline{WE}$ as described above for a fast page mode read cycle also apply to EDO cycles. Note that if the minimum $\overline{RAS}$ active time is specified

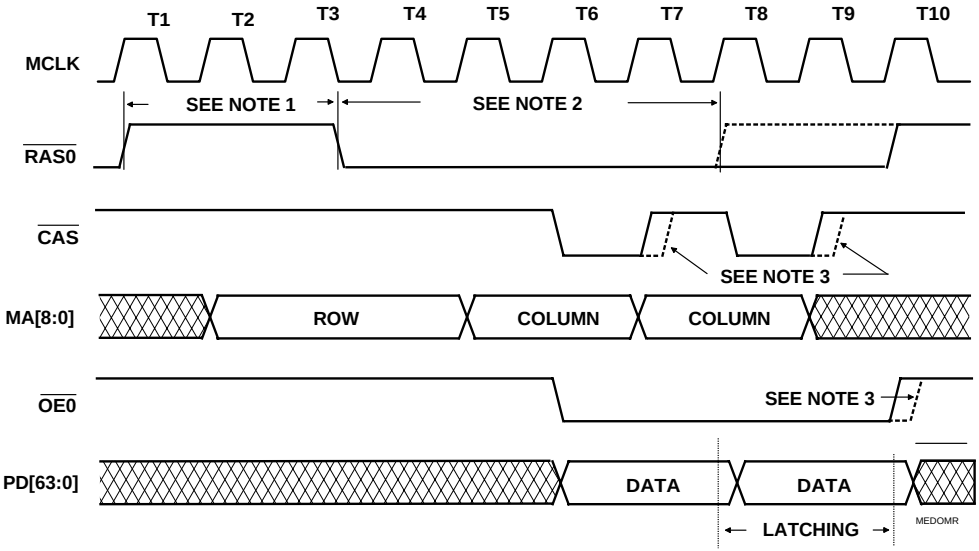


Figure 7-6. EDO Mode Read Cycle

Notes

1. The minimum $\overline{RAS}$ precharge time can be adjusted from 2.5 to 3.5 MCLKs via CR68_3, to 1.5 MCLKs via MM81EC_16, and reduced by 0.5 MCLK via CR58_7.
2. This figure shows a $\overline{RAS}$ low time for a single column access of 3.5 MCLKs. (The dashed line shows the $\overline{RAS}$ signal if the second page mode cycle were to be eliminated.) This $\overline{RAS}$ active time can be changed to 4.5 MCLKs via CR68_2 or to 2.5 MCLKs via MM81EC_15 and increased by 0.5 MCLK via CR58_7.
3. The $\overline{CAS}$ and $\overline{OE}$ active (low) times can be stretched via bits 1-0 of CR68.

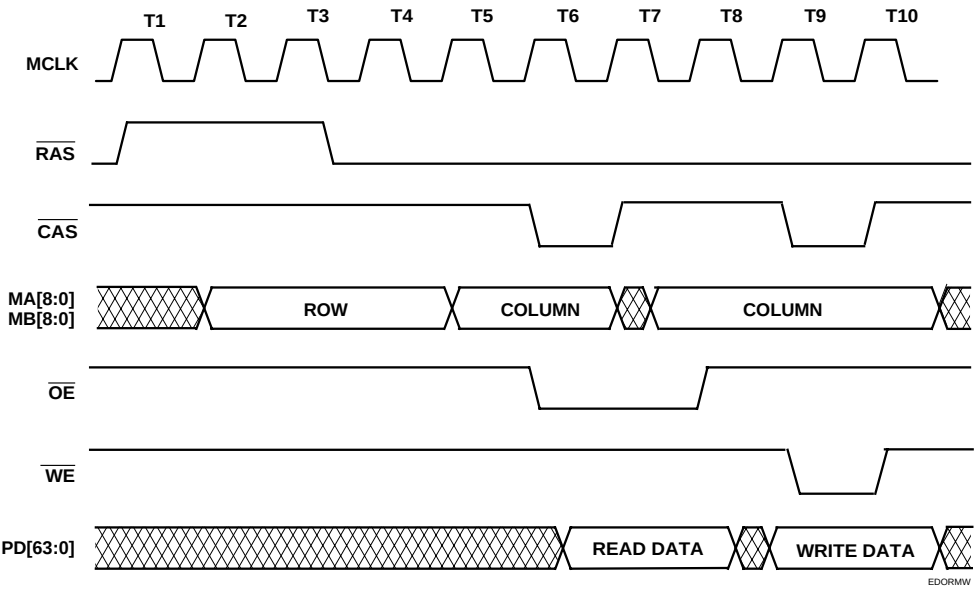


Figure 7-7. EDO Mode Read/Modify/Write Cycle

as 3.5 MCLKs, the actual minimum for a single EDO read cycle will be 4.5 MCLKs.

The cycle depicted in Figure 7-6 is for 64-bit PD bus operation (2 MBytes of memory and feature connector operation disabled). If the feature connector is enabled, $\overline{OE0}$ only enables data output on PD[31:0] and $\overline{OE1}$ (not shown) stays high the entire cycle to disable output on PD[63:32].

An EDO write cycle is functionally the same as a fast page mode write cycle.

Figure 7-7 shows the functional timing for an EDO mode read/modify/write cycle. Since read data is latched later than for a fast page mode cycle, there is less time available between the read and write.

7.4 1-CYCLE EDO DRAM SUPPORT

Bits 3-2 of CR36 are cleared to 00b to indicate that 1-cycle EDO DRAM operation is being used.

The functional timing for 1-cycle EDO reads and writes is provided by Figure 7-8. The DRAM drives valid read data after the $\overline{CAS}$ falling edge at T5. The chip latches the data on the next falling $\overline{CAS}$ edge. Note that a dummy cycle is required at the end to latch the last read. Write data is latched by the DRAM on the falling edge of $\overline{CAS}$. No dummy cycle is required, so RAS rises one cycle earlier than shown in Figure 7-8 and the last $\overline{CAS}$ shown in the figure does not occur.

Figure 7-9 shows a read/modify/write cycle with 1-cycle EDO operation. A dummy cycle is added between the read and write.

CPU (i.e., linear addressing) access to memory is not supported with 1-cycle EDO. 2-cycle EDO operation will automatically be used for this function.

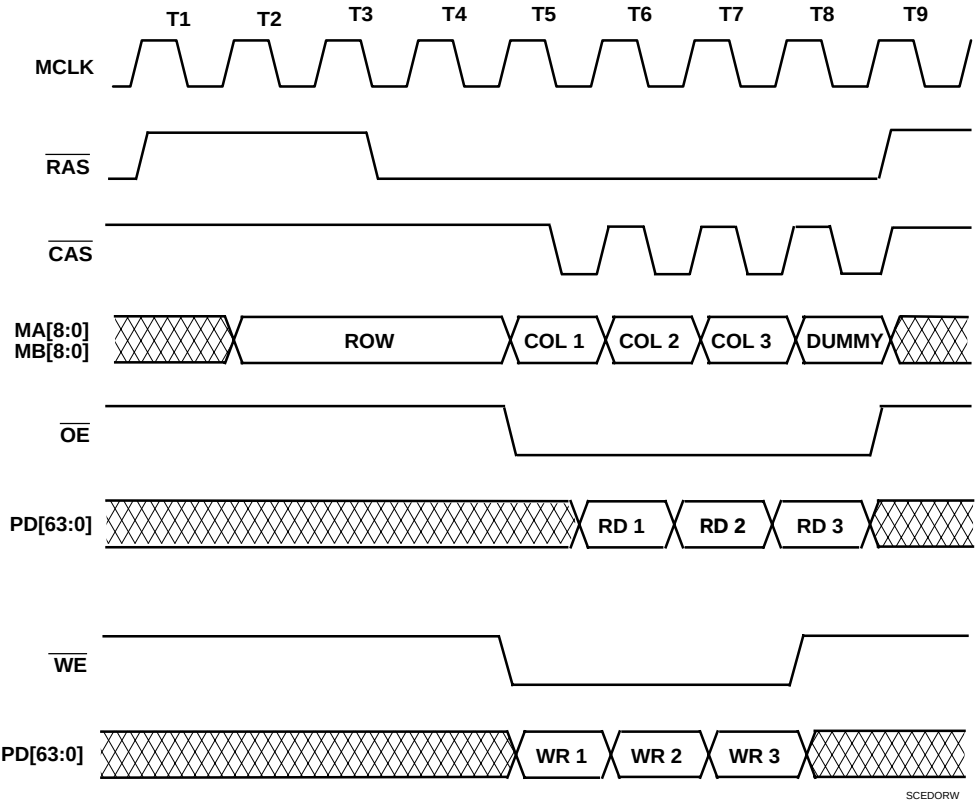


Figure 7-8. 1-Cycle EDO Mode Read/Write

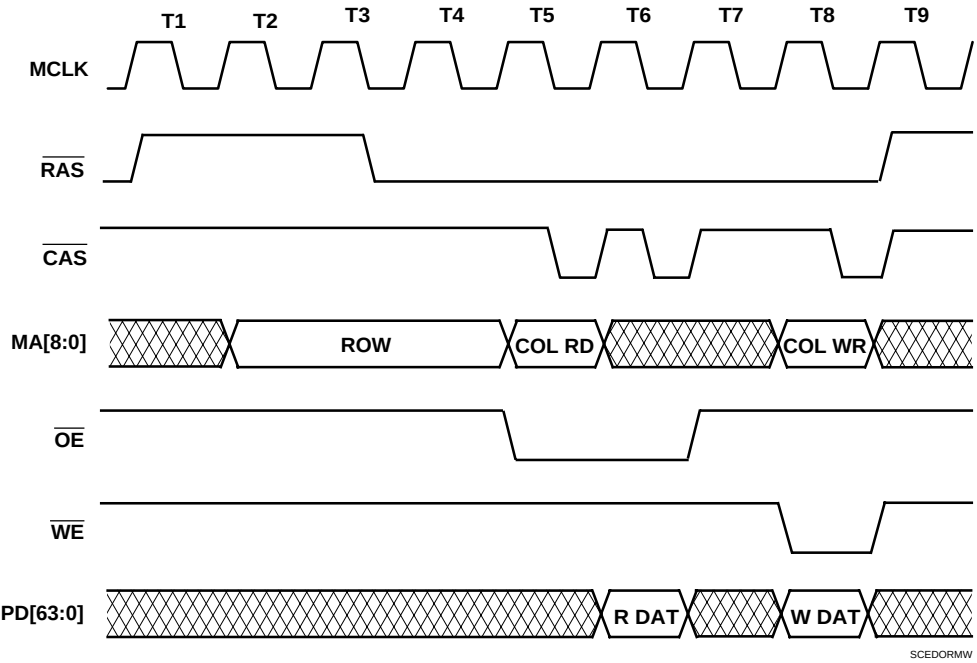


Figure 7-9. 1-cycle EDO Read/Modify/Write Cycle

7.5 DISPLAY MEMORY ACCESS CONTROL

A number of processes compete for access to display memory. These competing processes are (in decreasing order of access priority):

- Primary Stream high (N parameter)
- Secondary Stream high (N parameter)
- RAM refresh
- Hardware cursor fetch
- LPB (M parameter)
- CPU accesses (M parameter)
- Graphics Engine accesses (M parameter)
- Primary Stream low (N parameter)
- Secondary Stream low (N parameter)

The two processes with high and low priorities have associated threshold register fields (MM81EC, bits 14-10 and 9-5). If the current count is equal to or above the threshold level for a process, that process is given its low priority. Once the threshold is passed, the process is given its high priority.

The primary and secondary stream processes are responsible for screen refreshing and are associated with the N parameter (CR60_7-0). RAM refresh and hardware cursor fetch occur during blanking when FIFO fetches are not occurring. The other processes are associated with the M parameter (CR54_2, 7-3). Note that these are not the same as the PLL M and PLL N parameters used to specify the clock synthesizer frequencies.

When the Trio64V+ transfers data from display memory to the primary or secondary stream FIFO, the N parameter specifies the number of MCLKs available for FIFO filling before memory control is given up for M parameter processes. Note that this parameter is only effective when both FIFO threshold values are equal to or above the threshold level and therefore have low priority. Because of this, the FIFO threshold values have by far the greatest effect on performance. The N and M parameter settings will normally have little effect and can be left at their initial BIOS settings.

When N is effective and when N MCLKs have been used or the FIFO is filled, whichever comes first, the Trio64V+ then allows the other display memory processes access to memory. Filling of the FIFO also stops at the end of active display. FIFO filling cannot begin again until the scan line position defined by the Start Display FIFO register (CR3B), which is normally programmed with a value 5 less than the value programmed in CR0 (horizontal total). This provides time during the horizontal blanking period for RAM refresh and hardware cursor fetch.

The M parameter specifies the number of MCLKs available for shown in the bullet list above. When this number of MCLKs has occurred, memory control is returned for FIFO filling. If during the processing period controlled by the M parameter there is time when there are no memory access requests and the M value has not been reached, control is immediately returned to FIFO filling as specified by the N parameter.

Note that the M and N parameters should only be changed with the screen turned off. This is done by setting bit 5 of SR1 to 1.

Section 8: RAMDAC Functionality

For 8 bits/pixel modes, the Trio64V+ internal 24-bit RAMDAC provides three 256 6-bit word color look-up table (LUT) RAMs feeding three 8-bit DACs. A clock doubled mode is also provided for 8 bits/pixel modes. A 24-bit LUT bypass is provided for 15/16- and 24-bit color modes. A special 640x480x24 mode is provided to allow true color operation with 1 MByte of memory. The block diagram for the internal RAMDAC is shown in Figure 8-1.

8.1 OPERATING MODES

Depending on the setting of CR67_3-2, the following operating modes are available:

- Streams Processor Off
- Streams Processor On
- Streams Processor On - secondary stream overlaid on VGA Mode 13 background

With the Streams Processor off (CR67-3-1 = 00b), data from the video FIFO (memory) is processed by another Trio64V+ module and then passed directly to the RAMDAC. (Figure 8-1 shows the data going through the Streams Processor, but all Streams Processor functions are bypassed.) This mode is used for those video modes not supported by the Streams Processor. This includes all VGA modes except modes D, E, 10, 12

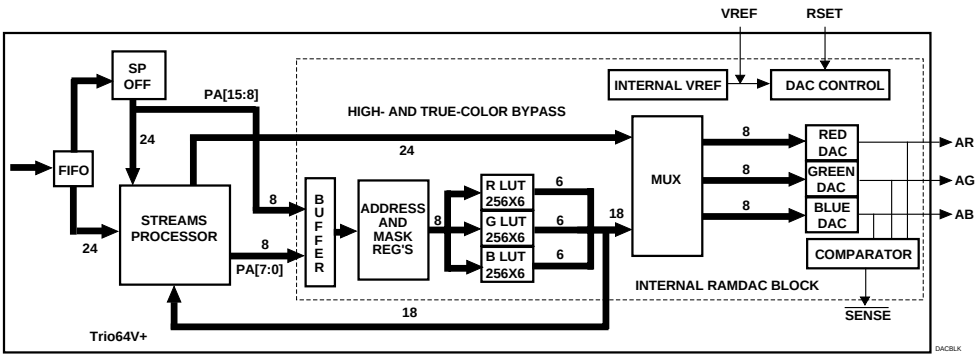


Figure 8-1. Internal RAMDAC Block Diagram

Table 8-1 Trio64V+ Color Modes

Color Mode	CR67 Bits 7-4	PA Bits	MAX DCLK	MAX Pixel Rate	Description
0	0000	7:0	80 MHz	80 MHz	8-bit pseudo-color (LUT) - Default
8	0001	15:0	67.5 MHz	135 MHz	Two 8-bit pseudo-color (LUT)
9	0011	15:0	80 MHz	80 MHz	15-bit high-color (LUT Bypass)
10	0101	15:0	80 MHz	80 MHz	16-bit high-color (LUT Bypass)
12	0000	23:0	75 MHz	25 MHz	640x480x24-bit packed (LUT Bypass)
13	1101	23:0	50 MHz	50 MHz	24-bit true-color (LUT Bypass)

and 13, all interlaced modes and the clock-doubled 8 bits/pixel mode.

With the Streams Processor on (CR67_3-2 = 11b), memory data is passed directly to the Streams Processor. 8 bits/pixel (palettized) data is passed directly to the RAMDAC, where it is interpreted by the color look-up table and returned to the Streams Processor as RGB666. This and other input data types are converted to RGB888 (if required) and then sent to the RAMDAC via the high and true color bypass.

8.2 COLOR MODES

The Trio64V+ internal RAMDAC provides 6 color modes of the following 3 primary types:

1. 8 bits (low byte of the internal pixel address bus) are latched each pixel clock and are used to select a LUT location.
2. 16 bits (low two bytes of the internal pixel address bus) are latched each pixel clock. These select two consecutive LUT locations, the data from which is clocked out to the DACs at twice the pixel clock rate.
3. 15 or 16 bits (lower two bytes of the internal pixel address bus) or 24 bits (all three bytes of the internal address bus) are transferred directly to the DACs each pixel clock.

Each of the 6 color modes is listed in Table 8-1. The desired mode is selected by programming bits 7-4 of CR67.

8.2.1 8 Bits/Pixel - Mode 0

Mode 0 is selected by setting bits 7-4 of CR67 to 0000b. In this mode, the low 8 internal pixel address bus bits are ANDed with the contents of the Pixel Read Mask register (3C6H). The result of the AND operation selects one of 256 LUT locations. This results in the output of 6 bits of color information to each of the DACs.

8.2.2 Output-doubled 8 Bits/Pixel - Mode 8

This mode is selected by setting bits 7-4 of CR67 to 0001b. In this mode, latching of pixel data from the lower two bytes of the internal pixel data bus is based on the pixel clock (VCLK) and output of pixel data from the latches to the DACs is based on an internal clock running at twice the VCLK rate. Either bit 4 or bit 6 of SR15 must be set to 1 when this mode is selected and bit 7 of SR18 must also be set to 1.

This mode processes two pixels per VCLK with a maximum VCLK rate of 67.5 MHz. This results in an effective pixel output clock rate of 135 MHz.

The internal pixel bus bits are ANDed with the contents of the Pixel Read Mask register. The result of the AND operation selects one of 256 LUT locations. This results in the output of 6 bits of color information to each of the DACs.

8.2.3 15/16-Bits/Pixel - Modes 9 and 10

These modes are selected by setting bits [7:4] of CR67 to 0011b (15 bits/pixel) or 0101b (16 bits/pixel). In either case, one pixel is transferred on the lower two bytes of the internal pixel bus each VCLK cycle. This data is sent directly to the DACs via the LUT bypass.

8.2.4 Packed 24 Bits/Pixel - Mode 12

This mode is selected by setting bit 3 of SRB to 1, bits 7-4 of SRB to 0111b and bits 7-4 of CR67 to 0000b. It is used for a resolution of 640x480x24. Each pixel is stored in 24 bits of memory, allowing operation with 1 MByte of memory. One byte of color data is retrieved each DCLK. DCLK is internally divided by 3 to provide the VCLK to the internal RAMDAC. Thus, one pixel is latched into the RAMDAC every three DCLKs. Bits 4-3 of CR65 must be set to 10b for this mode to delay $\overline{\text{BLANK}}$ to the RAMDAC by 2 DCLKs. The internal hardware cursor cannot be used in this mode and no acceleration is provided.

8.2.5 24 Bits/Pixel - Mode 13

This mode is selected by setting bits 7-4 of CR67 to 1101b. One pixel is transferred to the DACs each VCLK cycle via the LUT bypass.

8.3 RAMDAC REGISTER ACCESS

The standard VGA RAMDAC register set (3C6H - 3C9H) is used to access the internal RAMDAC registers.

8.4 RAMDAC SNOOPING

For PCI bus configurations, setting bit 5 of the Command configuration space register (Index 04H) to 1 causes the Trio64V+ to snoop for RAMDAC writes. This means that the Trio64V+ will write the data to its local RAMDAC but will not claim the cycle by asserting $\overline{\text{DEVSEL}}$. This allows the ISA controller to also generate a write cycle to a secondary RAMDAC. The Trio64V+ always provides the data for RAMDAC reads.

If bit 5 of the PCI Command register is cleared to 0, the Trio64V+ claims all RAMDAC read and write cycles.

Bits 2-0 of CR34 allow handling of PCI master aborts and retries to be individually enabled or disabled during RAMDAC cycles.

If power-on strapping bit 12 (CR37, bit 4) is pulled low at reset for a VL-Bus configuration, $\overline{\text{LOCA}}$ and $\overline{\text{SRDY}}$ are not generated by the Trio64V+ for RAMDAC write accesses. The Trio64V+ generates write cycles to the local RAMDAC and the ISA controller also generates cycles to an off-board RAMDAC (mirroring). RAMDAC reads are always from the local RAMDAC.

If bit 7 of CR37 is set to 1, the Trio64V+ claims all RAMDAC read and write cycles ($\overline{\text{LOCA}}$ and $\overline{\text{SRDY}}$ are generated).

8.5 $\overline{\text{SENSE}}$ GENERATION

The internal RAMDAC contains analog voltage comparators. These drive the internal $\overline{\text{SENSE}}$ signal active low whenever the output on any of the AR, AG or AB pins exceeds 330 mV $\pm$ 20%. The state of this internal signal can be read via bit 4 of 3C2H. This information can be used to detect the existence and type of monitor (color/mono) connected to the system.

8.6 POWER CONTROL

The Trio64V+ provides a $\overline{\text{PDOWN}}$ input pin. When a logic 0 signal is driven to this pin, the RGB analog outputs are turned off.

Section 9: Clock Synthesis and Control

The Trio64V+ contains two phase-locked loop (PLL) frequency synthesizers. These generate the DCLK (video clock) and MCLK (memory clock) signals for the graphics controller block.

9.1 CLOCK SYNTHESIS

Each PLL scales a single reference frequency input on the XIN pin. By placing a parallel-resonant crystal between the XOUT output pin and the XIN pin, the reference frequency is generated by the Trio64V+'s internal oscillator. Alternately, a CMOS-compatible clock input can be connected to XIN to provide the reference frequency.

The frequency synthesized by each PLL is determined by the following equation:

$$f_{OUT} = \frac{(M+2)}{(N+2)\times 2^{R}} \times f_{REF}$$

where R = 0, 1, 2 or 3

Programmed PLL M and PLL N values should be consistent with the following constraints:

1. $135\,MHz \leq \frac{(M+2)f_{REF}}{(N+2)} \leq 270\,MHz$

2. min N ≥ 1

Note that values used for the parameters are the integer equivalents of the programmed value. In particular, the R value is the code, not the actual frequency divisor.

The PLL M value can be programmed with any integer value from 1 to 127. The binary equivalent of this value is programmed in bits 6-0 of SR11 for the MCLK and in bits 6-0 of SR13 for the DCLK. The PLL feedback loop frequency from the voltage controlled oscillator stage is scaled by dividing that frequency by (M+2).

The PLL N value can be programmed with any integer value from 1 to 31. The binary equivalent of this value is programmed in bits 4-0 of SR10 for the MCLK and in bits 4-0 of SR12 for the DCLK. The reference frequency is divided by (N+2) before being fed to the phase detector stage of the PLL.

The PLL R value is a 2-bit range value that can be programmed with any integer value from 0 to 3. The R value is programmed in bits 6-5 of SR 10 for MCLK and bits 6-5 of SR12 for DCLK. This value codes the selection of a frequency divider for the PLL output. This is shown Table 9-1.

Table 9-1. PLL R Parameter Decoding

R-Range Code	Frequency Divider
00	1
01	2
10	4
11	8

The entire PLL block diagram is shown in Figure 9-1.

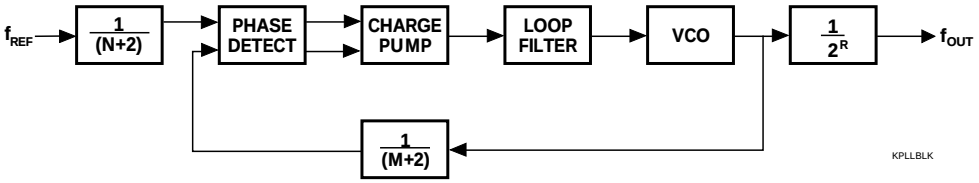


Figure 9-1. PLL Block Diagram

The following sequence may be followed to arrive at M and N values for any mode.

1. Calculate an R which does not violate the following constrains:

   $135\,MHz < 2^R \times f_{OUT} \leq 270\,MHz$

2. Start with N1 = 1 and calculate:

   $$M = [\frac{f_{OUT} \times (N+2) \times 2^R}{f_{REF}}] - 2$$

3. Determine if the following constraint is met:

   $$0.995\ f_{OUT} < \frac{(M+2)\ f_{REF}}{(N1+2)\ 2^{N2}} < 1.005\ f_{OUT}$$

4. If the constraint in step 3 is met, the M and N values used will generate the desired frequency (within the specified tolerance). If the constrain is not met, repeat steps 2 and 3 with N increased by 1 each time until the constraint in step 3 is met. Note that multiple combinations of M and N are possible for a given output frequency.

9.2 CLOCK REPROGRAMMING

The Trio64V+ powers up with a DCLK frequency of 25.175 MHz (standard VGA) and an MCLK frequency of 45 MHz. The DCLK frequency can be changed to 28.322 MHz by setting bits 3-2 of 3C2H to 01b and can be changed back to 25.125 MHz by setting bits 3-2 of 3C2H to 00b. The loading of the DCLK frequency values requires that bit 1 of SR15 be set to 1.

All other DCLK frequencies must be generated by re-programming SR12 and SR13. The new PLL parameter values can be loaded in one of two ways. If bit 5 of SR15 is cleared to 0, the new DCLK frequency is loaded by setting bit 1 of SR15 to 1 and then setting bits 3-2 of 3C2H to 11 (if they are not already programmed to this value). Bit 1 of SR15 should be left at a value of 1. Actual loading will be delayed for a short but variable period of time.

The alternate approach to loading the new DCLK frequency is to program bits 3-2 of 3C2 to 11 (if they are not already programmed to this value). Next, program SR12 and SR13 and then toggle bit 5 of SR15 by programming it to a 1 and then a 0. This immediately loads the DCLK and MCLK frequencies (no variable delay). For example, pseudocode to change DCLK to the frequency specified by PLL parameter values of 34H and 56H is:

```
3C2 ⇐ 6FH  ; DCLK specified by
           ; SR12 and SR13
3C4 ⇐ 12H  ; SR12 index
3C5 ⇐ 34H  ; SR12 PLL value
3C4 ⇐ 13H  ; SR13 index
3C5 ⇐ 56H  ; SR13 PLL value
3C4 ⇐ 15H  ; SR15 index
3C5 ⇐ RMW  ; Use read/modify/write to
           ; set bit 5 to 1 and leave
           ; other bits unchanged
3C5 ⇐ RMW  ; Use read/modify/write to
           ; clear bit 5 to 0 and
           ; leave other bits
           ; unchanged
```

Either loading approach should work. The second (immediate loading) approach helps with system testing since the timing of the load is predictable. The first approach (via bit 1 of SR15) has the advantage of separating the loading of DCLK from that of MCLK.

After power-up, all MCLK frequency changes must be made by re-programming SR10 and SR11. If bit 5 of SR15 is cleared to 0, the new frequency does not take effect until a 1 has been written to bit 0 of SR15. This bit must then be cleared to 0 to prevent repeated loading. Actual loading will be delayed for a short but variable period of time.

As explained above for DCLK, toggling bit 5 of SR15 (0,1,0) immediately loads both the DCLK values in SR12 and SR13 and the MCLK values in SR10 and SR11.

9.3 DCLK CONTROL

DCLK is generated by the internal clock synthesizer. VCLK is the signal used to clock pixel data into the internal RAMDAC. For most modes of operation, VCLK is generated directly from DCLK and has the same frequency and phase (neglecting internal gate delays). Bit 0 of CR67 provides the option to invert DCLK before it becomes VCLK.

In mode 8, the internal RAMDAC requires two clocks. The normal internal DCLK frequency is divided by two via bit 4 of SR15 to provide the standard VCLK input. Undivided DCLK provides the other input. This clock can be inverted via bit 6 of SR15.

Certain 4 bits/pixel modes require that DCLK be halved. This is the case for bit 6 of AR10 set to 1 and bit 4 of CR3A cleared to 0 and is enabled by setting bit 4 or SR15 to 1 and clearing bit 3 of CR33 to 0.

Section 10: Streams Processor

The S3 Streams Processor processes data from the graphics frame buffer, composes it and outputs the result to the internal DACs for generation of the analog RGB outputs to the monitor. The general data flow is shown in Figure 10-1. Note that the DAC shown in this figure is inside the Trio64V+.

10.1 INPUT STREAMS

The processor can compose data from up to 3 independent streams as shown in Figure 10-1:

1. Primary Stream - RGB graphics data
2. Secondary Stream - RGB or YUV/YCbCr (video) data from another region within the frame buffer
3. Hardware Cursor - 64x64x2 cursor, either Microsoft or X-11 definition

Regardless of the input formats, the Streams Processor creates a composite RGB-24 (8.8.8) output to the DACs. This means that, for example, RGB-8 pseudo-color graphics data can be overlaid with true-color-equivalent (24 bits/pixel) video data. The result is improved video quality and/or reduced memory bandwidth requirements as compared with systems that require both graphics and video to be stored in the same frame buffer format. In certain modes, the

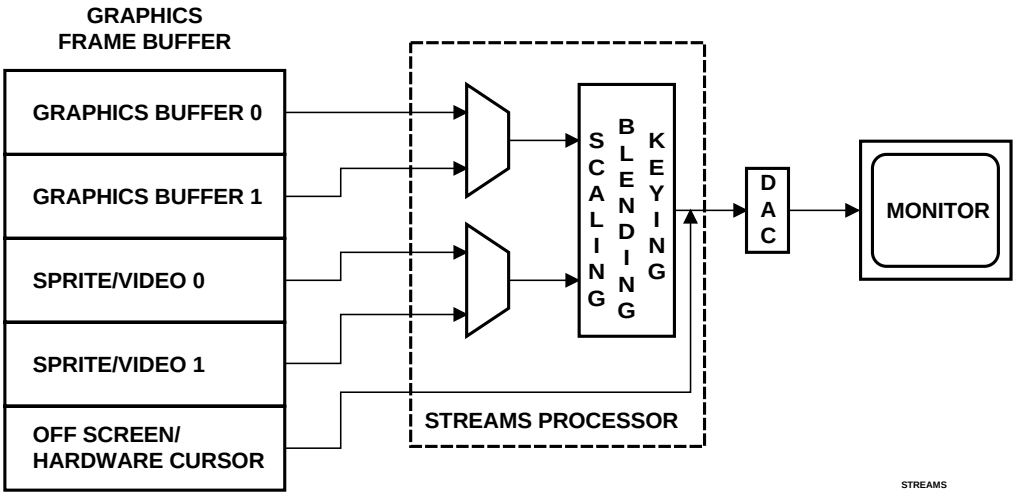


Figure 10-1. Streams Processor

Streams Processor also saves memory bandwidth by eliminating the need to save and restore the overlay background since the background (primary stream) is never overwritten in the frame buffer.

Streams Processor support is not available for clock-doubled 8 bits/pixel modes, 24 bits/pixel modes, interlaced graphics modes and standard VGA modes except for modes D, E, 10, 12 and 13.

Bits 3-2 of CR67 specify the Streams Processor mode of operation. If they are cleared to 00b, Streams Processor operation is disabled. They are programmed to 01b when the primary stream is VGA mode D, E, 10, 12 or 13 (the only supported modes). A secondary stream can be overlaid on the primary stream. CR67_3-2 are set to 11b to support an Enhanced mode primary stream and a secondary stream.

10.1.1 Primary Stream Input

The primary stream is generated by reading the RGB pixel data written to the frame buffer by the graphics controller. The format for this data can be any of the following as selected via bits 26-24 of MM8180.

- RGB-8 (Although not shown in Figure 1, the frame buffer data is first passed through the internal RAMDACs color lookup table (CLUT), where it is palettized before being passed to the Streams Processor.
- KRGB-16 (1.5.5.5) - The K bit is the color key.
- RGB-16 (5.6.5)
- XRGB-32 (X.8.8.8) - X is the ignored upper byte.

10.1.2 Secondary Stream Input

The secondary stream is generated by reading pixel data from a separate section of the frame buffer than that used to generate the primary screen. This might be RGB data written by the graphics controller, such as a sprite used by game programmers for moving objects. It could also be RGB, YUV or YCbCr data written to the frame buffer by some video source (CPU, decoder, digitizer). The format for this data can be any of the following as selected via bits 26-24 of MM8190.

- YCbCr-16 (4.2.2), 16 - 240 input range
- YUV-16 (4.2.2), 0 -255 input range
- KRGB-16 (1.5.5.5) - The K bit is the color key.
- YUV (2.1.1)
- RGB-16 (5.6.5)
- XRGB-32 (X.8.8.8) - X is the ignored upper byte.

The data can be passed through unscaled or scaled up horizontally and vertically by an arbitrary amount. YCbCr/YUV data is color space converted and all data is converted to RGB-24 (8.8.8) format.

10.1.3 Hardware Cursor Generation

Hardware cursor generation is explained in Section 15. The cursor is overlaid on the Streams Processor image.

10.1.4 Frame Buffer Organization/ Double Buffering

For each stream to be used, the starting location (offset) in the frame buffer and the stride (byte offset between vertically adjacent pixels on the screen) must be specified. Both the primary and the secondary streams can be double buffered as depicted in Figure 10-1. This means that duplicate frame buffer storage can be provided for both the primary and secondary image (or for either one of them). With double buffering, the programmer can rapidly switch from one primary or secondary image to the other. In addition, having two images allows more time for updating one image while the other is being displayed. Defining the frame buffer organization and implementing double buffering are done via the register fields described in Table 4-1. LPB stands for Local Peripheral Bus.

The secondary stream can be generated from data written to the frame buffer via the LPB when

Table 10-1. Register Fields Used For Specifying Frame Buffer Organization and Double Buffering

Register Field	Description
MM81C0_21-0	Primary Display Buffer Address 0. This is the starting address (offset) in the frame buffer for 1 primary graphics image.
MM81C4_21-0	Primary Display Buffer Address 1. This is the starting address (offset) in the frame buffer for a second primary graphics image.
MM81C8_11-0	Primary Stream Stride. This is the byte offset in the frame buffer from a pixel in a given primary image display line to the pixel directly below it on the next display line. The stride must be the same for both primary buffers.
MM81CC_0	Primary Stream Buffer Select 0 = Primary frame buffer starting address 0 (MM81C0_21-0) used for primary stream 1 = Primary frame buffer starting address 1 (MM81C4_21-0) used for primary stream
MM81CC_2-1	Secondary Stream Buffer Select 00 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream 01 = Secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream 10 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF0C_21-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF10_21-0) used for the LPB input stream. Which alternative applies is determined by LPB starting address register selected by bit 4 of this register. 11 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF0C_21-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF10_21-0) used for the LPB input stream. Which alternative applies is determined by the LPB starting address register selected by bit 4 of this register.
MM81CC_4	LPB Input Buffer Select 0 = LPB frame buffer starting address 0 (MMFF0C_21-0) used for LPB input 1 = LPB frame buffer starting address 1 (MMFF10_21-0) used for LPB input
MM81CC_5	LPB Input Buffer Select Loading 0 = The value programmed in bit 4 of this register takes effect immediately 1 = The value programmed in bit 4 of this register takes effect at the end of the next frame (completion of writing all the data for a frame into the frame buffer)
MM81CC_6	LPB Input Buffer Select Toggle 0 = End of frame (completion of writing all the data fro a from into the frame buffer) has no effect on the setting of bit 4 of this register 1 = End of frame causes the setting of bit 4 of this register to toggle

Table 10-1. Register Fields Used For Specifying Frame Buffer Organization and Double Buffering (continued)

Register Field	Description
MM81D0_21-0	Secondary Display Buffer Address 0. This is the starting address (offset) in the frame buffer for 1 secondary graphics or video image.
MM81D4_21-0	Secondary Display Buffer Address 1. This is the starting address (offset) in the frame buffer for a second secondary graphics or video image.
MM81D8_11-0	Secondary Stream Stride. This is the byte offset in the frame buffer from a pixel in a given secondary image display line to the pixel directly below it on the next display line. The stride must be the same for both secondary buffers.
MMFF0C_21-0	LPB Frame Buffer Address 0. This is the starting address (offset) in the frame buffer for one image buffer into which is written data from the LPB. The secondary stream can be generated from this buffer.
MMFF10_21-0	LPB Frame Buffer Address 1. This is the starting address (offset) in the frame buffer for a second image buffer into which is written data from the LPB. The secondary stream can be generated from this buffer.
MM81CC_6	LPB Input Buffer Select Toggle 0 = End of frame (completion of writing all the data fro a from into the frame buffer) has no effect on the setting of bit 4 of this register 1 = End of frame causes the setting of bit 4 of this register to toggle

LPB mode is enabled. In this case, the Secondary Display Buffer Address 0 and the LPB Frame Buffer Address 0 will normally be the same, as will the Address 1's for both the secondary stream and the LPB input if double buffering is used. The various LPB control bits described in Table 10-1 allow complete hardware control of the capture and display of video data using either single or double buffering.

10.2 INPUT PROCESSING

Different processing options are available for the primary and secondary input streams. These are explained next.

10.2.1 Primary Stream Processing

The primary stream input RGB format is converted (if required) to RGB-24 (8.8.8) format. Each color byte is padded as required with low order zeros. After this conversion, the data can be passed through unscaled or scaled up horizontally and vertically by a factor of 2 via bits 30-28 of MM8180. For MM8180_30-28 = 001, horizontal scaling is done via replication. If these bits are programmed to 010, horizontal scaling is done using interpolation. Vertical scaling is automatic and uses line replication. The 2x scaling allows a 320x240 image (as used by many games) to be displayed at a full-screen 640x480 resolution.

10.2.2 Secondary Stream Processing

The secondary stream input format is converted (if required) to RGB-24 (8.8.8) format. For YUV/YCbCr inputs, the required color space conversion is automatically performed. Before conversion, the data can be passed through unscaled or scaled up horizontally and/or vertically by arbitrary factors. Horizontal scaling uses filtering for interpolation. Vertical scaling uses line replication. The register fields involved in scaling up the secondary stream are described in Table 10-2. Figure 10-2 graphically describes the various fields.

For example, assume a 10x10 window that is to be scaled up horizontally by a factor of 2.5. The filter characteristics are set for bi-linear (2x to 4x stretch). The starting line width is 10 pixels and the ending line width is 25 pixels. The DDA horizontal accumulator initial value is 2 (10-1) - (25-1) = -6. The K1 horizontal factor is 10-1 = 9. The K2 horizontal factor is 10-25 = -15. Programming these parameters with these values results in a 2.5x horizontal stretch for the secondary stream window.

10.3 COMPOSITION/OUTPUT

A variety of output types can be composed from the streams described above. The compose modes are:

1. MM81A0_26-24 = 000b - Secondary stream overlaid on the primary stream in an opaque rectangular window. This is the default mode and can be used, for example, for a video window overlaying the graphics screen. Note that this mode will not work for the case where the user needs to pull down a graphics window over the video since the graphics window is defined as being under the video window. Color keying (number 5 in this list) must be used for this purpose.
2. MM81A0_26-24 = 001b - Primary stream overlaid on the secondary stream in an opaque rectangular window. This could be used, for example, to provide graphics captions for a video window. The video is not visible behind the rectangular graphics window.
3. MM81A0_26-24 = 010b - Secondary stream blended with the primary stream on a pixel by pixel basis within the secondary stream window. This is used to provide a dissolve between two scenes.
4. MM81A0_26-24 = 011b - Secondary stream blended with the primary stream on a pixel by pixel basis within the secondary stream window. This is used to provide a fade between two scenes.
5. MM81A0_26-24 = 101b - Secondary stream overlaid on the primary stream in an irregular window. This requires a color key. This would be used, for example, for game sprites. Only the graphics area behind the sprite shape would be covered up.
6. MM81A0_26-24 = 110b - Primary stream overlaid on the secondary stream in an irregular window. This requires a color/chroma key. This case allows, for example, graphics text to overlay video with the video appearing around and even inside of the text characters.

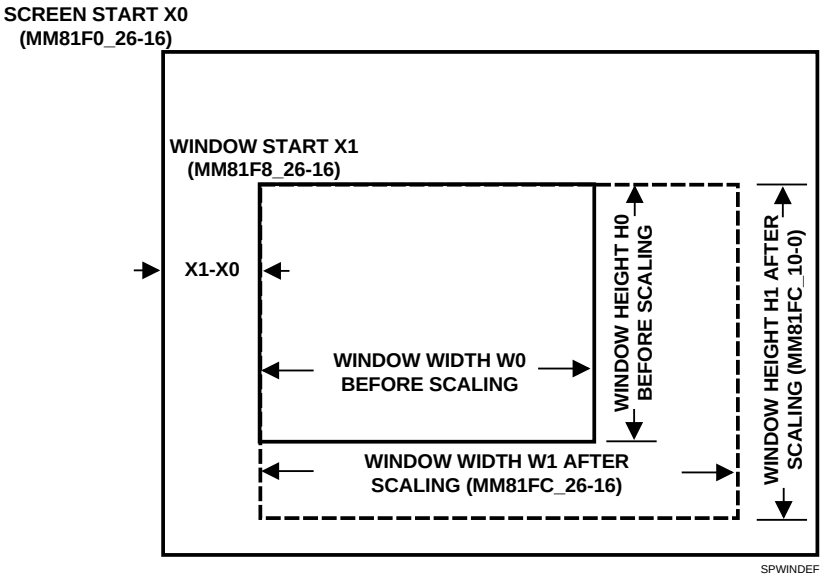


Figure 10-2. Screen Definition Parameters

Table 10-2. Register Fields Used For Scaling Up the Secondary Stream

Register Field	Description
MM8190_30-28	Filter Characteristics 000 = Secondary stream (pass-through) 001 = Secondary stream, linear, 0-2-4-2-0, for X stretch 010 = Secondary stream, bi-linear, for 2X to 4X stretch 011 = Secondary stream, linear, 1-2-2-2-1, for 4X stretch This selection applies only to horizontal scaling.
MM8190_11-0	DDA Horizontal Accumulator Initial Value. Value = 2 (W0-1) - (W1-1), where W0 is the line width in pixels before scaling and W1 is the line width after scaling. This is a signed value.
MM8198_10-0,	K1 Horizontal Factor. Value = W0-1, where W0 is the line width in pixels before scaling. This is a signed value.
MM8198_26-16	K2 Horizontal Factor. Value = W0-W1, where W0 is the line width in pixels before scaling and W1 is the line width after scaling. This is a signed value.
MM81E0_10-0,	K1 Vertical Factor. Value = [height (in lines) of the initial output window (before scaling)] -1. The initial output window height is the vertical resolution of the data written to the frame buffer and is shown as H0 in Figure 10-2.
MM81E4_10-0,	K2 Vertical Factor. Value = [height (in lines) of the initial output window (before scaling)] - [height (in lines) of the final output window (after scaling)] The initial output window height is the vertical resolution of the data written to the frame buffer and is shown as H0 in Figure 10-2. The final value is shown as H1 in Figure 10-2.
MM81E8_11-0,	DDA Vertical Accumulator Initial Value. Value = [height (in lines) of the output window after scaling] -1. This is shown as H1 in Figure 10-2.

10.3.1 Opaque Rectangular Overlaying

These modes are items 1 and 2 in the compose modes list. When one of these modes is used, the programmer can invoke a feature called opaque overlay control. This is enabled by setting MM81DC_31 to 1. If MM81A0_26-24 = 000b (secondary stream on top), then MM81DC_30 must be cleared to 0 to also specify secondary stream on top. Similarly, If MM81A0_26-24 = 001b (primary stream on top), then MM81DC_30 must be set to 1 to also specify primary stream on top. The next step is to define when to stop fetching pixels for a line from memory and when to restart fetching them. The goal is to not fetch those pixels in the background window that are covered up by the opaque rectangular overlay window, thus saving memory bandwidth.

The first pixel that does not need to be fetched is at horizontal position X1 shown in Figure 10-2. This is programmed in MM8158_26-16. The starting pixel position for the background (X0) is programmed in MM81F0_26-16. The difference (X1 - X0) must be converted into quadwords and then programmed in MM81DC_12-3. The value is (X1 - X0) x bytes per pixel/8. If the result is a fraction, it is rounded up to the next highest integer to ensure that the first pixel not fetched in inside the opaque overlay window. Note that if the secondary stream is in the background, then the value is (X0 - X1) x bytes per pixel/8, again rounded up.

Pixel fetching must start again before or at the last pixel position of the opaque overlay window. Using the terms in Figure 10-2, this position is (X1 - X0) + W1, with W1 programmed in MM81FC_26-16 (secondary stream is on top). Converting to quadwords, the value is [(X1 - X0) + W1] x bytes per pixel/8. If the result is a fraction, the result is truncated to the next lowest integer (minus 1) and programmed in MM81DC_28-19. Note that if the secondary stream is in the background, then (X0 - X1) is used and W1 is the value in MM81F4_26-16 (primary stream is on top).

Opaque overlay control cannot be used with keying or blending and should never be enabled when one of these modes is being used.

10.3.2 Blending

These modes are items 3 and 4 in the compose modes list. The blender accepts the primary and secondary pixel streams and blends them with an arithmetic weighting. The result is then overlaid with the cursor stream. Both blender inputs are RGB 8.8.8 from the outputs of the primary stream interpolator and secondary stream color space converter. Note that blending makes sense only when both streams are defined. In addition, when blending is selected, the concept of background/foreground or top and bottom window has no meaning.

Two types of blending are provided: dissolve and fade.

When dissolve is chosen, the output pixels are generated using the following equation:

[Pp x Kp + Ps x (8 - Kp)]/8

Pp and Ps are the primary and secondary stream pixel colors respectively, both RGB 8.8.8. Kp is the primary stream weighting factor. It is a 3-bit value programmed in MM81A0_12-10. This weight value is applied to each of the three color values for the pixel. If Kp = 0, only the secondary stream is displayed. As Kp is increased, more of the pixel color from the primary stream is blended into output. At the maximum (Kp = 7 or 111b), 7/8ths of the color will be due to the primary stream and 1/8th will be due to the secondary stream. Therefore, by starting with the primary stream only, then overlaying the secondary stream with Kp values decreasing from 7 to 0, the overlay window can be dissolved gradually from primary stream to secondary stream. Note that when the Kp value is reprogrammed, its new value does not take effect until the next VSYNC, so it can be reprogrammed during frame display without disruptive effects.

When fade is chosen, the output pixels are generated using the following equation:

[Pp x Kp + Ps x Ks]/8, where Kp + Ks must be ≤ 8.

Ks is the secondary stream weighting factor. It is a 3-bit value programmed in MM81A0_4-2. This weight value is applied to each of the three color values for the pixel. Note that when fading is selected, the default values for Kp and Ks (both 0) result in a color value of 0. As with Kp, when the Ks value is reprogrammed, its new value does not take effect until the next VSYNC.

10.3.3 Color/Chroma Keying

These modes are items 5 and 6 in the compose modes list. Keying is a way of selecting on a pixel by pixel basis which stream will be displayed. Color keying is used when the stream source is in RGB format (graphics). This is always the case for the primary stream. Chroma keying is used when the stream source is YUV or YCbCr (video). The secondary stream source can be either graphics or video, so either color or chroma keying might be used. If 81A0_26-24 (compose mode) = 101b and MM8184_28 = 1, the color key is compared with the primary stream pixel. If there is a match, the corresponding secondary stream pixel is displayed. If 81A0_26-24 = 110b and MM8184_28 = 1, the color or chroma key is compared with the secondary stream pixel. If there is a match, the corresponding primary stream pixel is displayed.

If the input format is KRGB-16 (1.5.5.5), selected when MM8180_26-24 or MM8190_26_24 = 011b, the most significant bit of each pixel value is used as a color key as long as MM8184_28 is cleared to 0. When the most significant pixel bit is a 0, the other stream pixel is displayed.

For other RGB input types (as specified by MM8180_26-24), a color key must be defined. This is done by programming MM8184_23-0 with a specific RGB 8.8.8 color value. MM8184_28 must be set to 1 to enable use of this value. The number of bits to compare for each color is specified in MM8184_26-24. If there is a color match with the keyed stream pixel, the corresponding other stream pixel is displayed.

If the secondary stream input format is YUV or YCbCr, the chroma key is specified as a range of color values. The lower bound value is defined in MM8184_23-0. The upper bound value is defined in MM8194_23-0. If the secondary stream pixel color value falls within this range (inclusive of the lower and upper bounds), the Streams Processor displays the corresponding pixel from the primary stream. If the secondary stream pixel color is outside this range, the secondary stream pixel is displayed.

10.3.4 Window Location

The starting X,Y coordinates and window size for the primary stream are specified in MM81F0 and MM81F4 respectively. The starting X,Y coordinates and window size for the secondary stream are specified in MM81F8 and MM81FC respectively.

10.4 STREAMS FIFO CONTROL

The streams FIFO can be reconfigured to optimize performance for various operating modes. The FIFO is 24 8-byte slots deep. By programming MM81EC_4-0, the FIFO can be reconfigured to assign all 24 slots to either the primary or secondary stream. Allocations of 16-8 and 12-12 slots between the two streams are also possible. As an example, if only a primary stream is being displayed, optimal performance is generated by assigning all 24 FIFO slots to the primary stream.

No matter what the allocation, FIFO thresholds must be specified for the primary and secondary streams. This is done via MM81EC_16-12 for the primary stream and MM81EC_10-6 for the secondary stream. When the FIFO empties to the threshold level, an internal signal is generated requesting the memory controller to begin refilling the FIFO. The programmed threshold levels must never exceed the corresponding FIFO depths. The optimal settings for the threshold levels will be system and operating mode dependent and will have to be determined by trial and error.

Section 11: Local Peripheral Bus

When PD24 is strapped low at reset, the Trio64V+ is placed in its Local Peripheral Bus (LPB) mode. The LPB mode pinout described in Section 3 takes effect when bit 0 of MMFF00 is set to 1. LPB clocking with LCLK must also be enabled by setting bit 24 of MMFF00 to 1. The LPB function provides the following:

- S3 Scenic Highway interface to the Scenic/MX2 MPEG Audio/Video Decoder (glueless, bi-directional)
- Scenic Highway interface to the C-Cube CL-480 Audio/Video Decoder (glueless video input and compressed data output)
- Scenic Highway interface to the Philips video digitizers (glue logic is required to convert 16-bit output to 8-bit Trio64V+ input for VL-Bus configurations. However, the Scenic/MX2 has a glueless SAA7100 interface which can be used to provide the 16- to 8-bit conversion). A 16-bit data interface is available on the Trio64V+ for PCI configurations.
- Host Video Data Pass-through. This allows decimation of 32-bit CPU data being written to the frame buffer.)
- LPB Feature Connector (glueless 8-bit bi-directional or 16-bit VAFC)
- 4-bit General Input Port and 4-bit General Output Port

The LPB mode also provides the support required for DDC2 monitor communications. This, the feature connector interfaces and the General Input/Output Port are described in Section 12.

The internal block diagram for the LPB is shown in Figure 11-1.

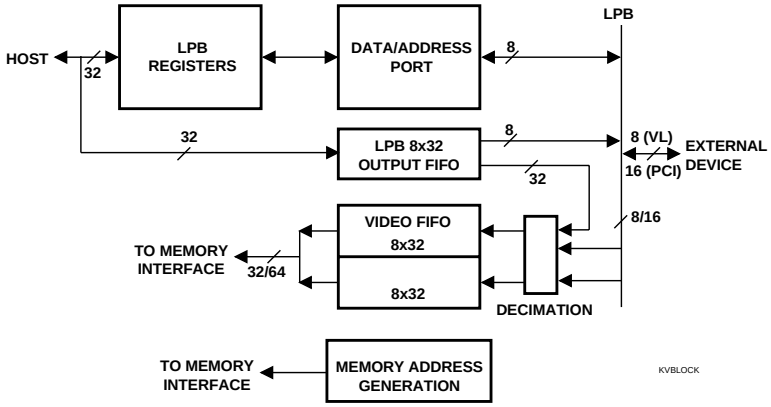


Figure 11-1. LPB Internal Block Diagram

11.1 Scenic/MX2 INTERFACE

The hardware interface to the Scenic/MX2 is shown in Figure 11-2.

When the Trio64V+ is in its LPB configuration, the Scenic/MX2 interface is selected by setting MMFF00_3-1 to 000b. This interface is fully bi-directional. Scenic/MX2 registers can be accessed, compressed data sent and decompressed video data received.

11.1.1 Scenic/MX2 Register/Memory Access

To read/write a Scenic/MX2 register or private memory location (other than to transfer compressed data), the LPB Direct Read/Write Address register (MMFF14) is written. The new register/memory data is then written to MMFF18. For a write access, this write triggers the sequence shown in Figure 11-3 if the Scenic/MX2 is ready to receive the data ($\overline{\text{CREQ}}$/CRDY remains high). One cycle after Trio64V+ asserts its $\overline{\text{VREQ}}$/VRDY signal, it sends the address in three byte writes. The first byte is composed of bits 23-16 of MMFF14. The three upper bits are 000b to define this as a write. Bit 4 is 1 for a register access and 0 for a memory access. Bits 3-0 are bits 19-16 of the address. The second byte is bits 15-8 of MMFF14 and the third byte is bits 7-0. The data immediately follows in four byte writes. Data is written in the opposite byte order to that for the address, i.e., least significant byte (bits 7-0) first and most significant byte (bits 31-24) last. The Trio64V+ then deasserts $\overline{\text{VREQ}}$/VRDY. The Host repeats the above sequence for another write if required.

If the Scenic/MX2 is not ready to receive data, it drives its $\overline{\text{CREQ}}$/CRDY signal low during the A0-0 byte (LSB) of the address phase. The Trio64V+ then delays sending the data until the Scenic/MX2 raises $\overline{\text{CREQ}}$/CRDY. This is depicted in Figure 11-4.

Figure 11-5 shows a Scenic/MX2 register/memory read when the Scenic/MX2 is ready to provide data. This is indicated by the Scenic/MX2 holding the $\overline{\text{CREQ}}$/CRDY high throughout the cycle. The three upper bits of the first address byte are 001 to define a read.

If the Scenic/MX2 is not ready to provide data, it drives its $\overline{\text{CREQ}}$/CRDY signal low during the ad-

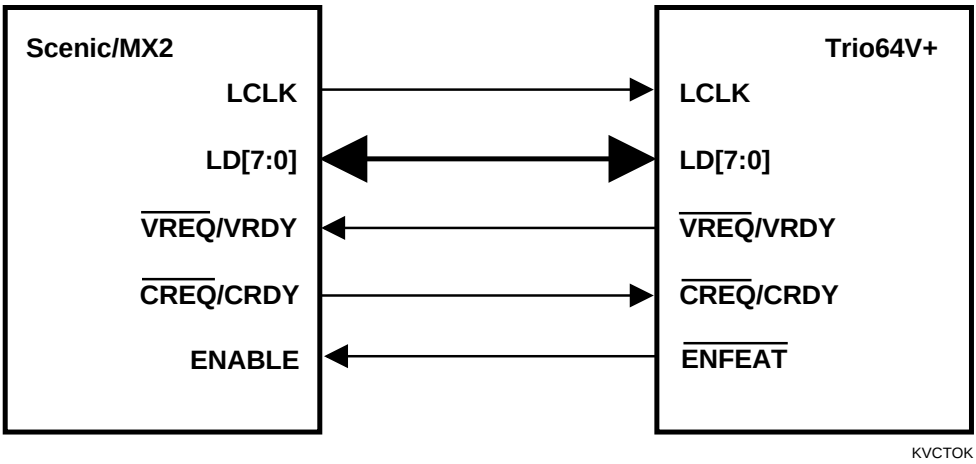


Figure 11-2. Trio64V+ to Scenic/MX2 Hardware Interface

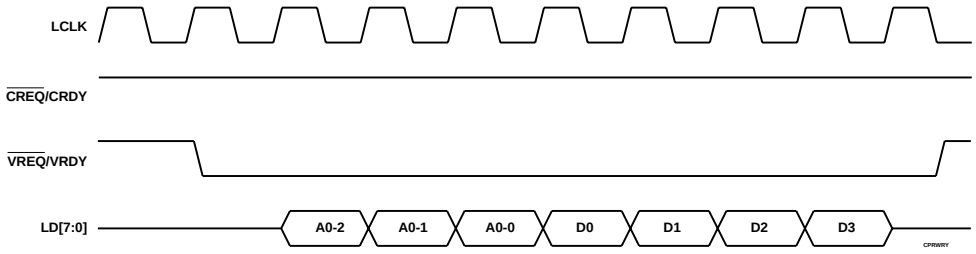


Figure 11-3. Scenic/MX2 Write (Scenic/MX2 Ready)

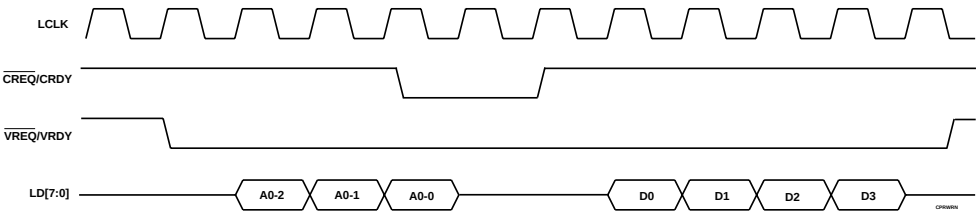


Figure 11-4. Scenic/MX2 Write (Scenic/MX2 Not Ready)

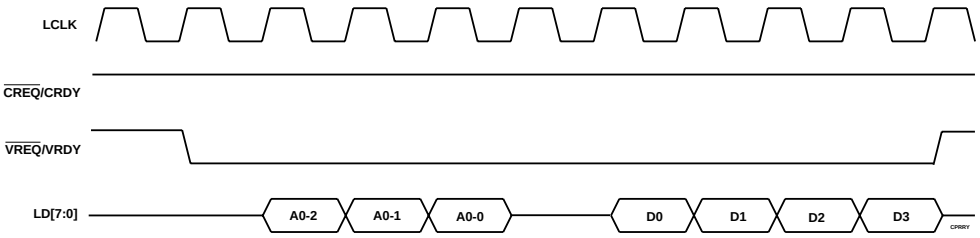


Figure 11-5. Scenic/MX2 Read (Scenic/MX2 Ready)

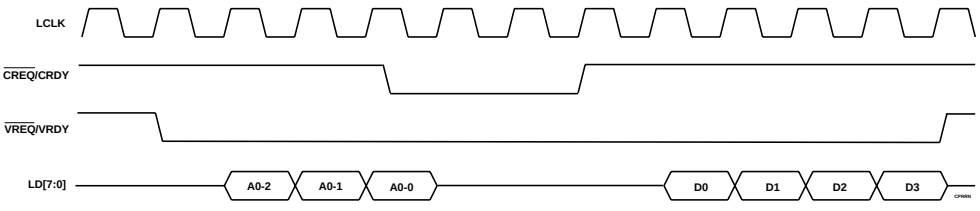


Figure 11-6. Scenic/MX2 Read (Scenic/MX2 Not Ready)

dress phase. The Trio64V+ then waits until the Scenic/MX2 raises CREQ/CRDY and provides register data. This is depicted in Figure 11-6.

To prevent data starvation and deal with request contention, the following protocol is followed.

- No transaction can be initiated if the bus is active
- There is one dead cycle on the bus following all transactions
- One device may not initiate a transaction until the second cycle following the completion of a transaction initiated by the other device
- Neither device may initiate a transaction until the third cycle following the completion of a transaction initiated by itself
- If CREQ/CRDY and VREQ/VRDY are both driven low on the same cycle (request contention), CREQ/CRDY (the Scenic/MX2) wins.

11.1.2 Scenic/MX2 Compressed Data Transfer

The Trio64V+ has an output FIFO for handling the transfer of compressed video data from the Host to the Scenic/MX2 (see Figure 11-1). The Host must first check the number of empty slots (MMFF04_3-0), then send no more than this many doublewords (32 bits) of compressed data to the FIFO. An eight doubleword address range (FF40H - FF5CH) is provided for this FIFO. Writes to any of these addresses are directed to the FIFO.

MMFF00_17-16 are programmed to specify the number of doublewords of data to burst to the Scenic/MX2. A write to the output FIFO then initiates a compressed data write to the Scenic/MX2. This is depicted in Figure 11-7 for a burst count of 2 (MMFF00_17-16 = 01b) for the case where the Scenic/MX2 is ready to receive the data. The address and first doubleword are transferred exactly as for a register/memory write. Following doublewords in the burst are each separated by one dead cycle. The address has no meaning except for the upper three bits, which are forced to 110b by hardware to specify a compressed data transfer. Note that burst writes that end because the FIFO is empty (as opposed to the maximum burst count being reached) hold VREQ/VRDY low for one more cycle than is shown in Figure 11-7.

The Scenic/MX2 cannot accept a burst larger than eight doublewords. If MMFF00_17-16 are programmed to 11b (burst all) and eight doublewords are loaded into the FIFO, software must ensure that the FIFO is empty before loading more data into the FIFO.

A compressed data transfer when the Scenic/MX2 is not ready to receive data is almost the same as a register write for the same circumstances (see Figure 11-4). The only difference is that after the Scenic/MX2 returns its CRDY signal,

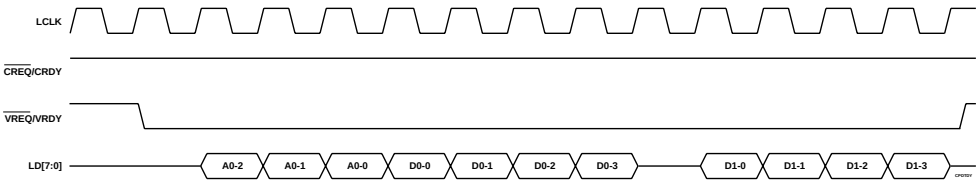


Figure 11-7. Scenic/MX2 Compressed Transfer (Ready)

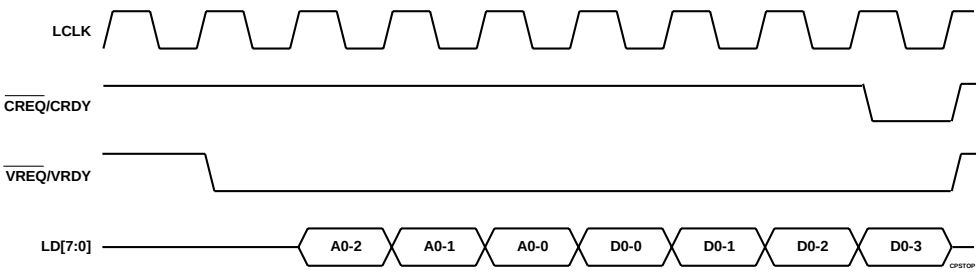


Figure 11-8. Scenic/MX2 Stopping a Compressed Xfer

additional doubleword packets may be burst to the Scenic/MX2 as shown in Figure 11-7.

The Scenic/MX2 can stop a compressed data transfer by pulling CREQ/CRDY low for one (and only one) cycle during byte three of any doubleword. This is shown in Figure 11-8.

An output FIFO empty interrupt can be enabled by setting MMFF08_17 to 1. The status is read via bit 1 of this same register.

11.1.3 Scenic/MX2 Video Capture

The following setup is done for Scenic/MX2 video capture:

- The LPB is placed in Scenic/MX2 mode (MMFF00_3-1 = 000b).
- One or two frame buffer starting addresses are defined (MMFF0C, MMFF10). One is required. The second is required for double buffering.
- The horizontal and vertical decimation registers are programmed (MMFF2C, MMFF30). This is optional.
- The line stride is programmed (MMFF34_10-0). This is not required if HSYNCs are not being sent.

The Trio64V+ signals its readiness to accept data by driving VREQ/VRDY high. This is done automatically when the Trio64V+ does not need to

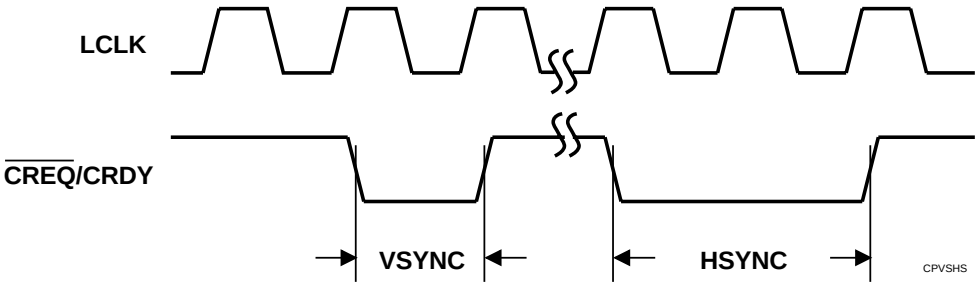


Figure 11-9. Scenic/MX2 VSYNC and HSYNC Protocols

drive this signal low such as to initiate a register access or to indicate an LPB video FIFO full state. The Scenic/MX2 responds by sending a VSYNC ($\overline{\text{CREQ}}$/CRDY low for one cycle) followed by an HSYNC ($\overline{\text{CREQ}}$/CRDY low for two cycles). This is shown in Figure 11-9. As indicated in the figure, the time between VSYNC and HSYNC is variable. The HSYNC sequence occurs after each line, but may not occur before the first line, depending on how the Scenic/MX2 is programmed.

After the VSYNC/HSYNC sequence, the Scenic/MX2 can pull $\overline{\text{CREQ}}$/CRDY low at any time and begin sending data three clocks later. This is shown in Figure 11-10. The Trio64V+ assumes data has begun any time $\overline{\text{CREQ}}$/CRDY is held low for more than two cycles. When the Scenic/MX2 is sending the last byte, it drives $\overline{\text{CREQ}}$/CRDY high. The Scenic/MX2 must always send data in 4-byte packets. If it has fewer to send for the last packet, it must pad the transmission with dummy writes to create a 4-byte packet.

Figure 11-10 shows what happens when the Trio64V+ is ready to receive all the data. If the Trio64V+ cannot accept more data, such as when its LPB video FIFO is full, it drives its $\overline{\text{VREQ}}$/VRDY signal low during the first byte phase of a 4-byte

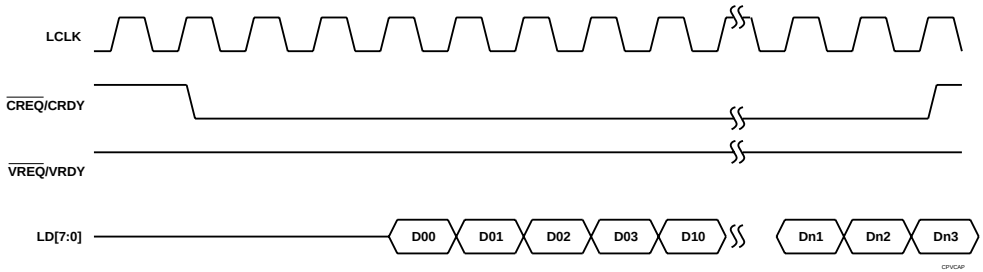


Figure 11-10. Scenic/MX2 Video Input (Trio64V+ Ready)

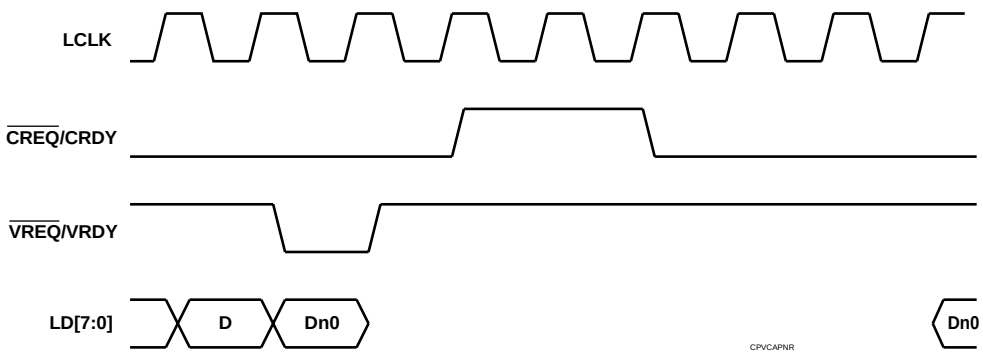


Figure 11-11. Scenic/MX2 Video Input (Trio64V+ Not Ready)

packet. All bytes starting with this one are rejected by the Trio64V+ and must be resent by the Scenic/MX2 after the Trio64V+ drives its VREQ/VRDY signal high again. This is depicted in Figure 11-11, where the Dn0 byte, which is the first byte of the nth 4-byte packet, is rejected. When the Trio64V+ can accept more data, it drives VREQ/VRDY high. The Scenic/MX2 drives CREQ/CRDY high (two cycles later) and then drives it low when it is ready to resend the data. The resend of Dn0 and subsequent bytes starts two cycles later.

When the Trio64V+ receives an HSYNC from the Scenic/MX2, it adds the line offset (MMFF34_10-0) to the previous line starting address and starts writing the next data at that location. In this way, for example, it can transfer 640-byte lines into a frame buffer configured for 1024-byte lines. If HSYNCs are not sent, memory will be written in a contiguous manner.

11.2 DIGITIZER INTERFACE

The hardware interface to the Philips digitizer in Video 8 In mode (MMFF00_3-1 = 010b) is shown in Figure 11-12. This section describes the interface to the Philips SAA7110 digitizer.

The functional timing for converting the SAA7110 16-bit video output to the 8-bit input required by the LPB in a VL-Bus configuration is shown in Figure 11-13.

In Video 16 mode (MMFF00_3-1 = 001b), which is available only for PCI configurations, no data conversion is required. Y[7:0] connect to LD[7:0] and UV[7:0] connect to LD[15:8].

As an alternative, the Scenic/MX2 provides a glueless interface to the SAA7110. In this case, the Scenic/MX2 handles the 16-bit to 8-bit conversion and also provides the I^2C interface to the SAA7110. The Trio64V+ then receives the video data, clock and controls from the Scenic/MX2. The Scenic/MX2 documentation describes this interface.

11.2.1 I^2C Register Interface

SAA7110 registers are programmed via a serial I^2C interface. This interface is described in Section 12.6.

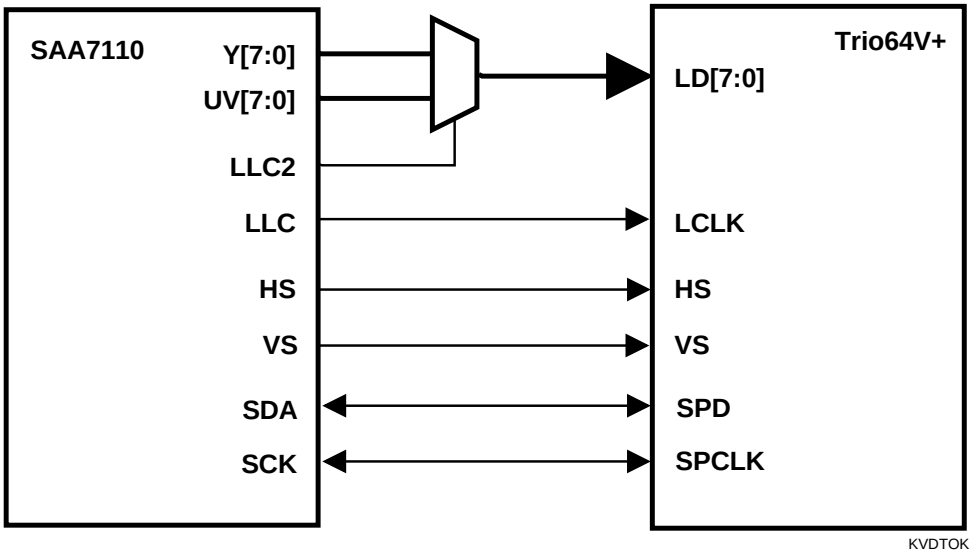


Figure 11-12. Trio64V+ to SAA7110 Digitizer Interface

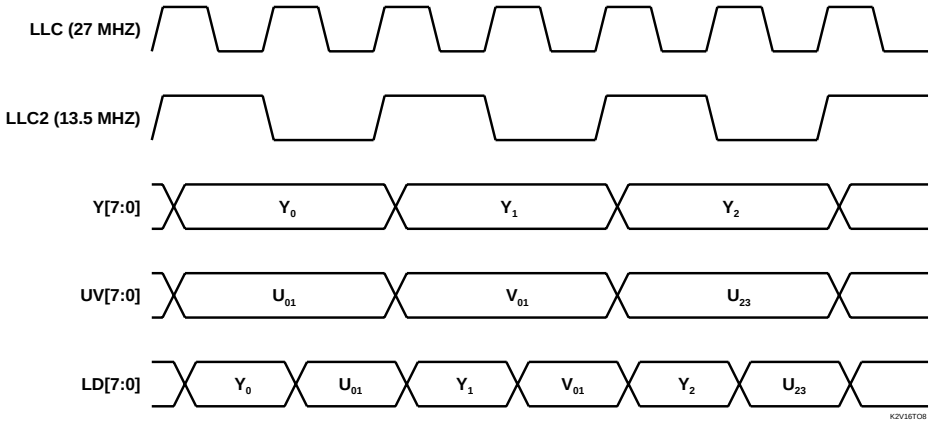


Figure 11-13. 16- to 8-bit Video Data Conversion

11.2.2 SAA7110 Video Input

The following setup is done for SAA7110 video input:

- The Trio64V+ is placed in Video 8 In mode (MMFF00_3-1 = 010) or Video 16 mode (MMFF00_3-1 = 001b) for PCI configurations.
- Byte swapping is disabled by setting MMFF00_6 to 1.
- The correct vertical and horizontal sync polarities are specified (MMFF00_9, 10).
- One or two frame buffer starting addresses are defined (MMFF0C, MMFF10). One is required. The second is required for double buffering.
- The horizontal and vertical decimation registers are programmed (MMFF2C, MMFF30). This is optional.
- The video input window size (height in lines and width in pixels) is programmed in MMFF24.

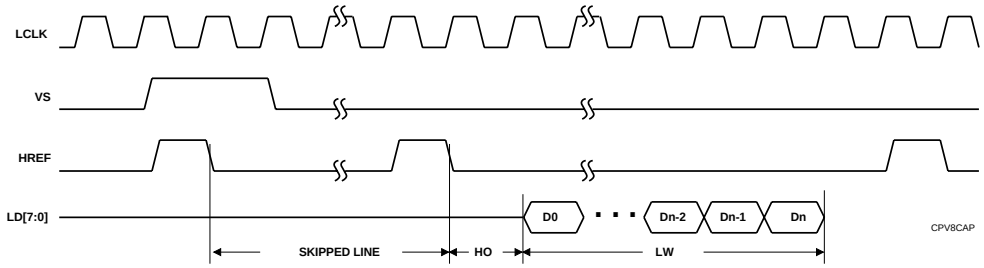


Figure 11-14. Video 8 In or 16 Mode Input

- The video data horizontal and vertical offsets are programmed in MMFF28.
- The line offset (stride) is programmed (MMFF34_10-0).

The SAA7110 then sends video data as shown in Figure 11-14. In this figure, both VSYNC (VS) and HSYNC (HS) have active high polarity. The vertical offset (MMFF28_24-16) is 1, meaning the first line is skipped. The horizontal offset HO (MMFF28_11-0) is 1, meaning that the first data starts one clock after the second HS goes low. HS goes high again some time after the last byte of the line, whose position is specified by the line width (LW) programmed in MMFF24_11-0. The widths of the VS and HS pulses shown may vary.

Alternate frames of the video input can be discarded (not written to memory) by setting bit 5 of MMFF00 to 1.

11.3 CL-480 INTERFACE

The CL-480 can be interfaced in two ways. In Video 8 In mode (MMFF00_3-1 = 010b) the interface is similar to the SAA7110 interface except that the CL-480 outputs 8 bits of data and programming of the CL-480 is done via the host bus, not I^2C. Therefore, only LD[7:0], HS, VS and LCLK are connected. This is shown by the top set of signals in Figure 11-15. The functional timing is the same as for the SAA7110 and is shown in Figure 11-12.

In Video 8 In/Out mode (MMFF00_3-1 = 011b), compressed data is sent to the CL-480 from the Trio64V+ and video data is returned to the Trio64V+. This interface is shown in Figure 11-15. Functional timing for the compressed data transfer is given in the CL-480 data book.

The following pseudocode shows how to write the CL-480 program counter register (3AH) with 5A5AH. The CL-480 requires that register writes be done as a sequence of 3 address writes followed by two data writes. The upper byte of the address must have 10b in bits 7-6 for register writes and the register address (3AH in this case) in bits 5-0. The complete address is then BA0000H, sent as 00H, 00H, BAH.

```
wr FF14 01H; address byte 0
wr FF18 00H: byte 0 data
wr FF14 02H; address byte 1
wr FF18 00H; byte 1 data
wr FF14 03H; address byte 2
wr FF18 BAH; byte 2 data
wr FF14 04H; data byte 0
wr FF18 5AH; byte 0 data
wr FF14 05H; data byte 1
wr FF18 5AH; byte 1 data
```

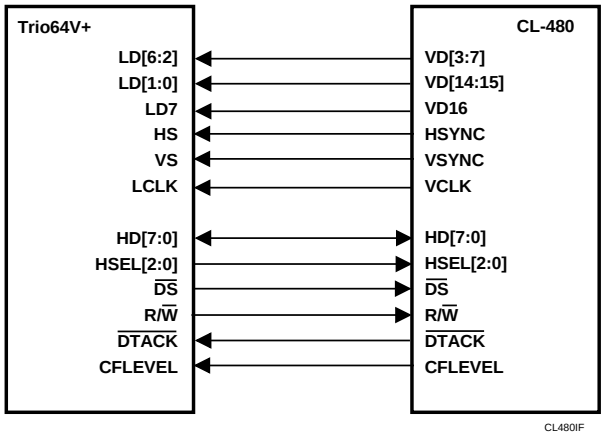


Figure 11-15. Video 8 In or 16 Mode Input

To read the value programmed above, use the same sequence except read the data bytes instead of writing them.

```
wr FF14 01H; address byte 0
wr FF18 00H: byte 0 data
wr FF14 02H; address byte 1
wr FF18 00H; byte 1 data
wr FF14 03H; address byte 2
wr FF18 BAH; byte 2 data
wr FF14 04H; data byte 0
rd FF18    ; returns 5
wr FF14 05H; data byte 1
rd FF18    ; returns 2H
```

Note that the last read returns 2 instead of the A originally written. The reason is that the 3AH register is physically 10 bits wide. Therefore, only the lower 2 bits of the upper nibble are actually written. For a value of AH, these are 10b, or 2 decimal. Functional timing for register accesses is given in the CL-480 data book.

11.4 HOST PASS-THROUGH

When pass-through mode is enabled (MMFF00_3-1 = 100b), the CPU can write 32-bit data to the output FIFO and have this data passed directly to the decimation block (bypassing the LPB bus). The data are sent exactly as for compressed video data to an MPEG decoder. The data will then be decimated according to the programming of MMFF2C (horizontal) and MMFF30 (vertical) and then passed to the video FIFO to be written to display memory. This path is shown in Figure 11-1.

When the Host sends an HSYNC (MMFF00_12 = 1) or VSYNC (MMFF00_11), the decimation registers are re-loaded. Therefore, the Host must ensure that at least 5 clocks pass between the sync and the start of data to allow time for this reloading.

When pass-through is used in LPB mode, bit 24 of MMFF00 provides the option of using SCLK to clock the LPB function.

Host pass-through can be used in Trio64-compatible mode (PD24 strapped high at reset). The LPB must be enabled (bit 0 of MMFF00 set to 1) and clocked by SCLK (bit 24 of MMFF00 set to 1).

Pass-through is not supported if big-endian addressing is being used.

11.5 LPB-ENABLED PIN ASSIGNMENTS

The pin assignments when the various LPB modes are enabled are shown in Table 11-1. Note that some functions are available only in PCI configurations. These have (PCI) next to the pin number.

Table 11-1. LPB-Enabled Pin Assignments

Pin #	Scenic/MX2 MMFF00_3-1 = 000	Video 16 or 8 In MMFF00_3-1 = 001 MMFF00_3-1 = 010	Video 8 In/Out MMFF00_3-1 = 011
146	LD0	LD0	LD0
147	LD1	LD1	LD1
148	LCLK	LCLK	LCLK
154	LD2	LD2	LD2
155	LD3	LD3	LD3
174	LD4	LD4	LD4
175	LD5	LD5	LD5
176(PCI)	NO FUNCTION	NO FUNCTION	HSEL2
177(PCI)	NO FUNCTION	NO FUNCTION	HSEL1
178(PCI)	NO FUNCTION	NO FUNCTION	HSEL0
179(PCI)	NO FUNCTION	NO FUNCTION	$\overline{DS}$
180(PCI)	NO FUNCTION	NO FUNCTION	R/$\overline{W}$
181(PCI)	NO FUNCTION	NO FUNCTION	$\overline{DTACK}$
182(PCI)	NO FUNCTION	NO FUNCTION	CFLEVEL
184	LD6	LD6	LD6
185 (PCI)	NO FUNCTION	LD8 (Video 16)	HD0
186 (PCI)	NO FUNCTION	LD9 (Video 16)	HD1
187 (PCI)	NO FUNCTION	LD10 (Video 16)	HD2
188 (PCI)	NO FUNCTION	LD11 (Video 16)	HD3
189 (PCI)	NO FUNCTION	LD12 (Video 16)	HD4
199 (PCI)	NO FUNCTION	LD13 (Video 16)	HD5
200 (PCI)	NO FUNCTION	LD14 (Video 16)	HD6
201 (PCI)	NO FUNCTION	LD15 (Video 16)	HD7
202	LD7	LD7	LD7
203	$\overline{VREQ}$/VRDY	HS	NO FUNCTION
204	$\overline{CREQ}$/CRDY	VS	NO FUNCTION

Section 12: Miscellaneous Functions

This section explains how the Trio64V+ interfaces to the video BIOS ROM and feature connector. Green PC support, the General I/O Ports, the serial communications port and interrupt generation are also described.

12.1 VIDEO BIOS ROM INTERFACE

The video BIOS ROM contains power-on initialization, mode setup, and video data read/write routines. The video BIOS can be part of the system ROM or it can be implemented separately.

12.1.1 Disabling BIOS ROM Accesses

If the video BIOS is integrated with the system BIOS in a VL-Bus configuration, then power-on strapping bit 4 (CR36, bit 4) must be pulled low to disable BIOS accesses. For this configuration, $\overline{\text{ROMCS}}$ is not required. Bits 1-0 of SR1C can be set to 11, making pin 153 function as a second General Output Port bit instead of as $\overline{\text{ROMCS}}$. For PCI configurations, bit 0 of the BIOS ROM Base Address register (Index 30H) is cleared to 0 to disable BIOS accesses.

12.1.2 BIOS ROM Hardware Interface

A separate implementation of the video BIOS for a PCI configuration is shown in Figure 12-1. The GD[7:0] and GA[15:0] signals are multiplexed on PD pins. Therefore, the BIOS ROM must be shadowed immediately after reset and BIOS access disabled to prevent interference with graphics operation.

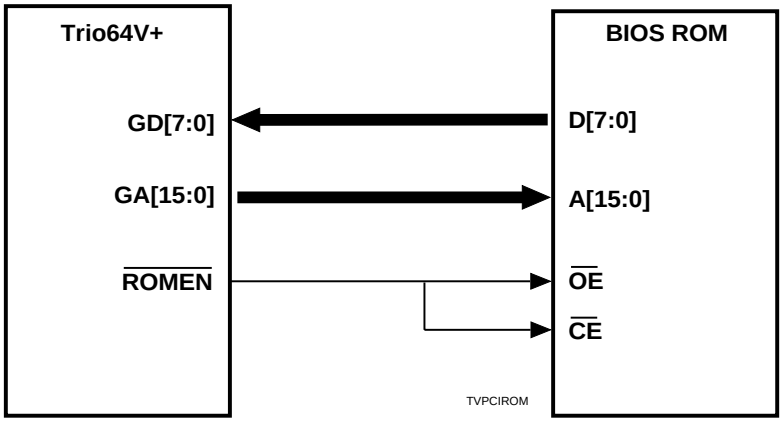


Figure 12-1. BIOS ROM PCI Configuration Interface

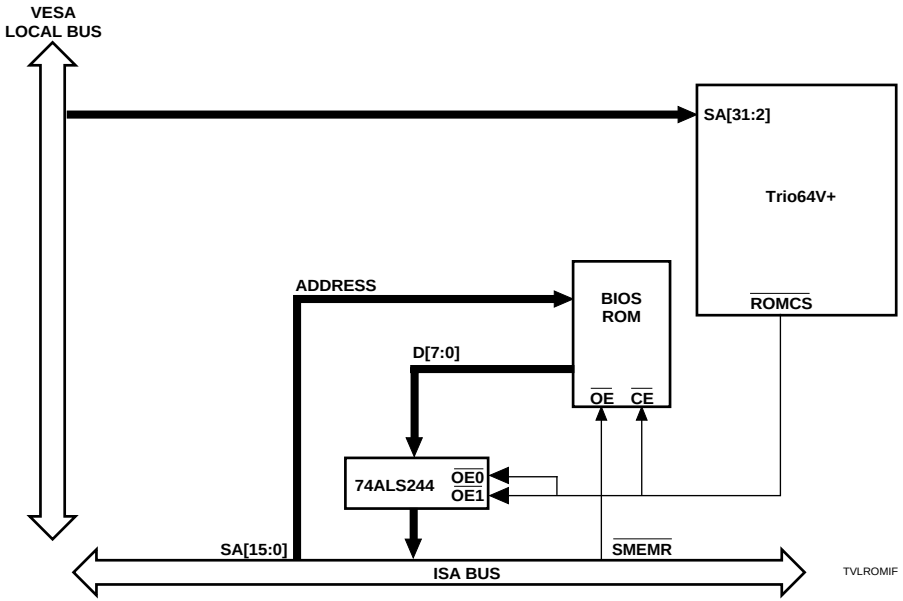


Figure 12-2. BIOS ROM VL-Bus Configuration Interface

The implementation for a VL-Bus configuration is shown in Figure 12-2. The ROM is accessed via the ISA bus. This allows a shadowed BIOS to be accessed by a CPU memory read without also generating data directly from the physical ROM. Only 8-bit ROMs are supported.

12.1.3 BIOS ROM Read Functional Timing

Figure 12-3 depicts the PCI configuration functional timing for reading one byte from the ROM. ROMEN is asserted to drive the byte of read data at the address on GA[15:0] to the General Data Bus. The Trio64V+ latches the data one clock before deassertion of ROMEN and then drives this data onto the AD bus.

The Trio64V+ also supports 16- and 32-bit ROM reads, as defined by the states of the byte enables. For a 16-bit read, the Trio64V+ automatically increments the lower address once and generates the second byte of read data. For a 32-bit read, the Trio64V+ automatically increments the lower address three times and generates the remaining three bytes of read data. In both cases, TRDY is delayed until all the required data is available on the AD bus. For 16-, 24- or 32-bit accesses, the ROM access time must be 10 SCLKs or less, as opposed to the 14 SCLKs shown in Figure 12.3 for an 8-bit access.

For a VL-Bus configuration, a BIOS ROM read is a standard ISA bus read cycle with the Trio64V+ providing its ROMCS output as the ROM chip and buffer enable (see Figure 12-2). ROMCS is asserted during the time the ROM address is valid and therefore will be active when the chipset asserts the ISA SMEMR signal.

12.1.4 BIOS ROM Address Mapping

The Trio64V+ maps the CPU memory address spaces for the video BIOS ROM into physical ROM addresses. If implemented separately for a VL-Bus system, the video BIOS normally uses the

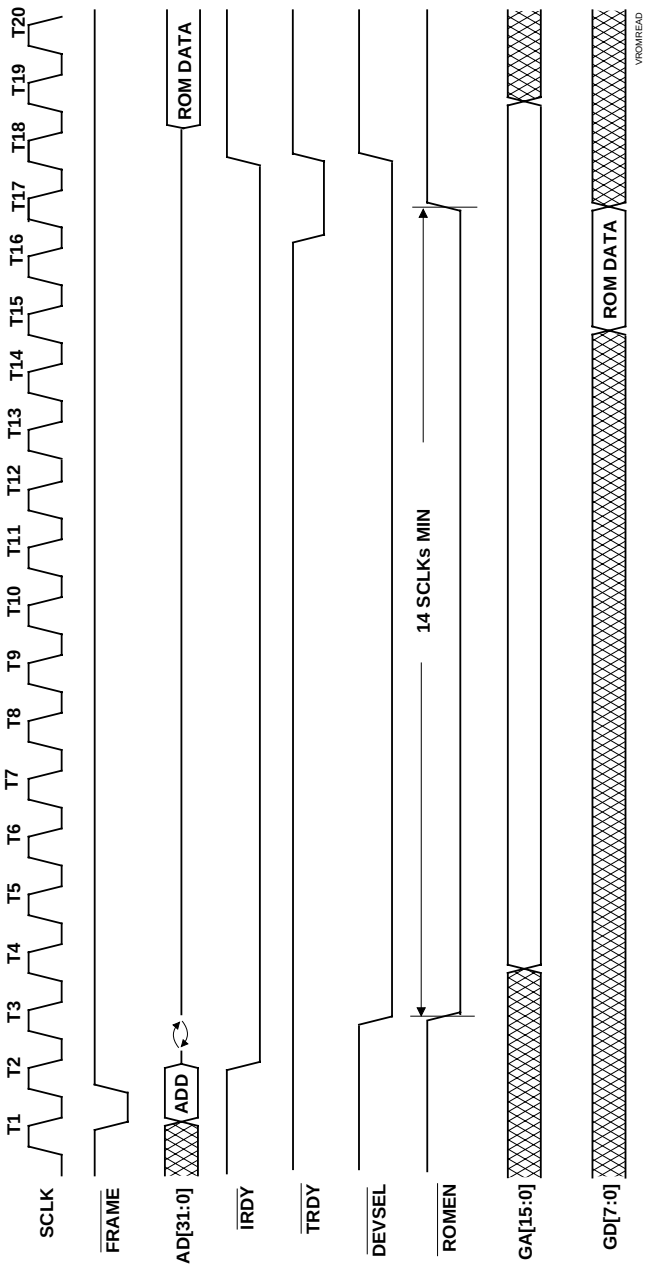


Figure 12-3. BIOS ROM Read Functional Timing - PCI

standard address range C0000H–C7FFFH (32 KBytes). If power-on strapping bit 10 (CR37, bit 2) is strapped low or if bit 2 of CR37 is cleared to 0 in a VL-Bus system, the video BIOS address range becomes C0000H-CFFFFH (64 KBytes). PCI systems support a relocatable 64-KByte video BIOS address range via the BIOS ROM Base Address configuration register (Index 30H).

12.2 GREEN PC SUPPORT

The Trio64V+ provides support for the VESA Display Power Management Signaling (DPMS) protocol by allowing independent control of the HSYNC and VSYNC signals. To use this capability, the bit pattern xxxx0110b must be written to the SR8 register to unlock access to the SRD register. Bits 5-4 of SRD then control the state of HSYNC and bits 7-6 of SRD control the state of VSYNC.

Driving pin 165 ($\overline{\text{PDOWN}}$) low turns off the RGB analog outputs of the internal DACs.

12.3 GENERAL INPUT PORT

The Trio64V+ provides a 4-bit General Input Port (GIP) for PCI configurations as part of its LPB function. The following steps are required to implement it.

1. Disable all other LPB uses.
2. Enable driving of the desired input data onto LD[7:4].
3. If the LPB General Output Port function is also in use, ensure that the correct output data is programmed in MMFF1C_3-0.
4. Program SR1C_1-0 to 01b.
5. Write (anything) to CR5C. The data on LD[7:4] are latched 2 DCLKs later into MMFF1C_7-4. (This also drives the contents of MMFF1C_3-0 onto LD[3:0] and generates the $\overline{\text{STWR}}$ pulse on pin 190. The input data is latched on the rising edge of $\overline{\text{STWR}}$. See Figure 12-6)
6. Disable driving of input data onto LD[7:4].

The Trio64V+ provides an 8-bit GIP for VL-Bus configurations. The block diagram this configuration is shown in Figure 12-4. The following steps implement the GIP function.

1. Set bit 2 of CR55 to 1 to enable the GIP read function.
2. Program SR1C_1-0 to 01b to enable output of $\overline{\text{GPIOSTR}}$ on pin 151.

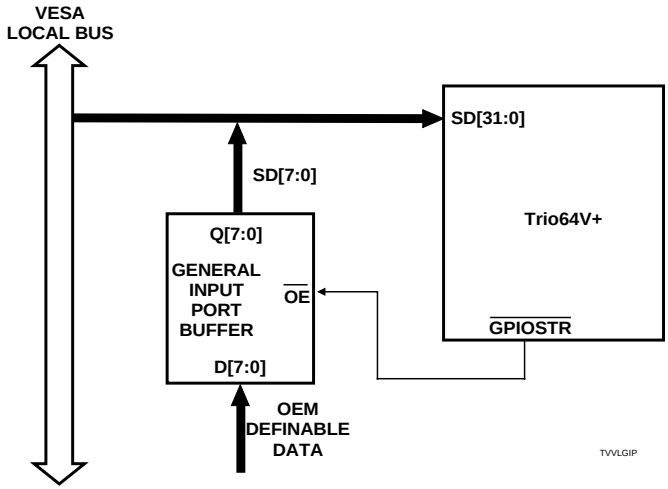


Figure 12-4. General Input Port Interface (VL-Bus)

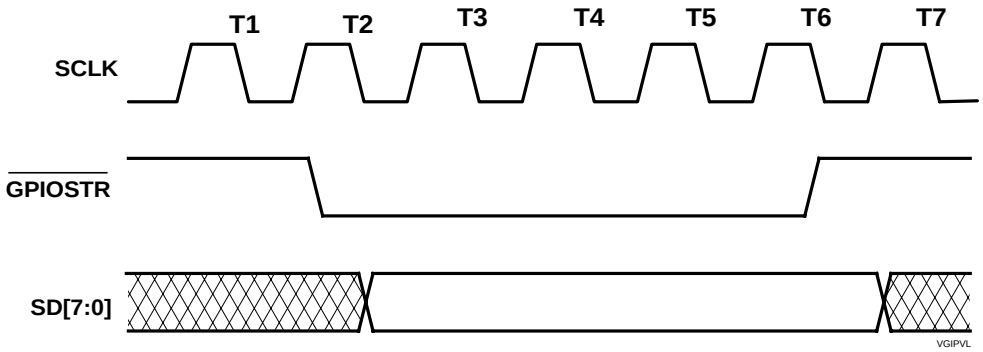


Figure 12-5. General Input Port Timing (VL-Bus)

3. The data is read from an external buffer by a read of port 3C8H (the same as the DAC Write Index off-chip register).

When GPIOSTR is asserted, the data is immediately placed on SD[7:0]. The functional timing for this operation is shown in Figure 12-5. The entire cycle from assertion of SADS to data being available on SD[7:0] takes approximately 18-20 SCLKs.

12.4 GENERAL OUTPUT PORT

The Trio64V+ provides a 4-bit General Output Port (GOP) for PCI configurations as part of its LPB function. To implement this:

1. Disable all other LPB uses.
2. Programmed the desired output in MMFF1C_3-0.
4. Program SR1C_1-0 to 01b to enable output of STWR on pin 190.
5. Write (anything) to CR5C. The data in MMFF1C_3-0 are immediately driven onto

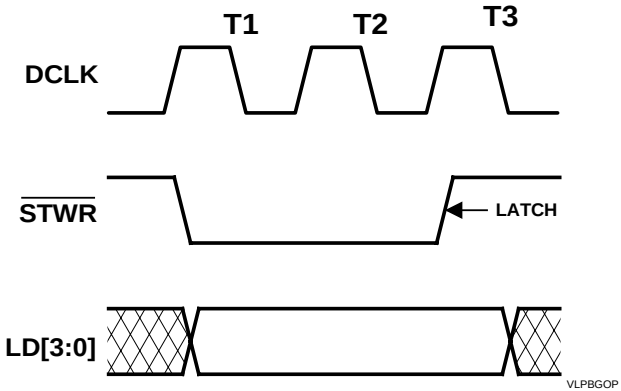


Figure 12-6. General I/O Port Timing (PCI)

LD[3:0] and the $\overline{\text{STWR}}$ pulse is generated. The rising edge of $\overline{\text{STWR}}$ (2 DCLKs after it is asserted) can be used to latch the data into an external device. The data is held valid for 1/2 DCLK after this edge. See Figure 12-6.

The Trio64V+ also provides a 2-bit GOP on dedicated pins for PCI configurations. To implement this:

1. Set SR1C_1 to 1.
2. Program the desired output in CR5C_1-0. This statically drives the state of CR5C_0 onto pin 151 and the state of CR5C_1 onto pin 190. These pin will continue to reflect the register bit states as long as SR1C_1 =1. The values in CR5C_1-0 can be reprogrammed at any time.

The Trio64V+ provides an 8-bit GOP for VL-Bus configurations. The block diagram this configuration is shown in Figure 12-7. Whatever is programmed to CR5C_7-0 is immediately provided to the latch via SD[15:8]. The functional timing for this is shown in Figure 12-8. Note that the data can be latched on either the rising or falling edge of $\overline{\text{GPIOSTR}}$. The entire cycle from assertion of $\overline{\text{SADS}}$ to latching of data in the GOP buffer takes approximately 6-8 SCLKs.

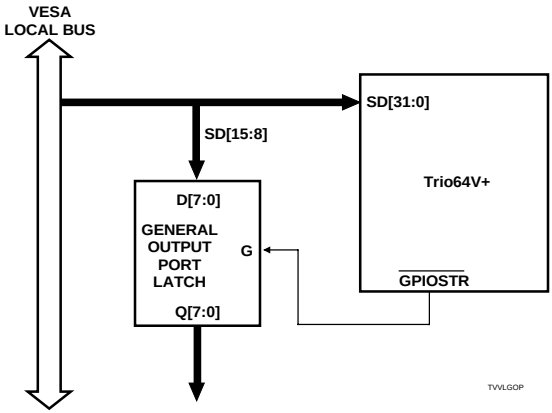


Figure 12-7. General Output Port Interface (VL-Bus)

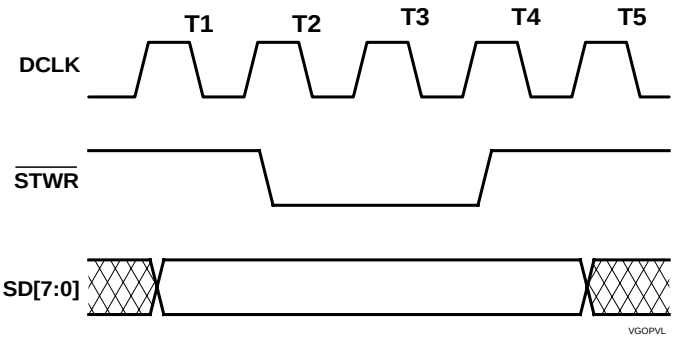


Figure 12-8. General Output Port Timing (VL-Bus)

If both an 8-bit GIP and an 8-bit GOP are required, the GPIOSTR enable input must be qualified with the SR/W signal. Additional discrete logic is required to ensure that only the GOP latch is enabled for writes and only the GIP buffer is enabled for reads.

The Trio64V+ also provides a 2-bit GOP on dedicated pins for VL-Bus configurations. To implement this:

1. Set SR1C_1-0 to 11b.
2. Program the desired output in CR5C_1-0. This statically drives the state of CR5C_0 onto pin 151 and the state of CR5C_1 onto pin 153. These pin will continue to reflect the register bit states as long as SR1C_1-0 =11b. The values in CR5C_1-0 can be reprogrammed at any time.

The 2-bit GOP is only useful for cases where the video BIOS is part of the system BIOS (motherboard implementations) and the ROMCS signal is not needed. If ROMCS is required, a 1-bit GOP is available by programming SR1C_1-0 to 10b. Whatever is programmed to CR5C_0 is reflected on pin 151.

When a VL-Bus configuration powers up with a default value of 00b for bits 1-0, both pin 151 and pin 153 will be driven high (logic 1). Pins 151 and 190 are driven high on power-up for PCI configurations. Thus, external devices with active low enables will not be enabled when connected to these pins.

12.5 FEATURE CONNECTOR INTERFACE

The Trio64V+ provides two approaches to interfacing with a feature connector. If SRD_1 is cleared to 0, this selects Trio64-compatible feature connector operation. This means that some of the feature connector signals are multiplexed on upper PD lines. The pins used to provide this type of operation are listed in Table 12-1.

Table 12-1 Trio64-compatible Feature Connector Configuration

Pin(s)	Signals
144,142, 140, 138, 134, 132, 130, 128, 127, 129, 131, 133, 136, 139, 141, 143	VFCPA[15:0]
151	VFCENFEAT
115	VFCBLANK
117	VFCVCLK
106	VFCVCLKI
109	VFCESYNC
111	VFCEVIDEO
113	VFCEVCLK
149	HSYNC
150	VSYNC

This configuration provides an interface to either a baseline VESA Advanced Feature Connector (VAFC) or pass-through bidirectional feature connector. In all cases, SRD_0 must be set to 1 to enable feature connector operation and SR1C_1-0 must be 00b to enable ENFEAT on pin 151.

For a VAFC implementation, VFCESYNC and EVFCVCLK are pulled up. This means that HSYNC, VSYNC, VFCBLANK and VFCVCLK are always outputs to the feature connector. Pixel address data (PA[15:0] is an output from the Trio64V+ if VFCEVIDEO is high and is an input to the Trio64V+ if VFCEVIDEO is low. If bit 1 of SRB is set to 1, pixel data input is strobed into the internal RAMDAC by VFCVCLKI.

Figure 12-9 shows a VAFC implementation for a 32-bit PD bus implementation (this is used for 1 MByte of video memory). No glue logic is required because the multiplexed pins are not required for PD operation.

Figure 12-10 shows the VAFC implementation for 64-bit PD bus designs. The additional buffers are required to isolate the PD bus from the feature connector during 64-bit operation. This means that memory size will be at least 2 MBytes. Setting bit 0 of SRD to 1 drives the ENFEAT pin low, enabling the isolation buffers. Note that the Trio64V+ always uses a 32-bit PD bus when feature connector operation is enabled and that the speed of the interface (VFCVCLK/DCLK) is limited

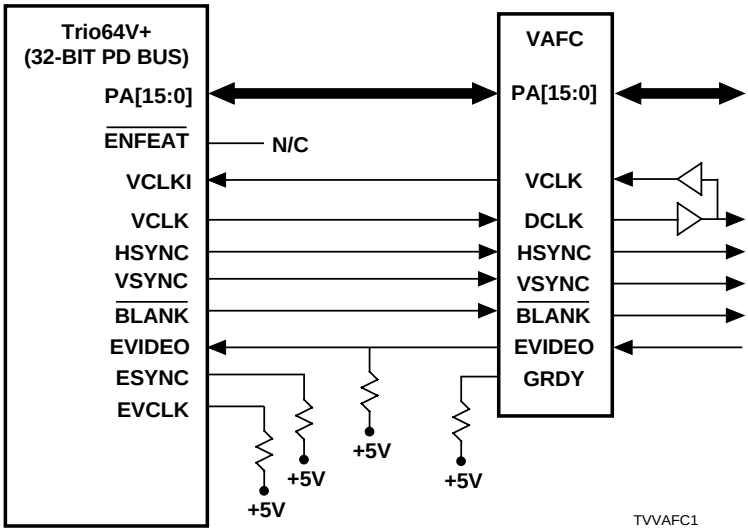


Figure 12-9. VAFC Implementation (32-bit PD Bus)

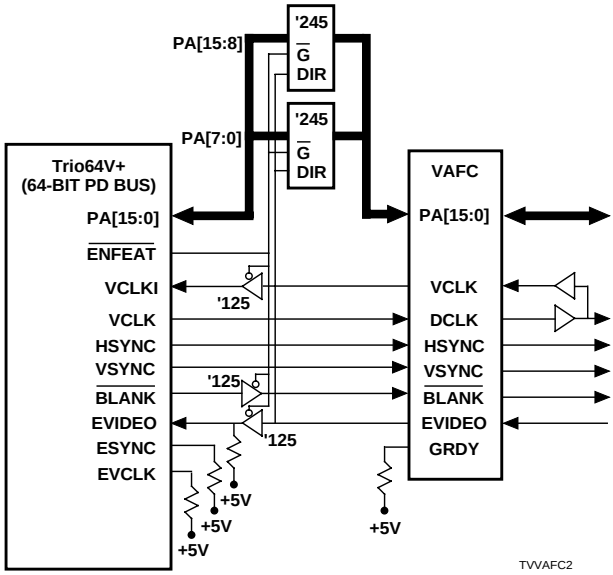


Figure 12-10. VAFC Implementation (64-bit PD Bus)

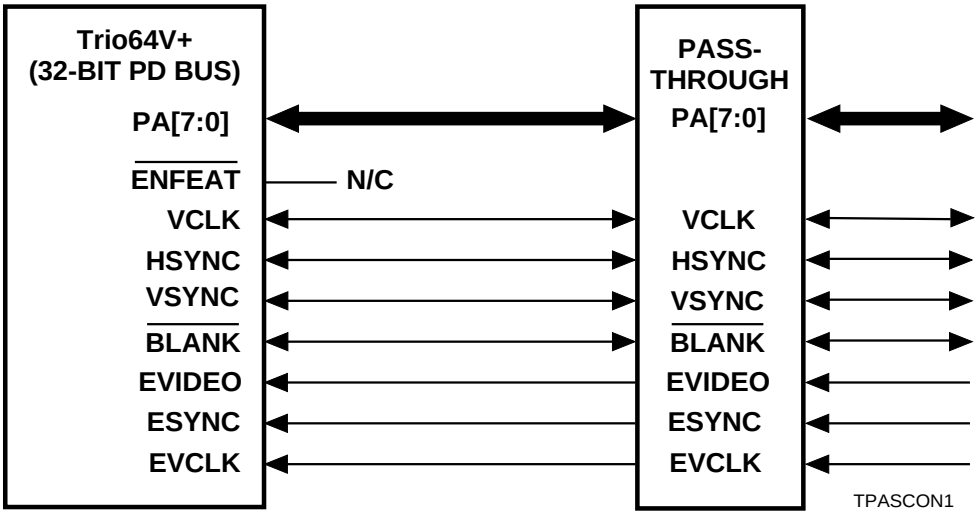


Figure 12-11. Pass-Thru Feature Connector (32-bit PD)

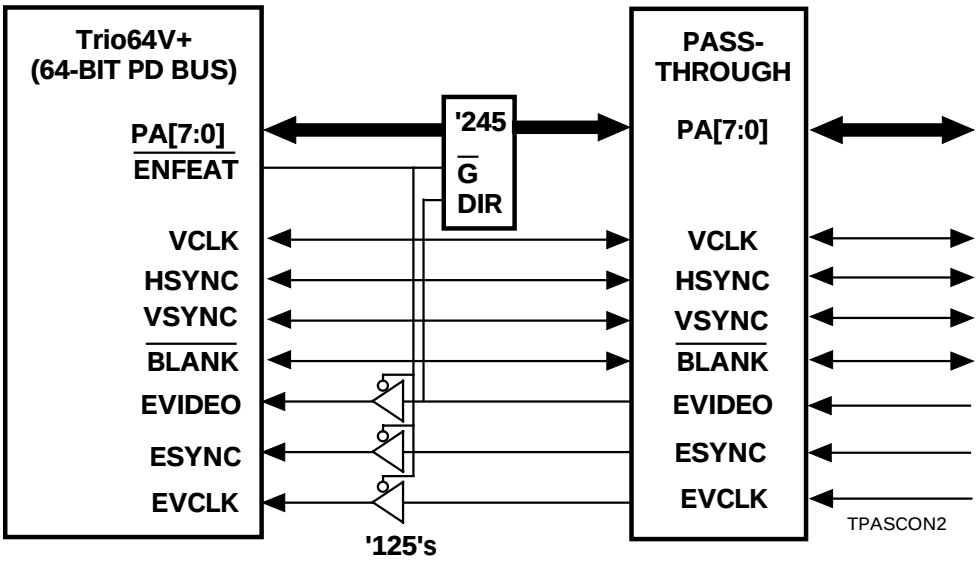


Figure 12-12. Pass-Thru Feature Connector (64-bit PD)

to 37.5 MHz. See the VESA VAFC specification for further description and timing specifications.

Figure 12-11 shows a bidirectional 8-bit pass-through feature connector implementation for the Trio64V+ configured for 32-bit PD bus operation (1 MByte of video memory). When the feature connector function is enabled by setting bit 0 of SRD to 1, the direction of the pixel data is controlled by the polarity of the VFCEVIDEO signal. If VFCEVIDEO is low, pixel data is an input to the Trio64V+. If VFCEVIDEO is high, the Trio64V+ outputs pixel data to the feature connector.

If VFCESYNC is low, HSYNC, VSYNC and $\overline{\text{VFCBLANK}}$ are inputs to the Trio64V+. If VFCESYNC is high, these three signals are outputs. If VFCEVCLK is low, VFCVCLK is an input to the Trio64V+ and is used to clock the pixel data to the internal RAMDAC. If VFCEVCLK is high, VFCVCLK is an output.

The Trio64V+ memory configurations of 2 MBytes and larger will use the entire 64-bit PD bus. In these cases, VFCEVIDEO, VFCESYNC, VFCEVCLK and PA[7:0] are multiplexed with some of the upper 32 PD lines. The buffers shown in Figure 12-12 prevent the PD lines from being driven by the feature connector during 64-bit PD bus operation. As with the VAFC connector, the Trio64V+ uses a 32-bit PD bus during feature connector operations.

Setting SRD_1 to 1 selects LPB feature connector operation. This configuration provides an interface to either a baseline VESA Advanced Feature Connector (VAFC) or pass-through bidirectional feature connector. In all cases, SRD_0 must be set to 1 to enable feature connector operation and SR1C_1-0 must be 00b to enable $\overline{\text{ENFEAT}}$ on pin 151. In addition, LPB operation must be disabled, (MMFF00_0 = 0) and Streams Processor operation must be disabled (CR67_3-2 = 00b) before feature connector operation is enabled.

LPB feature connector operation provides an 8-bit bi-directional feature connector for VL-Bus configurations. The pins used to provide this type of operation are listed in Table 12-2. The interface is the same as shown in Figure 12-11. However, the Trio64V+ is not restricted to 32-bit PD bus operation (as with the Trio64-compatible operation) and can use the full 64-bit PD bus for 2- or 4-MByte memory configurations.

Table 12-2 LPB Feature Connector Configuration (VL-Bus)

Pin(s)	Signals
202, 184, 175, 174, 155, 154, 147, 146	PA[7:0]
151	ENFEAT
206	BLANK
148	VCLK
183	ESYNC
203	EVIDEO
204	EVCLK
149	HSYNC
150	VSYNC

LPB feature connector operation provides a 16-bit bi-directional feature connector for PCI configurations. The pins used to provide this type of operation are listed in Table 12-3. The interface is the same as shown in Figure 12-9. However, the Trio64V+ is not restricted to 32-bit PD bus operation (as with the Trio64-compatible operation) and can use the full 64-bit PD bus for 2- or 4-MByte memory configurations.

Table 12-3 LPB Feature Connector Configuration (PCI)

Pin(s)	Signals
201-199, 189-185, 202, 184, 175, 174, 155, 154, 147, 146	PA[15:0]
151	ENFEAT
206	BLANK
148	VCLK
196	VCLKI
183	ESYNC
203	EVIDEO
204	EVCLK
149	HSYNC
150	VSYNC

8-bit feature connector operation is also available for PCI configurations.

12.6 SERIAL COMMUNICATIONS PORT

A serial communications port is implemented in the MMFF20 register. Bit 4 is set to 1 to enable the interface. The clock is written to bit 0 (= 0) and data to bit 1 (= 0), driving the SPCLK and SPD pins low respectively. The state of the SPCLK pin can be read via bit 2 and the state of the SPD pin can be read via bit 3. The SPCLK and SPD pins are tri-stated when their corresponding control bits are reset to 0, allowing other devices to drive the serial bus.

Typical uses for the serial port are for DDC monitor communications and I^2C interfacing. When SPCLK and SPD are tri-stated, the Trio64V+ can detect an I^2C start condition (SPD driven low while SPCLK is not driven low). This condition is generated by another I^2C master that wants control of the I^2C bus. If bit 19 of MMFF08 is set to 1, detection of a start condition generates an interrupt and sets bit 3 of MMFF08 to 1. If bit 24 of MMFF08 is set to 1, the Trio64V+ drives SPCLK low to generate I^2C wait states until the Host can clear the interrupt and service the I^2C bus.

The SPCLK and SPD signals are multiplexed with the ESYNC and BLANK feature connector signals on pins 205 and 206 for VL-Bus configurations. If DDC, I^2C and/or feature connector operation are required, the lines from pins 205 and 206 must be multiplexed to separate pairs of lines for each operation to provide the necessary signal isolation. The ENFEAT signal should be used to enable ESYNC and BLANK onto one pair of lines to the feature connector. When ENFEAT is high, one bit of the General Output Port can be used to select between I^2C and DDC operation, with a 1 enabling output on one pair of lines and a 0 enabling output on another.

The National Semiconductor CD4052B Dual 4-Channel Analog Multiplexer/Demultiplexer provides the capability to channel two lines to one of four pairs of lines based on two select signals. Each side can act as either an input or output. A set of schematics showing the use of this part is available.

For PCI LPB configurations, SPCLK and SPD are not multiplexed. This reduces the isolation requirements.

If PD26 is strapped low at reset, strapping of PD25 selects either E2H (PD25 pulled high) or E8H (PD25 pulled low) as the I/O port address for the serial port register MMFF20. This allows the ports to be used for serial communications, typically I^2C, when the Trio64V+ in not enabled. If analog switches are used for isolation as explained in the previous paragraph, designers must ensure that the I^2C function is enabled by default on reset. If I/O access is desired after the Trio64V+ has been enabled and then disabled, programmers must ensure that the I^2C function is selected before the Trio64V+ is disabled because the General Output Port may not be available to change the selection.

12.7 INTERRUPT GENERATION

For a PCI configuration, pin 152 is pulled low to signal an interrupt (INTA). For a VL-Bus configuration, pin 152 is pulled high to signal an interrupt (SINTR).

Whatever the mode of operation (VGA or Enhanced), bit 4 of CR32 must be set to 1 to enable interrupt generation.

When the Trio64V+ is being operated in VGA mode (CR66_0 = 0), only a vertical retrace can generate an interrupt. This is enabled when bit 5 of CR11 is cleared to 0 and a 1 has been programmed into bit 4 of CR11. When an interrupt occurs, it is cleared by writing a 0 to bit 4 of CR11. The interrupt must then be re-enabled by writing a 1 to the same bit. Note that the BIOS clears both bit 4 and bit 5 of CR11 to 0 during power-on, a mode set or a reset. Thus, interrupt generation is disabled until bit 4 is set to 1.

When the Trio64V+ is being operated in Enhanced mode (CR66_0 = 1), interrupts can be generated by a vertical retrace, Graphics Engine busy, command FIFO overflow and command FIFO empty. These interrupts are enabled and cleared and their status reported via 42E8H.

Multiple interrupts can be enabled at the same time in Enhanced mode. The interrupt pin will

remain asserted until all interrupt status bits are cleared.

Section 13: Basic Software Functions

This section describes the basic operations required to program the Trio64V+.

13.1 CHIP WAKEUP

The following program wakes up the Trio64V+. This is required for systems that do not use the S3 style of video BIOS, e.g., UNIX.

```
mov dx,3c3h       ; Video Subsystem Enable register address
mov al,01h        ; bit 0 = 1, enable graphics display
out dx,al         ; write new bit values to 3c3h
[load CRTCs]      ; program CRTC registers
mov dx,3C6h       ; DAC Mask register address
mov al,FFh        ; DAC Mask register initialization value
out dx,al         ; Initialize DAC mask and release BLANK signal
 .
 .
 .
```

13.2 REGISTER ACCESS

S3 has added a number of graphics registers to the standard VGA set. These can be locked when not in use to prevent accidental access and unlocked when access is requires. This section explains how this is done.

13.2.1 Unlocking the S3 Registers

The S3 registers (CR30 and higher plus the Enhanced Commands registers) must be unlocked before they can be accessed by the CPU. The code to do this is:

Note: Byte operations are used in the following examples for clarity. Word operations, e.g..,

```
mov ax, 4838h
out dx,ax
```

should be used for efficiency instead of the operations used in the first example below.

```
; Write code to SR8 to provide access to the S3 extended Sequencer registers
(SR9-SRFF)
;
   mov dx,3c4h       ; copy index register address into dx
   mov al,08h        ; copy index for SR8 register into al
   out dx,al         ; write index to index register
   inc dx            ; increment dx to 3c5h (data register address)
   mov al,06h        ; copy unlocking code (xxxx0110b, x=don't care) to al
   out dx,al         ; write the unlocking code to the data register
   dec dx            ; restore the index register address to dx
;
; Write code to CR38 to provide access to extended CRTC registers CR2D-CR3F
;
   mov dx,3d4h       ; copy index register address into dx
   mov al,38h        ; copy index for CR38 register into al
   out dx,al         ; write index to index register
   inc dx            ; increment dx to 3D5h (data register address)
   mov al,48h        ; copy unlocking code (01xx10xxb, x=don't care) to al
   out dx,al         ; write the unlocking code to the data register
   dec dx            ; restore the index register address to dx
;
; Write code to CR39 to provide access to extended CRTC registers CR40-CRFF
;
; dx is already loaded with 3D4h because of the previous instruction
;
   mov al,39h        ; copy index for CR39 register into al
   out dx,al         ; write index to index register
   inc dx            ; increment dx to 3D5h (data register address)
   mov al,0a5h       ; copy unlocking code to al (the code a5H also unlocks
                     ; access to configuration registers CR36, CR37 and CR68
   out dx,al         ; write the unlocking code to the data register
   dec dx            ; restore the index register address to dx
;
; Set bit 0 in CR40 to enable access to the Enhanced Programming registers.
;
; dx is already loaded with 3D4h because of previous instruction
   mov al,40h        ; copy index for CR40 register into al
   out dx,al         ; write index to index register
   inc dx            ; increment dx to 3D5h (data register address)
   in al,dx          ; read register data for read/modify/write operation
   or al,1           ; set bit 0 to 1
   out dx,al         ; write the unlocking code to the data register
   dec dx            ; restore the index register address to dx
```

13.2.2 Locking the S3 Registers

Relocking the S3 registers is done by repeating the code used to unlock the registers except:

1. The values written to the SR8, CR38 and CR39 registers must change at least one of the significant bits in the valid code pattern. For example, 00h will always accomplish this.

2. After first verifying that the Graphics Engine is not busy (bit 9 of 9AE8H is 0), bit 0 of CR40 must be cleared to 0. A read-modify-write cycle must be used instead of the code used above to prevent overwriting of any changes made to bits 7-1 in CR40 since reset.

```
mov dx,3d4h       ; copy index register address into dx
mov al,40h        ; copy index for CR40 register into al
out dx,al         ; write index to index register
inc dx            ; increment dx to 3D5h (data register address)
in al,dx          ; read content of CR40 into al
and al,0feh       ; clear bit 0 to 0
out dx,al         ; write to CR40 to lock the Enhanced Commands registers
dec dx            ; restore the index register address to dx
```

13.3 TESTING FOR THE PRESENCE OF A Trio64V+ CHIP

After unlocking, a Trio64V+ chip can be identified via CR2E and CR2F.

```
   mov dx,3d4h       ; copy index register address into dx
   mov al,2eh        ; copy index for CR2E register into al
   out dx,al         ; write index to index register
   inc dx            ; increment dx to 3D5h (data register address)
   in al,dx          ; read content of CR2E into al
   cmp al,11h        : compare chip ID to the desired chip ID (11h)
   jne not_TV+       ; jump to a label if chip ID does not match desired ID
   mov dx,3d4h       ; copy index register address into dx
   mov al,2fh        ; copy index for CR2F register into al
   out dx,al         ; write index to index register
   inc dx            ; increment dx to 3D5h (data register address)
   in al,dx          ; read content of CR2F into al
   and al,40h        ; mask out all but bit 6
   cmp al,40h        : compare chip revision to the desired chip revision (4xh)
   jne not_TV+       ; jump to a label if revision ID is not correct
   .                 : Trio64V+ found - continue with setup
   .
   .
```

Note that the value in CR2F may be different than the 4xH shown in this example. The correct value can be determined from the stepping information for the chip. The PCI configuration space device and revision ID fields can also be used to identify the chip for PCI configurations.

13.4 GRAPHICS MODE SETUP

Some programs may require a graphics mode other than that provided by standard operation. For example, a DOS game may require a resolution of 640x400x8 (VESA mode 100) instead of the standard DOS mode, e.g., mode 03. The following code fragment shows how this is done.

```
mov ax,4f02h      ; VESA super VGA mode function call
mov bx,100h       ; mode 100
int 10h           ; call video BIOS
```

Section 14: VGA Compatibility Support

This section describes Trio64V+ support for standard VGA and VESA Super VGA graphics standards.

14.1 VGA COMPATIBILITY

The Trio64V+ is compatible with the VGA standard. These modes are not accelerated using the Graphics Engine. However, other design features provide excellent VGA performance.

Several of the standard VGA registers have been modified or extended in the Trio64V+. Table 14-1 describes these changes.

Table 14-1. Standard VGA Registers Modified or Extended in the Trio64V+

Register	Change to Standard VGA Definition
CR0	Extension bit 8 is bit 0 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size.
CR1	Extension bit 8 is bit 1 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size.
CR2	Extension bit 8 is bit 2 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size.
CR3	The length of the blanking pulse defined in this register can be extended by 64 DCLKs via bit 3 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size.
CR4	Extension bit 8 is bit 4 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size.
CR5	The length of the HSYNC pulse defined in this register can be extended by 32 DCLKs via bit 5 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size.
CR6	In addition to the standard VGA extensions (bit 8 is bit 0 of CR7, bit 9 is bit 5 of CR47), bit 10 is bit 0 of CR5E. Bit 4 of CR35 controls access to this register.
CR7	Bit 4 of CR35 controls access to bits 0, 2, 3, 5 and 7 of this register.
CR9	Bit 4 of CR35 controls access to bit 5 of this register.
CRC	The display start address is a 20-bit value for the Trio64V+. The extension bits (20-16) are bits 4-0 of CR69.
CRE	The cursor location address is a 20-bit value for the Trio64V+. The extension bits (20-16) are bits 4-0 of CR69.

CR10	In addition to the standard VGA extensions (bit 8 is bit 2 of CR7, bit 9 is bit 7 of CR7), bit 10 is bit 4 of CR5E. Bit 4 of CR35 controls access to this register.
CR11	Bit 4 of CR35 controls access to bits 3-0 of this register. Bit 6 (3/5 refresh cycles per line) can be overridden by CR3A_2-0. Setting bit 1 of CR33 to 1 disables the write protect effect of bit 7 of this register on bits 1 and 6 of CR7.
CR12	In addition to the standard VGA extensions (bit 8 is bit 1 of CR7, bit 9 is bit 6 of CR7), bit 10 is bit 1 of CR5E.
CR13	Bit 2 of CR43 is the old extension bit (bit 8) of this register. Bits 5-4 of CR51 are the new extension bits (bits 9-8) of this register.
CR15	In addition to the standard VGA extensions (bit 8 is bit 3 of CR7, bit 9 is bit 5 of CR9), bit 10 is bit 2 of CR5E. Bit 4 of CR35 controls access to this register.
CR16	Bit 4 of CR35 controls access to this register.
CR17	Bit 5 of CR35 controls access to bit 2 of this register.
CR18	In addition to the standard VGA extensions (bit 8 is bit 4 of CR7, bit 9 is bit 6 of CR9), bit 10 is bit 6 of CR5E.
AR00-AR0F	Bit 6 of CR33 controls access to these registers.
3C6H-3C9H	Bit 4 of CR33 controls writes to these registers.

For a detailed discussion of VGA programming, see *Programmer's Guide to the EGA, VGA and Super VGA Cards, 3rd Edition* by Richard F. Ferraro (Addison-Wesley Publishing Company, Inc).

14.2 VESA SUPER VGA SUPPORT

The Trio64V+ supports the extended (Super) VGA modes defined by VESA. All modes are accelerated by the Graphics Engine except for the planar (4 bits/pixel) ones.

Section 15: Enhanced Mode Programming

Enhanced mode provides a level of performance far beyond what is possible with the VGA architecture. Hardware line drawing, BitBLT, rectangle fill and other drawing functions are implemented. Also implemented are data manipulation functions, such as data extension, data source selection, and read/write bitplane control. Hardware clipping is supported by 4 registers that define a rectangular clipping area. While in Enhanced mode, the display memory bit map can be updated in two ways. One is to have the CPU write directly to memory. (This is also possible in non-Enhanced modes via paging.) The other is to have the CPU issue commands to the Graphics Engine, which then controls pixel updating. This section explains these two methods and provides a comprehensive set of Enhanced mode programming examples.

15.1 LINEAR ADDRESSING FOR DIRECT VIDEO MEMORY CPU ACCESSES

Linear addressing is useful when software requires direct access to display memory. Enhanced mode operation must be enabled before linear addressing is enabled. This means that bit 0 of 4AE8H is set to 1 to enable Enhanced mode functions and bit 3 of CR31 is set to 1 to specify Enhanced mode memory mapping.

The Trio64V+ provides linear addressing of up to 4 MBytes of display memory. The Graphics Engine busy flag, bit 9 of 9AE8H, should be verified to be 0 (not busy) before linear addressing is enabled by setting bit 4 of CR58 to 1. The size of the linear address window is set via bits 1-0 of CR58. The base address for the linear addressing window is set via CR59 and CR5A (or via the Base Address 0 (Index 10H) PCI configuration register for PCI systems).

For operation in real mode, the linear addressing window size can be set to 64 KBytes. The base address for the window is set to A0000H by programming bits 31-16 of the window position in CR59-CR5A to 000AH. If bit 0 of CR31 is set to 1, the memory page offset (64K bank) specified in bits 5-0 of CR6A is added to the linear addressing window position base address, allowing access to up to 4 MBytes of display memory through a 64-KByte window.

The above discussion applies when the Trio64V+ is programmed for backwards-compatible MMIO operation. See Section 15.3.2 for instructions on how to perform linear addressing when new MMIO is enabled.

15.2 VIDEO MEMORY ACCESS THROUGH THE GRAPHICS ENGINE

When updating the display bitmap through the Graphics Engine, all CPU data moves through the Pixel Data Transfer registers (E2E8H and E2EAH). These can be memory mapped as explained in Memory Mapping of Enhanced Mode Registers later in this section.

The Graphics Engine manipulates the bits for each pixel to assign a color index or true color value, which is then translated via a programmable RAMDAC before being displayed on a CRT. Selected bits in a pixel can be masked off from being displayed by programming the DAC Mask register (3C6H). The Trio64V+ can manipulate 64 bits each clock cycle, from two 32-bit pixels to eight 8-bit pixels.

Figure 15-1 is a flowchart for the process of updating the color of each pixel. Start at the block labeled 'New Color' in the middle of Figure 15-1. At this stage, a color has been determined that may or may not be used to update a pixel in the bitmap. How this color is determined will be covered later.

The first hurdle for the new color is the color compare process. If this is turned off (bit 8 of BEE8H, Index 0EH = 0), the new color is passed to the Write Mask register (AAE8H). If the plane to which the pixel update is directed has been masked off in this register, no update occurs. Otherwise, the new color value is written to the bitmap.

If color compare is enabled (bit 8 of BEE8H, Index 0EH = 1), the new color value (source) is compared to a color value programmed into the Color Compare (B2E8H) register. The sense of the color comparison is determined by the SRC NE (source not equal) bit (bit 7) of BEE8H, Index 0EH. If this bit is 0, the new pixel color value is passed to the write mask only when the source color does not match the color in the Color Compare register. If this bit is 1, the new pixel color value is passed to the write mask only when the source color matches the color in the Color Compare register. If the new pixel color value is not passed to the write mask, no update occurs. Notice that the source color is used for the comparison, as opposed to the destination (bitmap) color used by the standard VGA color compare operation.

The new color is the result of a logical mix performed on a color source and the current color in the bitmap. For example, the color source could be XORed with the bitmap color. The new color can also be selected by operating on only the color source or the bitmap color, e.g., NOT color source. Both the color source and the logical mix operation are specified in either the Background Mix register (B6E8H) or the Foreground Mix register (BAE8H). Which of these two registers is used is determined by the settings of bits [7:6] of the Pixel Control register (BEE8H, Index 0AH).

To set up the pixel color updating scheme, the programmer specifies one of four color sources by writing bits 6-5 of the Background Mix and Foreground Mix registers. The color sources are:

- Background Color register (A2E8H)
- Foreground Color register (A6E8H)
- CPU (via the Pixel Data Transfer registers (E2E8H, E2EAH))
- Current display bitmap color index

One of 16 logical operations is chosen by writing bits 3-0 of the Background Mix and Foreground Mix registers. Examples of logical operations are making the new pixel color index equal to the NOT of the current bitmap color index or making the new index equal to the XOR of the source and current bitmap indices.

When the logical operation and color source have been specified in the Background and Foreground Mix registers, bits 7-6 of the Pixel Control register are written to specify the source of the mask bit

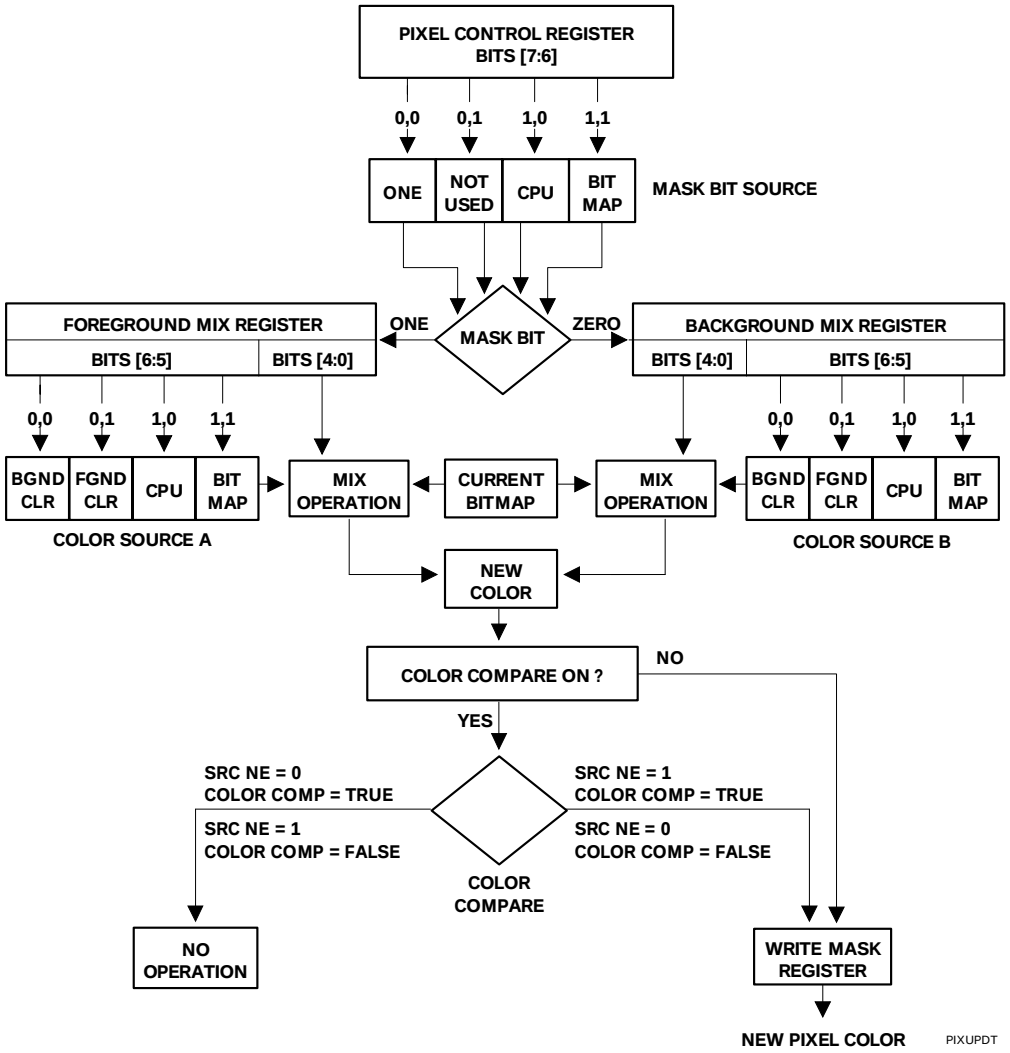


Figure 15-1. Pixel Update Flowchart

value. If the resulting mask bit is a 'ONE', the Foreground Mix register is used to determine the color source and mix. If the mask bit is a 'ZERO', the Background Mix register is used to determine the color source and mix. There are three sources for the mask bit value:

- Always ONE (Foreground Mix register used)
- CPU (via the Pixel Data Transfer registers (E2E8H, E2EAH))
- Bitmap

Setting bits 7-6 to 00b sets the mask bit to 'ONE'. All drawing updates to the video bitmap use the Foreground Mix register settings. This setup is used to draw solid lines, through-the-plane image transfers to display memory and BitBLTs.

If bits 7-6 are set to 10b, the mask bit source is the CPU. After the draw operation command is issued to the Drawing Command register (9AE8), a mask bit corresponding to every pixel drawn on the display must be provided via the Pixel Data Transfer register(s). If the mask bit is 'ONE', the Foreground Mix register is used. If the mask bit is 'ZERO', the Background Mix register is used. Note that if the color source is the CPU, the mask bit source cannot also be the CPU, and vice versa. This setup is used to transfer monochrome images such as fonts and icons to the screen.

If bits 7-6 are set to 11b, the current display bit map is selected as the mask bit source. The Read Mask register (AAE8H) is set up to indicate the active planes. When all bits of the read-enabled planes for a pixel are a 1, the mask bit 'ONE' is generated. If any one of the read-enabled planes is a 0, then a mask bit 'ZERO' is generated. If the mask bit is 'ONE', the Foreground Mix register is used. If the mask bit is 'ZERO', the Background Mix register is used. Note that if the color source is the bitmap, the mask bit source cannot also be the bitmap, and vice versa. This setting is used to BitBLT patterns and character images.

15.3 MEMORY MAPPING OF REGISTERS

The Trio64V+ provides two memory-mapped I/O (MMIO) schemes. One method is identical to that provided by the Trio64 and provides compatibility with older software. This provides memory mapping of a limited number of Enhanced mode registers plus the new LPB and Streams Processor registers. Packed register access is also provided. The second method incorporates linear addressing and provides memory mapping of all registers, including the packed registers. The second method also allows big or little endian addressing. Each of these MMIO methods is described below.

15.3.1 Backward-Compatible MMIO

Most of the Enhanced registers can be memory-mapped (MMIO). This function is enabled by setting bits 4-3 of CR53.

Image writes normally made via I/O addresses E2E8H and E2EAH (the Pixel Data Transfer registers) are made instead by accessing any memory location in the 32-KByte address space from A0000H to A7FFFH. This allows efficient use of the MOVSW and MOVSD assembly language commands. Accesses must be to even word or doubleword addresses, depending on the specification of the bus width via bits 10-9 of 98E8H. Software must not make E2E8H, E2EAH writes beyond the A7FFFH range.

Accesses to the Enhanced command registers are made to particular locations in the A8000H to AFFFFH address range as shown in Table 15-1. Both 16-bit reads and writes are supported. Only 32-bit writes (bit 9 of BEE8H_E set to 1) are supported.

If MMIO is enabled, bit 7 of SR9 allows register access to be either I/O or MMIO or MMIO only.

Table 15-1 Enhanced Registers Memory Mapping

Register Mnemonic	I/O Address (Hex) MMIO = Axxxx	Register Mnemonic (Packed)	Packed MMIO Address (Hex) (Axxxx)
CUR_Y, CUR_X	82E8, 86E8	ALT_CURXY	8100, 8102
DESTY_AXSTP, DESTX_DIASTP	8AE8, 8EE8	ALT_STEP	8108, 810A
ERR_TERM	92E8		8110
CMD	9AE8		8118
SHORT_STROKE	9EE8		811C
BKGD_COLOR	A2E8		8120
FRGD_COLOR	A6E8		8124
WRT_MASK	AAE8		8128
RD_MASK	AEE8		812C
COLOR_CMP	B2E8		8130
BKGD_MIX, FRGD_MIX	B6E8, BAE8	ALT_MIX	8134, 8136
SCISSORS_T, SCISSORS_R	BEE8_1, BEE8_2		8138, 813A
SCISSORS_B, SCISSORS_R	BEE8_3, BEE8_4		813C, 813E
PIX_CNTL, MULT_MISC2	BEE8_A, BEE8_D		8140, 8142
MULT_MISC, READ_SEL	BEE8_E, BEE8_F		8144
MIN_AXIS_PCNT, MAJ_AXIS_PCNT	BEE8_0, 96E8	ALT_PCNT	8148, 814A
PIX_TRANS	E2E8, E2EA	PIX-TRANS	

For improved performance, most of the Enhanced mode registers can also be written (but not read) via a packed configuration. The 16-bit registers are paired so that two registers can be accessed via a single 32-bit write. The addresses for this packed configuration are given in Table 15-1. The packed register access function is enabled when MMIO is enabled.

The Trio64V+ supports the Trio64 MMIO scheme when bits 4-3 of CR53 are programmed to 10b and bit 5 of CR53 is cleared to 0. In addition, the new LPB and Streams Processor registers are also accessible in the A8000H - AFFFFH window. If bit 5 of CR53 is set to 1, the registers are accessible in the B8000H - BFFFFH window. However, image writes cannot be made to B0000H - B7FFFH. This region and the entire A0000H - AFFFFH region are left free for VGA memory and other uses.

The Trio64 scheme is also available as explained in the previous paragraph when bit 4-3 of CR53 are set to 11b. In this case, the registers can be accessed either by this scheme or by the new MMIO explained in the next section.

15.3.2 New MMIO

The new MMIO method for the Trio64V+ is available for PCI configurations and provides a 64-MByte addressing window starting at the base address specified in CR59-5A. This space is divided into a 32-MByte space for little endian (Intel-style) addressing and a 32-MByte space for big endian (Power PC-style) addressing. All registers and data transfer locations are mapped into this area as shown in Table 15-2.

Table 15-2 New MMIO Addresses

Lower 32 MBytes - Little Endian Addressing	
Description	**Offset From Base (Hex)**
Linear Addressing (16M)	000 0000 - 0FF FFFF
Image Data Transfer (32K)	100 0000 - 100 7FFF
PCI Configuration Space Registers	100 8000 - 100 8043
Packed Enhanced Registers	100 8100 - 100 814A
Streams Processor Registers	100 8180 - 100 81FF
Current Y Position Register	100 82E8
CRT VGA 3B? Registers	100 83B0 - 100 83Bx
CRT VGA 3C? Registers	100 83C0 - 100 83Cx
CRT VGA 3D? Registers	100 83D0 - 100 83Dx
Subsystem Status Enhanced Register (42E8H)	100 8504
Advanced Function Control Register (4AE8H)	100 850C
Enhanced Registers	100 86E8 - 100 EEEA
Local Peripheral Bus Registers	100 FF00 - 100 FF5C

The new MMIO (only) is enabled by setting bits 4-3 of CR53 to 01b. It is also enabled in conjunction with the old MMIO scheme when bits 4-3 of CR53 are set to 11b. This is the default for a PCI bus configuration, allowing PCI software immediate access to all registers and the ability to relocate the address space. VL-Bus configurations power up with bits 4-3 of CR53 cleared to 00b, disabling both old and new MMIO operation. If either the old or new MMIO is enabled, bit 7 of SR9 allows register access to be either programmed I/O (IN, OUT) or MMIO (MOV) or MMIO only.

With the new MMIO enabled, the first 16 MBytes of each 32M address space (big and little endian) are dedicated to linear addressing. A maximum of 4 MBytes of each address space (starting at the lowest address of the space) is usable with the Trio64V+. The base address is taken from bits 31-26 of the linear address window position (bits 7-2 of CR59 or the high order 6 bits of the the PCI Base Address 0). This is concatenated with the display memory address specified by the programmer.

In addition to enabling the new MMIO, the programmer must also enable linear addressing and specify the window size exactly as required for the old linear addressing. Note that since only bits 31-26 are used to specify the base address, A0000H cannot be specified and the 64K banking scheme possible with the old linear addressing cannot be used with the new linear addressing.

When big endian addressing is used, the required byte swapping for linear addressing is specified by bits 2-1 of CR53. This applies to both reads and writes.

15.4 PROGRAMMING

Three different programming schemes are available, I/O, standard MMIO and packed register MMIO. Examples of how each is used to assign vertical and horizontal coordinates to Current X and Y Position registers (82E8H and 86E8H) are:

I/O Format:

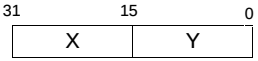
```
MOV  DX,CUR_X
MOV  AX,X
OUT  DX,AX
MOV  DX,CUR_Y
MOV  AX,Y
OUT  DX,AX
```

Standard MMIO Format:

```
Enable MMIO
Point ES to A000H
Load x and y values into AX and BX
MOV  ES:[CUR_Y], BX
MOV  ES:[CUR_X], AX
```

Packed Register MMIO:

```
Enable MMIO
Point ES to A000H
Load the x and y values into EAX (y value in the low word and x value in the high word), I.e.,
```




```
MOV  ES:[ALT_CURXY], EAX
```

The packed register MMIO scheme is the most efficient and is used where appropriate in the programming examples provided later in this section. All assume that the ES register points to A000H.

15.4.1 Notational Conventions

The REGMNEMONIC on the left hand side of the arrow is the register mnemonic of the I/O port being written into. Text following a ';' is a comment.

```
REGMNEMONIC ⇐ XXXXH                 ; Load a hexadecimal value into the register.
REGMNEMONIC ⇐ XXXXD                 ; Load a decimal value into the register.
REGMNEMONIC ⇐ XXXX                  ; Load a decimal value into the register
REGMNEMONIC ⇐ XXXXXXXXXXXXXXXXB    ; Load a binary value into the register.
```

Image transfers (CPU pixel data writes to the frame buffer) are notated as follows:

```
COUNT
PIX_TRANS ⇐ IMAGEDATA
```

The COUNT is the number of CPU writes. PIX_TRANS means either the E2E8H, E2EAH pixel transfer registers or the 32K memory space from A0000H to A7FFFH as explained in Section 15.3.1 above.

15.4.2 Initial Setup

All examples assume the desired mode is selected.

The Bitmap Access Through the Graphics Engine section earlier in this section explains in detail how the colors, mixes and the data extensions are set for each example. These registers need not be set repeatedly before a series of draw commands if they use the same colors, mixes and data extension.

All bitmap updates are affected by the settings in the clipping registers (BEE8H, Indices 1-4) and the choice of internal or external clipping (BEE8H, Index E, bit 5). These must be set up so they include the area being drawn into.

If color compare is to be used, it must be enabled by setting bit 8 of BEE8H, Index 0EH to 1. Bit 7 of this register determines whether a TRUE or FALSE comparison allows the pixel update to continue. The comparison color is programmed into the Color Compare register (B2E8).

All planes are enabled for writing unless explicitly set otherwise in an example. This is done via the Write Mask register (AAE8H).

15.4.3 Programming Examples

This section provides programming examples for the following Enhanced mode drawing operations:

- Solid Line
- Textured Line
- Rectangle Fill Solid
- Image Transfer—Through the Plane
- Image Transfer—Across the Plane
- BitBLT—Through the Plane
- BitBLT—Across the Plane
- PatBLT—Through the Plane
- PatBLT—Across the Plane
- Short Stroke Vectors
- Programmable Hardware Cursor

Some programming steps are repeated in multiple examples. They are explained in detail at their first occurrence. Therefore, readers are encouraged to work through the examples from first to last. The register mnemonics used in the examples are listed in Table 15-1. Other mnemonics used are:

Mnemonic	Description
NEW	Mix = 00111b in bits 4-0 of BAE8H or B6E8H. This overwrites the present bitmap color value with a new value.
XOR	Mix = 00101b in bits 4-0 of BAE8H or B6E8H. The current bitmap color is XORed with the new color.

15.4.3.1 Solid Line

This command draws a one pixel wide solid line from screen coordinates x1,y1 to x2,y2. Bresenham parameters are used to define the line. The Pixel Control register (BEE8H, Index AH) must be set to A000H to select the Foreground Mix register to specify the color source and mix type.

Setup:

Drawing a line using axial coordinates requires programming the axial step constant into the Destination Y-Position/Axial Step Constant (8AE8H) register (DESTY_AXSTP), the diagonal step constant into the Destination X-Position/Diagonal Step Constant (8EE8H) register (DESTX_DIASTP) and the error term into the Error Term (92E8H) register (ERR_TERM). Calculation of these Bresenham parameters is based on the MAX and MIN parameters as calculated below.

MAX = maximum(ABS(x2–x1), ABS(y2–y1))
MIN = minimum(ABS(x2–x1), ABS(y2–y1))

where maximum means choose the largest of the two terms in parentheses and minimum means choose the smallest. ABS means take the absolute value of the expression.

Bits 7-5 of the Drawing Command (9AE8H) register (CMD) specify the drawing direction. Setting bit 7 to 1 means that the Y drawing direction is positive (y1 < y2). Clearing bit 7 to 0 means the Y drawing direction is negative (y1 > y2). Setting bit 6 to 1 means that Y is the major (longer) axis (ABS(x2–x1) > ABS(y2–y1)). Clearing bit 6 to 0 means that X is the major axis. Setting bit 5 to 1 means that the X drawing direction is positive (x1 < x2). Clearing bit 5 to 0 means that the X drawing direction is negative (x1 > x2). These values replace the DDD sequence in the write to the CMD register shown in the pseudocode below.

The mix NEW represents a setting of 0111b in bits 3-0 of the Foreground Mix (BAE8H) register (FRGD_MIX). This overwrites the present bitmap color value with a new value.

The remainder of the setup is:

```
ES:[FRGD_MIX] ⇐ 0027H              ; color source is FRGD_COLOR, mix type is NEW
ES:FRGD_COLOR] ⇐ 00000002H         ; color index
ES:[PIXEL_CNTL] ⇐ A000H            ; FRGD_MIX provides color source and mix type
```

Drawing Operation:

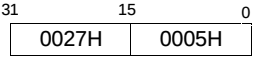
```
                    31          15          0
ES:[ALT_CURXY] ⇐   |    x1     |    y1     |   ; set starting coordinate

ES:[MAJ_AXIS_PCNT] ⇐ MAX - 1       ; length in pixels of the major axis - 1
                    31          15          0
ES:[ALT_STEP] ⇐    | 2*(MIN–MAX) |  2*MIN    |  ; diagonal and axial step constants

If the X drawing direction is positive then
     ES:[ERR_TERM] ⇐ 2 * MIN – MAX          ; error term
else if the X drawing direction is negative
     ES[ERR_TERM] ⇐ 2 * MIN – MAX – 1       ; error term
ES:[CMD] ⇐ 00100000DDD10001b       ; Draw line command (bits 15-13, 11), draw (as opposed to
                                   ; just move current position)(bit 4), bit 0 is always 1
```

15.4.3.2 Textured Line

The line draw command can be used to draw a one pixel wide textured line from screen coordinates x1,y1 to x2,y2. The texture is created by (1) setting bits 7-6 of the Pixel Control register (BEE8H, Index AH) to A080H to specify the CPU as the source of the mask bit selecting the mix register, (2) specifying a background and foreground color, (3) setting bit 8 of the Command register (9AE8H) to 1 (wait for CPU data) and (4) setting bit 1 of the Command register to 1 (multi-pixel). When the pattern bit sent by the CPU is a 1, the Foreground Mix register specifies the the color source and mix. When the bit is a 0, the Background Mix register specifies the color source and mix. This example uses the mix NEW for the foreground mix, XOR for the background mix, foreground color index 2 and background color index 4. The 32-bit line texture/pattern (PATTERN) is 00110000111100110011000011110011b. This requires that bits 10-9 of the Command register be set to 10b to specify a 32-bit bus.

Setup:

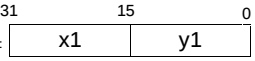
The XOR mix corresponds to a setting of 0101b in bits 3-0 of the Background Mix (B6E8H) register (BKGD_MIX). See the Solid Line example for an explanation of other parameters and registers used in this example.



; FRGD_COLOR is color source and NEW is mix,
; BKGD_COLOR is color source and XOR is mix

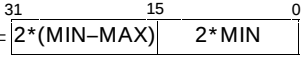
ES:[FRGD_COLOR] ⇐ 00000002H ; color index
ES:[BKGD_COLOR] ⇐ 00000004H ; color index
ES:[PIXEL_CNTL] ⇐ A080H ; mask data selecting mix register is provided by the CPU

Drawing Operation:



; set starting coordinates

ES:[MAJ_AXIS_PCNT ⇐ MAX - 1 ; length in pixels of the major axis - 1



; diagonal and axial step constants

If the X drawing direction is positive then
ES:[ERR_TERM] ⇐ 2 * MIN – MAX ; error term
else if the X drawing direction is negative
ES[ERR_TERM] ⇐ 2 * MIN – MAX – 1 ; error term
ES:[CMD] ⇐ 00100101DDD10011b ; Draw line (bits 15-13, 11), 32-bit bus (bits 10-9), wait for data
; from the CPU (bit 8), draw (bit 4), multi-pixel (bit 1)

COUNT (of PATTERN dwords) = (MAX + 31)/32 (See Note)
PIX_TRANS ⇐ 00110000111100110011000011110011b ; Output PATTERN to Pixel Data Transfer
; registers COUNT times

Note

The COUNT of the number of writes required by the CPU is a function of the number of bits to be transferred and the width of the transfer (8, 16 or 32 bits as specified by bits 10-9 of the Drawing Command register (9AE8H)). The number of bits transferred per line must be an even multiple of the transfer width. If this is not the case, the last write per line must be padded with one or more dummy

bits to meet this requirement. For example, if the transfer width is 8 bits and nine bits are to be transferred for the line, two bytes must be written per line, with the upper 7 bits of the second byte padded. In general, the number of padding bits per line will vary from 0 to (n-1), where n is the transfer width in bits.

With a transfer width of 8 bits, the number of byte writes required per line can be determined from the formula n = (MAX+7)/8, with n being truncated to an integer if the result contains a fraction. Thus a MAX = 11 transfer requires (11+7)/8 = 2 1/4 = 2 bytes. The formulas for all transfer widths are given below.

8-bit transfers: COUNT = (MAX+7)/8 bytes
16-bit transfers: COUNT = (MAX+15)/16 words
32-bit transfers: COUNT = (MAX+31)/32 dwords

15.4.3.3 Rectangle Fill Solid

This command draws a solid rectangle with its top left corner at x1,y1, height = HEIGHT and width = WIDTH. The Pixel Control register (BEE8H, Index AH) must be set to A000H to select the Foreground Mix register to specify the color source and mix type. This example uses the mix NEW and color index 2. The drawing direction (bits 7-5 in the write to the CMD register below) is set to X positive, X major and Y positive (101b).

Setup:

```
ES:[FRGD_MIX] ⇐ 0027H              ; color source is FRGD_COLOR, NEW mix type
ES:[FRGD_COLOR] ⇐ 00000002H        ; color index
ES:[PIXEL_CNTL] ⇐ A000H            ; FRGD_MIX specifies the color source and mix type
```

Drawing Operation:

```
                    31          15          0
ES:[ALT_CURXY] ⇐    | x1        | y1        |   ; set starting coordinates

                    31          15          0
ES:[ALT_PCNT] ⇐     | WIDTH-1   | HEIGHT-1  |   ; rectangle width

ES:[CMD] ⇐ 0100000010110001b       ; Draw rectangle (bits 15-13, 11), draw (bit 4)
```

Note

The rectangle can be defined by specifying any one of the four corners and setting bits 7-5 accordingly. Always select X as the major axis (bit 6 =0). No matter how the rectangle is defined, it always fills from left to right and top to bottom.

Corner	X direction (bit 5)	Y direction (bit 7)
top left	positive (1)	positive (1)
top right	negative (0)	positive (1)
bottom left	positive (1)	negative (0)
bottom right	negative (0)	negative (0)

15.4.3.4 Image Transfer—Through the Plane

This command transfers a rectangular image from the CPU to the display memory through the plane. "through the plane" means the complete color index is transferred for each pixel, e.g., in 8 bits/pixel mode, one byte is required to transfer one pixel to memory. The image is stored as an array of pixels arranged in row major fashion (consecutively increasing memory addresses). The Pixel Control register must be set to A000H to select the Foreground Mix register to specify the color source and mix type. The color source must be specified as the CPU. Bit 12 of the Command register must be set to 1 (swap ON) for Intel-type architectures. Bit 8 of the Command register must be set to 1 (wait for CPU data) and bits 6 and 5 must also be set to 1 to specify X as the major axis and a left-to-right drawing direction. This example uses a mix type of NEW and x1,y1 is the top left corner of the rectangle on the screen. The height and width of the rectangle (in pixels) are HEIGHT and WIDTH. Doublword CPU writes are supported by setting bits 10-9 of the Command register to 10b.

Setup:

```
ES:[FRGD_MIX] ⇐ 0047H          ; color source is the CPU, mix type is NEW
ES:[PIXEL_CNTL] ⇐ A000H        ; FRGD_MIX is the source for color source and mix type
```

Drawing Operation:

```
                    31          15          0
ES:[ALT_CURXY] ⇐   |    x1     |    y1     |   ; set destination starting coordinates

                    31          15          0
ES:[ALT_PCNT] ⇐    | WIDTH-1   | HEIGHT-1  |   ; rectangle width
```

```
Wait for Graphics Engine not busy   ; loop till bit 9 of 9AE8H register is 0
ES:[CMD] ⇐ 01010101D0110001b        ; Draw rectangle (bits 15-13, 11), swap ON (bit 12),
                                    ; 32-bit transfers (bits 10-9), wait for CPU data (bit 8),
                                    ; always X Major (bit 6) & X Positive (bit 5), draw (bit 4)
```

COUNT (of image pixel data to transfer) = (See Note)
PIX_TRANS ⇐ IMAGEDATA; Output image data to the Pixel Data Transfer registers for COUNT dwords.

Note

The COUNT of the number of writes required by the CPU is a function of the number of pixels to be transferred, the width of the transfer (8, 16 or 32 bits as specified by bits 10-9 of the Drawing Command register (9AE8H)) and the color depth (bits/pixel). The number of pixels transferred per line must be an even multiple of the transfer width. If this is not the case, the last write per line must be padded with one or more dummy pixels to meet this requirement. For example, at 4 bits/pixel, each byte holds two pixels. If the transfer width is one byte and three pixels are to be transferred per line, two bytes must be written per line, with the upper nibble of the second byte a dummy pixel. If the transfer width is 16 bits, from one to three dummy pixels may be required to make the number of pixels per line an even multiple of 16. The number of word writes required per line can be determined from the formula n = (W+3)/4, with n being truncated to an integer if the result contains a fraction. Thus a six pixel transfer requires (6+3)/4 = 2.25 = 2 words. This is then multiplied by the height of the image (in pixels) to determine the COUNT of words to be transferred. Similar procedures apply to every other combination of the variables affecting the COUNT. The formulas for all cases are given below, where W is the width of the image and H is the height of the image, both in pixels.

COUNT for 4 bits/pixel modes

8-bit transfers: COUNT = (W+1)/2 * H bytes
16-bit transfers: COUNT = (W+3)/4 * H words
32-bit transfers: COUNT = (W+7)/8 * H dwords

COUNT for 8 bits/pixel modes

8-bit transfers: COUNT = W * H bytes
16-bit transfers: COUNT = (W+1)/2 * H words
32-bit transfers: COUNT = (W+3)/4 * H dwords

COUNT for 16 bits/pixel modes

8-bit transfers: Do not use this combination
16-bit transfers: COUNT = W * H words
32-bit transfers: COUNT = (W+1)/2 * H dwords

COUNT for 32 bits/pixel modes

8-bit transfers: COUNT = Do not use this combination
16-bit transfers: COUNT = 2W * H words
32-bit transfers: COUNT = W * H dwords

Note that in 32 bits/pixel modes, the upper byte is a dummy byte providing padding for a 24-bit pixel.

15.4.3.5 Image Transfer—Across the Plane

The image transfer command can also be used to transfer a rectangular image from the CPU to the display memory across the plane. "across the plane" means that each bit sent by the CPU is stored in display memory as a single pixel. These pixels are arranged in row major fashion (consecutively increasing memory addresses). An "across the plane" transfer is created by (1) setting bits 7-6 of the Pixel Control register (BEE8H, Index AH) to A080H to specify the CPU as the source of the mask bit selecting the mix register, (2) specifying a background and foreground color, (3) setting bit 8 of the Command register (9AE8H) to 1 (wait for CPU data) and (4) setting bit 1 of the Command register to 1 (multi-pixel). When the pattern bit sent by the CPU is a 1, the Foreground Mix register specifies the the color source and mix. When the bit is a 0, the Background Mix register specifies the color source and mix. This example uses a mix type of NEW, and x1,y1 is the top left corner of the rectangle on the screen. The height and width of the rectangle (in pixels) are HEIGHT and WIDTH. The monochrome image is translated so that pixels corresponding to a 1 in the bit image are given color index 4 and pixels corresponding to a 0 in the bit image are given color index 0. This example uses word transfers from the CPU as specified by setting bits 10-9 of the Command register to 01b for a 16-bit bus width.

Setup:

```
                    31          15          0
ES:[ALT_MIX] ⇐      | 0027H     | 0005H     |   ; FRGD_COLOR color source and mix is NEW
                                                ; BKGD_COLOR is color source and mix is XOR
ES:[FRGD_COLOR] ⇐ 00000004H     ; foreground color index 4
ES:[BKGD_COLOR] ⇐ 00000000H     ; background color index 0
ES:[PIXEL_CNTL] ⇐ A080H         ; selection of mix register is based on data from the CPU
```

Drawing Operation:

```
                    31          15          0
ES:[ALT_CURXY] ⇐    | x1        | y1        |   ; set destination starting coordinates

                    31          15          0
ES:[ALT_PCNT] ⇐     | WIDTH-1   | HEIGHT-1  |   ; rectangle width

Wait for Graphics Engine not busy   ; loop till bit 9 of 9AE8H register is 0
CMD ⇐ 01010011D0110011b             ; Draw rectangle (bits 15-13, 11), swap ON (bit 12),
                                    ; 16-bit transfers (bits 10-9), wait for CPU data (bit 8),
                                    ; always X Major (bit 6) & X Positive (bit 5), draw (bit 4),
                                    ; multi-pixel (bit 1)
```

COUNT (of image pixel data to transfer) = ((WIDTH +15)/16)*HEIGHT words
PIX_TRANS ⇐ IMAGEDATA; Output image data to Pixel Transfer register for COUNT words

Notes

The COUNT of the number of writes required by the CPU is a function of the number of pixels to be transferred and the width of the transfer (8, 16 or 32 bits as specified by bits 10-9 of 9AE8H). Except for the case where bits 10-9 of 9AE8H are 11b, the number of pixels transferred per line must be an even multiple of the transfer width. If this is not the case, the last write per line must be padded with one or more dummy pixels to meet this requirement. For example, if the transfer width is 8 bits and nine pixels are to be transferred per line, two bytes must be written per line, with the upper 7 bits of the second byte padded. In general, the number of padding bits per line will vary from 0 to (n-1), where n is the transfer width in bits.

With a transfer width of 8 bits, the number of byte writes required per line can be determined from the formula n = (W+7)/8, with n being truncated to an integer if the result contains a fraction. Thus a 13-bit pixel transfer requires (13+7)/8 = 2.5 = 2 bytes. This is then multiplied by the height of the image (in pixels) to determine the COUNT of bytes to be transferred. Similar procedures apply to every other combination of the variables affecting the COUNT. The formulas for all cases are given below, where W is the width of the image and H is the height of the image, both in pixels.

8-bit transfers: COUNT = (W+7)/8 * H bytes (9AE8H_10-9 = 00b)
16-bit transfers: COUNT = (W+15)/16 * H words (9AE8H_10-9 = 01b)
32-bit transfers: COUNT = (W+31)/32 * H dwords (9AE8H_10-9 = 10b)
New 32-bit transfers: COUNT = (((W+7)/8*H)+3)/4 dwords (9AE8H_10-9 = 11b) (Trio32 only)

The differences between the two 32-bit transfer options are:

1. For 9AE8H_10-9 set to 10b, every line of the transfer must start with a fresh doubleword. In other words, all unneeded bits in a doubleword transfer for a given line are discarded. After a rectangular image is transferred, the current drawing position is a the bottom left, meaning the next rectangle, if drawn, will be below the previous rectangle.
2. For 9AE8H_10-9 set to 11b, only bits from the end of the line width to the next byte boundary are discarded. Data for the next line begins with the next byte. After a rectangular image is transferred, the current drawing position is a the top right, meaning the next rectangle, if drawn, will be to the right of the previous rectangle.

To write to a single plane, set the foreground mix to ‘logical one’ (0002H), the background mix to ‘logical zero’ (0001H), and the Write Mask register (AAE8H) to select the desired (single) plane for updates.

15.4.3.6 BitBLT—Through the Plane

This command copies a source rectangular area in display memory to another location in display memory. The Pixel Control register must be set to A000H to select the Foreground Mix register to specify the color source and mix type. The color source must be specified as the bitmap (display memory). Bit 6 of the Command register must be set to 1 to specify X as the major axis. For this example, assume x1,y1 is the top left corner of the source rectangle in display memory and x2,y2 is the top left corner of the destination rectangle. The rectangles can be overlapping or disjoint. The height and width (in pixels) of the rectangle being copied are HEIGHT and WIDTH.

Setup:

First, the values of the Srcx, Srcy, Destx and Desty must be determined.

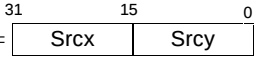
Case 1: Source and destination rectangles do not overlap

For X Positive, Y Positive: Srcx = x1, Srcy = y1, Destx = x2, Desty = y2

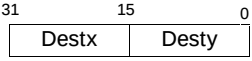
Case 2: Source and destination rectangles overlap

```
If x1 > x2
     then if X Positive, Srcx = x1, Destx = x2
else
     Srcx = x1 + WIDTH –1, Destx = x2 + WIDTH –1          ; X Negative

If y1 > y2
     then if Y Positive, Srcy = y1, Desty = y2
else
     Srcy = y1 + HEIGHT –1, Desty = y2 + HEIGHT –1        ; Y Negative

ES:[PIXEL_CNTL] ⇐ A000H          ; FRGD_MIX is the source of color source and mix type
ES:[FRGD_MIX] ⇐ 0067H            ; color source is display memory and mix type is NEW
```

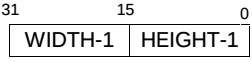
Draw Operation:

ES:[ALT_CURXY] ⇐ 

; set starting coordinates

ES:[ALT_STEP] ⇐ 

; set destination coordinates

ES:[ALT_PCNT] ⇐ 

; rectangle width and height

ES:[CMD] ⇐ 11000000D0D10001b ; BitBLT (bits 15-13, 11), always X Major (bit 6) , draw (bit 4)

15.4.3.7 BitBLT—Across the Plane

This uses the same command as a BitBLT through the plane. However, instead of copying complete pixels (with color affected only by the mix), this 'across the plane" transfer uses only the bits in the color planes specified by setting the Read Mask register (AEE8H), e.g., bit 3 of every pixel, to determine the destination rectangle. With more than one plane enabled for read, if all the bits in the planes enabled for read are '1's then a '1' is read. If a bit in any one of the planes enabled for read is a '0', then '0' is read. An "across the plane" transfer is created by (1) setting bits 7-6 of the Pixel Control register (BEE8H, Index AH) to A0C0H to specify the bitmap as the source of the mask bit selecting the mix register, (2) programming the Read and Write Mask registers to specify the plane to read from and write to and (3) setting bit 1 of the Command register to 1 (multi-pixel). In this example, when the bit read is a 1, a 1 is copied as specified by the foreground mix. When the bit read is a 0, a 0 is copied as specified by the background mix. Assume x1,y1 is the top left corner of the source rectangle on the display, and x2,y2 is the top left corner of the destination rectangle. The image is read from plane 0 and written to plane 2. The rectangles could be overlapping or disjoint. The height and width (in pixels) of the rectangle are HEIGHT and WIDTH.

Setup:

First, the values of the Srcx, Srcy, Destx and Desty must be determined.

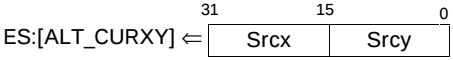
Case 1: Source and destination rectangles do not overlap

For X Positive, Y Positive: Srcx = x1, Srcy = y1, Destx = x2, Desty = y2

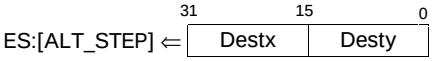
Case 2: Source and destination rectangles overlap

```
If x1 > x2
     then if X Positive, Srcx = x1, Destx = x2
else
     Srcx = x1 + WIDTH –1, Destx = x2 + WIDTH –1          ; X Negative

If y1 > y2
     then if Y Positive, Srcy = y1, Desty = y2
else
     Srcy = y1 + HEIGHT –1, Desty = y2 + HEIGHT –1        ; Y Negative

ES:[PIXEL_CNTL] ⇐ A0C0H              ; data from display memory selects mix register
                  31        15     0
ES:[ALT_MIX] ⇐  | 0002H | 0001H |    ; result of foreground mix is always logical 1,
                                     ; result of background mix is always logical 0
ES:[RD_MASK] ⇐ 00000001H             ; read from plane 0
ES:[WRT_MASK] ⇐ 00000004H            ; plane 2 enabled for write
```

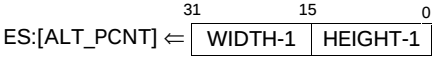
Draw Operation:



; set starting coordinates



; set destination coordinates



; rectangle width and height

```
ES:[CMD] ⇐ 11000000D0D10001b    ; BitBLT (bits 15-13, 11), always X Major (bit 6) , draw (bit 4),
                                ; multi-pixel (bit 1)
```

Note

It is possible to translate a monochrome image, e.g., text fonts, stored in a single plane in display memory into a 2-color image. This is accomplished by setting the mix registers differently and setting the desired background and foreground colors. If the source bit is a '1', then the corresponding pixel at the destination is colored with the foreground color index. The destination pixel is colored with the background color index if the corresponding source bit is a '0'. The setup for this is as follows:

```
ES:[WRT_MASK] ⇐ FFFFFFFFH       ; enable all planes for writing
ES:[FRGD_MIX] ⇐ 0027H           ; color source foreground, mix type NEW
ES:[BKGD_MIX] ⇐ 0007H           ; color source background, mix type NEW
ES:[FRGD_COLOR] ⇐ 00000004H     ; foreground color
ES:[BKGD_COLOR] ⇐ 00000001H     ; background color
```

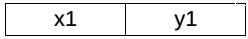
15.4.3.8 PatBLT—Pattern Fill Through the Plane

An 8x8 pixel pattern is initially copied into an off-screen area of display memory using an image transfer operation or a direct write (linear addressing). This command then repeatedly tiles this source pattern into a destination rectangle of arbitrary size. The colors of the destination pixels are affected only by the mix selected. The destination rectangle must not overlap the source pattern. Each copy is aligned to an 8-pixel boundary (x coordinate = 0, 8, etc.), with pixels outside the destination rectangle boundary not being drawn. The Pixel Control register must be set to A000H to select the Foreground Mix register to specify the color source and mix type. The color source must be specified as the bitmap (display memory). Bit 6 of the Command register must be set to 1 to specify X as the major axis. In this example, assume x1,y1 is the top left corner of the pixel pattern and x2,y2 is the top left corner of the destination rectangle. The height and width (in pixels) of the rectangle are HEIGHT and WIDTH.

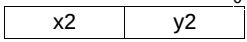
Setup:

```
ES:[PIXEL_CNTL] ⇐ A000H          ; FRGD_MIX is the source of color source and mix type
ES:[FRGD_MIX] ⇐ 0067H            ; color source is display memory, mix type is NEW
```

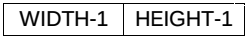
Draw Operation

ES:[ALT_CURXY] ⇐ 

; set starting coordinates

ES:[ALT_STEP] ⇐ 

; set destination coordinates

ES:[ALT_PCNT] ⇐ 

; rectangle width and height

```
ES:[CMD] ⇐ 11100000D0D10001b     ; PatBLT (bits 15-13,11), always X Major (bit 6) , draw (bit 4)
```

15.4.3.9 PatBLT—Pattern Fill Across the Plane

This uses the same command as a PatBLT through the plane. However, instead of copying complete pixels (with color affected only by the mix), this 'across the plane" transfer uses only the bits in the color planes specified by setting the Read Mask register (AEE8H), e.g., bit 3 of every pixel, to determine the destination rectangle. With more than one plane enabled for read, if all the bits in the planes enabled for read are '1's then a '1' is read. If a bit in any one of the planes enabled for read is a '0', then '0' is read. An "across the plane" transfer is created by (1) setting bits 7-6 of the Pixel Control register (BEE8H, Index AH) to A0C0H to specify the bitmap as the source of the mask bit selecting the mix register, (2) programming the Read and Write Mask registers to specify the plane to read from and write to and (3) setting bit 1 of the Command register to 1 (multi-pixel). In this example, when the bit read is a 1, a 1 is copied as specified by the foreground mix. When the bit read is a 0, a 0 is copied as specified by the background mix. In this example, assume x1,y1 is the top left corner of the pixel pattern and x2,y2 is the top left corner of the destination rectangle. The image is read from plane 0 and written to plane 2. The height and width of the destination rectangle are HEIGHT and WIDTH.

Setup:

```
ES:[PIXEL_CNTL] ⇐ A0C0H          ; data from display memory selects mix register
```

```
                  31        15        0
ES:[ALT_MIX] ⇐   | 0002H   | 0001H   |   ; result of foreground mix is always logical 1,
                                           ; result of background mix is always logical 0
```

```
ES:[RD_MASK] ⇐ 00000001H         ; read from plane 0
ES:[WRT_MASK] ⇐ 00000004H        ; plane 2 enabled for write
```

Draw Operation:

```
                  31        15        0
ES:[ALT_CURXY] ⇐ | x1      | y1      |   ; set starting coordinates
```

```
                  31        15        0
ES:[ALT_STEP] ⇐  | x2      | y2      |   ; set destination coordinates
```

```
                  31        15        0
ES:[ALT_PCNT] ⇐  | WIDTH-1 | HEIGHT-1 |  ; rectangle width and height
```

```
ES:[CMD] ⇐ 11100000D0D10011b     ; PatBLT (bits 15-13, 11), always X Major (bit 6) , draw (bit 4),
                                 ; multi-pixel (bit 1)
```

Note

To expand the source mono pattern into a 2-color pattern, set the foreground mix to 27H, the background mix to 7H and the foreground and background colors as desired. Also set the write mask (AAE8H) to FFFFFFFFH. This needs to be set only once. It is altered only by another write.

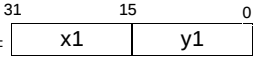
15.4.3.10 Short Stroke Vectors

This command rapidly draws short lines (up to 15 pixels in length). Such lines are constrained to one of the 8 directions at 45 degree increments starting at 0 degrees. The current point x1,y1 is set and a NOP command is issued to set all the desired drawing parameters without actually writing a pixel. For example, bit 2 (Last Pixel Off) would be set to 1 (OFF) for drawing connected lines until the last line is drawn. The short stroke vector parameters are then loaded in the Short Stroke Vector Transfer (9EE8H) register (SHORT_STROKE). Two vectors can be defined at a time, one in the low byte and one in the high byte. For the low byte, bits [7:5] define the direction, with bit 4 set to '1' for a draw operation or to '0' for a move current position operation. Bits 3-0 define the length of the short line. Let SSVD0, SSVD1, ...SSVDN–1 bytes be the short stroke vector data for N lines.

Setup:

```
ES:[PIXEL_CNTL] ⇐ A000H              ; FRGD_MIX is the source of color source and mix type
ES:[FRGD_MIX] ⇐ 0027H                ; use the foreground color, mix type NEW
ES:[FRGD_COLOR]⇐ 00000004H           ; foreground color index 4
```

Draw Operation:




```
ES:[CMD] ⇐ 00010010XXX11111b         ; NOP (bits 15-13, 11), byte swap (bit 12), 16-bit transfers
                                     ; (bits 10-9) , draw (bit 4), radial drawing direction (bit 3),
                                     ; last pixel off (bit 2), multi-pixel (bit 1)

While space available in the FIFO
ES:[SHORT_STROKE] ⇐ SSVD1 SHL 8 + SSVD0 ; SSVD1 shifted to high byte, SSVD0 in low byte
ES:[SHORT_STROKE] ⇐ SSVD3 SHL 8 + SSVD2 ; byte swap turned on to read vectors out in
                                        ; correct order
            .
            .
            .
ES:[SHORT_STROKE] ⇐ SSVDN-1 SHL 8 + SSVDN-2
```

15.4.3.11 Programmable Hardware Cursor

A programmable cursor is supported which is compatible with the Microsoft Windows (bit 4 of CR55 = 0) and X11 (bit 4 of CR55 = 1) cursor definitions. The cursor size is 64 pixels wide by 64 pixels high, with the cursor pattern stored in an off-screen area of display memory. Two monochrome images 64 bits wide by 64 bits high (512 bytes per image) define the cursor shape. The first bit image is an AND mask and the second bit image is an XOR mask. The following is the truth table for the cursor display logic.

AND Bit	XOR Bit	Displayed (Microsoft Windows)	Displayed (X11)
0	0	Cursor Background Color	Current Screen Pixel
0	1	Cursor Foreground Color	Current Screen Pixel
1	0	Current Screen Pixel	Cursor Background Color
1	1	NOT Current Screen Pixel	Cursor Foreground Color

The hardware cursor color is taken from the Hardware Graphics Cursor Foreground Stack (CR4A) and the Hardware Graphics Cursor Background Stack (CR4B) registers. Each of these is a stack of three 8-bit registers. The stack pointers are reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). The color value is then programmed by consecutive writes (low byte, second byte, third byte) to the appropriate (foreground or background) register.

Enabling/Disabling the Cursor

The hardware cursor is disabled when a VGA-compatible mode is in use. It can be enabled or disabled when in Enhanced mode (bit 0 of 4AE8H = 1), as follows.

```
CR39 ⇐ A0H          ; Unlock System Control registers
CR45_0 ⇐ 1          ; Enable hardware cursor
CR45_0 ⇐ 0          ; Disable hardware cursor
CR39 ⇐ 00H          ; Lock System Control registers
```

Positioning the Cursor

The cursor can be positioned at any point on the display, with the X,Y coordinates ranging from 0 to 2047. This enables the full cursor images to be displayed on the screen and partial cursor images to be displayed at the right edge and the bottom edge of the screen. The cursor offset OX,OY has to be set to 0,0 for a 1024x768 resolution. If X is > (1024 – 64) or Y is > (768 – 64), then a partial cursor is visible at the right edge or top edge of the screen respectively. Note that if Y ≥ 768 then the cursor is not visible; it is residing in the off-screen area.

A partial cursor image can be displayed at the left edge or the top edge of the screen. To enable partial cursor display at the top edge of the screen, Y is set to 0 and the Y offset register is set to OY (range from 0 to 63). This displays the bottom 64–OY rows of the cursor image at the currently set X position and the top edge of the screen. Similarly, a partial cursor can be displayed at the left edge of the screen by setting X to 0 and the X offset register to OX (range from 0 to 63). This displays the right 64–OX columns of the cursor image at the currently set X and the left edge of the screen. The following pseudocode illustrates cursor positioning.

```
CR39 ⇐ A0H                          ; Unlock System Control registers
CR46_10-8 ⇐ MS 3 bits of X cursor position
CR47_7-0 ⇐ LS 8 bits of X cursor position
```

CR49_7-0 ⇐ LS 8 bits of Y cursor position
CR4E_5-0 ⇐ Cursor Offset X position
CR4F_5-0 ⇐ Cursor Offset Y position
CR48_10-8 ⇐ MS 3 bits of Y cursor position
CR39 ⇐ 00H ; Lock System Control registers

The cursor position is updated by the hardware once each frame. Therefore, the programmer should ensure that the position is re-programmed no more than once for each vertical sync period.

Programming the Cursor Shape

The AND and the XOR cursor image bitmaps are 512 bytes each. These bitmaps are word interleaved in a contiguous area of display memory, i.e., AND word 0, XOR word 0, AND word 1, XOR word 1 ... AND word 255, XOR word 255. The starting location must be on a 1024-byte boundary. This location is programmed into the Hardware Graphics Cursor Start Address registers (CR4C and CR4D) as follows:

CR39 ⇐ A0H ; Unlock System Control registers
CR4C_11-8 ⇐ MS 4 bits of the cursor storage start 1024-byte segment.
CR4D ⇐ LS 8 bits of the cursor storage start 1024-byte segment
CR39 ⇐ 0 ; Lock System Control registers

The value programmed is the 1024-byte segment of display memory at which the beginning of the hardware cursor bit pattern is located. For example, for an 800x600x8 mode on a 1 MByte system, there are 1024 1K segments. Programming CR4C_11-8 with 3H and CR4D with FEH specifies the starting location as the 1022nd (0-based) 1K segment. The cursor pattern is programmed (using linear addressing) at FF800H offset from the base address of the frame buffer.

Note

If the cursor is not 64 bits by 64 bits, the given images should be padded to make the cursor image 64 bits by 64 bits. The padded area should be made transparent by padding the extra AND mask bits with ‘1’s and the extra XOR bits by ‘0’s.

15.5 RECOMMENDED READING

Graphics Programming for the 8514/A by Jake Richter and Bud Smith (M&T Publishing, Inc) provides extensive explanations and examples for programming most of the bits in the S3 Enhanced Registers. This book may be out of print.

Programmer’s Guide to the EGA, VGA and Super VGA Cards, 3rd Edition by Richard F. Ferraro (Addison-Wesley Publishing Company, Inc) includes a section on programming for S3 accelerator chips.

Section 16: VGA Standard Register Descriptions

In the following register descriptions, 'U' stands for undefined or unused and 'R' stands for reserved (write = 0, read = U). A question mark in an address stands for a hexadecimal value of either 'B' or 'D'. If bit 0 of the Miscellaneous Output Register (3C2H, Write) is set to 1, the address is based at 3DxH for color emulation. If this bit is reset to 0, the address is based at 3BxH for monochrome emulation.

See Appendix A for a table listing each register in this section and its page number.

16.1 GENERAL REGISTERS

This section describes general input status and output control registers.

Miscellaneous Output Register (MISC)

Write Only Address: 3C2H
Read Only Address: 3CCH
Power-On Default: 00H

This register controls miscellaneous output signals. A hardware reset sets all bits to zero.

7	6	5	4	3	2	1	0
VSP	HSP	PGSL	= 0	CLK SEL 1	CLK SEL 0	ENB RAM	IOA SEL

Bit 0 IOA SEL - I/O Address Select
0 = Monochrome emulation. Address based at 3Bx
1 = Color emulation. Address based at 3Dx

Bit 1 ENB RAM - Enable CPU Display Memory Access
0 = Disable access of the display memory from the CPU
1 = Enable access of the display memory from the CPU

Bits 3–2 Clock Select - Select the Video Clock Frequency
00 = Selects 25.175 MHz DCLK for 640 horizontal pixels
01 = Selects 28.322 MHz DCLK for 720 horizontal pixels
10 = Reserved
11 = Enables loading of DCLK PLL parameters in SR12 and SR13.

A setting of either 00b or 01b causes the appropriate values to be programmed into the DCLK PLL registers if bit 1 of SR15 is set to 1.

Bit 4 Reserved = 0

Bit 5 PGSL -Select High 64K Page
0 = Select the low 64K page of memory
1 = Select the high 64K page of memory

Bit 6 $\overline{\text{HSP}}$ - Select Negative Horizontal Sync Pulse
0 = Select a positive horizontal retrace sync pulse
1 = Select a negative horizontal retrace sync pulse

Bit 7 $\overline{\text{VSP}}$ - Select Negative Vertical Sync Pulse
0 = Select a positive vertical retrace sync pulse
1 = Select a negative vertical retrace sync pulse

Feature Control Register (FCR_WT, FCR_AD)

Write Only Address: 3?AH
Read Only Address: 3CAH
Power-On Default: 00H

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	VSSL	= 0	= 0	= 0

Bits 2–0 Reserved = 0

Bit 3 VSSL - Vertical Sync Type Select
0 = Enable normal vertical sync output to the monitor
1 = The 'vertical sync' output is the logical OR of 'vertical sync' and 'vertical active display enable' (an internal signal)

Bits 7–4 Reserved = 0

Input Status 0 Register (STATUS_0)

Read Only Address: 3C2H
Power-On Default: Undefined

This register indicates the status of the VGA adapter.

7	6	5	4	3	2	1	0
CRT INTPE	= 0	= 0	MON SENS	= 0	= 0	= 0	= 0

Bits 3–0 Reserved = 0

Bit 4 MON SENS - Monitor Sense Status
0 = The internal $\overline{\text{SENSE}}$ signal is a logical 0
1 = The internal $\overline{\text{SENSE}}$ signal is a logical 1

Bits 6–5 Reserved = 0

Bit 7 CRT INTPE - CRT Interrupt Status
0 = Vertical retrace interrupt cleared
1 = Vertical retrace interrupt pending

See Section 12.7 for an explanation of interrupt generation.

Input Status 1 Register (STATUS_1)

Read Only Address: 3?AH
Power-On Default: Undefined

This register indicates video sync timing and video wraparound.

7	6	5	4	3	2	1	0
= 0	= 0	TST-VDT 1	0	VSY	= 1	R	DTM

Bit 0 $\overline{\text{DTM}}$ - Display Mode Inactive
0 = The display is in the display mode.
1 = The display is not in the display mode. Either the horizontal or vertical retrace period is active

Bit 1 Reserved = 0

Bit 2 Reserved = 1

Bit 3 VSY - Vertical Sync Active
0 = Display is in the display mode
1 = Display is in the vertical retrace mode

Bits 5–4 TST-VDT - Video Signal Test
Video Data Feedback 1,0. These bits are feedback video signals to do read back tests. These bits are selectively connected to two of the eight color outputs of the attribute controller. Bits 5 and 4 of the color plane enable register (AR12) control the multiplexer for this video output observation.

Bits 7–6 Reserved = 0

Video Subsystem Enable Register

Write Only Address: 3C3H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	VGA ENB

Bit 0 VGA ENB - VGA Enable
0 = VGA display disabled
1 = VGA display enabled

Bits 7–1 Reserved

16.2 SEQUENCER REGISTERS

The sequencer registers are located at two-byte address spaces. These registers are accessed by first writing the data to the index register of the sequencer at I/O address 3C4H and then writing to or reading from the data register at 3C5H. A word write of both address and data at 3C4H can also be performed.

Sequencer Index Register (SEQX)

Read/Write Address: 3C4H
Power-On Default: Undefined

This register is loaded with a binary value that indexes the sequencer register for read/write data. This value is referred to as the "Index Number" of the SR register in this document.

7	6	5	4	3	2	1	0
R	R	R	SEQ ADDRESS				

Bits 4–0 SEQ ADDRESS - Sequencer Register Index
A binary value indexing the register where data is to be accessed.

Bits 7–5 Reserved

Sequencer Data Register (SEQ_DATA)

Read/Write Address: 3C5H
Power-On Default: Undefined

This register is the data port for the sequencer register indexed by the Sequencer Index register (3C4H).

7	6	5	4	3	2	1	0
SEQ DATA							

Bits 7–0 SEQ DATA - Sequencer Register Data
Data to the sequencer register indexed by the sequencer address index.

Reset Register (RST_SYNC) (SR0)

Read/Write Address: 3C5H, Index 00H
Power-On Default: 00H

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	SYN RST	ASY RST

Bit 0 $\overline{\text{ASY}}$ RST - Asynchronous Reset

This bit is for VGA software compatibility only. It has no function for the Trio64V+.

Bit 1 $\overline{\text{SYN}}$ RST - Synchronous Reset

This bit is for VGA software compatibility only. It has no function for the Trio64V+.

Bits 7–2 Reserved = 0

Clocking Mode Register (CLK_MODE) (SR1)

Read/Write Address: 3C5H, Index 01H
Power-On Default: 00H

This register controls the operation mode of dot clock and character clock.

7	6	5	4	3	2	1	0
= 0	= 0	SCRN OFF	SHF 4	DCK 1/2	SHF LD	= 0	8DC

Bit 0 8DC - 8 Dot Clock Select
0 = Character clocks 9 dots wide are generated
1 = Character clocks 8 dots wide are generated

Bit 1 Reserved = 0

Bit 2 SHF LD - Load Serializers Every Second Character Clock
0 = Load the video serializer every character clock
1 = Load the video serializers every other character clock

Bit 3 DCK 1/2 - Internal Dot Clock = 1/2 DCLK
0 = Set the internal dot clock to the same frequency as DCLK
1 = Set the internal dot clock to 1/2 the frequency of DCLK

This bit is used for horizotal pixel doubling.

Bit 4 SHF 4 - Load Serializers Every Fourth Character Clock
0 = Load the serializers every character clock cycle
1 = Load the serializers every fourth character clock cycle

Bit 5 SCRN OFF - Screen Off
0 = Screen is turned on.
1 = Screen is turned off

Bits 7–6 Reserved = 0

Enable Write Plane Register (EN_WT_PL) (SR2)

Read/Write Address: 3C5H, Index 02H
Power-On Default: 00H

This register selects write protection or write permission for CPU write access into video memory.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	EN.WT.PL.			

Bits 3–0 EN.WT.PL - Enable Write to a Plane
0 = Disables writing into the corresponding plane
1 = Enables the CPU to write to the corresponding color plane

Bits 7–4 Reserved = 0

Character Font Select Register (CH_FONT_SL) (SR3)

Read/Write Address: 3C5H, Index 03H
Power-On Default: 00H

7	6	5	4	3	2	1	0
= 0	= 0	SLA 2	SLB 2	SLA 1	SLA 0	SLB 1	SLB 0

In text modes, bit 3 of the attribute byte normally turns the foreground intensity on or off. This bit can be redefined to be a switch between two character sets. The switch is enabled when there is a difference between the value of character font select A and character font select B bits. Memory Mode (SR4) register bit 1 = 1 (extended memory) enables all bits of this function; otherwise character fonts 0 and 4 are available. 256 KBytes of video memory support 8 character sets. This register is reset to 0 asynchronously during a system reset.

Bits 4, 1–0 SLB - Select Font B
This value selects the portion of plane 2 used to generate text character fonts when bit 3 of the attribute byte is a logical 1, according to the following table:

Bits 4,1,0	Font Table Location	Bits 4, 1,0	Font Table Location
000	First 8K of plane 2	100	Second 8K of plane 2
001	Third 8K of plane 2	101	Fourth 8K of plane 2
010	Fifth 8K of plane 2	110	Sixth 8K of plane 2
011	Seventh 8K of plane 2	111	Eighth 8K of plane 2

Bits 5, 3–2 SLA - Select Font A
This value selects the portion of plane 2 used to generate text character fonts when bit 3 of attribute byte is a logical 0, according to the same table as the character font select A.

Bits 7–6 Reserved = 0

Memory Mode Control Register (MEM_MODE) (SR4)

Read/Write Address: 3C5H, Index 04H
Power-On Default: 00H

This register controls CPU memory addressing mode.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	CHN 4M	SEQ MODE	EXT MEM	= 0

Bit 0 Reserved = 0

Bit 1 EXT MEM - Extended Memory Access
0 = Memory access restricted to 16/32 KBytes
1 = Allows complete memory access to 256 KBytes. Required for VGA

Bit 2 SEQ MODE - Sequential Addressing Mode
This bit affects only CPU write data accesses into video memory. Bit 3 of this register must be 0 for this bit to be effective.
0 = Enables the odd/even addressing mode. Even addresses access planes 0 and 2. Odd addresses access planes 1 and 3
1 = Directs the system to use a sequential addressing mode

Bit 3 CHN 4M - Select Chain 4 Mode
0 = Enables odd/even mode.
1 = Chain 4 Mode. This bit selects modulo 4 addressing for CPU access to display memory. A logical 1 directs the two lower order bits of the CPU address used to select the plane in video memory to be accessed as follows:

A1	A0	Plane Selected
0	0	0
0	1	1
1	0	2
1	1	3

Bits 7–4 Reserved = 0

Unlock Extended Sequencer Register (SR8)

Read/Write Address: 3C5H, Index 08H
Power-On Default: 00H

Loading xxxx0110b (e.g., 06H) unlocks accessing of all the S3 extensions (SR9 - SR1C) to the standard VGA Sequencer register set. (x = don't care).

7	6	5	4	3	2	1	0
R	R	R	R	=0	=1	=1	=0

Extended Sequencer 9 Register (SR9)

Read/Write Address: 3C5H, Index 09H
Power-On Default: 00H

7	6	5	4	3	2	1	0
MMIO-ONLY	R	R	R	R	R	R	R

Bits 6-0 Reserved

Bit 7 MMIO-ONLY - Memory-mapped I/O register access only
0 = When MMIO is enabled, both programmed I/O and memory-mapped I/O register accesses are allowed
1 = When MMIO is enabled, only memory-mapped I/O register accesses are allowed to extended (non-standard VGA) registers. Both I/O and MMIO accesses can be made to standard VGA registers.

Extended Sequencer A Register (SRA)

Read/Write Address: 3C5H, Index 0AH
Power-On Default: 00H

7	6	5	4	3	2	1	0
2 MCLK	P50 SEL	PD-NTRI	R	R	R	R	R

Bits 4-0 Reserved

Bit 5 PD-NTRI - PD[63:0] Not Tri-stated
0 = PD[63:0] tri-stated
1 = PD[63:0] not tri-stated

The default value of 0 reduces power consumption. The pins are enabled for output only as needed. Note that output pads for PD[63:29] also latch the most recent output state.

Bit 6 P50 SEL - Pin 50 Function Select
0 = If bit 2 of CR36 is set to 1 to indicate fast page memory, pin 50 outputs a signal equivalent to $\overline{OE0}$ (fast page) or $\overline{OE1}$ (EDO). This setting should always be used with 1- or 2-MByte memory configurations. With this setting and EDO memory, the $\overline{OE1}$ output is held high whenever Trio64-compatible VAFC feature connector operation is enabled (SRD_1 = 0). This disables output to the multiplexed PD lines.
1 = Pin 50 outputs $\overline{RAS1}$ for either fast page or EDO memory. This setting should always (and only) be used for 4-MByte configurations. Trio64-compatible VAFC feature connector operation cannot be used with this setting and should never be enabled.

Bit 7 2MCLK - 2 MCLK CPU writes to memory
0 = 3 MCLK memory writes
1 = 2 MCLK memory writes

Setting this bit to 1 improves performance for systems using an MCLK less than 57 MHz. For MCLK frequencies between 55 and 57 MHz, bit 7 of SR15 should also be set to 1 if linear addressing is being used.

Extended Sequencer B Register (SRB)

Read/Write Address: 3C5H, Index 0BH
Power-On Default: 00H

7	6	5	4	3	2	1	0
ALT COLOR MODE				24 BPP	R	VAFC VCLKI	DOT= VCLKI

Bit 0 DOT = VCLKI - Dot clock = VCLKI
0 = Use internal dot clock
1 = Use VCLKI input for all internal dot clock functions

This bit is used for S3 test purposes only.

Bit 1 VAFC VCLKI - Use VCLKI input with VAFC
0 = Pixel data from pass-through feature connector latched by incoming VCLK
1 = Pixel data from VAFC latched by VCLKI input

Bit 2 Reserved

Bit 3 24 BPP - 24 Bits/Pixel (packed Mode 12)
0 = 24 bits/pixel operation disabled
1 = 24 bits/pixel operation enabled if both SRB_7-4 = 0111b and CR67_7-4 = 0000b

Bits 7-4 ALT COLOR MODE - Color Mode for feature connector input
0000 = Mode 0: 8-bit color, 1 pixel/VCLK
0001 = Mode 8: 8-bit color, 2 pixels/VCLK
0011 = Mode 9: 15-bit color, 1 pixel/VCLK
0101 = Mode 10: 16-bit color, 1 pixel/VCLK
0111 = Mode 12: Packed 24-bit color, 1 pixel/3 VCLKs
1101 = Mode 13: 24-bit color, 1 pixel/VCLK

All other mode values are reserved. Setting mode 0001 (clock doubled mode) also requires that either bit 4 or bit 6 of SR15 be set to 1 and that bit 7 of SR18 be set to 1. Clock doubling cannot be used with the Streams Processor active.

Extended Sequencer D Register (SRD)

Read/Write Address: 3C5H, Index 0DH
Power-On Default: 00H

This register provides feature connector control and also provides independent control of the HSYNC and VSYNC signals, therefore supporting the VESA DPMS (Display Power Management Control) standard.

7	6	5	4	3	2	1	0
VSY-CTL 1	0	HSY-CTL 1	0	R	R	LPB FEAT	EN-FEAT

Bit 0 EN-FEAT - Enable Feature Connector
0 = $\overline{\text{ENFEAT}}$ (pin 151) is high. VCLK, HSYNC and VSYNC are outputs.
1 = $\overline{\text{ENFEAT}}$ (pin 151) is low. The direction of VCLK is controlled by EVCLK and the direction of $\overline{\text{BLANK}}$, HSYNC and VSYNC is controlled by ESYNC. In both cases, assertion (low) specifies an input and a logic high specifies an output.

This bit is set to 1 to drive pin 151 with a logic 0. This enables the feature connector buffers required when the Trio64-compatible VAFC feature connector is enabled for memory configuration of 2 MBytes or larger.

Bit 1 LPB FEAT - Select LPB Feature Connector
0 = Trio64-type VAFC feature connector (using multiplexed PD pins)
1 = LPB VAFC feature connector

The LPB must be disabled and feature connector operation enabled for this bit to have an effect.

Bits 3–2 Reserved

Bits 5–4 HSY-CTL - HSYNC Control
00 = Normal operation
01 = HSYNC = 0
10 = HSYNC = 1
11 = Reserved

Bits 7–6 VSY-CTL - VSYNC Control
00 = Normal operation
01 = VSYNC = 0
10 = VSYNC = 1
11 = Reserved

MCLK Value Low Register (SR10)

Read/Write Address: 3C5H, Index 10H
Power-On Default: See description below.

The power-on default value for this register in conjunction with the power-on default value for SR11 generate an MCLK value of 45 MHz. All other MCLK values must be specified by programming of SR10 and SR11. Loading of a new value is enabled by either bit 0 or bit 5 of SR15.

7	6	5	4	3	2	1	0
R	PLL R VALUE		PLL N-DIVIDER VALUE				

Bits 4-0 PLL N-DIVIDER VALUE
These bits contain the binary equivalent of the integer (1-31) divider used to scale the input to the MCLK PLL. See Section 9 for a detailed explanation.

Bits 6-5 PLL R VALUE
These bits contain the binary equivalent of the integer (1, 2, 4, 8) range value used to scale the output of the MCLK PLL. See Section 9 for a detailed explanation.

Bit 7 Reserved

MCLK Value High Register (SR11)

Read/Write Address: 3C5H, Index 11H
Power-On Default: See description below.

The power-on default value for this register in conjunction with the power-on default value for SR10 generate an MCLK value of 45 MHz. All other MCLK values must be specified by programming of SR10 and SR11. Loading of a new value is enabled by either bit 0 or bit 5 of SR15.

7	6	5	4	3	2	1	0
R	PLL M-DIVIDER VALUE						

Bits 6-0 PLL M-DIVIDER VALUE
These bits contain the binary equivalent of the integer (1-127) divider used in the feedback loop of the MCLK PLL. See Section 9 for a detailed explanation.

Bit 7 Reserved

DCLK Value Low Register (SR12)

Read/Write Address: 3C5H, Index 12H
Power-On Default: See description below.

The power-on default value for this register in conjunction with the power-on default value for SR13 generate a DCLK value of 25.175 MHz. The default value is automatically placed in this register when bits 3-2 of 3C2H are programmed to 00b. If bits 3-2 of CR2H are programmed to 01b, the appropriate PLL R and PLL N values for a 28.322 MHz DCLK will automatically be placed in this register. All other DCLK values must be specified by programming of SR12 and SR13. Loading of a new value is enabled by either bit 1 or bit 5 of SR15 and by setting bits 3-2 of 3C2H to 11b.

7	6	5	4	3	2	1	0
CLKx2	PLL R VALUE		PLL N-DIVIDER VALUE				

Bits 4-0 N-DIVIDER VALUE
These bits contain the binary equivalent of the integer (1-31) divider used to scale the input to the DCLK PLL. See Section 9 for a detailed explanation.

Bits 6-5 PLL R VALUE
These bits contain the binary equivalent of the integer (1, 2, 4, 8) range value used to scale the output of the DCLK PLL. See Section 9 for a detailed explanation.

Bit 7 CLKx2 - Enable clock doubled mode
0 = RAMDAC clock doubled mode (0001) disabled
1 = RAMDAC clock doubled mode (0001) enabled

This bit must be set to 1 when mode 0001 is specified in bits 7-4 of CR67 or SRC. Either bit 4 or bit 6 of SR15 must also be set to 1. This bit has the same function as SR18_7. It allows enabling of clock doubling at the same time as the PLL parameters are programmed , resulting in more controlled VCO operation.

DCLK Value High Register (SR13)

Read/Write Address: 3C5H, Index 13H
Power-On Default: See description below.

The power-on default value for this register in conjunction with the power-on default value for SR12 generate a DCLK value of 25.175 MHz. The default value is automatically placed in this register when bits 3-2 of 3C2H are programmed to 00b. If bits 3-2 of CR2H are programmed to 01b, the appropriate PLL M value for a 28.322 MHz DCLK will automatically be placed in this register. All other DCLK values must be specified by programming of SR12 and SR13. Loading of a new value is enabled by either bit 1 or bit 5 of SR15 and by setting bits 3-2 of 3C2H to 11b.

7	6	5	4	3	2	1	0
R	PLL M-DIVIDER VALUE						

Bits 6-0 PLL M- DIVIDER VALUE
These bits contain the binary equivalent of the integer (1-127) divider used in the feedback loop of the DCLK PLL. See Section 9 for a detailed explanation.

Bit 7 Reserved

CLKSYN Control 1 Register (SR14)

Read/Write Address: 3C5H, Index 14H
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT DCLK	EXT MCLK	P151 SEL	CLR CNT	M TEST	EN CNT	MPLL PD	DPLL PD

Bit 0 DPLL PD - Power down DCLK PLL
0 = DCLK PLL powered
1 = DCLK PLL powered down

This bit is used for S3 test purposes only.

Bit 1 MPLL PD - Power down MCLK PLL
0 = MCLK PLL powered
1 = MCLK PLL powered down

This bit is used for S3 test purposes only.

Bit 2 EN CNT - Enable clock synthesizer counters
0 = Clock synthesizer counters disabled
1 = Clock synthesizer counters enabled

This bit is used for S3 test purposes only.

Bit 3 M TEST - MCLK Test
0 = Test DCLK
1 = Test MCLK

This bit is used for S3 test purposes only.

Bit 4 CLR CNT - Clear clock synthesizer counters
0 = No effect
1 = Clear the clock synthesizer counters

This bit is used for S3 test purposes only.

Bit 5 P151 SEL - Pin 151 function select
0 = Pin 151 functions normally
1 = Pin 151 is tri-stated

Setting this bit to 1 allows pin 151 to act as an MCLK input. This is enabled by setting bit 6 of this register to 1.

Bit 6 EXT MCLK - External MCLK Select
0 = MCLK provided by internal PLL
1 = MCLK is input on pin 151

This bit can also be set to 1 at reset via power-on strapping of PD11. An external MCLK is only used for S3 test purposes.

Bit 7 EXT DCLK - External DCLK Select
0 = DCLK provided by internal PLL
1 = DCLK is input on pin 156.

This bit can also be set to 1 at reset via power-on strapping of PD11. An external DCLK is only used for S3 test purposes.

CLKSYN Control 2 Register (SR15)

Read/Write Address: 3C5H, Index 15H
Power-On Default: 00H

7	6	5	4	3	2	1	0
2 CYC MWR	DCLK\ INV	CLK LOAD	DCLK/ 2	VCLK OUT	MCLK OUT	DRFQ EN	MFRQ EN

Bit 0 MFRQ EN - Enable new MCLK frequency load
0 = Register bit clear
1 = Load new MCLK frequency

When new MCLK PLL values are programmed, this bit can be set to 1 to load these values in the PLL. The loading may be delayed a small but variable amount of time. This bit should be cleared to 0 after loading to prevent repeated loading. Alternately, use bit 5 of this register to produce an immediate load.

Bit 1 DFRQ EN - Enable new DCLK frequency load
0 = Register bit clear
1 = Load new DCLK frequency

When new DCLK PLL values are programmed, this bit can be set to 1 to load these values in the PLL. Bits 3-2 of 3C2H must also be set to 11b if they are not already at this value. The loading may be delayed a small but variable amount of time. This bit should be programmed to 1 at power-up to allow loading of the VGA DCLK value and then left at this setting. Use bit 5 of this register to produce an immediate load.

Bit 2 MCLK OUT - Output internally generated MCLK
0 = Pin 147 functions normally
1 = Pin 147 outputs the internally generated MCLK

This is used only for testing.

Bit 3 VCLK OUT - VCLK direction determined by $\overline{\text{EVCLK}}$
0 = Pin 148 outputs the internally generated VCLK regardless of the state of $\overline{\text{EVCLK}}$
1 = VCLK direction is determined by the $\overline{\text{EVCLK}}$ signal

This bit is effective only when the LPB feature connector is enabled.

Bit 4 DCLK/2 - Divide DCLK by 2
0 = DCLK unchanged
1 = Divide DCLK by 2

Either this bit or bit 6 of this register must be set to 1 for clock doubled RAMDAC operation (mode 0001).

Bit 5 CLK LOAD - MCLK, DCLK load
0 = Clock loading is controlled by bits 0 and 1 of this register
1 = Load MCLK and DCLK PLL values immediately

To produce an immediate MCLK and DCLK load, program this bit to 1 and then to 0. Bits 3-2 of 3C2H must also then be programmed to 11b to load the DCLK values if they are not already programmed to this value. This register must never be left set to 1.

Bit 6 DCLK INV - Invert DCLK
0 = DCLK unchanged
1 = Invert DCLK

Either this bit or bit 4 of this register must be set to 1 for clock doubled RAMDAC operation (mode 0001).

Bit 7 2 CYC MWR - Enable 2 cycle memory write
0 = 3 MCLK memory write
1 = 2 MCLK memory write

Setting this bit to 1 bypasses the VGA logic for linear addressing when bit 7 of SRA is set to 1. This can allow 2 MCLK operation for MCLK frequencies between 55 and 57 MHz.

CLKSYN Test High Register (SR16)

Read/Write Address: 3C5H, Index 16H
Power-On Default: 00H

This register is reserved for S3 testing of the internal clock synthesizer.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

CLKSYN Test Low Register (SR17)

Read Only Address: 3C5H, Index 17H
Power-On Default: 00H

This register is reserved for S3 testing of the internal clock synthesizer.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

RAMDAC/CLKSYN Control Register (SR18)

Read/Write Address: 3C5H, Index 18H
Power-On Default: 00H

7	6	5	4	3	2	1	0
CLKx 2	LUT WR	DAC PD	TST BLUE	TST GRN	TST RED	TST RST	TST EN

Bit 0 TST EN - Enable test counter
0 = RAMDAC test counter disabled
1 = RAMDAC test counter enabled

This bit is used for S3 test purposes only.

Bit 1 TST RST - Reset test counter
0 = No effect
1 = Reset the RAMDAC test counter

This bit is used for S3 test purposes only.

Bit 2 TST RED - Test red data
0 = No effect
1 = Place red data on internal data bus

This bit is used for S3 test purposes only.

Bit 3 TST GRN - Test green data
0 = No effect
1 = Place green data on internal data bus

This bit is used for S3 test purposes only.

Bit 4 TST BLUE - Test blue data
0 = No effect
1 = Place blue data on internal data bus

This bit is used for S3 test purposes only.

Bit 5 DAC PD - RAMDAC power-down
0 = RAMDAC powered
1 = RAMDAC powered-down

When the RAMDAC is powered down, the RAMDAC memory retains its data.

Bit 6 LUT WR - LUT write cycle control
0 = 2 DCLK LUT write cycle (default)
1 = 1 DCLK LUT write cycle

Bit 7 CLKx2 - Enable clock doubled mode
0 = RAMDAC clock doubled mode (0001) disabled
1 = RAMDAC clock doubled mode (0001) enabled

This bit must be set to 1 when mode 0001 is specified in bits 7-4 of CR67 or SRC. Either bit 4 or bit 6 of SR15 must also be set to 1.

Extended Sequencer 1C Register (SR1C)

Read/Write Address: 3C5H, Index 1CH
Power-On Default: 00H

The bits in this register are effective only in LPB mode.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	SIGSEL	

Bits 1–0 SIGSEL - Signal Select
(For VL)
00 = Pin 151 is $\overline{\text{ENFEAT}}$; pin 153 is $\overline{\text{ROMCS}}$
01 = Pin 151 is $\overline{\text{GPIOSTR}}$; pin 153 is $\overline{\text{ROMCS}}$
10 = Pin 151 is GOP0; pin 153 is $\overline{\text{ROMCS}}$
11 = Pin 151 is GOP0; pin 153 is GOP1
(For PCI)
00 = Pin 151 is $\overline{\text{ENFEAT}}$; pin 153 is $\overline{\text{ROMEN}}$, pin 190 is $\overline{\text{STWR}}$
01 = Pin 151 is reserved; pin 153 is $\overline{\text{ROMEN}}$, pin 190 is $\overline{\text{STWR}}$
10 = Pin 151 is GOP0; pin 153 is $\overline{\text{ROMEN}}$, pin 190 is GOP1
11 = Pin 151 is GOP0; pin 153 is $\overline{\text{ROMEN}}$, pin 190 is GOP1

GOP0 and GOP1 are bits 0-1 of the General Output Port register (CR5C).

When the system powers up with a default value of 00b for bits 1-0, both pin 151 and pin 153 will be driven high (logic 1).

Bits 7–2 Reserved

16.3 CRT CONTROLLER REGISTERS

The CRT controller registers are located at two locations in I/O address space. These registers are accessed by first writing to the index register of the CRT controller and then accessing the data register. The index register is located at I/O address 3?4H and the CRT Controller Data register is at 3?5H. Which address is used (3BX or 3DX) depends on bit 0 of the Miscellaneous Output register at 3C2H. A word write of both address and data at 3?4H can also be performed.

CRT Controller Index Register (CRTC_ADR) (CRX)

Read/Write Address: 3?4H
Power-On Default: 00H

This register is loaded with a binary value that indexes the CRT controller register where data is to be accessed. This value is referred to as the "Index Number" of the CR register (CR00–18). This register is also used as an index to the S3 VGA registers, the System Control Registers and the System Extension registers.

7	6	5	4	3	2	1	0
CRTC ADDRESS							

Bits 7–0 CRTC ADDRESS - CRTC Register Index
A binary value indexing the register where data is to be accessed.

CRT Controller Data Register (CRTC_DATA) (CRT)

Read/Write Address: 3?5H
Power-On Default: Undefined

This register is the data port for the CRT controller register indexed by the CRT Controller Address register.

7	6	5	4	3	2	1	0
CRTC DATA							

Bits 7–0 CRTC DATA - CRTC Register Data
Data to the CRT controller register indexed by the CRT controller address index.

Horizontal Total Register (H_TOTAL) (CR0)

Read/Write Address: 3?5H, Index 00H
Power-On Default: Undefined

This register defines the number of character clocks from HSYNC going active to the next HSYNC going active. In other words, it is the total time required for both the displayed and non-displayed portions of a single scan line. Bit 8 of this value is bit 0 of CR5D.

7	6	5	4	3	2	1	0
HORIZONTAL TOTAL							

Bits 7–0 HORIZONTAL TOTAL.
9-bit Value = (number of character clocks in one scan line) - 5. This register contains the least significant 8 bits of this value.

Horizontal Display End Register (H_D_END) (CR1)

Read/Write Address: 3?5H, Index 01H
Power-On Default: Undefined

This register defines the number of character clocks for one line of the active display. Bit 8 of this value is bit 1 of CR5D.

7	6	5	4	3	2	1	0
HORIZONTAL DISPLAY END							

Bits 7–0 HORIZONTAL DISPLAY END
9-bit Value = (number of character clocks of active display) - 1. This register contains the least significant 8 bits of this value.

Start Horizontal Blank Register (S_H_BLNK) (CR2)

Read/Write Address: 3?5H, Index 02H
Power-On Default: Undefined

This register specifies the value of the character clock counter at which the $\overline{\text{BLANK}}$ signal is asserted. Bit 8 of this value is bit 2 of CR5D.

7	6	5	4	3	2	1	0
START HORIZONTAL BLANK							

Bits 7–0 START HORIZONTAL BLANK
9-bit Value = character clock value at which horizontal blanking begins. This register contains the least significant 8 bits of this value.

End Horizontal Blank Register (E_H_BLNK) (CR3)

Read/Write Address: 3?5H, Index 03H
Power-On Default: Undefined

This register determines the pulse width of the $\overline{\text{BLANK}}$ signal and the display enable skew.

7	6	5	4	3	2	1	0
R	DSP-SKW 1	0	END HORIZONTAL BLANK				

Bits 4–0 END HORIZONTAL BLANK
7-bit Value = least significant 7 bits of the character clock counter value at which time horizontal blanking ends. To obtain this value, add the desired $\overline{\text{BLANK}}$ pulse width in character clocks to the Start Horizontal Blank value, which is also in character clocks. The 5 least significant bits of this sum are programmed into this field. The sixth bit is programmed into bit 7 of CR5. The seventh bit is programmed into bit 3 of CR5D.

Bits 6–5 DSP-SKW - Display Skew
These two bits determine the amount of display enable skew. Display enable skew control provides sufficient time for the CRT Controller to access the display buffer to obtain a character and attribute code, access the character generator font, and then go through the Horizontal Pixel Panning register in the Attribute Controller. Each access requires the display enable signal to be skewed one character clock unit so the video output is synchronous with the HSYNC and VSYNC signals. The bit values and amount of skew are shown in the following table:
00 = Zero character clock skew
01 = One character clock skew
10 = Two character clock skew
11 = Three character clock skew

Bit 7 Reserved

Start Horizontal Sync Position Register (S_H_SY_P) (CR4)

Read/Write Address: 3?5H, Index 04H
Power-On Default: Undefined

This register is used to adjust the screen center horizontally and to specify the character position at which HSYNC becomes active. Bit 8 of this value is bit 4 of CR5D.

7	6	5	4	3	2	1	0
START HORIZONTAL SYNC POSITION							

Bits 7–0 START HORIZONTAL SYNC POSITION.
9-bit Value = character clock counter value at which HSYNC becomes active. This register contains the least significant 8 bits of this value.

End Horizontal Sync Position Register (E_H_SY_P) (CR5)

Read/Write Address: 3?5H, Index 05H
Power-On Default: Undefined

This register specifies when the HSYNC signal becomes inactive and the horizontal skew. The HSYNC pulse defined by this register can be extended by 32 DCLKs via bit 5 of CR5D.

7	6	5	4	3	2	1	0
EHB b5	HOR-SKW 1	0	END HORIZONTAL SYNC POS				

Bits 4–0 END HORIZONTAL SYNC POS
6-bit Value = 6 least significant bits of the character clock counter value at which time HSYNC becomes inactive. To obtain this value, add the desired HSYNC pulse width in character clocks to the Start Horizontal Sync Position value, also in character clocks. The 5 least significant bits of this sum are programmed into this field. The sixth bit is programmed into bit 5 of CR5D.

Bits 6–5 HOR-SKW - Horizontal Skew
These bits control the skew of the HSYNC signal. A binary 00 equals no HSYNC delay. For some modes, it is necessary to provide an HSYNC signal that takes up the entire blanking interval. Some internal timings are generated by the falling edge of the HSYNC signal. To guarantee the signals are latched properly, HSYNC is asserted before the end of the display enable signal, and then skewed several character clock times to provide the proper screen centering.
00 = Zero character clock skew
01 = One character clock skew
10 = Two character clock skew
11 = Three character clock skew

Bit 7 EHB b5
End Horizontal Blanking bit 5.

Vertical Total Register (V_TOTAL) (CR6)

Read/Write Address: 3?5H, Index 06H
Power-On Default: Undefined

This register specifies the number of scan lines from one VSYNC active to the next VSYNC active. The scan line counter resets to 0 at this point. Bit 8 is bit 0 of CR7. Bit 9 is bit 5 of CR7. Bit 10 is bit 0 of CR5E.

7	6	5	4	3	2	1	0
VERTICAL TOTAL							

Bits 7–0 VERTICAL TOTAL
11-bit Value = (number of scan lines from VSYNC active to the next VSYNC active) - 2.
This register contains the least significant 8 bits of this value.

CRTC Overflow Register (OVFL_REG) (CR7)

Read/Write Address: 3?5H, Index 07H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
VRS 9	VDE 9	VT 9	LCM 8	SVB 8	VRS 8	VDE 8	VT 8

This register provides extension bits for fields in other registers.

Bit 0 Bit 8 of the Vertical Total register (CR6)

Bit 1 Bit 8 of the Vertical Display End register (CR12)

Bit 2 Bit 8 of the Vertical Retrace Start register (CR10)

Bit 3 Bit 8 of the Start Vertical Blank register (CR15)

Bit 4 Bit 8 of the Line Compare register (CR18)

Bit 5 Bit 9 of the Vertical Total register (CR6)

Bit 6 Bit 9 of the Vertical Display End register (CR12)

Bit 7 Bit 9 of the Vertical Retrace Start register (CR10)

Preset Row Scan Register (P_R_SCAN) (CR8)

Read/Write Address: 3?5H, Index 08H
Power-On Default: Undefined

This register is used for the pixel scrolling and panning, and text formatting and vertical scrolling.

7	6	5	4	3	2	1	0
= 0	BYTE-PAN 1	0	PRE-SET ROW SCAN COUNT				

Bits 4–0 PRE-SET ROW SCAN COUNT
Value = starting row within a character cell for the first character row displayed after vertical retrace. This allows a partial character row to be displayed at the top of the display and is used for scrolling.

Bits 6–5 BYTE-PAN
Value = number of bytes to pan. The number of pixels to pan is specified in AR13.

Bit 7 Reserved = 0

Maximum Scan Line Register (MAX_S_LN) (CR9)

Read/Write Address: 3?5H, Index 09H
Power-On Default: Undefined

This register specifies the number of scan lines per character row and provides one scanning control bit and two overflow bits.

7	6	5	4	3	2	1	0
DBL SCN	LCM 9	SVB 9	MAX SCAN LINE				

Bits 4–0 MAX SCAN LINE
Value = (number of scan lines per character row) - 1

Bit 5 SVB 9
Bit 9 of the Start Vertical Blank Register (CR15)

Bit 6 LCM 9
Bit 9 of the Line Compare Register (CR18)

Bit 7 DBL SCN
0 = Normal operation
1 = Enables double scanning operation. Each line is displayed twice by repeating the row scan counter and video memory address. Vertical parameters in the CRT controller are not affected.

Cursor Start Scan Line Register (CSSL) (CRA)

Read/Write Address: 3?5H, Index 0AH
Power-On Default: Undefined

The cursor start register defines the row scan of a character line where the cursor begins.

7	6	5	4	3	2	1	0
= 0	= 0	CSR OFF	CSR CURSOR START SCAN LINE				

Bits 4–0 CSR CURSOR START SCAN LINE
Value = (starting cursor row within the character cell) - 1. When the cursor start register is programmed with a value greater than the cursor end register, no cursor is generated.

Bit 5 CSR OFF
0 = Turns on the text cursor
1 = Turns off the text cursor

Bits 7–6 Reserved = 0

Cursor End Scan Line Register (CESL) (CRB)

Read/Write Address: 3?5H, Index 0BH
Power-On Default: Undefined

This register defines the row scan of a character line where the cursor ends.

7	6	5	4	3	2	1	0
= 0	CSR-SKW 1	0	CURSOR END SCAN LINE				

Bits 4–0 CURSOR END SCAN LINE
Value = ending scan line number within the character cell for the text cursor. If the value of the cursor start scan line is greater than the value of cursor end line, then no cursor is generated.

Bits 6–5 CSR-SKW - Cursor Skew
These bits control the delay skew of the cursor signal. Cursor skew delays the text cursor by the selected number of clocks. For example, a skew of 1 moves the cursor right one character position on the screen.
00 = Zero character clock skew
01 = One character clock skew
10 = Two character clock skew
11 = Three character clock skew

Bit 7 Reserved = 0

Start Address High Register (STA(H)) (CRC)

Read/Write Address: 3?5H, Index 0CH
Power-On Default: Undefined

15	14	13	12	11	10	9	8
DISPLAY START ADDRESS (HIGH)							

20-bit Value = the first address after a vertical retrace at which the display on the screen begins on each screen refresh. These along with bits 5-0 of CR69 are the high order start address bits.

Start Address Low Register (STA(L)) (CRD)

Read/Write Address: 3?5H, Index 0DH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
DISPLAY START ADDRESS (LOW)							

Start address (low) contains the 8 low order bits of the address.

Cursor Location Address High Register (CLA(H)) (CRE)

Read/Write Address: 3?5H, Index 0EH
Power-On Default: Undefined

15	14	13	12	11	10	9	8
CURSOR LOCATION ADDRESS (HIGH)							

20-bit Value = the cursor location address of the video memory where the text cursor is active. This register along with bits 5-0 of CR69 are the high order bits of the address.

Cursor Location Address Low Register (CLA(L)) (CRF)

Read/Write Address: 3?5H, Index 0FH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
CURSOR LOCATION ADDRESS (LOW)							

Cursor location address (low) contains the 8 low order bits of the address.

Vertical Retrace Start Register (VRS) (CR10)

Read/Write Address: 3?5H, Index 10H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
VERTICAL RETRACE START							

Bits 7–0 VERTICAL RETRACE START.
11-bit Value = scan line counter value at which VSYNC becomes active. These are the low-order 8 bits. Bit 8 is bit 2 of CR7. Bit 9 is bit 7 of CR7. Bit 10 is bit 4 of CR5E.

Vertical Retrace End Register (VRE) (CR11)

Read/Write Address: 3?5H, Index 11H
Power-On Default: 0xH

This register controls the vertical interrupt and CR0-7

7	6	5	4	3	2	1	0
LOCK R0-7	REF 3/5	DIS VINT	CLR VINT	VERTICAL RETRACE END			

Bits 3–0 VERTICAL RETRACE END
Value = least significant 4 bits of the scan line counter value at which VSYNC goes inactive. To obtain this value, add the desired VSYNC pulse width in scan line units to the CR10 value, also in scan line units. The 4 least significant bits of this sum are programmed into this field. This allows a maximum VSYNC pulse width of 15 scan line units.

Bit 4 $\overline{\text{CLR}}$ VINT - Clear Vertical Retrace Interrupt
0 = Vertical retrace interrupt cleared
1 = The flip-flop is able to catch the next interrupt request

At the end of active vertical display time, a flip-flop is set for a vertical interrupt. The output of this flip-flop goes to the system interrupt controller. The CPU has to reset this flip-flop by writing a logical 0 to this bit while in the interrupt process, then set the bit to 1 to allow the flip-flop to catch the next interrupt request. Do not change the other bits in this register. This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on.

Bit 5 DIS VINT - Disable Vertical Interrupt
0 = Vertical retrace interrupt enabled if CR32_4 = 1
1 = Vertical interrupt disabled. This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on

Bit 6 REF $\overline{3}$/5 - Refresh Cycle Select
0 = Three DRAM refresh cycles generated per horizontal line
1 = Five DRAM refresh cycles generated per horizontal line. Selecting five refresh cycles allows use of the VGA chip with slow sweep rate displays (15.75 KHz). This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on. This setting can be overridden via bits 1-0 of CR3A

Bit 7 LOCK R0-7 - Lock Writes to CRT Controller Registers
0 = Writing to all CRT Controller registers enabled
1 = Writing to all bits of the CRT Controller registers CR0–CR7 except bit 4 of CR7 (LCM8) disabled. This bit is set to 1 by the BIOS during a mode set, a reset or power-on

Vertical Display End Register (VDE) (CR12)

Read/Write Address: 3?5H, Index 12H
Power-On Default: Undefined

The vertical display enable end register defines 8 bits of the 10-bit address of the scan line where the display on the screen ends. Bit 8 and Bit 9 are bits 1 and 6 of CR7. Bit 10 is bit 1 of CR5E.

7	6	5	4	3	2	1	0
VERTICAL DISPLAY END							

Bit 7–0 VERTICAL DISPLAY END
11-bit Value = (number of scan lines of active display) - 1. This register contains the least significant 8 bits of this value.

Offset Register (SCREEN-OFFSET) (CR13)

Read/Write Address: 3?5H, Index 13H
Power-On Default: Undefined

This register specifies the logical line width of the screen and is sometimes called the screen pitch. The starting memory address for the next display row is larger than the current row by two, four or eight times this amount. Bits 5-4 of CR51 are extension bits 9-8 of this register. If these bits are 00b, bit 2 of CR43 is extension bit 8 of this register.

7	6	5	4	3	2	1	0
LOGICAL SCREEN WIDTH							

Bits 7–0 LOGICAL SCREEN WIDTH
10-bit Value = quantity that is multiplied by 2 (word mode), 4 (doubleword mode) or 8 (quadword mode) to specify the difference between the starting byte addresses of two consecutive scan lines. This register contains the least significant 8 bits of this

value. The addressing mode is specified by bit 6 of CR14 and bit 3 of CR17. Setting bit 3 of CR31 to 1 forces doubleword mode.

Underline Location Register (ULL) (CR14)

Read/Write Address: 3?5H, Index 14H
Power-On Default: Undefined

This register specifies the horizontal row scan position of underline and display buffer addressing modes.

7	6	5	4	3	2	1	0
= 0	DBWD MODE	CNT BY4	UNDER LINE LOCATION				

Bits 4–0 UNDER LINE LOCATION
5-bit Value = (scan line count of a character row on which an underline occurs) -1

Bit 5 CNT BY4 - Select Count by 4 Mode
0 = The memory address counter depends on bit 3 of CR17 (count by 2)
1 = The memory address counter is incremented every four character clocks

The CNT BY4 bit is used when double word addresses are used.

Bit 6 DBLWD MODE - Select Doubleword Mode
0 = The memory addresses are byte or word addresses
1 = The memory addresses are doubleword addresses

Bit 7 Reserved = 0

Start Vertical Blank Register (SVB) (CR15)

Read/Write Address: 3?5H, Index 15H
Power-On Default: Undefined

This register specifies the scan line at which the vertical blanking period begins. Bit 8 is bit 3 of CR7. Bit 9 is bit 5 of CR9. Bit 10 is bit 2 of CR5E.

7	6	5	4	3	2	1	0
START VERTICAL BLANK							

Bits 7–0 START VERTICAL BLANK.
11-bit value = (scan line count at which $\overline{\text{BLANK}}$ becomes active) - 1. This register contains the least significant 8 bits of this value.

End Vertical Blank Register (EVB) (CR16)

Read/Write Address: 3?5H, Index 16H
Power-On Default: Undefined

This register specifies the scan line count value when the vertical blank period ends.

7	6	5	4	3	2	1	0
END VERTICAL BLANK							

Bits 7–0 END VERTICAL BLANK
Value = least significant 8 bits of the scan line counter value at which vertical blanking ends. To obtain this value, add the desired width of the vertical blanking pulse in scan lines to [(value in the Start Vertical Blank register)-1], also in scan lines. The 8 least significant bits of this sum are programmed into this field. This allows a maximum vertical blanking pulse of 255 scan line units.

CRTC Mode Control Register (CRT_MD) (CR17)

Read/Write Address: 3?5H, Index 17H
Power-On Default: 00H

This register is a multifunction control register, with each bit defining a different specification.

7	6	5	4	3	2	1	0
RST	BYTE MODE	ADW 16K	= 0	WRD MODE	VT X2	4BK HGC	2BK CGA

Bit 0 $\overline{2BK}$ CGA - Select Bank 2 Mode for CGA Emulation
0 = Row scan counter bit 0 is substituted for memory address bit 13 during active display time
1 = Memory address bit 13 appears on the memory address output bit 13 signal of the CRT controller

This bit allows memory mapping compatibility with the IBM CGA graphics mode.

Bit 1 $\overline{4BK}$ HGC - Select Bank 4 Mode for HGA Emulation
0 = Row scan counter bit 1 is substituted for memory address bit 14 during active display time
1 = Memory address bit 14 appears on the memory address output bit 14 signal of the CRT controller

The combination of this bit and bit 0 of this register allows compatibility with Hercules HGC graphics memory mapping.

Bit 2 VT X2 - Select Vertical Total Double Mode
0 = Horizontal retrace clock selected
1 = Horizontal retrace clock divided by two selected

This bit selects horizontal retrace clock or horizontal retrace clock divided by two as the clock that controls the vertical timing counter. If the vertical retrace counter is clocked with the horizontal retrace clock divided by 2, then the vertical resolution is double.

Bit 3 CNT BY2 - Select Word Mode
0 = Memory address counter is clocked with the character clock input, and byte mode addressing for the video memory is selected
1 = Memory address counter is clocked by the character clock input divided by 2, and word mode addressing for the video memory is selected

Bit 4 Reserved = 0

Bit 5 $\overline{\text{ADW}}$ 16K - Address Wrap
0 = When word mode is selected by bit 6 of this register, memory address counter bit 13 appears on the memory address output bit 0 signal of the CRT controller and the video memory address wraps around at 16 KBytes
1 = When word mode is selected by bit 6 of this register, memory address counter bit 15 appears on the memory address output bit 0 signal of the CRT controller

This bit is useful in implementing IBM CGA mode.

Bit 6 BYTE MODE - Select Byte Addressing Mode
0 = Word mode shifts all memory address counter bits down one bit, and the most significant bit of the counter appears on the least significant bit of the memory address output
1 = Byte address mode

Bit 7 $\overline{\text{RST}}$ - Hardware Reset
0 = Vertical and horizontal retrace pulses always inactive
1 = Vertical and horizontal retrace pulses enabled

This bit does not reset any other registers or outputs.

Line Compare Register (LCM) (CR18)

Read/Write Address: 3?5H, Index 18H
Power-On Default: Undefined

This register is used to implement a split screen function. When the scan line counter value is equal to the content of this register, the memory address counter is cleared to 0. The linear address counter then sequentially addresses the display buffer starting at address 0. Each subsequent row address is determined by the addition of the Offset (CR13) register content. Bit 8 is bit 4 of CR7. Bit 9 is bit 6 of CR9. Bit 10 is bit 6 of CR5E.

7	6	5	4	3	2	1	0
LINE COMPARE POSITION							

Bit 7–0 LINE COMPARE POSITION
11-bit Value = number of scan lines at which the screen is split into screen A and screen B. This register contains the least significant 8 bits of this value.

CPU Latch Data Register (GCCL) (CR22)

Read Only Address: 3?5H, Index 22H
Power-On Default: Undefined

This register is used to read the CPU latch in the Graphics Controller.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER CPU LATCH - N							

Bits 7–0 GRAPHICS CONTROLLER CPU LATCH - N
Bits 1-0 of GR4 select the latch number N (3-0) of the CPU Latch.

Attribute Index Register (ATC_F/I) (CR24)

Read Only Address: 3?5H, Index 24H, 26H
Power-On Default: Undefined

This register is used to read the value of the Attribute Controller Index register and its associated internal address flip-flop (AFF). It can be read at either index 24H or 26H.

7	6	5	4	3	2	1	0
AFF	= 0	ENV	ATTRIBUTE CONTROLLER INDEX				

Bits 4–0 ATTRIBUTE CONTROLLER INDEX
This value is the Attribute Controller Index Data at I/O port 3C0H.

Bit 5 ENV- Enable Video Display
This is the setting of bit 5 of 3C0H, indicating video display enabled status (1 = enabled).

Bit 6 Reserved = 0

Bit 7 $\overline{\text{AFF}}$
Inverted Internal Address flip-flop

16.4 GRAPHICS CONTROLLER REGISTERS

The graphics controller registers are located at a two byte I/O address space. These registers are accessed by first writing an index to the Graphics Address register (at 3CEH) and then accessing the Data register (at 3CFH).

Graphics Controller Index Register (GRC_ADR)

Read/Write Address: 3CEH
Power-On Default: Undefined

This register is loaded with a binary index value that determines which graphics controller register will be accessed. This value is referred to as the "Index Number" of the GR register (GR0–6).

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	GR CONT ADDRESS			

Bits 3–0 GR CONT ADDRESS - Graphics Controller Register Index
A binary value indexing the register where data is to be accessed.

Bits 7–4 Reserved = 0

Graphics Controller Data Register (GRC_DATA)

Read/Write Address: 3CFH
Power-On Default: Undefined

This register is the data port for the graphics controller register indexed by the Graphics Controller Index register.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER DATA							

Bit 7–0 GRAPHICS CONTROLLER DATA
Data to the Graphics Controller register indexed by the graphics controller address.

Set/Reset Data Register (SET/RST_DT) (GR0)

Read/Write Address: 3CFH, Index 00H
Power-On Default: Undefined

This register represents the value written to all 8 bits of the respective memory plane when the CPU executes a memory write in write modes 0 and 3.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	SET/RESET DATA			

Bits 3–0 SET/RESET DATA
These bits become the color value for CPU memory write operations. In write mode 0, the set/reset data can be enabled on the corresponding bit of the Enable Set/Reset Data register. In write mode 3, there is no effect on the Enable Set/Reset Data register.

Bits 7–4 Reserved = 0

Enable Set/Reset Data Register (EN_S/R_DT) (GR1)

Read/Write Address: 3CFH, Index 01H
Power-On Default: Undefined

These bits enable the set/reset data, and affect write mode 0.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	ENB SET/RST DATA			

Bits 3–0 ENB SET/RST DATA
When each bit is a logical 1, the respective memory plane is written with the value of the Set/Reset Data register. A logical 0 disables the set/reset data in a plane, and that plane is written with the value of CPU write data.

Bits 7–4 Reserved = 0

Color Compare Register (COLOR-CMP) (GR2)

Read/Write Address: 3CFH, Index 02H
Power-On Default: Undefined

These bits represent a 4-bit color value to be compared. In read mode 1, the CPU executes a memory read, the read data is compared with this value and returns the results. This register works in conjunction with the Color Don't Care register.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	COLOR COMPARE DATA			

Bits 3–0 COLOR COMPARE DATA
This value becomes the reference color used to compare each pixel. Each of the 8-bit positions of the read data are compared across four planes and a logical 1 is returned in each bit position for which the colors match.

Bits 7–4 Reserved = 0

Raster Operation/Rotate Count Register (WT_ROP/RTC) (GR3)

Read/Write Address: 3CFH, Index 03H
Power-On Default: Undefined

This register selects a raster operation function and indicates the number of bits the CPU data will be rotated (right) on the video memory write operation.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	RST-OP 1	0	ROTATE-COUNT		

Bits 2–0 ROTATE-COUNT
These bits define a binary encoded value of the number of positions to right-rotate data during a CPU memory write. To write non-rotated data, the CPU must preset a count of 0.

Bits 4–3 RST-OP - Select Raster Operation
The data written to memory can operate logically with the data already in the processor latches. This function is not available in write mode 1. The logical functions are defined as follows:
00 = No operation
01 = Logical AND with latched data
10 = Logical OR with latched data
11 = Logical XOR with latched data

The logical function specified by this register is applied to data being written to memory while in modes 0, 2 and 3.

Bits 7–5 Reserved = 0

Read Plane Select Register (RD_PL_SL) (GR4)

Read/Write Address: 3CFH, Index 04H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	RD-PL-SL 1	0

The contents of this register represent the memory plane from which the CPU reads data in read mode 0. This register has no effect on the color compare read mode (read mode 1). In odd/even mode, bit 0 is ignored. Four memory planes are selected as follows:

Bits 1–0 RD-PL-SL - Read Plane Select
The memory plane is selected as follows:
00 = Plane 0
01 = Plane 1
10 = Plane 2
11 = Plane 3

Bits 7–2 Reserved = 0

Graphics Controller Mode Register (GRP_MODE) (GR5)

Read/Write Address: 3CFH, Index 05H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
	SHF-MODE		O/E	RD		WRT-MD	
= 0	256	O/E	MAP	CMP	= 0	1	0

This register controls the mode of the Graphics Controller as follows:

Bit 1–0 WRT-MD - Select Write Mode
These bits select the CPU write mode into video memory. The function of each mode is defined as follows:
00 = Write Mode 0. Each of four video memory planes is written with the CPU data rotated by the number of counts in the rotate register. If the Set/Reset register is enabled for any of four planes, the corresponding plane is written with the data stored in the set/reset register. Raster operations and bit mask registers are effective
01 = Write Mode 1. Each of four video memory planes is written with the data in the processor latches. These latches are loaded during previous CPU read operations. Raster operation, rotate count, set/reset data, enable set/reset data and bit mask registers are not effective
10 = Write Mode 2. Memory planes 0-3 are filled with 8 bits of the value of CPU write data bits 0-3, respectively. For example, if write data bit 0 is a 1, eight 1's are written to memory plane 0. The data on the CPU data bus is treated as the color value. The Bit Mask register is effective as the Mask register. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A logical 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the processor latches. The Set/Reset, Enable Set/Reset and Rotate Count registers are ignored
11 = Write Mode 3. Each of four video memory planes is written with 8 bits of the color value contained in the set/reset register for that plane. The Enable Set/Reset register is not effective. Rotated CPU write data is ANDed with the bit mask register to form an 8-bit value that performs the same function as the Bit Mask register in write modes 0 and 2. This write mode can be used to fill an area with a single color and pattern

Bit 2 Reserved = 0

Bit 3 RD CMP - Enable Read Compare
0 = The CPU reads data from the video memory planes. The plane is selected by the Read Plane Select register. This is called read mode 0
1 = The CPU reads the results of the logical comparison between the data in four video memory planes selected by the contents of the Color Don't Care register and the contents of the Color Compare register. The result is a 1 for a match and 0 for a mismatch on each pixel. This is called read mode 1

Bit 4 O/E MAP - Select Odd/Even Addressing
0 = Standard addressing.
1 = Odd/even addressing mode selected. Even CPU addresses access plane 0 and 2, while odd CPU addresses access plane 1 and 3. This option is useful for emulating the CGA compatible mode. The value of this bit should be the inverted value programmed in bit 2 of the Sequencer Memory Mode register (SR4). This bit affects reading of display memory by the CPU

Bit 5 SHF-MODE - Select Odd/Even Shift Mode
0 = Normal shift mode
1 = The video shift registers in the graphics section are directed to format the serial data stream with even-numbered bits from both planes on the even-numbered planes and odd-numbered bits from both planes on the odd planes

Bit 6 SHF-MODE - Select 256 Color Shift Mode
0 = Bit 5 in this register controls operation of the video shift registers
1 = The shift registers are loaded in a manner that supports the 256 color mode

Bit 7 Reserved = 0

Memory Map Mode Control Register (MISC_GM) (GR6)

Read/Write Address: 3CFH, Index 06H
Power-On Default: Undefined

This register controls the video memory addressing.

7	6	5	4	3	2	1	0
				MEM-MAP		CHN	TXT
= 0	= 0	= 0	= 0	1	0	O/E	/GR

Bit 0 $\overline{\text{TXT}}$/GR - Select Text/Graphics Mode
0 = Text mode display addressing selected
1 = Graphics mode display addressing selected. When set to graphics mode, the character generator address latches are disabled

Bit 1 CHN O/E - Chain Odd/Even Planes
0 = A0 address bit unchanged
1 = CPU address bit A0 is replaced by a higher order address bit. The content of A0 determines which memory plane is to be addressed. A0 = 0 selects planes 0 and 2, and A0 = 1 selects planes 1 and 3. This mode can be used to double the address space into video memory

Bits 3–2 MEM-MAP - Memory Map Mode
These bits control the address mapping of video memory into the CPU address space. The bit functions are defined below.
00 = A0000H to BFFFFH (128 KBytes)
01 = A0000H to AFFFFH (64 KBytes)
10 = B0000H to B7FFFH (32 KBytes)
11 = B8000H to BFFFFH (32 KBytes)

Bits 7–4 Reserved = 0

Color Don't Care Register (CMP_DNTC) (GR7)

Read/Write Address: 3CFH, Index 07H
Power-On Default: Undefined

This register is effective in read mode 1, and controls whether the corresponding bit of the Color Compare Register is to be ignored or used for color comparison.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	COMPARE PLANE SEL			

Bits 3–0 COMPARE PLANE SEL - Compare Plane Select
0 = The corresponding color plane becomes a don't care plane when the CPU read from the video memory is performed in read mode 1
1 = The corresponding color plane is used for color comparison with the data in the Color Compare register

Bits 7–4 Reserved = 0

Bit Mask Register (BIT_MASK) (GR8)

Read/Write Address: 3CFH, Index 08H
Power-On Default: Undefined

Any bit programmed to 0 in this register will cause the corresponding bit in each of four memory planes to be immune to change. The data written into memory in this case is the data which was read in the previous cycle, and was stored in the processor latches. Any bit programmed to 1 allows unimpeded writes to the corresponding bits in the plane.

7	6	5	4	3	2	1	0
BIT MASK							

Bits 7–0 BIT MASK
A logical 0 means the corresponding bit of each plane in memory is set to the corresponding bit in the processor latches. A logical 1 means the corresponding bit of each plane in memory is set as specified by other conditions.

16.5 ATTRIBUTE CONTROLLER REGISTERS

The attribute controller registers are located at the same byte I/O address for writing address and data. An internal address flip-flop (AFF) controls the selection of either the attribute index or data registers. To initialize the address flip-flop (AFF), an I/O read is issued at address 3BAH or 3DAH. This presets the address flip-flop to select the index register. After the index register has been loaded by an I/O write to address 3C0H, AFF toggles and the next I/O write loads the data register. Every I/O write to address 3C0H toggles this address flip-flop. However, it does not toggle for I/O reads at address 3C0H or 3C1H. The Attribute Controller Index register is read at 3C0H, and the Attribute Controller Data register is read at address 3C1H.

Attribute Controller Index Register (ATR_AD)

Read/Write Address: 3C0H
Power-On Default: Undefined

This register is loaded with a binary index value that determines which attribute controller register will be accessed. This value is referred to as the "Index Number" of the AR register (AR0–14).

7	6	5	4	3	2	1	0
R	R	ENB PLT	ATTRIBUTE ADDRESS				

Bits 4–0 ATTRIBUTE ADDRESS
A binary value that points to the attribute controller register where data is to be written.

Bit 5 ENB PLT - Enable Video Display
0 = Video display access to the palette registers disabled. The Attribute Controller register can be accessed by the CPU
1 = Display video using the palette registers enabled (normal display operation). The palette registers (AR0–ARF) cannot be accessed by the CPU

This bit is effective only in 8-bit PA mode (CR67_4 = 0).

Bits 7–6 Reserved

Attribute Controller Data Register (ATR_DATA)

Read/Write Address: R: 3C1H/W: 3COH
Power-On Default: Undefined

This register is the data port for the attribute controller register indexed by the Attribute Controller Index register.

7	6	5	4	3	2	1	0
ATTRIBUTE DATA							

Bits 7–0 ATTRIBUTE DATA
Data to the attribute controller register indexed by the attribute controller address.

Palette Registers (PLT_REG) (AR00-0F)

Read/Write Address: 3C1H/3C0H, Index 00H-0FH
Power-On Default: Undefined

These are 16, 6-bit registers pointed to by the index and color code. They allow a dynamic mapping between the text attribute or graphics color input and the display color on the CRT screen.

7	6	5	4	3	2	1	0
		SECONDARY			PRIMARY		
= 0	= 0	SR	SG	SB	R	G	B

Bits 5–0 PALETTE COLOR
The six bit display color, bits 5-0 are output as SR, SG/I, SB/V, R, G and B, respectively.

Bits 7–6 Reserved = 0

Attribute Mode Control Register (ATR_MODE) (AR10)

Read/Write Address: 3C1H/3C0H, Index 10H
Power-On Default: 00H

The contents of this register controls the attribute mode of the display function.

7	6	5	4	3	2	1	0
SEL V54	256 CLR	TOP PAN	= 0	ENB BLNK	ENB LGC	MONO ATRB	TX /GR

Bit 0 $\overline{TX}$/GR - Select Graphics Mode
0 = Selects text attribute control mode
1 = Selects graphics control mode

Bit 1 MONO ATRB - Select Monochrome Attributes
0 = Selects color display text attributes
1 = Selects monochrome display text attributes

Bit 2 ENB LGC - Enable Line Graphics
0 = The ninth dot of a text character (bit 0 of SR1 = 0) is the same as the background
1 = Special line graphics character codes enabled

When this bit is set to 1, it forces the ninth dot of a line graphics character to be identical to the eighth dot of the character. The line graphics character codes are C0H through DFH. For other characters, the ninth dot is the same as the background.

Bit 3 ENB BLNK - Enable Blinking
0 = Selects the background intensity for the text attribute input
1 = Selects blink attribute in text modes

This bit must also be set to 1 for blinking graphics modes. The blinking counter is operated by the vertical retrace counter (VRTC) input. It divides the VRTC input by 32. The blinking rates are ON for 16 VRTC clocks and OFF for 16 VRTC clocks. In the graphics mode, when blink is activated, the most significant color bit (bit 3) for each dot is inverted alternately, thus allowing two different colors to be displayed for 16 VRTC clocks each.

When the cursor is displayed in the text mode, it is blinked at a rate of ON for 8 VRTC clocks and OFF for 8 VRTC clocks (period by 16 frames). The displayed characters are independently blinked at the rate of 32 frames as above.

Bit 4 Reserved = 0

Bit 5 TOP PAN - Top Panning Enable
0 = Line compare has no effect on the output of the pixel panning register
1 = Forces the output of the pixel panning register to 0 after matching line compare until VSYNC occurs in the CRT controller. At the top of screen the output of the Pixel Panning register returns to its programmed value. This bit allows a top portion of a split screen to be panned.

Bit 6 256 CLR - Select 256 Color Mode
0 = 4 bits of video (translated to 6 bits by the palette) are output every internal dot-clock cycle
1 = Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot-clock

Bit 7 SEL V54 - Select V[5:4]
0 = In VGA, mode, bits 5-4 of video output are generated by the attribute palette registers. Bits 7-6 of video output are always generated by bits 3-2 of AR14
1 = Bits 5-4 of video output are generated by bits 1-0 of AR14

Border Color Register (BDR_CLR) (AR11)

Read/Write Address: 3C1H/3C0H, Index 11H
Power-On Default: 00H

7	6	5	4	3	2	1	0
BORDER COLOR							

Bits 7–0 Border Color. This 8-bit register determines the border color displayed on the CRT screen. The border is an area around the screen display area.

This register is only effective in 8-bit PA modes (CR67_4 = 0). See also CR33_5.

Color Plane Enable Register (DISP_PLN) (AR12)

Read/Write Address: 3C1H/3C0H, Index 12H
Power-On Default: 00H

This register enables the respective video memory color plane 3–0 and selects video color outputs to be read back in the display status.

7	6	5	4	3	2	1	0
= 0	= 0	VDT-SEL 1	0	DISPLAY PLANE ENBL			

Bits 3–0 DISPLAY PLANE ENBL
A 0 in any of these bits forces the corresponding color plane bit to 0 before accessing the internal palette. A 1 in any of these bits enables the data on the corresponding color plane.

Bits 5–4 VDT-SEL - Video Test Select
These bits select two of the eight bit color outputs to be available in the Input Status 1 register. The output color combinations available on the status bits are as follows:

D STS MUX		STS 1	
Bit 5	**Bit 4**	**Bit 5**	**Bit 4**
0	0	Video 2	Video 0
0	1	Video 5	Video 4
1	0	Video 3	Video 1
1	1	Video 7	Video 6

Bits 7–6 Reserved = 0

Horizontal Pixel Panning Register (H_PX_PAN) (AR13)

Read/Write Address: 3C1H/3C0H, Index 13H
Power-On Default: 00H

This register specifies the number of pixels to shift the display data horizontally to the left. Pixel panning is available in both text and graphics modes. It is not available with Enhanced mode memory mappings (CR31_3 = 1).

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	NUMBER OF PAN SHIFT			

Bits 3–0 NUMBER OF PAN SHIFT
This register selects the number of pixels to shift the display data horizontally to the left. In the 9 pixels/character text mode, the output can be shifted a maximum shift of 8 pixels. In the 8 pixels/character text mode and all graphics modes, except 256 color mode, a maximum shift of 7 pixels is possible. In the 256 color mode, bit 0 of this register must be 0 resulting in only 4 panning positions per display byte. The panning is controlled as follows:

	Number of pixels shifted in		
Bits 3–0	**9 pixel/char.**	**8 pixel/char.**	**256 color mode**
0000	1	0	0
0001	2	1	–
0010	3	2	1
0011	4	3	–
0100	5	4	2
0101	6	5	–
0110	7	6	3
0111	8	7	–
1000	0	–	–

Bits 7–4 Reserved = 0

Pixel Padding Register (PX_PADD) (AR14)

Read/Write Address: 3C1H/3C0H, Index 14H
Power-On Default: 00H

This register specifies the high-order bits of video output when pixel padding is enabled and disabled in the 256 color mode.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	PIXEL PADDING V7	V6	V5	V4

Bits 1–0 PIXEL PADDING V5, V4
These bits are enabled with a logical 1 of bit 7 of AR10, and can be used in place of the V5 and V4 bits from the Palette registers to form the 8-bit digital color value output.

Bits 3–2 PIXEL PADDING V7, V6
In all modes except 256 color mode, these bits are the two high-order bits of the 8-bit digital color value output.

Bits 7–4 Reserved = 0

16.6 RAMDAC REGISTERS

All of the RAMDAC registers described in this section are physically located inside the Trio64V+.

DAC Mask Register (DAC_AD_MK)

Read/Write Address: 3C6H
Power-On Default: Undefined

This register is the pixel read mask register to select pixel video output. The CPU can access this register at any time.

7	6	5	4	3	2	1	0
DAC ADDRESS MASK							

Bits 7–0 DAC ADDRESS MASK
The contents of this register are bit-wise logically ANDed with the pixel select video output (PA[7:0]). This register is initialized to FFH by the BIOS during a video mode set.

DAC Read Index Register (DAC_RD_AD)

Write Only Address: 3C7H
Power-On Default: Undefined

This register contains the pointer to one of 256 palette data registers and is used when reading the color palette.

7	6	5	4	3	2	1	0
DAC READ ADDRESS							

Bits 7–0 DAC READ ADDRESS
Each time the color code is written to this register, it identifies that a read sequence will occur. A read sequence consists of three successive byte reads from the RAM-DAC data register at I/O address 3C9H. The least significant 6 bits of each byte taken from the RAMDAC data register contain the corresponding color value, and the most significant 2 bits contain zeros. The order is red byte first, then green, and finally blue. The sequence of events for a read cycle is:

1. Write the color code to this register (RAMDAC Read Index) at address 3C7H.
2. The contents of the location in the color look-up table pointed to by the color code are transferred to the RAMDAC data register at address 3C9H.
3. Three bytes are read back from the RAMDAC data register.
4. The contents of this register auto-increment by one.

5. Go to step 2.

The effects of writing to the RAMDAC data register during a three-byte read cycle or reading from the RAMDAC data register during a 3-byte write cycle (i.e., interrupting the sequence) are undefined and may change the look-up table contents.

DAC Status Register (DAC_STS)

Read Only Address: 3C7H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	DAC-STS	

Bits 1–0 DAC-STS - RAMDAC Cycle Status
The last executing cycle was:
00 = Write Palette cycle
11 = Read Palette cycle

Reads from the RAMDAC Write Index at address 3C8H or the DAC status register at address 3C7H do not interfere with read or write cycles and may take place at any time.

Bits 7–2 Reserved = 0

DAC Write Index Register (DAC_WR_AD)

Read/Write Address: 3C8H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
DAC WRITE ADDRESS/GIP READ DATA							

Bits 7–0 DAC WRITE ADDRESS/GIP READ DATA
This register contains the pointer to one of 256 palette data registers and is used during a palette load. Each time the color code is written to this register, it identifies that a write sequence will occur. A write sequence consists of three successive byte writes to the DAC data register at I/O address 3C9H. The least significant 6 bits of each byte are concatenated to form the value placed in the 18-bit data register. The order is red byte first, then green, and finally blue. Once the third byte has been written, the value in the data register is written to the location pointed to by the color code. The sequence of events for a write cycle is:

1. Write the color code to this register (DAC Write Index) at address 3C8H.
2. Three bytes are written to the DAC Data register at address 3C9H.

3. The contents of the DAC data register are transferred to the location in the color look-up table pointed to by the color code.
4. The DAC Write Index register auto-increments by 1.
5. Go to step 2.

If bit 2 of the Extended RAMDAC Control register (CR55) is set to 1 to enable the General I/O Port read function, a read of 3C8H retrieves data from an external input buffer. The data is transmitted via GD[7:0] to AD[7:0] for a PCI bus configuration and directly to SD[7:0] for a VL-Bus configuration.

RAMDAC Data Register (DAC_DATA)

Read/Write Address: 3C9H
Power-On Default: Undefined

This register is a data port to read or write the contents of the location in the color look-up table pointed to by the DAC Read Index or the DAC Write Index registers.

7	6	5	4	3	2	1	0
DAC READ/WRITE DATA							

Bits 7–0 DAC READ/WRITE DATA
To prevent "snow flicker" on the screen, an application reading data from or writing data to the DAC Data register should ensure that the $\overline{\text{BLANK}}$ input to the RAMDAC is asserted. This can be accomplished either by restricting data transfers to retrace intervals, checking bit 3 of the Input Status 1 register (3?AH) to determine when retrace is occurring, or by using the screen-off bit in the Clocking Mode register of the sequencer (bit 5 of SR1).

Section 17: S3 VGA Register Descriptions

The Trio64V+ has additional registers to extend the functions beyond VGA. These registers are located in CRT Controller address space at locations not used by the IBM® VGA. All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, the Register Lock 1 register (CR38) must be loaded with a changed key pattern (see the register description). The registers will remain unlocked until the key pattern is reset by altering a significant bit.

In the following register descriptions, 'R' stands for reserved (write =0, read = undefined). See Appendix A for a table listing each register in this section and its page number.

Device ID High Register (CR2D)

Read Only Address: 3?5H, Index 2DH
Power-On Default: 88H

This register should contain the same value as the upper byte of the PCI Device ID (Index 02H) register.

7	6	5	4	3	2	1	0
CHIP ID HIGH							

Bits 7–0 CHIP ID HIGH

value = 88H (hardwired)

Device ID Low Register (CR2E)

Read Only Address: 3?5H, Index 2EH
Power-On Default: 11H

7	6	5	4	3	2	1	0
CHIP ID LOW							

Bits 7–0 CHIP ID LOW

value = 11H (hardwired)

Revision Register (CR2F)

Read Only Address: 3?5H, Index 2FH
Power-On Default: 4xH

7	6	5	4	3	2	1	0
REVISION LEVEL							

Bits 7–0 REVISION LEVEL

The Trio64V+ is differentiated from the Trio64 by a 4 or 5 in the upper nibble of this register. The “x” in the lower nibble will change with each revision of the chip.

Chip ID/REV Register (CHIP-ID/REV) (CR30)

Read Only Address: 3?5H, Index 30H
Power-On Default: E1H

Should use CR2D, CR2E and CR2F for chip ID information.

7	6	5	4	3	2	1	0
CHIP ID				REVISION STATUS			

Bits 7–0 CHIP ID AND REVISION STATUS

value = E1H (hardwired)

Memory Configuration Register (MEM_CNFG) (CR31)

Read/Write Address: 3?5H, Index 31H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	HST DFF	OLD-DSAD 17	16	ENH MAP	VGA 16B	SCRN 2.PG	CPUA BASE

Bit 0 CPUA BASE - Enable Base Address Offset
0 = Address offset bits 3-0 of CR35 and bits 3-2 of CR51 or the new address offset bits (5-0 of CR6A) are disabled
1 = Address offset bits 3-0 CR35 and bits 3-2 of CR51 or the new address offset bits (5-0 of CR6A) are enabled for specifying the 64K page of display memory. Bits 5-0 of CR6A are used if this field contains a non-zero value. This allows access to up to 4 MBytes of display memory through a 64K window. (2 MBytes for the Trio32)

Bit 1 SCRN 2.PG - Enable Two-Page Screen Image
0 = Normal Mode
1 = Enable 2K x 1K x 4 map image screen for 1024 × 768 or 800 x 600 screen resolution, or 2K x 512 x 8 map image screen for 640 x 480 screen resolution

Bit 2 VGA 16B - Enable VGA 16-bit Memory Bus Width
0 = 8-bit memory bus operation
1 = Enable 16-bit bus VGA memory read/writes

This is useful in VGA text modes when VGA graphics controller functions are typically not used.

Bit 3 ENH MAP - Use Enhanced Mode Memory Mapping
0 = Force IBM VGA mapping for memory accesses
1 = Force Enhanced Mode mappings

Setting this bit to 1 overrides the settings of bit 6 of CR14 and bit 3 of CR17 and causes the use of doubleword memory addressing mode. Also, the function of bits 3-2 of GR6 is overridden with a fixed 64K map at A0000H.

Bits 5–4 OLD-DSAD 17, 16 - Old Display Start Address Bits 17-16
Bits 17-16 of start address (CRC, CRD) and cursor location (CRE, CRF)

Bits 1-0 of the Extended System Control 2 register (CR51) are bits 19-18 of the address and enable access to up to 4 MBytes of display memory. If a value is programmed into bits 3-0 of the Extended System Control 3 register (CR69), this value becomes the upper 4 bits of the display start base address and bits 5-4 of CR31 and bits 1-0 of CR51 are ignored. The Trio32 only supports 2 MBytes, so the upper bit is not used.

Bit 6 HST DFF - Enable High Speed Text Display Font Fetch Mode
0 = Normal font access mode
1 = Enable high speed text display

Setting this bit to 1 is only required for DCLK rates greater than 40 MHz. See bit 5 of CR3A.

Bit 7 Reserved

Backward Compatibility 1 Register (BKWD_1) (CR32)

Read/Write Address: 3?5H, Index 32H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	VGA FXPG	R	INT EN	R	R	R	R

Bits 3–0 Reserved

Bit 4 INT EN -Interrupt Enable
0 = All interrupt generation disabled
1 = Interrupt generation enabled

Bit 5 Reserved

Bit 6 VGA FXPG - Use Standard VGA Memory Wrapping
0 = Memory accesses extending past a 256K boundary do not wrap
1 = Memory accesses extending past a 256K boundary wrap at the boundary

The standard 256K VGA memory page always ends on a natural 256K boundary and accesses beyond this boundary will wrap. If the starting address is moved via bits 4-0 of CR69 (or bits 5-4 of CR31 and bits 1-0 of CR51), the 256K page may not end on a 256K boundary and accesses past the boundary will not wrap. This is the case when this bit is cleared to 0. For standard VGA compatibility when the page base address is moved, this bit is set to 1 to cause wrapping at a 256K boundary.

Bit 7 Reserved

Backward Compatibility 2 Register (BKWD_2) (CR33)

Read/Write Address: 3?5H, Index 33H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	LOCK PLTW	BDR SEL	LOCK DACW	VCLK= -DCK	R	DIS VDE	R

Bit 0 Reserved

Bit 1 DIS VDE - Disable Vertical Display End Extension Bits Write Protection
0 = VDE protection enabled
1 = Disables the write protect setting of the bit 7 of CR11 on bits 1 and 6 of CR7

Bit 2 Reserved

Bit 3 VCLK = -DCK - VCLK is Inverted DCLK
0 = VCLK is the external VCLK (pass-through feature connector clock input enabled) or is divided by 2 for 4 bits/pixel modes (see bit 6 of AR10 or bit 4 of CR3A) or is the internal DCLK (if neither of the first two cases apply)
1 = VCLK is forced to inverted DCLK

Bit 4 LOCK DACW - Lock RAMDAC Writes
0 = Enable writes to RAMDAC registers
1 = Disable writes to RAMDAC registers

Bit 5 BDR SEL - Blank/Border Select
0 = $\overline{\text{BLANK}}$ active time is defined by CR2 and CR3
1 = $\overline{\text{BLANK}}$ is active during entire display inactive period (no border)

Bit 6 LOCK PLTW - Lock Palette/Border Color Registers
0 = Unlock Palette/Border Color registers
1 = Lock Palette/Border Color registers

Bit 7 Reserved

Backward Compatibility 3 Register (BKWD_3) (CR34)

Read/Write Address: 3?5H, Index 34H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	ENB SFF	R	PCI RET	PCI ABT	PCI SNP

Bit 0 PCI SNP - PCI DAC snoop method
0 = Handling of PCI master aborts and retries during DAC cycles controlled by bits 1 and 2 of this register
1 = PCI master aborts and retries are not handled during DAC cycles

Bit 1 PCI ABT - PCI master aborts during DAC cycles
0 = PCI master aborts handled during DAC cycles
1 = PCI master aborts not handled during DAC cycles

Bit 0 of this register must be cleared to 0 for this bit to be effective.

Bit 2 PCI RET - PCI retries during DAC cycles
0 = PCI retries handled during DAC cycles
1 = PCI retries not handled during DAC cycles

Bit 0 of this register must be cleared to 0 for this bit to be effective.

Bit 3 Reserved

Bit 4 ENB SFF - Enable Start Display FIFO Fetch Register
0 = Start Display FIFO Fetch register (CR3B) disabled
1 = Start Display FIFO Fetch register (CR3B) enabled

Bits 7–5 Reserved

CRT Register Lock Register (CRTR_LOCK) (CR35)

Read/Write Address: 3?5H, Index 35H
Power-On Default: 00H

7	6	5	4	3	2	1	0
		LOCK	LOCK	OLD-CPU-BASE-ADDRESS			
R	R	HTMG	VTMG	17	16	15	14

Bits 3–0 OLD-CPU-BASE-ADDRESS
CPU Base Address bits 17-14. These four bits define the CPU address base in 64 KByte units of display memory. These bits are added with CPU address bit 17 (MSB of video memory addressing) to bit 14 for display buffer accesses.

Bits 3-2 of the Extended System Control 2 register (CR51) are bits 19-18 of the address and enable access to up to 4 MBytes of display memory. If a value is programmed into bits 5-0 of the Extended System Control 4 register (CR6A), this value becomes the upper 6 bits of the CPU base address and bits 3-0 of CR35 and bits 3-2 of CR51 are ignored. The Trio32 only supports 2 MBytes, so the upper bit is not used.

Bit 4 LOCK VTMG - Lock Vertical Timing Registers
0 = Vertical timing registers are unlocked
1 = The following vertical timing registers are locked:

CR6
CR7 (bits 7,5,3,2,0)
CR9 (bit 5)
CR10
CR11 (bits 3-0)
CR15
CR16

CR6, CR7 registers are also locked by bit 7 of the Vertical Retrace End register (CR11).

Bit 5 LOCK HTMG - Lock Horizontal Timing Registers
0 = Horizontal timing registers are unlocked
1 = The following horizontal timing registers are locked:

CR00
CR1
CR2
CR3
CR4
CR5
CR17 (bit 2)

All these registers (except bit 2 of CR17) are also locked by bit 7 of the Vertical Retrace End register (CR11).

Bit 7-6 Reserved

Configuration 1 Register (CONFG_REG1) (CR36)

Read/Write* Address: 3?5H, Index 36H
Power-On Default: Depends on Strapping

* Bits 1-0 are read only. The other bits can be written only after 0A5H is written to CR39.

This register samples the reset state from PD bus pins [7:0]. Other configuration strapping bits are found in CR37, CR68 and CR6F.

7	6	5	4	3	2	1	0
MEM SIZE			EVB	MEM MODE		SYS BUS	

Bits 1–0 SYS BUS - System Bus Select
00 = Reserved
01 = VESA local bus
10 = PCI local bus
11 = Reserved

Bits 3-2 MEM MODE - Memory Mode Select
00 = 1-cycle Extended Data Out (EDO) mode
01 = Reserved
10 = 2-cycle Extended Data Out (EDO) mode
11 = fast page mode

Bit 4 EVB - Enable Video BIOS (VL-Bus only)
0 = Disable video BIOS accesses
1 = Enable video BIOS accesses

Bit 7-5 MEM SIZE - Memory Size
000 = 4 MBytes
100 = 2 MBytes
110 = 1 MByte

All other values are reserved.

Configuration 2 Register (CONFG_REG2) (CR37)

Read/Write* Address: 3?5H, Index 37H
Power-On Default: Depends on Strapping

* These bits can be written only after 0A5H is written to CR39.

This register samples the reset state from PD bus pins [15:8]. Other configuration strapping bits are found in CR36 and CR68 and CR6F.

7	6	5	4	3	2	1	0
R	R	R	DACS	CS	VBS	R	ETV

Bits 0 ETV - Enable Trio64V+ (VL-Bus only)
0 = Trio64V+ disabled except for video BIOS accesses
1 = Trio64V+ enabled

Bit 1 Reserved

Bit 2 VBS - Video BIOS Size (VL-Bus only)
0 = 64 KByte BIOS ROM
1 = 32 KByte BIOS ROM

Bit 3 CS - Clock Select
0 = Use external DCLK and MCLK (test purposes only)
1 = Use internal DCLK and MCLK

Bit 4 DACS - RAMDAC Write Snooping (VL-Bus only)
0 = Disable LOCA/SRDY for RAMDAC writes
1 = Enable LOCA/SRDY for RAMDAC writes

Bits 7-5 Reserved

Register Lock 1 Register (REG_LOCK1) (CR38)

Read/Write Address: 3?5H, Index 38H
Power-On Default: 00H

Loading 01xx10xx (e.g., 48H) into this register unlocks the S3 VGA register set for read/writes. (x = don't care)

7	6	5	4	3	2	1	0
= 0	= 1			= 1	= 0		

Register Lock 2 Register (REG_LOCK2) (CR39)

Read/Write Address: 3?5H, Index 39H
Power-On Default: 00H

Loading 101xxxxx (e.g., A0H) unlocks the system control and system extension registers for reading/writing (x = don't care). Loading A5H allows bits 7-2 of CR36, bits 7-0 of CR37, bits 7-0 of CR68 and bits 7-0 of 6F to be written.

7	6	5	4	3	2	1	0
= 1	= 0	= 1					

Miscellaneous 1 Register (MISC_1) (CR3A)

Read/Write Address: 3?5H, Index 3AH
Power-On Default: 00H

7	6	5	4	3	2	1	0
PCIRB DISA	R	HST DFW	ENH 256	TOP MEM	ENB RFC	REF-CNT 1	REF-CNT 0

Bits 1–0 REF-CNT - Alternate Refresh Count Control
00 = Refresh Count 0
01 = Refresh Count 1
10 = Refresh Count 2
11 = Refresh Count 3

If enabled by setting bit 2 of this register to 1, these bits override the refresh count in bit 6 of CR11 and specify the number of refresh cycles per horizontal line.

Bit 2 ENB RFC - Enable Alternate Refresh Count Control
0 = Alternate refresh count control (bits 1-0) is disabled
1 = Alternate refresh count control (bits 1-0) is enabled

Bit 3 TOP MEM - Enable Top of Memory Access
0 = Top of memory access disabled
1 = Simultaneous VGA text and Enhanced modes are enabled. CPU and CRTC accesses are then directed to the top 32- or 64-KByte area of display memory depending on whether address bit 13 is 0 or 1 respectively.

Bit 4 ENH 256 - Enable 8 Bits/Pixel or Greater Color Enhanced Mode
0 = Attribute controller shift registers configured for 4-bit modes
1 = Attribute controller shift register configured for 8-, 16- and 24/32-bit color Enhanced modes

Bit 5 HST DFW - Enable High Speed Text Font Writing
0 = Disable high speed text font writing
1 = Enable high speed text font writing

Setting this bit to 1 is only required for DCLK rates greater than 40 MHz. See bit 6 of CR31.

Bit 6 Reserved

Bit 7 PCIRB DISA - PCI Read Bursts Disabled
0 = PCI read burst cycles enabled
1 = PCI read burst cycles disabled

Note: Bit 7 of CR66 must be set to 1 before this bit is set to 1.

Start Display FIFO Register (DT_EX_POS) (CR3B)

Read/Write Address: 3?5H, Index 3BH
Power-On Default: 00H

This value must lie in the horizontal blanking period and is typically 5 less than the value programmed in CR0. This parameter helps to ensure that adequate time is available during horizontal blanking for activities such as RAM refresh that require control of the display memory. Bit 9 of this value is bit 6 of CR5D. This register must be enabled by setting bit 4 of CR34 to 1. When the Streams Processor is enabled, FIFO fetching starts ar a fixed point based on a internal signal and this register is not effective.

7	6	5	4	3	2	1	0
START DISPLAY FIFO FETCH							

Bits 7–0 START DISPLAY FIFO FETCH

9-bit value = the time in character clocks from the active display start until the restart of fetching of FIFO data after the start of horizontal blanking. This register contains the low-order 8 bits of this value.

Interlace Retrace Start Register (IL_RTSTART) (CR3C)

Read/Write Address: 3?5H, Index 3CH
Power-On Default: 00H

This value allows determination of the even/odd row active display starting positions when operating in an interlaced mode. This register is enabled by bit 5 of CR42.

7	6	5	4	3	2	1	0
INTERLACE RETRACE START POSITION							

Bits 7–0 INTERLACE RETRACE START POSITION

value = offset in terms of character clocks for Interlaced mode start/end in even/odd frames.

Section 18: System Control Register Descriptions

System Control registers are configuration registers, mode control registers, and hardware graphics cursor control registers. They are positioned in the same indexed register space as VGA S3 registers. All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, the Register Lock 2 register (CR39) must be loaded with a key pattern (see the register description). The registers will remain unlocked until the key pattern is reset by changing a significant bit.

In the following register descriptions, 'R' stands for reserved (write = 0, read = undefined). See Appendix A for a table listing each of the registers in this section and its page number.

System Configuration Register (SYS_CNFG) (CR40)

Read/Write Address: 3?5H, Index 40H
Power-On Default: 30H

7	6	5	4	3	2	1	0
=0	=0	WDL DLAY	RDY CTL	R	R	R	EN ENH

Bit 0 EN ENH - Enable Enhanced Register Access
0 = Enhanced register access disabled
1 = Enhanced register (x2E8H) access enabled

Bits 3–1 Reserved

Bits 4 RDY CTL- Ready Control (VL-Bus only)
0 = Minimum 0 wait state delay from $\overline{\text{SADS}}$ asserted to assertion of $\overline{\text{SRDY}}$. Address latching occurs during the T1 cycle.
1 = Minimum 1 wait state delay from $\overline{\text{SADS}}$ asserted to assertion of $\overline{\text{SRDY}}$ (Default) With this setting, bit 3 of CR58 determines when the address is latched.

Bit 5 Reserved = 1 (Default)

Bits 7–6 Reserved = 00b

BIOS Flag Register (BIOS_FLAG) (CR41)

Read/Write Address: 3?5H, Index 41H
Power-On Default: 00H

7	6	5	4	3	2	1	0
BIOS-FLAG-REGISTER-1							

Bits 7–0 BIOS-FLAG-REGISTER-1
Used by the video BIOS.

Mode Control Register (MODE_CTL) (CR42)

Read/Write Address: 3?5H, Index 42H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	INTL MODE	R	R	R	R	R

Bits 4–0 Reserved

Bit 5 INTL MODE - Interlaced Mode
0 = Noninterlaced
1 = Interlaced

This bit enables the function of CR3C.

Bits 7–6 Reserved

Extended Mode Register (EXT_MODE) (CR43)

Read/Write Address: 3?5H, Index 43H
Power-On Default: 00H

7	6	5	4	3	2	1	0
HCTR X2	R	R	R	R	OLD LSW8	R	R

Bits 1–0 Reserved

Bit 2 OLD LSW8 - Logical Screen Width Bit 8
This is an extension of the Offset (Screen Width) register (CR13). This is disabled if bits 5-4 of the Extended System Control 2 register (CR51) are not 00b.

Bits 6–3 Reserved

Bit 7 HCTR X2 - Horizontal Counter Double Mode
0 = Disable horizontal counter double mode
1 = Enable horizontal counter double mode (horizontal CRT parameters are doubled)

Hardware Graphics Cursor Mode Register (HGC_MODE) (CR45)

Read/Write Address: 3?5H, Index 45H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	HWGC 1280	R	R	R	HWGC ENB

Bit 0 HWGC ENB - Hardware Graphics Cursor Enable
0 = Hardware graphics cursor disabled in any mode
1 = Hardware graphics cursor enabled in Enhanced mode

Bits 3-1 Reserved

Bit 4 HWGC 1280 - Hardware Cursor Right Storage
0 = Function disabled
1 = For 4 bits/pixel, the last 256 bytes in each 1-KByte line of the hardware cursor start address become the hardware graphics cursor storage area. For 8 bits/pixel, the last 512 bytes in each 2-KByte line of the hardware cursor start address become the hardware graphics cursor storage area. In either case, bits 1-0 of CR4D must be 11b.

Bits 7–5 Reserved

Hardware Graphics Cursor Origin-X Registers (HWGC_ ORGX(H)(L)) (CR46, CR47)

Read/Write Address: 3?5H, Index 46H, 47H
Power-On Default: 0000H

The high order three bits are written into CR46 and the low order byte is written into CR47.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	HWGC ORG X (H)			HWGC ORG X (L)							

Bits 10–0 HWGC ORG X(H) (L) - X-Coordinate of Cursor Left Side

Bits 15–11 Reserved

Hardware Graphics Cursor Origin-Y Registers (HWGC_ORGY(H)(L)) (CR48, CR49)

Read/Write Address: 3?5H, Index 48H, 49H
Power-On Default: Undefined

The high order three bits are written into CR48 and the low order byte is written into CR49.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	HWGC ORG Y (H)			HWGC ORG Y (L)							

Bits 10–0 HWGC ORG Y (H)(L) - Y-Coordinate of Cursor Upper Line
The cursor X, Y position is registered upon writing HWGC ORG Y (H).

Bits 15–11 Reserved

Hardware Graphics Cursor Foreground Color Stack Register (HWGC_FGSTK) (CR4A)

Read/Write Address: 3?5H, Index 4AH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TRUE COLOR FOREGROUND STACK (0-2)							

Bits 7–0 TRUE COLOR FOREGROUND STACK (0-2)

Three foreground color registers are stacked at this address. The stack pointer (common with CR4B) is reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). Each write to this register (CR4A) increments the stack pointer by 1, so three writes provide 24 bits of true color information.

Hardware Graphics Cursor Background Color Stack Register (HWGC_BGSTK) (CR4B)

Read/Write Address: 3?5H, Index 4BH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TRUE COLOR BACKGROUND STACK (0-2)							

Bits 7–0 TRUE COLOR BACKGROUND STACK (0-2)

Three background color registers are stacked at this address. The stack pointer (common with CR4A) is reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). Each write to this register (CR4B) increments the stack pointer by 1, so three writes provide 24 bits of true color information.

Hardware Graphics Cursor Storage Start Address Registers (HWGC_STA(H)(L) (CR4C, CR4D)

Read/Write Address: 3?5H, Index 4CH, 4DH
Power-On Default: Undefined

The high order four bits are written into CR4C and the low order byte is written into CR4D.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	HWGC STA(H)				HWGC STA(L)							

Bits 11–0 HWGC STA(H)(L) - Hardware Graphics Cursor Storage Start Address

Bits 15–12 Reserved

Hardware Graphics Cursor Pattern Display Start X-PXL-Position Register (HWGC_DX) (CR4E)

Read/Write Address: 3?5H, Index 4EH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HWGC PAT DISP START X-POS					

Bits 5–0 HWGC PAT DISP START X-POS - HWGC Pattern Display Start-X Pixel Position

This value is the offset (in pixels) from the left side of the 64x64 cursor pixel pattern from which the cursor is displayed. This allows a partial cursor to be displayed at the left border of the display.

Bits 7–6 Reserved

Hardware Graphics Cursor Pattern Disp Start Y-PXL-Position Register (HGC_DY) (CR4F)

Read/Write Address: 3?5H, Index 4FH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HWGC PAT DISP START Y-POS					

Bits 5–0 HWGC PAT DISP START Y-POS - HWGC Pattern Display Start-Y Pixel Position

This value is the offset (in pixels) from the top of the 64x64 cursor pixel pattern from which the cursor is displayed. This allows a partial cursor to be displayed at the top of the display.

Bits 7–6 Reserved

Section 19: System Extension Register Descriptions

These registers provide extended system and memory control, external sync control and addressing window control. They are enabled in the same way as the System Control registers via the Register Lock 2 register (CR39).

In the following register descriptions, 'R' stands for reserved (write = 0, read = undefined). See Appendix A for a table listing each of the registers in this section and its page number.

Extended System Cont 1 Register (EX_SCTL_1) (CR50)

Read/Write Address: 3?5H, Index 50H
Power-On Default: 00H

7	6	5	4	3	2	1	0
GE-SCR-W 1	0	PXL-LNGH 1	0	R	R	R	GESW 2

Bit 0 Extension bit 2 of the screen width definition. See bits 7-6 below.

Bits 3-1 Reserved

Bits 5–4 PXL-LNGH - Pixel Length Select
00 = 1 byte (Default). This corresponds to a pixel length of 4 or 8 bits/pixel in bit 7 of the Subsystem Status register (42E8H)
01 = 2 bytes. 16 bits/pixel
10 = Reserved
11 = 4 bytes. 32 bits/pixel

These bits select the pixel length for Enhanced mode command execution through the Graphics Engine.

Bits 7–6 GE-SCR-W - Graphics Engine Command Screen Pixel Width
Bit 0 of this register is the most significant bit of this definition.
000 = 1024 (or 2048 if bit 1 of CR31 =1) (Default)
001 = 640
010 = 800 (or 1600x1200x4 if bit 2 of 4AE8H = 0)
011 = 1280
100 = 1152
101 = Reserved
110 = 1600
111 = Reserved

Extended System Control 2 Register (EX_SCTL_2) (CR51)

Read/Write Address: 3?5H, Index 51H
Power-On Default: 00H

7	6	5	4	3	2	1	0
		LOG-SCR-W		OLD-CBAD		OLD-DSAD	
R	R	9	8	19	18	19	18

Bits 1–0 OLD-DSAD - Old Display Start Address Bits 19-18
These are extension bits of Memory Configuration register (CR31) bits 5-4 (Display Start Base Address). If the upper 4 display start address bits are programmed into bits 3-0 of CR69, these bits and bits 5-4 of CR31 are ignored.

Bits 3–2 OLD-CBAD - Old CPU Base Address Bits 19-18
These are extension bits of CRT Register Lock register (CR35) bits 3-0 (CPU Base Address). They becomes bits 19-18 of the CPU base address, enabling access to up to 4 MBytes of display memory. If the upper 6 CPU base address bits are programmed into bits 5-0 of CR6A, these bits and bits 3-0 of CR35 are ignored.

Bits 5–4 LOG-SCR-W - Logical Screen Width Bits 9-8
These are two extension bits of the Offset register (CR13). If the value of these bits is not 00b, bit 2 of the Extended Mode register (CR43) is disabled.

Bits 7–6 Reserved

Extended BIOS Flag 1 Register (EXT_BBFLG1) (CR52)

Read/Write Address: 3?5H, Index 52H
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-1							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-1

See the S3 video BIOS documentation for the coding of this register. Note that this coding is different from that used with previous S3 accelerators.

Extended Memory Control 1 Register (EX_MCTL_1) (CR53)

Read/Write Address: 3?5H, Index 53H
Power-On Default: See Bit Descriptions

7	6	5	4	3	2	1	0
R	SWP NBL	MMIO WIN	MMIO SELECT		BIG ENDIAN LIN ADDR		R

Bit 0 Reserved

Bits 2-1 BIG ENDIAN LIN ADDR - Big Endian Data Byte swap (linear addressing only)
00 = No swap (Default)
01 = Swap bytes within each word
10 = Swap all bytes in doublewords (bytes reversed)
11 = Reserved

Bits 4-3 MMIO SELECT
00 = Disable MMIO (Default for VL-Bus)
01 = New MMIO (relocatable) enabled (Default for PCI)
10 = Trio64-type MMIO enabled at window selected by bit 5 of this register
11 = Trio64-type MMIO and new MMIO enabled

Refer to the MMIO explanation in Section 15 for more information.

Bit 5 MMIO WIN - Trio64-type MMIO Window
0 = Trio64-type MMIO window enabled at A8000H - AFFFFH. A0000H - A7FFF available for image transfers (Default)
1 = Trio64-type MMIO window enabled at B8000H - BFFFFH. A0000H - B7FFFH are not used (no image transfer area)

Bits 4-3 of this register must be programmed to 10b for this bit to be effective.

Bit 6 SWP NBL - Swap Nibbles
0 = No nibble swap (Default)
1 = Swap nibbles in each byte of a linear memory address read or write operation

Bit 7 Reserved

Extended Memory Control 2 Register (EX_MCTL_2) (CR54)

Read/Write Address: 3?5H, Index 54H
Power-On Default: 00H

7	6	5	4	3	2	1	0
M PARAMETER					R	BIG ENDIAN	

Bits 1–0 BIG ENDIAN - Big Endian Data Byte Swap (not linear addressing or image writes)
00 = No swap (Default)
01 = Swap bytes within each word
10 = Swap all bytes in doublewords (bytes reversed)
11 = Swap according to $\overline{BE[3:0]}$ (VL-Bus) or $\overline{C/BE[3:0]}$ (PCI)

Byte enable settings for a bit setting of 11b:
0000 = Swap all bytes in doublewords (bytes reversed)
0011 = Swap bytes within selected word
1100 = Swap bytes within selected word
All other values = no swap

Bits 2, 7–3 M PARAMETER
6-bit Value = maximum number of MCLKs that the LPB, CPU and Graphics Engine can use to access memory before giving up control of the memory bus. See Section 7.5 for more information. Bit 2 is the high order bit of this value.

Extended RAMDAC Control Register (EX_DAC_CT) (CR55)

Read/Write Address: 3?5H, Index 55H
Power-On Default: 00H

7	6	5	4	3	2	1	0
TOFF VCLK	R	R	MS /X11	R	ENB GIR	R	R

Bits 1–0 Reserved

Bit 2 ENB GIR - Enable General Input Port Read
0 = RAMDAC reads enabled
1 = General Input Port read enabled

When this bit is set to 1, the $\overline{\text{STRD}}$ strobe for reading General Input Port data is generated when 3C8H is read. The data is transmitted via GD[7:0] to AD[7:0] for PCI configurations and directly to SD[7:0] for VL-Bus configurations.

Bit 3 Reserved

Bit 4 MS/X11 - Hardware Cursor MS/X11 Mode
0 = MS-Windows mode (Default)
1 = X11-Windows mode

This bit select the type of decoding used for the 64x64x2 storage array of the hardware graphics cursor. See the Programming the Hardware Cursor section for a description of the decoding.

Bits 6–5 Reserved

Bit 7 TOFF VCLK - Tri-State Off VCLK Output
0 = Normal operation
1 = VCLK output is tri-stated off

External Sync Control 1 Register (EX_SYNC_1) (CR56)

Read/Write Address: 3?5H, Index 56H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	DIS VSYN	DIS HSYN	R

Bit 0 Reserved

Bit 1 DIS HSYN - Tri-state off HSYNC
0 = HSYNC output buffer tri-stated on
1 = HSYNC output buffer tri-stated off

Bit 2 DIS VSYN - Tri-state off VSYNC
0 = VSYNC output buffer tri-stated on
1 = VSYNC output buffer tri-stated off

Bits 7–3 Reserved

Linear Address Window Control Register (LAW_CTL) (CR58)

Read/Write Address: 3?5H, Index 58H
Power-On Default: See the bit descriptions.

7	6	5	4	3	2	1	0
RAS PRE	R	R	ENB LA	LAT DEL	R	LAW-SIZE 1	LAW-SIZE 0

Bits 1–0 LAW-SIZE - Linear Address Window Size
00 = 64 KBytes (Default)
01 = 1 MByte
10 = 2 MBytes
11 = 4 MBytes

The 64K window is not available if new MMIO is enabled (CR53_3 = 1).

Bit 2 Reserved

Bit 3 LAT DEL - Address Latch Delay Control (VL-Bus only)
0 = Address latching is delayed one clock (T2 cycle) (Default)
1 = Address latching occurs in the T1 cycle

This bit is effective only when one decode wait state is selected by setting bit 4 of CR40 to 1.

Bit 4 ENB LA - Enable Linear Addressing
0 = Disable linear addressing (Default for VL-Bus)
1 = Enable linear addressing (Default for PCI Bus)

Enabling linear addressing disables access to the A000H-AFFFH region unless banking is enabled via bit 0 of CR31, the window size is set to 64K via bits 1-0 of this register and A000H is specified as the base in CR59-5A.

Bits 6–5 Reserved

Bit 7 RAS PRE - RAS Pre-charge Time Adjust
0 = $\overline{\text{RAS}}$ pre-charge (high) time is defined by CR68_3 or MM81EC_16 (Default)
1 = $\overline{\text{RAS}}$ pre-charge (high) time is decreased by 0.5 MCLKs over that specified by CR68_3 and the corresponding $\overline{\text{RAS}}$ low time (CR68_2) is increased by 0.5 MCLKs. This leaves the total cycle time unchanged.

Linear Address Window Position Registers (LAW_POS(X) (CR59-5A)

Read/Write Address: 3?5H, Index 59H-5AH
Power-On Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINEAR-ADDRESS-WINDOW-POSITION															

CR59 contains the upper byte (15-8) and CR5A contains the lower byte (7-0). These registers specify system address bits 31-16 of the Linear Address Window Position in 32-bit CPU address space. The Linear Address Window resides on a 64KB, 1MB, 2MB or 4MB memory boundary (size-aligned boundary). Some LSBs of this register (illustrated by "xx..xx" in the following table) are ignored because of the size-aligned boundary scheme.

LAW Size	Linear Address Window Position Register Bit(s)									
64KB	31-25	24	23	22	21	20	19	18	17	16
1MB	31-25	24	23	22	21	20	xx	xx	xx	xx
2MB	31-25	24	23	22	21	xx	xx	xx	xx	xx
4MB	31-25	24	23	22	xx	xx	xx	xx	xx	xx

Bits 15–0 LINEAR-ADDRESS-WINDOW-POSITION - LA Window Position Bits 31-16
16-bit Value = the linear address window position in 32-bit CPU address space.

Bits 15-0 are common with bits 31-16 of the base address programmed into the PCI Base Address 0 register at address 10H-12H. Writes to these bits in either register will also be written to the other. Writes to CR59 and CR5A should be read-modify- writes that do not change the upper 6 bits, as these bits are written by the system BIOS to place the Trio64V+ in a unique address space. Note that system BIOS writes will leave bits 9-0 in an indeterminate state, so these should be properly initialized before linear addressing is enabled.

If a 64K window is specified and bit 0 of CR31 is set to 1, bits 5-0 of CR6A specify the 64K page of display memory to be accessed through a 64K window located at the address specified in these registers.

If new MMIO is enabled (CR53_3 = 1), the address is specified by CR59_7-2 (or the high order 6 bits of the PCI Base Address 0 register). This is concatenated with the display memory address specified by the programmer.

General Output Port Register (GOUT_PORT) (CR5C)

Read/Write Address: 3?5H, Index 5CH
Power-On Default: 00H

7	6	5	4	3	2	1	0
GENERAL-OUT-PORT							

Bits 7–0 GENERAL-OUT-PORT

This register can be used in a variety of ways. See Section 12-4 for a complete description.

Extended Horizontal Overflow Register (EXT_H_OVF) (CR5D)

Read/Write Address: 3?5H, Index 5DH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	SFF 8	EHS 6	SHS 8	EHB 7	SHB 8	HDE 8	HT 8

Bit 0 HT 8 - Horizontal Total (CR0) Bit 8

Bit 1 HDE 8 - Horizontal Display End (CR1) Bit 8

Bit 2 SHB 8 - Start Horizontal Blank (CR2) Bit 8

Bit 3 EHB 7 - End Horizontal Blank (CR3) Bit 6

Bit 4 SHS 8 - Start Horizontal Sync Position (CR4) Bit 8

Bit 5 EHS 6 - End Horizontal Sync (CR5) Bit 6

Bit 6 SFF 8 - Start FIFO Fetch (CR3B) Bit 8

Bit 7 Reserved

Extended Vertical Overflow Register (EXT_V_OVF) (CR5E)

Read/Write Address: 3?5H, Index 5EH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	LCM 10	R	VRS 10	R	SVB 10	VDE 10	VT 10

Bit 0 VT 10 - Vertical Total (CR6) Bit 10

Bit 1 VDE 10 - Vertical Display End (CR12) Bit 10

Bit 2 SVB 10 - Start Vertical Blank (CR15) Bit 10

Bit 3 Reserved

Bit 4 VRS 10 - Vertical Retrace Start (CR10) Bit 10

Bit 5 Reserved

Bit 6 LCM 10 - Line Compare Position (CR18) Bit 10

Bit 7 Reserved

Extended Memory Control 3 Register (EXT-MCTL-3) (CR60)

Read/Write Address: 3?5H, Index 60H
Power-On Default: 00H

7	6	5	4	3	2	1	0
N(DISP-FETCH-PAGE)							

Bits 7-0 N(DISP-FETCH-PAGE) - N Parameter
Value = Number of MCLKs allocated to Streams Processor FIFO filling before control of the memory bus is relinquished. See Section 7.5 for more information.

Extended Memory Control 4 Register (EXT-MCTL-4) (CR61)

Read/Write Address: 3?5H, Index 61H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	BIG ENDIAN		R	R	R	R	R

Bits 4-0 Reserved

Bits 6-5 BIG ENDIAN - Big Endian Data Bye Swap (image writes only)
00 = No swap (Default)
01 = Swap bytes within each word
10 = Swap all bytes in doublewords (bytes reversed)
11 = Reserved

Bit 7 Reserved

Extended Miscellaneous Control Register (EXT-MISC-CTL) (CR65)

Read/Write Address: 3?5H, Index 65H
Power-On Default: 00H

7	6	5	4	3	2	1	0
			DLY BLANK				
R	R	R	1	0	R	R	R

Bits 2-0 Reserved

Bits 4-3 DLK BLANK - Delay $\overline{\text{BLANK}}$ by DCLK
00 = No delay of $\overline{\text{BLANK}}$
01 = Delay $\overline{\text{BLANK}}$ for 1 DCLK
10 = Delay $\overline{\text{BLANK}}$ for 2 DCLKs (required for color mode 12)
11 = Delay $\overline{\text{BLANK}}$ for 3 DCLKs

Bits 7-5 Reserved

Extended Miscellaneous Control 1 Register (EXT-MISC-1) (CR66)

Read/Write Address: 3?5H, Index 66H
Power-On Default: 00H

7	6	5	4	3	2	1	0
PCI DE	TOFF PADT	R	R	PCI DIS	R	SW RST	EN ENH

Bit 0 EN ENH - Enable Enhanced Functions
0 = Disable enhanced functions
1 = Enable enhanced functions

This bit is a duplicate of 4AE8_0. Writing to this location also update the bit value at the other location.

Bit 1 SW RST - Software Reset
0 = No function
1 = Software reset of the Graphics Engine

Setting this bit has the same function as setting 42E8H (write)_15-14 to 10b.

Bit 2 Reserved

Bit 3 PCI DIS - PCI Disconnect
0 = No effect
1 = An attempt to write data with the Command FIFO or LPB output FIFO full or to read data with the Command FIFO not empty generates a PCI bus disconnect cycle

Bit 7 of this register must also be set to 1 to enable this feature.

Bits 5-4 Reserved

Bit 6 TOFF PADT - Tri-State Off Pixel Address Bus
0 = Normal operation
1 = PA[15:0] are set to tri-state off

Bit 7 PCI DE - PCI bus disconnect enable
0 = PCI bus disconnect disabled
1 = PCI bus disconnect enabled

Setting this bit to 1 allows PCI burst cycles to be interrupted if AD[1:0] $\neq$ 00b or if the address during the burst goes outside the address ranges supported by the Trio64V+. See also bit 3 of this register.

Extended Miscellaneous Control 2 Register (EXT-MISC-2)(CR67)

Read/Write Address: 3?5H, Index 67H
Power-On Default: 00H

7	6	5	4	3	2	1	0
COLOR MODE							VCLK
3	2	1	0	R	R	R	PHS

Bit 0 VCLK PHS - VCLK Phase With Respect to DCLK
0 = VCLK is 180° out of phase with DCLK (inverted)
1 = VCLK is in phase with DCLK

Bit 1 Reserved

Bits 3–2 STREAMS MODE
00 = Streams Processor disabled
01 = Secondary stream overlaid on VGA mode background
10 = Reserved
11 = Full Streams Processor operation (primary and secondary streams from all supported sources)

The Streams Processor should only be enabled or disabled during the VSYNC period.

Bits 7–4 COLOR MODE - RAMDAC Color Mode
0000 = Mode 0: 8-bit color, 1 pixel/VCLK
0001 = Mode 8: 8-bit color, 2 pixels/VCLK
0011 = Mode 9: 15-bit color, 1 pixel/VCLK
0101 = Mode 10: 16-bit color, 1 pixel/VCLK
0111 = Mode 12: 640x480x24-bit color (packed), 1 pixel/3 DCLKs
1101 = Mode 13: 24-bit color, 1 pixel/VCLK

All other mode values are reserved.

Configuration 3 Register (CNFG-REG-3) (CR68)

Read/Write Address: 3?5H, Index 68H
Power-On Default: Depends on Strapping

This is one of the power-on strapping bits (along with CR36, CR37 and CR6F). PD[23:16] are sampled on power-on reset and their states are written to bits 7-0 of this register. A5H must be written to CR39 to provide read/write access to this register.

7	6	5	4	3	2	1	0
MDB	BIOS 3	BIOS 2	BIOS 1	RAS - PCG	RAS - LOW	CAS/OE STR	CAS/OE STR

Bits 1-0 $\overline{CAS}$,$\overline{OE}$ Stretch Time
00 = approximately 6.5 ns stretch (nominal)
01 = approximately 5 ns stretch (nominal)
10 = approximately 3.5 ns stretch (nominal)
11 = no stretch

This parameter adjusts the timing for the rising edges of the $\overline{CAS}$ and $\overline{OE}$ signals. This allows stretching of the signal active time for $\overline{CAS}$ and $\overline{OE}$ to allow more time for valid pixel data to be available. The delay time shown above is an approximation. It is affected by both process and signal loading and must be measured for each design.

Bit 2 $\overline{RAS}$-LOW - $\overline{RAS}$ Low Timing Select
0 = 4.5 MCLKs
1 = 3.5 MCLKs

This parameter specifies the length of the $\overline{RAS}$ active time for a single row/column access. $\overline{RAS}$ may be held low longer to accommodate additional page mode accesses to the same row.

Bit 3 $\overline{RAS}$-PCG - $\overline{RAS}$ Precharge Timing Select
0 = 3.5 MCLKs
1 = 2.5 MCLKs

When $\overline{RAS}$ goes high to end a memory cycle, this parameter specifies the minimum period it must be held high before beginning another memory access cycle.

Bits 6-4 BIOS - Reserved for use by the video BIOS.

Bit 7 MDB - Memory Data Bus Size
0 = Memory data bus is 32 bits
1 = Memory data bus is 32 bits (1 MByte of memory) or 64 bits (2 or 4 MBytes of memory)

Extended System Control 3 Register (EXT-SCTL-3)(CR69)

Read/Write Address: 3?5H, Index 69H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	DISPLAY-START-ADDRESS			

Bits 3–0 DISPLAY-START-ADDRESS
This field contains the upper 4 bits (19-16) of the display start address, allowing addressing of up to 4 MBytes of display memory. When a non-zero value is programmed in this field, bits 5-4 of CR31 and 1-0 of CR51 (the old display start address bits) are ignored.

Bits 7–4 Reserved

Extended System Control 4 Register (EXT-SCTL-4)(CR6A)

Read/Write Address: 3?5H, Index 6AH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	CPU-BASE-ADDRESS					

Bits 5–0 CPU-BASE-ADDRESS
This field contains the upper 6 bits (19-14) of the CPU base address, allowing accessing of up to 4 MBytes of display memory via 64K pages. When a non-zero value is programmed in this field, bits 3-0 of CR35 and 3-2 of CR51 (the old CPU base address bits) are ignored. Bit 0 of CR31 must be set to 1 to enable this field. If linear addressing is enabled and a 64 KByte window is specified, these bits specify the 64K page to be accessed at the base address specified in CR59 and CR5A. Otherwise, the base address is normally at A000H.

Bits 7–6 Reserved

Extended BIOS Flag 3 Register (EBIOS-FLG3)(CR6B)

Read/Write Address: 3?5H, Index 6BH
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-3							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-3
This register is reserved for use by the S3 BIOS.

Extended BIOS Flag 4 Register (EBIOS-FLG4)(CR6C)

Read/Write Address: 3?5H, Index 6CH
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-4							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-4
This register is reserved for use by the S3 BIOS.

Extended BIOS Flag 5 Register (CR6D)

Read/Write Address: 3?5H, Index 6DH
Power-On Default: 00H

This register is reserved for use by the BIOS.

7	6	5	4	3	2	1	0
RESERVED							

Bits 7–0 Reserved

Extended BIOS Flag 6 Register (CR6E)

Read/Write Address: 3?5H, Index 6EH
Power-On Default: 00H

This register is reserved for use by the BIOS.

7	6	5	4	3	2	1	0
RESERVED							

Bits 7–0 Reserved

Configuration 4 Register (CR6F)

See description Address: 3?5H, Index 6FH
Power-On Default: Depends on Strapping

This is the fourth byte of power-on strapping bits. PD[28:24] are sampled at reset and the values are written to bits 4-0 of this register. A5H must be written to CR39 to provide read/write access to this register. This register will power up with a value of 1FH if any of PD[28:24] are not pulled low.

7	6	5	4	3	2	1	0
R	R	R	WE DELAY		IOEN	IOSEL	MODE

Bit 0 MODE - Trio64 Compatible Mode Select
0 = The Trio64V+ is configured for LPB mode
1 = The Trio64V+ is configured for Trio64-compatible mode

Bit 1 IOSEL - Serial Port I/O Address Select (read/write)
0 = MMFF20 is accessed at I/O address 000E8H
1 = MMFF20 is accessed at I/O address 000E2H

Bit 2 of this register must be cleared to 0 for this bit to have effect.

Bit 2 IOEN - Serial Port Address Type Select (read/write)
0 = MMFF20 is accessed at the I/O port defined in bit 1 of this register or at its MMIO address
1 = MMFF20 is accessed at its MMIO address only (no I/O)

Enabling I/O access allows the serial port to be used for I^2C communications when the Trio64V+ is disabled.

Bits 4-3 WE Delay (read/write)
00 = 3 units delay
01 = 2 units delay
10 = 1 unit delay
11 = 0 units delay

Both the rising and falling edges of $\overline{WE}$ are delayed by the amount specified in these bits.

Bits 7-5 Reserved

Section 20: Enhanced Commands Register Descriptions

These registers support the Enhanced mode drawing commands. Access to these registers is enabled via bit 0 of the System Configuration register (CR40).

In the following register descriptions, 'R' stands for reserved (write = 0, read = undefined). See Appendix A for a table listing each of the registers in this section and its page number.

Subsystem Status Register (SUBSYS_STAT)

Read Only Address: 42E8H
Power-On Default: 0000H

This read-only register provides information on interrupt status, monitor I.D. and the number of bits per pixel. See the Subsystem Control (42E8H, Write Only) register for details on enabling and clearing interrupts.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	PXL LNG	R	R	R	FIFO EMP	FIFO OVF	GE BSY	VSY INT

Bit 0 VSY INT - Vertical Sync Interrupt Status
0 = No interrupt
1 = Interrupt generated if enabled

Bit 1 GE BSY - Graphics Engine Busy Interrupt Status
0 = No interrupt
1 = Interrupt generated if enabled

Bit 2 FIFO OVF - Command FIFO Overflow Interrupt Status
0 = No interrupt
1 = Interrupt generated if enabled

Bit 3 FIFO EMP - Command FIFO Empty Interrupt Status
0 = No interrupt
1 = Interrupt generated if enabled

Bits 4–6 Reserved

Bit 7 PXL LNG - Pixel Length (# of bit planes)
0 = 4-bit
1 = 8-bit

This reflects the number of bit planes when CR50_5-4 = 00b.

Bits 15-8 Reserved

Subsystem Control Register (SUBSYS_CNTL)

Write Only Address: 42E8H
Power-On Default: 0000H

This register allows each of several interrupt sources to be enabled or disabled. Interrupt status (Subsystem Status (42E8H, Read Only) can be cleared. This register also controls the software reset of the graphics engine.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GE-RST				FIFO-ENB		GE	VSY					FIFO	FIFO	GEB	VSY
1	0	R	R	EMP	OVF	BSY	ENB	R	R	R	R	CLE	CLO	CLR	CLR

Bit 0 VSY CLR - Clear Vertical Sync Interrupt Status
0 = No change
1 = Clear

Bit 1 GEB CLR - Clear Graphics Engine Busy Interrupt Status
0 = No change
1 = Clear

Bit 2 FIFO CLO - Clear Command FIFO Overflow Interrupt Status
0 = No change
1 = Clear

Bit 3 FIFO CLE - Clear Command FIFO Empty Interrupt Status
0 = No change
1 = Clear

Bits 7–4 Reserved

Bit 8 VSY ENB - Vertical Sync Interrupt Enable
0 = Disable
1 = Enable if CR32_4 = 1

Bit 9 GE BSY- Graphics Engine Busy Interrupt Enable
0 = Disable
1 = Enable if CR32_4 = 1

Bit 10 FIFO-ENB OVF - Command FIFO Overflow Interrupt Enable
0 = Disable
1 = Enable if CR32_4 = 1

Bit 11 FIFO-ENB EMP - Command FIFO Empty Interrupt Enable
0 = Disable
1 = Enable if CR32_4 = 1

Bits 13–12 Reserved

Bits 15–14 GE-RST - Graphics Engine Software Reset
00 = No change
01 = Graphics Engine enabled
10 = Reset
11 = Reserved

Advanced Function Control Register (ADVFUNC_CNTL)

Read/Write Address: 4AE8H
Power-On Default: 0000H

This register enables or disables the Enhanced display functions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	LA	R	ENH PL	R	ENB EHFC

Bit 0 ENB EHFC - Enable Enhanced Functions
0 = Enable VGA and VESA planar (4 bits/pixel) modes
1 = Enable all other modes (Enhanced and VESA non-planar)

Bit 1 Reserved

Bit 2 ENH PL - Enhanced mode pixel length
0 = 4 bits/pixel enhanced mode
1 = 8 or more bits/pixel enhanced mode

CR50_5-4 are used to differentiate between 8-, 16- and 32-bit pixel lengths.

Bit 3 Reserved

Bit 4 LA - Enable Linear Addressing
0 = Disable linear addressing
1 = Enable linear addressing

This bit is ORed with bit 4 of CR58 and is equivalent to it.

Bits 15–5 Reserved

Current Y-Position Register (CUR_Y)

Read/Write Address: 82E8H
Power-On Default: Undefined

For line draws (solid, textured, short stroke or polyline), rectangle draws and image transfers, writing to this register defines the vertical screen coordinate at which the first pixel will be drawn. For BitBLTs, this is the vertical coordinate for the upper left hand corner of the destination. For PatBLTs, this is the vertical coordinate of the upper left hand corner of the off-screen pattern. Reading this register produces the current vertical drawing coordinate.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	CURRENT Y-POSITION											

Bits 11–0 CURRENT Y-POSITION

Bits 15–12 Reserved

Current X-Position Register (CUR_X)

Read/Write Address: 86E8H
Power-On Default: Undefined

For line draws (solid, textured, short stroke or polyline), rectangle draws and image transfers, writing to this register defines the horizontal screen coordinate at which the first pixel will be drawn. For BitBLTs, this is the horizontal coordinate for the upper left hand corner of the destination. For PatBLTs, this is the horizontal coordinate of the upper left hand corner of the off-screen pattern. Reading this register produces the current horizontal drawing coordinate.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	CURRENT X-POSITION											

Bits 11–0 CURRENT X-POSITION

Bits 15–12 Reserved

Destination Y-Position/Axial Step Constant Register (DESTY_AXSTP)

Read/Write Address: 8AE8H
Power-On Default: Undefined

For BitBLTs and PatBLTs, this register defines the vertical position for the top of the destination rectangle. For solid and textured line draws, this is axial step constant used in the definition of the line.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	DESTINATION Y-POSITION											

Bits 11–0 DESTINATION Y-POSITION

Bits 15–12 Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LINE PARAMETER AXIAL STEP CONSTANT													

Axial Step Constant = 2 * (min(|dx|,|dy|)) In other words, when drawing a line from point A to point B, determine the change in the X coordinate from A to B and the change in the Y coordinate from A to B. Take the smaller of the two changes and multiply its absolute value by 2.

Bits 13–0 LINE PARAMETER AXIAL STEP CONSTANT

Bits 15–14 Reserved

Destination X-Position/Diagonal Step Constant Register (DESTX_DIASTP)

Read/Write Address: 8EE8H
Power-On Default: Undefined

For BitBLTs and PatBLTs, this register defines the horizontal position for the left side of the destination rectangle. For solid and textured line draws, this is diagonal step constant used in the definition of the line.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	DESTINATION X-POSITION											

Bits 11–0 DESTINATION X-POSITION

Bits 15–12 Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LINE PARAMETER DIAGONAL STEP CONSTANT													

Diagonal Step Constant = 2 * [min(|dx|,|dy|) - max(|dx|,|dy|)]. See the Destination Y-Position/Axial Step Constant (8AE8H) register for an explanation of the terms used in this equation.

Bits 13–0 LINE PARAMETER DIAGONAL STEP CONSTANT

Bits 15–14 Reserved

Line Error Term Register (ERR_TERM)

Read/Write Address: 92E8H
Power-On Default: Undefined

This register specifies the initial error term for solid and textured line draws.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LINE PARAMETER/ERROR TERM													

Error Term = 2 * min(|dx|,|dy|) - max(|dx|,|dy| - 1 if the starting X < the ending X
Error Term = 2 * min(|dx|,|dy|) - max(|dx|,|dy| if the starting X ≥ the ending X

See the Destination Y-Position/Axial Step Constant (8AE8H) register for an explanation of the terms used in these equations.

Bits 13–0 LINE PARAMETER/ERROR TERM

Bits 15–14 Reserved

Major Axis Pixel Count Register (MAJ_AXIS_PCNT)

Read/Write Address: 96E8H
Power-On Default: Undefined

This register specifies the length (in pixels) of the major (longest) axis for solid and textured lines and the width for rectangles, image transfers, BitBLTs and PatBLTs.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	RECTANGLE WIDTH/LINE PARAMETER MAX											

Bits 11–0 RECTANGLE WIDTH/LINE PARAMETER MAX
The value is the number of pixels along the major axis - 1.

Bits 15–12 Reserved

Graphics Processor Status Register (GP_STAT)

Read Only Address: 9AE8H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO-STATUS						HDW		FIFO-STATUS							
9	10	11	12	13	AE	BSY	R	1	2	3	4	5	6	7	8

Bits 7–0 FIFO-STATUS

In the following table, the leftmost column represents the value of FIFO status bit 1 (register bit 7). Each column to the right represents the value of the next higher FIFO status bit. A value of 0 read from any particular status bit position guarantees at least as many open FIFO slots as the number of that status bit. For example, if a 0 is read from status bit 6 (register bit 2), there are at least 6 open FIFO slots. Bits 15-11 provide the upper 5 FIFO status bits.

0000000000000 = 13 FIFO slots available
0000000000001 = 12 FIFO slots available
0000000000011 = 11 FIFO slots available
0000000000111 = 10 FIFO slots available
0000000001111 = 9 FIFO slots available
0000000011111 = 8 FIFO slots available
0000000111111 = 7 FIFO slots available
0000001111111 = 6 FIFO slots available
0000011111111 = 5 FIFO slots available
0000111111111 = 4 FIFO slots available
0001111111111 = 3 FIFO slots available
0011111111111 = 2 FIFO slots available
0111111111111 = 1 FIFO slots available
1111111111111 = 0 FIFO slots available

Bit 8 Reserved

Bit 9 HDW BSY - Hardware (Graphics Engine) Busy
0 = not busy
1 = busy - graphics command is executing

Bit 10 AE - All FIFO Slots Empty
0 = At least one FIFO slot is occupied
1 = All FIFO slots empty

Bits 15–11 FIFO-STATUS
These are the upper 5 bits of the FIFO status. See bits 7-0 for the interpretation.

Drawing Command Register (CMD)

Write Only Address: 9AE8H
Power-On Default: Undefined

This register specifies the drawing command and a number of associated control parameters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD-TYPE			BYTE		BUS SIZE		WAIT	DRWG-DIR.			DRAW	DIR	LAST	PX	
2	1	0	SWP	R	1	0	YES	2	1	0	YES	TYP	POF	MD	= 1

Bit 0 This bit must always be programmed to 1.

Bit 1 PX MD - Select Across the Plane Pixel Mode
0 = Single pixel transferred at a time
1 = Multiple pixels transferred at a time (across the plane mode)

Bit 2 LAST POF - Last Pixel Off
0 = Last pixel of line or vector draw will be drawn
1 = Last pixel of line or vector draw will not be drawn

Bit 3 DIR TYP - Select Radial Direction Type
0 = x-y (axial)
1 = Radial

Bit 4 DRAW YES - Draw Pixel
0 = Move the current position only - don't draw
1 = Draw pixel(s)

Bits 7–5 DRWG-DIR - Select Drawing Direction
In the following table, radial drawing angle is measured counterclockwise from the X axis. For axial line draws, the line is drawn from left to right or a +X and from right to left for a -X, down for a +Y and up for a -Y. X or Y maj specifies the longest axis.

7–5	Radial (bit 3 = 1)	x-y (Axial - bit 3 = 0)
000	0°	–Y,X maj,–X
001	45°	–Y,X maj,+X
010	90°	–Y,Y maj,–X
011	135°	–Y,Y maj,+X
100	180°	+Y,X maj,–X
101	225°	+Y,X maj,+X
110	270°	+Y,Y maj,–X
111	315°	+Y,Y maj,+X

Bit 8 WAIT YES - Wait for CPU Data
0 = Use Graphics Engine-based data
1 = Wait for data to be transferred to or from the CPU through the E2E8H port

Bits 10–9 BUS SIZE - Select image write (E2E8H, E2EAH) bus transfer width
00 = 8 bits
01 = 16 bits
10 = 32 bits. All doubleword bits beyond the image rectangle width are discarded. Each line starts with a fresh doubleword. The current drawing position ends up one pixel below the lower left hand corner of the image rectangle.
11 = 32 bits. This setting applies only to image transfers across the plane (each bit transferred is converted to a pixel). Only bits from the end of the line width to the next byte boundary are discarded. Data for the next line begins with the next byte. The current drawing position ends up one pixel to the right of the top right corner of the image rectangle.

This parameter applies only to writing data through the Pixel Data Transfer (E2E8H, E2EAH) registers (programmed I/O or memory-mapped I/O).

Bit 11 Reserved

Bit 12 BYTE SWP - Enable Byte Swap
0 = High byte first, low byte second
1 = Low byte first, high byte second

Bits 15–13 CMD-TYPE - Select Command Type

000 = NOP. This is used to set up short stroke vector drawing without writing a pixel.
001 = Draw Line. If bit 3 of this register is cleared to 0, the axial step constant, diagonal step constant and error term are used to draw the line. If bit 3 is set to 1, the line will be drawn at the angle specified by bits 7-5 and with a length in pixels as specified by the Major Axis Pixel Count (96E8H) register.
010 = Rectangle Fill. The position, width and height of a rectangle are defined. The rectangle is filled with a solid color if it not used for an image transfer.
110 = BitBLT. A rectangle of defined location, width and height is moved to another defined location in display memory.
111 = PatBLT. An 8x8 pixel patterned rectangle of defined location is transferred repeatedly to a destination rectangle of defined location, width and height. The pattern copy is always aligned to an 8 pixel boundary and transfers continue until the pattern is tiled into the entire destination rectangle. The starting X coordinate of the source pattern rectangle should always be on an 8 pixel boundary.

Short Stroke Vector Transfer Register (SHORT_STROKE)

Write Only Address: 9EE8H
Power-On Default: Undefined

This register defines two short stroke vectors. These are drawn one at a time based on the setting of the BYTE SWAP bit (bit 12) in the Command (9AE8H) register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRWG-DIR			DRW	PIXEL-LENGTH				DRWG-DIR.			DRW	PIXEL-LENGTH			
2	1	0	-MV	3	2	1	0	2	1	0	-MV	3	2	1	0

Bits 3–0 PIXEL-LENGTH
Value = # pixels - 1

Bit 4 DRW -MV - Draw Pixel
0 = Move current position only - don't draw
1 = Draw pixel

Bits 7–5 DRWG-DIR.- Select Drawing Direction (measured counterclockwise from the X axis)
000 = 0°
001 = 45°
010 = 90°
011 = 135°
100 = 180°
101 = 225°
110 = 270°
110 = 315°

Bits 15–8 These bits duplicate bits 7-0 to define the second short stroke vector.

Background Color Register (BKGD_COLOR)

Read/Write Address: A2E8H
Power-On Default: Undefined

See the Enhanced Mode Bitmap Accessing Through the Graphics Engine section in the Functional Description for a detailed explanation of how and when this color value is used when writing a pixel to display memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BACKGROUND COLOR															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BACKGROUND COLOR															

Bits 31–0 BACKGROUND COLOR
If bit 9 of BEE8_EH is set to 1 for programmed I/O (not MMIO), this becomes a 32-bit register. If bit 9 of BEE8_EH is cleared to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Foreground Color Register (FRGD_COLOR)

Read/Write Address: A6E8H
Power-On Default: Undefined

See the Enhanced Mode Bitmap Accessing Through the Graphics Engine section in the Functional Description for a detailed explanation of how and when this color value is used when writing a pixel to display memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOREGROUND COLOR															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FOREGROUND COLOR															

Bits 31–0 FOREGROUND COLOR
If bit 9 of BEE8_EH is set to 1 for programmed I/O (not MMIO), this becomes a 32-bit register. If bit 9 of BEE8_EH is cleared to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Bitplane Write Mask Register (WRT_MASK)

Read/Write Address: AAE8H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT-PLANE WRITE MASK															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BIT-PLANE WRITE MASK															

Bits 31–0 BIT-PLANE WRITE MASK
If bit i = 0, bitplane i is not updated
If bit i = 1, bitplane i is updated

Bits 31-0 control planes 31-0 respectively. If bit 9 of BEE8_EH is set to 1 for programmed I/O (not MMIO), this becomes a 32-bit register. If bit 9 of BEE8_EH is cleared to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Bitplane Read Mask Register (RD_MASK)

Read/Write Address: AEE8H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT-PLANE READ MASK															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BIT-PLANE READ MASK															

Bits 31–0 BIT-PLANE READ MASK
If bit i = 0, bitplane i is not used as a data source
If bit i = 1, bitplane i is used as a data source

Bit-plane read mask for BitBLT and image transfer functions. Bits 31-0 control planes 31-0 respectively. If bit 9 of BEE8_EH is set to 1 for programmed I/O (not MMIO), this becomes a 32-bit register. If bit 9 of BEE8_EH is cleared to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Color Compare Register (COLOR_CMP)

Read/Write Address: B2E8H
Power-On Default: Undefined

This register contains the color value that is compared against the current bitmap color if the color compare option is turned on by setting bit 8 of the Pixel Control (BEE8H, Index 0EH) to 1. Bit 7 of the Pixel Control register determines whether a match or a non-match results in a pixel update.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMPARISON COLOR WITH SOURCE															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COMPARISON COLOR WITH SOURCE															

Bits 31–0 COMPARISON COLOR WITH SOURCE
If bit 9 of BEE8_EH is set to 1 for programmed I/O (not MMIO), this becomes a 32-bit register. If bit 9 of BEE8_EH is cleared to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Background and Foreground Mix Registers (BKGD_MIX, FRGD_MIX)

Read/Write Address: B6E8H (Background), BAE8H (Foreground)
Power-On Default: Undefined

See the Enhanced Mode Bitmap Accessing Through the Graphics Engine section in the Functional Description for a detailed explanation of how and when these registers are used when writing a pixel to display memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									CLR-SRC			MIX-TYPE			
R	R	R	R	R	R	R	R	R	1	0	R	3	2	1	0

Bits 3–0 MIX-TYPE - Select Mix Type
In the general case, a new color is defined. A logical operation such as AND or OR is then performed between it and the current bitmap color. If the bitplane to be written is enabled, the result of this logical "mix" is written to the bitmap as the new pixel color. The following table shows the mix types available (! = logical NOT).

0000	!current	1000	!current OR !new
0001	logical zero	1001	current OR !new
0010	logical one	1010	!current OR new
0011	leave current as is	1011	current OR new
0100	!new	1100	current AND new
0101	current XOR new	1101	!current AND new
0110	!(current XOR new)	1110	current AND !new
0111	new	1111	!current AND !new

Bit 4 Reserved

Bits 6–5 CLR-SRC - Select Color Source
00 = Background Color register is the color source
01 = Foreground Color register is the color source
10 = CPU data (the CPU is the color source)
11 = Display memory (the display memory is the color source)

Bits 15–7 Reserved

Read Register Data Register (RD_REG_DT)

Read Only Address: BEE8H
Power-On Default: Undefined

A read of this register produces a read of the register specified by bits 2-0 of the Read Register Select (BEE8H, Index 0FH) register. Each read of BEE8H causes the read index (bits 2-0 of BEE8H, Index 0FH) to increment by one. Registers BEE8H, Indices 0H to 0EH, 9AE8H and 42E8H can thus be rapidly read by successive reads from BEE8H.

Note: Writes to the BEE8H registers (except the read index register, Index 0FH) are pipelined. Therefore, to correctly read back a write to one of these registers, issue a NOP drawing command (a write to 9AE8H with bits 15-13 programmed to 000b) immediately after the BEE8H register write. Next, write the desired register index to BEE8H, Index 0FH and read the data from BEE8H.

The BEE8H registers are written directly by writing to BEE8H with the appropriate register index in bits 15-12.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Minor Axis Pixel Count Register (MIN_AXIS_PCNT)

Write Only Address: BEE8H, Index 0H
Power-On Default: Undefined

This register specifies the height for rectangles, image transfers, BitBLTs and PatBLTs.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	RECTANGLE HEIGHT											

Bits 11–0 RECTANGLE HEIGHT
Value = (number of pixels in the height of the rectangle) - 1

Bits 15–12 INDEX = 0H

Top Scissors (SCISSORS_T)

Write Only Address: BEE8H, Index 1H
Power-On Default: Undefined

This register specifies the top of the clipping rectangle. It is the lowest Y value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	CLIPPING TOP LIMIT											

Bits 11–0 CLIPPING TOP LIMIT

Bits 15–12 INDEX = 1H

Left Scissors (SCISSORS_L)

Write Only Address: BEE8H, Index 2H
Power-On Default: Undefined

This register specifies the left side of the clipping rectangle. It is the lowest X value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	CLIPPING LEFT LIMIT											

Bits 11–0 CLIPPING LEFT LIMIT

Bits 15–12 INDEX = 2H

Bottom Scissors (SCISSORS_B)

Write Only Address: BEE8H, Index 3H
Power-On Default: Undefined

This register specifies the bottom of the clipping rectangle. It is the highest Y value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	CLIPPING BOTTOM LIMIT											

Bits 11–0 CLIPPING BOTTOM LIMIT

Bits 15–12 INDEX = 3H

Right Scissors (SCISSORS_R)

Write Only Address: BEE8H, Index 4H
Power-On Default: Undefined

This register specifies the right side of the clipping rectangle. It is the highest X value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	CLIPPING RIGHT LIMIT											

Bits 11–0 CLIPPING RIGHT LIMIT

Bits 15–12 INDEX = 4H

Pixel Control Register (PIX_CNTL)

Write Only Address: BEE8H, Index 0AH
Power-On Default: Undefined

See Bitmap Access Through the Graphics Engine in the Enhanced Mode Programming section for an explanation of how and when bits 7-6 of this register are used when writing a pixel to display memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DT-EX-SRC							
1	0	1	0	R	R	R	R	1	0	R	R	R	R	R	R

Bits 5–0 Reserved

Bits 7–6 DT-EX-SRC - Select Mix Register
00 = Foreground Mix register is always selected
01 = Reserved
10 = CPU data determines Mix register selected
11 = Display memory current value determines Mix register selected

Bits 11–8 Reserved

Bits 15–12 INDEX = 0AH

Multifunction Control Miscellaneous 2 Register (MULT_MISC2)

Write Only Address: BEE8H, Index 0DH
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
=1	=1	=0	=1	=0	=0	=0	=0	=0	SRC-BASE			=0	DST=BASE		

Bits 2–0 DST-BASE - Destination Base Address
000 = First destination memory address is in the 1st MByte of display memory
001 = First destination memory address is in the 2nd MByte of display memory
010 = First destination memory address is in the 3rd MByte of display memory
011 = First destination memory address is in the 4th MByte of display memory

This field supersedes bits 1-0 of BEE8H, Index E if any of these 3 bits are set to 1.

Bit 3 Reserved

Bits 6–4 SRC-BASE - Source Base Address
000 = First source memory address is in the 1st MByte of display memory
001 = First source memory address is in the 2nd MByte of display memory
010 = First source memory address is in the 3rd MByte of display memory
011 = First source memory address is in the 4th MByte of display memory

This field supersedes bits 3-2 of BEE8H, Index E if any of these three bits are set to 1.

Bits 11–7 Reserved

Bits 15–12 INDEX = 0DH

Multifunction Control Miscellaneous Register (MULT_MISC)

Write Only Address: BEE8H, Index 0EH
Power-On Default: Undefined

Software must initialize this register appropriately before the Graphics Engine is used. See the description for BEE8H, read only, for the required two step register update sequence.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	R	1C EDO	CMR 32B	ENB CMP	SRC NE	R	EXT CLIP	RSF	SRC-BA 21	20	DEST-BA 21	20

Bits 1–0 DEST-BA 21 20 - Destination Base Address Bits 21-20
00 = First destination memory address is in the 1st MByte of display memory
01 = First destination memory address is in the 2nd MByte of display memory
10 = First destination memory address is in the 3rd MByte of display memory
11 = First destination memory address is in the 4th MByte of display memory

This field is superseded by bits 2-0 of BEE8H, Index D if any of the BEE8H Index D bits is set to 1.

Bits 3–2 SRC-BA 21 20 - Source Base Address Bits 21-20
00 = First source memory address is in the 1st MByte of display memory
01 = First source memory address is in the 2nd MByte of display memory
10 = First source memory address is in the 3rd MByte of display memory
11 = First source memory address is in the 4th MByte of display memory

This field is superseded by bits 6-4 of BEE8H Index D if any of the BEE8H Index D bits is set to 1.

Bit 4 RSF - Select Upper Word in 32 Bits/Pixel Mode
0 = Selects lower 16 bits for accesses to 32-bit registers in 32 bpp mode
1 = Selects upper 16 bits for accesses to 32-bit registers in 32 bpp mode

Bit 5 EXT CLIP - Enable External Clipping
0 = Only pixels inside the clipping rectangle are drawn
1 = Only pixels outside the clipping rectangle are drawn

Bit 6 Reserved

Bit 7 SRC NE - Don't Update Bitmap if Source Not Equal to Color Compare Color
0 = Don't update current bitmap if the Color Compare (B2E8) register value is equal to the color value of the source bitmap
1 = Don't update current bitmap if the Color Compare (B2E8) register value is not equal to the color value of the source bitmap

This bit is only active if bit 8 of this register is set to 1.

Bit 8 ENB CMP - Enable Color Compare
0 = Disable color comparison
1 = Enable color comparison

Bit 9 CMR 32B - Select 32-Bit Command Registers
0 = Command registers (A2E8H, A6E8H, AAE8H, AEE8H, B2E8H) are 16-bit
1 = Command registers (A2E8H, A6E8H, AAE8H, AEE8H, B2E8H) are 32-bit. Byte and word accesses cannot be made.

This bit applies to programmed I/O accesses only and is a don't care for MMIO accesses.

Bit 10 1C EDO - Disable 1-cycle EDO Operation
0 = Allow 1-cycle EDO operation
1 = Disable 1-cycle EDO operation

Bit 11 Reserved = 0

Bits 15–12 INDEX = 0EH

Read Register Select Register (READ_SEL)

Write Only Address: BEE8H, Index 0FH
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	R	R	R	R	R	R	R	R	READ-REG-SEL			

Bits 3–0 READ-REG-SEL - Read Register Select

When BEE8H is read, the value returned is determined by this read register index according to the following:
0000 = BEE8H, Index 0H
0001 = BEE8H, Index 1H
0010 = BEE8H, Index 2H
0011 = BEE8H, Index 3H
0100 = BEE8H, Index 4H
0101 = BEE8H, Index 0AH
0110 = BEE8H, Index 0EH
0111 = 9AE8H (Bits 15-13 of the read data are forced to 0)
1000 = 42E8H (Bits 15-12 of the read data are forced to 0)
1001 = Reserved
1010 = BEE8H, Index 0DH

The read register index increments by one with each reading of BEE8H.

Bits 11–4 Reserved

Bits 15–12 INDEX = 0FH

Pixel Data Transfer Register (PIX_TRANS)

Write Only Address: E2E8H
Power-On Default: Undefined

All data from the CPU to the Graphics Engine must pass through this register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMAGE WRITE DATA															

Bits 15–0 IMAGE WRITE DATA

Pixel Data Transfer - Extension Register (PIX_TRANS_EXT)

Write Only Address: E2EAH
Power-On Default: Undefined

This register is an extension of E2E8H for 32-bit operations.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMAGE WRITE DATA															

Bits 15–0 IMAGE WRITE DATA

Section 21: Streams Processor Register Descriptions

Streams Processor registers can only be accessed via memory-mapped I/O. The register identifier MMxxxx means that the register is memory mapped at offset xxxx from the base address.

Primary Stream Control (MM8180)

Read/Write Address: 8180H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	PSFC			R	PSIDF			R	R	R	R	R	R	R	R

Bits 23-0 Reserved

Bits 26-24 PSIDF - Primary Stream Input Data Format
000 = RGB-8 (CLUT)
001 = Reserved
010 = Reserved
011 = KRGB-16 (1.5.5.5)
100 = Reserved
101 = RGB-16 (5.6.5)
110 = Reserved
111 = XRGB-32 (X.8.8.8)

Bit 27 Reserved

Bits 30-28 PSFC - Primary Stream Filter Characteristics
000 = Primary stream
001 = Primary stream for 2X stretch (replication)
010 = Primary stream, bi-linear for 2X stretch (interpolation)
Other values reserved

Bit 31 Reserved

Color/Chroma Key Control (MM8184)

Read/Write Adds: 8184H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G/U/Cb KEY (LOW)								B/V/Cr KEY (LOW)							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	KC	R	RGB CC			R/Y KEY (LOW)							

Bits 7-0 B/V/Cr key value (lower bound for chroma)

Bits 15-8 G/U/Cb key value (lower bound for chroma)

Bits 23-16 R/Y key value (lower bound for chroma)

Bits 26-24 RGB CC - RGB Color Comparison Precision
000 = Compare bit 7 of RGB (compare red bit 7's, green bit 7's and blue bit 7's)
001 = Compare bits 7-6 of RGB
010 = Compare bits 7-5 of RGB
011 = Compare bits 7-4 of RGB
100 = Compare bits 7-3 of RGB
101 = Compare bits 7-2 of RGB
110 = Compare bits 7-1 of RGB
111 = Compare bits 7-0 of RGB

Bit 27 Reserved

Bit 28 KC - Key Controll
0 = Extract key data from input stream key bit (if present). (KRGB-16, 1.5.5.5 only)
If the K bit is 0, the pixel from the other stream is used (transparent). If the K bit is 1, the key bit streams pixel is used (opaque)
1 = Enable color or chroma keying for all modes other than KRGB-16

Bits 31-29 Reserved

Secondary Stream Control (MM8190)

Read/Write Address: 8190H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	DDA HORIZONTAL ACCUMULATOR											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	SFC				SDIF			R	R	R	R	R	R	R	R

Bits 11-0 DDA Horizontal Accumulator Initial Value

Value = 2 (W0-1) - (W1-1), where W0 is the line width in pixels before scaling and W1 is the line width in pixels after scaling. This is a signed value.

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 23-12 Reserved

Bits 26-24 SDIF - Secondary Stream Input Data Format
000 = Reserved
001 = YCbCr-16 (4.2.2), 16-240 input range
010 = YUV-16 (4.2.2), 0-255 input range
011 = KRGB-16 (1.5.5.5)
100 = YUV (2.1.1)
101 = RGB-16 (5.6.5)
110 = Reserved
111 = XRGB-32 (X.8.8.8

When this field is programmed, the value does not take effect until the next VSYNC.

Bit 27 Reserved

Bits 30-28 SFC - Secondary Stream Filter Characteristics
000 = Secondary stream
001 = Secondary stream, linear, 0-2-4-2-0, for X stretch
010 = Secondary stream, bi-linear, for 2X to 4X stretch
011 = Secondary stream, linear, 1-2-2-2-1, for 4X stretch
Other values reserved

When this field is programmed, the value does not take effect until the next VSYNC.

Bit 31 Reserved

Chroma Key Upper Bound (MM8194)

Read/Write Address: 8194H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U/Cb KEY (UPPER)								V/Cr KEY (UPPER)							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	Y KEY (UPPER)							

Bits 7-0 V/Cr key value (upper bound)

Bits 15-8 U/Cb key value (upper bound)

Bits 23-16 Y key value (upper bound)

Bits 31-24 Reserved

Secondary Stream Stretch/Filter Constants (MM8198)

Read/Write Address: 8198H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	K1 HORIZONTAL SCALE FACTOR										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	K2 HORIZONTAL SCALE FACTOR										

Bits 10-0 K1 Horizontal Scale Factor

Value = W0-1, where W0 is the width in pixels of the initial output window (before scaling)

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 15-11 Reserved

Bits 26-16 K2 Horizontal Scale Factor

Value = W0-W1, where W0 is the initial (unscaled) window width in pixels and W1 is the final output window width in pixels. This is a signed value and will always be negative.

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 31-27 Reserved

Blend Control (MM81A0)

Read/Write Address: 81A0H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	KP			R	R	R	R	R	KS			R	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	COMP MODE			R	R	R	R	R	R	R	R

Bits 1-0 Reserved

Bits 4-2 Ks

Value = secondary stream blend coefficient

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 9-5 Reserved

Bits 12-10 Kp

Value = primary stream blend coefficient

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 23-13 Reserved

Bits 26-24 Compose Mode
000 = Secondary stream opaque overlay on primary stream
001 = Primary stream opaque overlay on secondary stream
010 = Dissolve, [Pp x Kp + Ps x (8 - Kp)]/8, ignore Ks
011 = Fade, [Pp x Kp + Ps x Ks]/8, where Kp + Ks must be ≤ 8
100 = Reserved
101 = Color key on primary stream (secondary stream overlay on primary stream)
110 = Color or chroma key on secondary stream (primary stream overlay on secondary stream)
111 = Reserved

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 31-27 Reserved

Primary Stream Frame Buffer Address 0 (MM81C0)

Read/Write Address: 81C0H
Power-on Default: Undefined

If a primary stream is enabled, this register specifies the starting address in the frame buffer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRIMARY BUFFER ADDRESS 0															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	PRIMARY BUFFER ADDRESS 0					

Bits 21-0 Value = Primary stream frame buffer starting address 0

This value must be quadword aligned.

Bits 31-22 Reserved

Primary Stream Frame Buffer Address 1 (MM81C4)

Read/Write Address: 81C4H
Power-on Default: Undefined

If the primary stream is double buffered, this register specifies the starting address in the frame buffer for the second buffer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRIMARY BUFFER ADDRESS 1															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	PRIMARY BUFFER ADDRESS 1					

Bits 21-0 Value = Primary stream frame buffer starting address 1

This value must be quadword aligned.

Bits 31-22 Reserved

Primary Stream Stride (MM81C8)

Read/Write Address: 81C8H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	PRIMARY STREAM STRIDE											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 11-0 Primary stream stride

Value = byte offset of vertically adjacent pixels in the primary stream buffer(s)

If double buffering is used, the stride must be the same for both buffers.

Bits 31-12 Reserved

Double Buffer/LPB Support (MM81CC)

Read/Write Address: 81CCH
Power-on Default: xxxxxx00H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	LST	LSL	LIS	R	SBS		PBS
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 0 PBS - Primary Stream Buffer Select
0 = Primary frame buffer starting address 0 (MM81C0_21-0) used for the primary stream
1 = Primary frame buffer starting address 1 (MM81C4_21-0) used for the primary stream

Bits 2-1 SBS - Secondary Stream Buffer Select
00 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream
01 = Secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream
10 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF0C_21-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF10_21-0) used for the LPB input stream. Which alternative applies is determined by LPB starting address register selected by bit 4 of this register
11 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF10_21-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF0C_21-0) used for the LPB input stream. Which alternative applies is determined by the LPB starting address register selected by bit 4 of this register

Bit 3 Reserved

Bit 4 LIS - LPB Input Buffer Select
0 = LPB frame buffer starting address 0 (MMFF0C_21-0) used for the LPB input
1 = LPB frame buffer starting address 1 (MMFF10_21-0) used for the LPB input

This bit selects the starting address for writing LPB data into the frame buffer. When the value programmed to this bit takes effect is determined by the setting of bit 5 of this register. This bit can be toggled at the completion of writing all the data for a frame to the frame buffer via bit 6 of this register

Bit 5 LSL - LPB Input Buffer Select Loading
0 = The value programmed into bit 4 of this register takes effect immediately
1 = The value programmed into bit 4 of this register takes effect at the next end of frame (completion of writing all the data for a frame into the frame buffer)

Bit 6 LST - LPB Input Buffer Select Toggle
0 = End of frame (completion of writing all the data for a frame into the frame buffer) has no effect on the setting of bit 4 of this register
1 = End of frame causes the setting of bit 4 of this register to toggle

Bits 31-7 Reserved

Secondary Stream Frame Buffer Address 0 (MM81D0)

Read/Write Address: 81D0H
Power-on Default: Undefined

If a secondary stream is enabled, this register specifies the starting address in the frame buffer

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SECONDARY BUFFER ADDRESS 0															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	SECONDARY BUFFER ADDRESS 0					

Bits 21-0 Value = Secondary stream frame buffer starting address 0

This value must be quadword aligned.

Bits 31-22 Reserved

Secondary Stream Frame Buffer Address 1 (MM81D4)

Read/Write Address: 81D4H
Power-on Default: Undefined

If the secondary stream is double buffered, this register specifies the starting address in the frame buffer for the second buffer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SECONDARY BUFFER ADDRESS 1															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	SECONDARY BUFFER ADDRESS 1					

Bits 21-0 Value = Secondary stream frame buffer starting address 1

This value must be quadword aligned.

Bits 31-22 Reserved

Secondary Stream Stride (MM81D8)

Read/Write Address: 81D8H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	SECONDARY STREAM STRIDE											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 11-0 Secondary stream stride

Value = byte offset of vertically adjacent pixels in the secondary stream buffer(s)

If double buffering is used, the stride must be the same for both buffers.

Bits 31-12 Reserved

Opaque Overlay Control (MM81DC)

Read/Write Address: 81DCH
Power-on Default: Undefined except bits 31-30 are 00b.

When an opaque overlay mode is being used (bits 26-24 of MM81A0 = 000b or 001b), the fields in this register can be programmed to eliminate the fetching of the pixels for the rectangular area under the top (opaque) window. This reduces the memory bandwidth requirements. The bottom window should be full-screen when this feature is enabled. None of the fields in this register have an effect unless bit 31 is set to 1. Note that only horizontal coordinates must be specified. The vertical coordinates are handled automatically by the hardware.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	PIXEL STOP FETCH										R	R	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OOC	TSS	R	PIXEL RESUME FETCH										R	R	R

Bits 2-0 Reserved

Bits 12-3 Pixel Stop Fetch

Value = [Offset in quadwords from the background starting pixel horizontal position to the first pixel of the line not to be fetched from memory (hidden background)] + 1 quadword

If the primary stream is the background, MM81F0_26-16 define the starting position for each line in the background window (X0) and MM81F8_26-16 define the first pixel position for each line in the top window (X1). The latter is the first background pixel that does not need to be fetched. The value programmed in this field is then [(X1 - X0) x bytes per pixel/8] +1. If the result is a fraction, it is rounded up the next highest integer. This gives the required quadword offset (O) for this field. This value is also used in the calculation for the field value of bits 28-19 of this register.

If the secondary stream is the background, the value is [(X0 - X1) x bytes per pixel/8] + 1.

Bits 18-13 Reserved

Bits 28-19 Pixel Resume Fetch

Value = {Offset in quadwords from the background starting pixel horizontal position to the line position of the resumption of pixel fetching from memory (i.e., visible background)} - 1 quadword

The value is determined by adding the Pixel Stop Fetch field value (O) above (bits 12-3) to the width in quadwords of the top window (W). The width of the top window in pixels (P) is found in MM81F4_26-16 if the primary stream is on top and in MM81FC_26-16 if the secondary stream is on top. W in quadwords = P x bytes per pixel/8. If this is a fraction, the result is truncated to the next lowest integer. The value in this field is then [W + O] - 1.

Bit 29 Reserved

Bit 30 TSS - Top Stream Select
0 = Secondary stream on top
1 = Primary stream on top

Bit 31 OOC - Opaque Overlay Control Enable
0 = Opaque overlay control disabled
1 = Opaque overlay control enabled

K1 Vertical Scale Factor (MM81E0)

Read/Write Address: 81E0H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	K1 VERTICAL SCALE FACTOR										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 10-0 K1 Vertical Scale Factor

Value = [height (in lines) of the initial output window (before scaling)] - 1

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 31-11 Reserved

K2 Vertical Scale Factor (MM81E4)

Read/Write Address: 81E4H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	K2 VERTICAL SCALE FACTOR										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 10-0 K2 Vertical Scale Factor

Value = [height (in lines) of the initial output window (before scaling)] - [height (in lines) of the final output window (after scaling)]

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 31-11 Reserved

DDA Vertical Accumulator Initial Value (MM81E8)

Read/Write Address: 81E8H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	DDA VERTICAL ACCUMULATOR											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 11-0 DDA Vertical Accumulator Initial Value

Value = 2's complement of {[height (in lines) of the output window after scaling] - 1}

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 31-12 Reserved

Streams FIFO and RAS Controls (MM81EC)

Read/Write Address: 81ECH
Power-on Default: 00003000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RL	PFIFO THRESHOLD					SFIFO THRESHOLD					FIFO ALLOCATION				
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	PDD	MAR	TSM	EWS	R	RP

Bits 4-0 Streams FIFO Allocation
00000 = Primary Stream = 24 slots, Secondary Stream = 0 slots
01000 = Primary Stream = 16 slots, Secondary Stream = 8 slots
01100 = Primary Stream = 12 slots, Secondary Stream =12 slots
10000 = Primary Stream = 8 slots, Secondary Stream = 16 slots
11000 = Primary Stream = 0 slots, Secondary Stream = 24 slots

All other values are reserved and must not be programmed. Each slot holds one quadword.

Bits 9-5 Secondary FIFO Threshold

Value = Number of secondary FIFO slots

When the secondary FIFO empties down to this value, an internal signal is generated requesting re-filling of the secondary FIFO. This value must be less than or equal to the secondary stream FIFO size specified in bits 4-0.

Bits 14-10 Primary FIFO Threshold

Value = Number of primary FIFO slots

When the primary FIFO empties down to this value, an internal signal is generated requesting re-filling of the primary FIFO. This value must be less than or equal to the primary stream FIFO size specified in bits 4-0.

Bit 15 RL - $\overline{RAS}$ Low Time Control
0 = $\overline{RAS}$ low time specified by CR68_2 (3.5 or 4.5 MCLKs)
1 = RAS low time = 2.5 MCLKs

Bit 16 RP - $\overline{RAS}$ Pre-Charge Control
0 = $\overline{RAS}$ pre-charge specified by CR68_3 (2.5 or 3.5 MCLKs)
1 = $\overline{RAS}$ pre-charge = 1.5 MCLKs

Bit 17 Reserved

Bit 18 EWS - EDO Memory Wait State Control (LPB Memory Cycles Only)
0 = Standard 2-cycle memory operation
1 = 1-cycle EDO memory operation (requires EDO memory capable of this)

This bit is only valid for 64-bit PD bus operation (2 or 4 MBytes of memory). It should not be set for 32-bit (1 MByte) configurations.

Bit 19 TSM - Tri-state Memory Data Lines
0 = Tri-state PD[63:16] during ROM cycles
1 = Do not tri-state PD[63:16] during ROM cycles

PD[15:0] are driven with the ROM address. This bit should normally be left at its default value of 0.

Bit 20 MAR - Memory Arbitration
0 = Arbitrate for the memory bus when ROM cycle initiated
1 = ROM cycle immediately uses memory bus

This bit should normally be left at its default value of 0.

Bit 21 PDD - PD Output Delay
0 = Delay output of PD[63:0] for 0.5 MCLKs
1 = No delay of PD[63:0] ouput

This bit should normally be left at its default value of 0.

Bits 31-22 Reserved

Primary Stream Window Start Coordinates (MM81F0)

Read/Write Address: 81F0H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	PRIMARY STREAM Y-START										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	PRIMARY STREAM X-START										

Bits 10-0 Primary Stream Y-Start

Value = Screen line number +1 of the first line of the primary stream window

Bits 15-11 Reserved

Bits 26-16 Primary Stream X-Start

Value = Screen pixel number +1 of the first pixel of the primary stream window

Bits 31-27 Reserved

Primary Stream Window Size (MM81F4)

Read/Write Address: 81F4H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	PRIMARY STREAM HEIGHT										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	PRIMARY STREAM WIDTH										

Bits 10-0 Primary Stream Height

Value = Number of lines displayed in the primary stream window

Bits 15-11 Reserved

Bits 26-16 Primary Stream Width

Value = Number of pixels -1 displayed in each line in the primary stream window

Bits 31-27 Reserved

Secondary Window Start Coordinates (MM81F8)

Read/Write Address: 81F8H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	SECONDARY STREAM Y-START										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	SECONDARY STREAM X-START										

Bits 10-0 Secondary Stream Y-Start

Value = Screen line number +1 of the first line of the secondary stream window

Bits 15-11 Reserved

Bits 26-16 Secondary Stream X-Start

Value = Screen pixel number +1 of the first pixel of the secondary stream window

Bits 31-27 Reserved

Secondary Window Size (MM81FC)

Read/Write Address: 81FCH
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	SECONDARY STREAM HEIGHT										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	SECONDARY STREAM WIDTH										

Bits 10-0 Secondary Stream Height

Value = Number of lines displayed in the secondary stream window

Bits 15-11 Reserved

Bits 26-16 Secondary Stream Width

Value = Number of pixels -1 displayed in each line in the primary stream window

Bits 31-27 Reserved

Section 22: LPB Register Descriptions

LPB registers can only be accessed via memory-mapped I/O. The register identifier MMxxxx means that the register is memory mapped at offset xxxx from the base address.

LPB Mode (MMFF00)

Read/Write Address: FF00H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LBA	CHS	CVS	LHS	LVS	R	R	CBS	SF	LR	LPB MODE			LE
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	ILC	SNO	CS	R	VFT		R	R	R	MBS	

Bit 0 LE - LPB Enable
0 = LPB Disabled
1 = LPB Enabled

Enabling the LPB causes the LPB mode pin configurations described in Section 2 to take effect. The exact pin configuration depends on which LPB mode is enabled via bits 3-1 of this register or which feature connector option is selected. Once enabled, the LPB is reset either by a system reset or via bit 4 of this register.

Bits 3-1 LPB MODE
000 = Scenic/MX2 Mode. Pins 203 and 204 act as VREQ/VRDY and CREQ/CRDY respectively.
001 = Video 16 Mode (PCI only). Pins 203 and 204 act as HS and VS respectively and pins 201-199, 189-185 act as LD[15:8]. The Trio64V+ expects 16-bit Philips digitizer input.
010 = Video 8 In Mode. Pins 203 and 204 to act as HS and VS respectively and the Trio64V+ expects video data in 8-bit units (LD[7:0]).
011 = Video 8 In/Out Mode. This setting enables the bi-directional CL-480 interface.
100 = Pass-through Mode. 32-bit data from the output FIFO is passed directly to the decimation input to the video FIFO. This allows decimation of CPU-provided data.

All other values are reserved.

Bit 4 LR- LPB Reset
0 = No effect
1 = Reset LPB

This bit should be set and then reset before switching between LPB modes.

Bit 5 SF - Skip Frames
0 = Write all received frames to memory
1 = Write every other received frame to memory (1, 3, etc.)

Bit 6 CBS - Color Byte Swap
0 = Incoming video is in U_{01}, Y_0, V_{01}, Y_1 format (e.g., CL-480), byte swap enabled
1 = Incoming video is in Y_0, U_{01}, Y_1, V_{01} format (e.g., SAA7110), no byte swap

Bits 8-7 Reserved

Bit 9 LVS - LPB Vertical Sync Input Polarity
0 = LPB vertical sync input is active low
1 = LPB vertical sync input is active high

Bit 10 LHS - LPB Horizontal Sync Input Polarity
0 = LPB horizontal sync input is active low
1 = LPB horizontal sync input is active high

Bit 11 CVS - CPU VSYNC (Write Only)

Writing a 1 to this bit causes the Trio64V+ to do whatever functions it is programmed to do upon receipt of a VSYNC. For example, values programmed in certain registers only take effect at the next VSYNC.

Bit 12 CHS - CPU HSYNC (Write Only)

Writing a 1 to this bit causes the Trio64V+ to do whatever functions it is programmed to do upon receipt of an HSYNC.

Bit 13 LBA - Load Base Address (Write Only)

Writing a 1 to this bit immediately loads the base address currently being pointed to.

Bits 15-14 Reserved

Bits 17-16 MBS - Maximum LPB to Scenic/MX2 Compressed Data Burst Size (Scenic/MX2 mode only)
00 = Burst 1 32-bit word
01 = Burst 2 32-bit words
10 = Burst 3 32-bit words
11 = Burst all 32-bit words (until empty)

With a setting of 11b, software must ensure that no more than eight 32-bit words are burst to the Scenic/MX2 in a single burst. For example, if the FIFO is full (8 entries), no more entries should be written until the burst is complete.

Bits 20-18 Reserved

Bits 22-21 VFT - Video FIFO Threshold
00 = 1 FIFO slot
01 = 2 FIFO slots
10 = 4 FIFO slots
11 = 6 FIFO slots

When this many slots are filled in the video FIFO, a request is generated to the memory manager to begin emptying the FIFO. This is used to maximize the efficiency of the memory interface.

Bit 23 Reserved

Bit 24 CS - LPB Clock Source
0 = LPB clock driven by SCLK (pin 194)
1 = LPB clock driven by LCLK (pin 148)

This bit allows for the LPB to be used in pass-through mode (MMFF00_3-1 = 100b) when the Trio64V+ is configured for compatible mode. The LPB is normally driven by LCLK, but this is not available in compatible mode.

Bit 25 SNO - Sync Non-Overlap
0 = No effect
1 = Don't add stride after first HSYNC

This bit must be set when the first HSYNC does not occur within the VSYNC active period.

Bit 26 ILC - Invert LCLK
0 = Use LCLK as received
1 = Invert the LCLK input

Bit 24 of this register must be set to 1 for this bit to be effective.

Bits 30-27 Reserved

Bit 31 CFL - CFLEVEL Status (Read Only)

This bit reflects the state of the CFLEVEL input (pin 182) in Video In/Out (CL-480) mode.

LPB FIFO Status (MMFF04)

Read Only Address: FF04H
Power-on Default: 00000008H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	OFAE	OFE	OFF	R	R	R	R	R	R	R	OFIFO STATUS			
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VF1AE	VF1E	VF1F	R	R	R	R	R	R	VF0AE	VF0E	VF0F	R	R	R	R

Bits 3-0 LPB Output FIFO Status
0000 = 0 FIFO slots free
0001 = 1 FIFO slot free
0010 = 2 FIFO slots free
0011 = 3 FIFO slots free
0100 = 4 FIFO slots free
0101 = 5 FIFO slots free
0110 = 6 FIFO slots free
0111 = 7 FIFO slots free
1000 = 8 FIFO slots free

Each slot contains 4 bytes

Bits 10-4 Reserved

Bit 11 OFF - LPB Output FIFO Full
0 = Output FIFO not full
1 = Output FIFO full

Bit 12 OFE - LPB Output FIFO Empty
0 = Output FIFO not empty
1 = Output FIFO empty

Bit 13 OFAE - LPB Output FIFO Almost Empty
0 = Output FIFO has something other than 1 slot filled
1 = Output FIFO has one slot filled

Bits 19-14 Reserved

Bit 20 VF0F - LPB Video FIFO 0 Full
0 = Video FIFO 0 not full
1 = Video FIFO 0 full

Bit 21 VF0E - LPB Video FIFO 0 Empty
0 = Video FIFO 0 not empty
1 = Video FIFO 0 empty

Bit 22 VF0AE - LPB Video FIFO 0 Almost Empty
0 = Video FIFO 0 has something other than 1 slot filled
1 = Video FIFO 0 has one slot filled

Bits 28-23 Reserved

Bit 29 VF1F - LPB Video FIFO 1 Full
0 = Video FIFO 1 not full
1 = Video FIFO 1 full

Bit 30 VF1E - LPB Video FIFO 1 Empty
0 = Video FIFO 1 not empty
1 = Video FIFO 1 empty

Bit 31 VF1AE - LPB Video FIFO 1 Almost Empty
0 = Video FIFO 1 has something other than 1 slot filled
1 = Video FIFO 1 has one slot filled

LPB Interrupt Flags (MMFF08)

Read/Write Address: FF08H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	SPS	EFI	ELI	FEI
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	SPW	R	R	R	R	SPM	EFM	ELM	FEM

Bit 0 FEI - LPB Output FIFO Empty Interrupt Status
0 = No interrupt
1 = LPB output FIFO empty

Writing a 1 to this bit clears the interrupt.

Bit 1 ELI - End of Line Interrupt Status
0 = No interrupt
1 = The Trio64V+ has received an HSYNC input on pin 203

Writing a 1 to this bit clears the interrupt.

Bit 2 EFI - End of Frame Interrupt Status
0 = No interrupt
1 = The Trio64V+ has received a VSYNC input on pin 204

Writing a 1 to this bit clears the interrupt.

Bit 3 SPS - Serial Port Start Detect Interrupt Status
0 - No interrupt
1 = The Trio64V+ has detected a serial port start condition

A serial port start condition occurs when SPD (pin 206) is driven low by another device while SPCLK (pin 205) is not being driven low. Writing a 1 to this bit clears the interrupt.

Bits 15-4 Reserved

Bit 16 FEM - LPB Output FIFO Empty Interrupt Enable Mask
0 = LPB output FIFO empty interrupt disabled
1 = LPB output FIFO empty interrupt enabled

Bit 17 ELM - End of Line Interrupt Enable Mask
0 = End of Line interrupt disabled
1 = End of Line interrupt enabled

Bit 18 EFM - End of Frame Interrupt Enable Mask
0 = End of frame interrupt disabled
1 = End of frame interrupt enabled

Bit 19 SPM - Serial Port Start Detect Interrupt Mask
0 = Serial port start detect interrupt disabled
1 = Serial port start detect interrupt enabled

Bits 23-20 Reserved

Bit 24 SPW - Serial Port Wait
0 = Release SPCLK (pin 205) to float high
1 = Drive SPCLK (pin 205) low upon receipt of a serial port start condition

Setting this bit to 1 enables serial port wait states until the Host is ready to process the data.

Bit 31-25 Reserved

LPB Frame Buffer Address 0 (MMFF0C)

Read/Write Address: FF0CH
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPB BUFFER ADDRESS 0															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	LPB BUFFER ADDRESS 0					

Bits 21-0 LPB Frame Buffer Address 0

Value = starting address 0 (offset in bytes from the start of the frame buffer) for writing LPB data to the frame buffer

This value will normally be the same as the secondary stream frame buffer address 0. The value must start on an 8-byte boundary. A value programmed in this field does not take effect until the next LPB VSYNC.

Bits 31-22 Reserved

LPB Frame Buffer Address 1 (MMFF10)

Read/Write Address: FF10H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPB BUFFER ADDRESS 1															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	LPB BUFFER ADDRESS 1					

Bits 21-0 LPB Frame Buffer Address 1

Value = starting address 1 (offset in bytes from the start of the frame buffer) for writing LPB data to the frame buffer

This value will normally be the same as the secondary stream frame buffer address 1. Both address 0 and address 1 are defined when double buffering is used. The value must start on an 8-byte boundary. A value programmed in this field does not take effect until the next LPB VSYNC.

Bits 31-22 Reserved

LPB Direct Read/Write Address (MMFF14)

Read/Write Address: FF14H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPB DIRECT READ/WRITE ADDRESS															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	TT			LPB READ/WRITE ADDRESS				

Bits 20-0 LPB Direct Read/Write Address

Value = address of Scenic/MX2/CL-480 register to read/write

Bits 23-21 TT - Transaction Type (Scenic/MX2)
000 = Register write
001 = Register read
110 = Compressed video data write from the output FIFO. This value is automatically generated by hardware when data is written to the output FIFO.

Bits 31-24 Reserved

LPB Direct Read/Write Data (MMFF18)

Read/Write Address: FF18H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPB DIRECT READ/WRITE DATA															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LPB DIRECT READ/WRITE DATA															

Bits 31-0 LPB Direct Read/Write Data

A write to this register triggers a read/write sequence based on the address information in MMFF14_23-0.

LPB General Purpose Input/Output Port (MMFF1C)

Read/Write - see bit definitions Address: FF1CH
Power-on Default: Undefined

This register is available only for PCI bus configurations.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	LPB GIP				LPB GOP			
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 3-0 LPB General Purpose Output Data Port

These bits are driven onto the LPB LD[3:0] lines whenever a write is performed to CR5C. $\overline{\text{STWR}}$ is asserted (low) at this time for use as an enable strobe for latching the data into an external buffer.

Bits 7-4 LPB General Purpose Input Data Port (Read only)

Whenever a write is performed to CR5C, $\overline{\text{STWR}}$ is asserted (low). This strobe can be used to enable a register to drive data onto any or all of the LD[7:4] lines. This data is then latched into these bits.

Bits 31-8 Reserved

Serial Port (MMFF20)

Read/Write Address: FF20H
Power-on Default: 00000000H

This register can also be accessed at I/O ports E2H or E8H. See the Serial Communications Port description in Section 4.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	B4M	B3M	B2M	B1M	B0M	R	R	R	SPE	SDR	SCR	SDW	SCW
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 0 SCW - Serial Clock Write
0 = Pin 205 is driven low
1 = Pin 205 is tri-stated

Pin 205 carries the DDC/I^2C clock, depending on the operational mode. When pin 205 is tri-stated, other devices may drive this line. The actual state of the pin is read via bit 2 of this register.

Bit 1 SDW - Serial Data Write
0 = Pin 206 is driven low
1 = Pin 206 is tri-stated

Pin 206 carries the DDC/I^2C data, depending on the operational mode. When pin 206 is tri-stated, other devices may drive this line. The actual state of the pin is read via bit 3 of this register.

Bit 2 SCR - Serial Clock Read (Read Only)
0 = Pin 205 is low
1 = Pin 205 is tri-stated (no device is driving this line)

Bit 3 SDR - Serial Data Read (Read Only)
0 = Pin 206 is low
1 = Pin 206 is tri-stated (no device is driving this line)

Bit 4 SPE - Serial Port Enable
0 = Use of bits 1-0 of this register disabled
1 = Use of bits 1-0 of this register enabled

Bits 5-7 Reserved

Bit 8 B0M - Bit 0 Mirror (Read Only)
0 = Pin 205 is driven low
1 = Pin 205 is tri-stated

Bit 9 B1M - Bit 1 Mirror (Read Only)
0 = Pin 206 is driven low
1 = Pin 206 is tri-stated

Bit 10 B2M - Bit 2 Mirror (Read Only)
0 = Pin 205 is low
1 = Pin 205 is tri-stated (no device is driving this line)

Bit 11 B3M -Bit 3 Mirror (Read Only)
0 = Pin 206 is low
1 = Pin 206 is tri-stated (no device is driving this line)

Bit 12 B4M - Bit 4 Mirror (Read Only)
0 = Use of bits 1-0 of this register disabled
1 = Use of bits 1-0 of this register enabled

This bit mirrors bit 4 and allows reading of this data on byte lane 2 at I/O address E2H.

Bits 31-13 Reserved

LPB Video Input Window Size (MMFF24)

Read/Write Address: FF24H
Power-on Default: Undefined

This register applies only to Video 8 In or Video 16 mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	VIDEO INPUT LINE WIDTH											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	VIDEO INPUT WINDOW HEIGHT								

Bits 11-0 Video Input Line Width

Value = [# pixels x 2] - 2 for Video 8 mode
Value = # pixels -2 for Video 16 mode

This is the width of the displayed line after the offset specified in MMFF28_11-0. Before the 2 is subtracted, the number of pixels must be a multiple of 4. For example, in Video 16 mode, if the line width is 637 pixels, this must be rounded up to 640. The programmed value is then 640 - 2 = 638.

Bits 15-12 Reserved

Bits 24-16 Video Input Window Height

Value = [height in lines of each video input frame] - 1

This is the number of displayed lines - 1 after the offset specified in MMFF28_24_16.

Bits 31-25 Reserved

LPB Video Data Offsets (MMFF28)

Read/Write Address: FF28H
Power-on Default: Undefined

This register applies only to Video 8 In or Video 16 mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	HORIZONTAL VIDEO DATA OFFSET											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	VERTICAL VIDEO DATA OFFSET								

Bits 11-0 Horizontal Video Data Offset

Value = [number of LCLKs between HSYNC and the start of valid pixel data] - 2

Bits 15-12 Reserved

Bits 24-16 Vertical Video Data Offset

Value = number of HSYNCs between VSYNC and the first valid data line

Bits 31-25 Reserved

LPB Horizontal Decimation Control (MMFF2C)

Read/Write Address: FF2CH
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO DATA BYTE MASK															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VIDEO DATA BYTE MASK															

Bits 31-0 Video Data Byte Mask

Each 32 bytes of video data input is compared with this mask. If a bit in this mask is 1, the corresponding byte is discarded. If a bit is a 0, the corresponding byte is passed to the video memory. In Video 16 mode, each bit masks 2 bytes. In pass-through mode, each bit masks 4 bytes. Normally, decimation starts with bit 0 after an HSYNC. If a horizontal video data offset is specified in MMFF28_11-0 (video 8 or 16 modes only), decimation aligns with the start of data after the offset.

LPB Vertical Decimation Control (MMFF30)

Read/Write Address: FF30H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO DATA LINE MASK															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VIDEO DATA LINE MASK															

Bits 31-0 Video Data Line Mask

Each 32 lines of video data input is compared with this mask. If a bit in the mask is 0, the corresponding line is passed to video memory. If a bit is a 1, the corresponding line is discarded. If a vertical video data offset is specified in MMFF28_24-16 (video 8 or 16 modes only), decimation does not align with the starting line after the offset and instead starts from VSYNC.

LPB Line Stride (MMFF34)

Read/Write Address: FF34H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	LINE STRIDE											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R		R	R	R	R	R	R	R	R	R	R

Bits 11-0 Line Stride

Value = byte offset of vertically adjacent pixels

This offset is added to the line starting address each HSYNC to get the new line starting address. Each line must begin on an 8-byte boundary.

Bits 31-12 Reserved

LPB Output FIFO (MMFF40)

Read/Write Address: FF40H, FF44H...,FF5CH
Power-on Default: 00000000H

Writes to any of the addresses in this 8 doubleword address range will be transferred to the LPB input FIFO. This allows efficient use of the MOVSD assembly language instruction. Accesses must be to doubleword addresses.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUT FIFO DATA															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUT FIFO DATA															

Bits 31-0 Output FIFO Data

Note: Software must never transfer more compressed data than there is room for in the output FIFO. This information is read from MMFF04_3-0.

Section 23: PCI Register Descriptions

The PCI specification defines a configuration register space. These registers allow device relocation, device independent system address map construction and automatic configurations. The Trio64V+ provides a subset of these registers, which are described below.

The configuration register space occupies 256 bytes. When a configuration read or write command is issued, the AD[7:0] lines contain the address of the register in this space to be accessed. The Trio64V+ supports or returns 0 for the first 64 bytes of this space.

In the following register descriptions, 'R' stands for reserved (write = 0, read = undefined). See Appendix A for a table listing each of the registers in this section and its page number.

Vendor ID

Read Only Address: 00H
Power-On Default: 5333H

This read-only register identifies the device manufacturer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vendor ID															

Bits 15–0 Vendor ID

This is hardwired to 5333H to identify S3 Incorporated.

Device ID

Read Only Address: 02H
Power-On Default: 8811H

This read-only register contains the same value for all Trio family products. The Trio64V+ is identified by a value of 4xH in CR2F and the PCI revision ID field, where "x" will vary by revision.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device ID															

Bits 15–0 Device ID

value = 8811H (hardwired)

Command

Read/Write Address: 04H
Power-On Default: 0000H

This register controls which types of PCI cycles the Trio64V+ can generate and respond to.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	DAC SNP	R	R	R	MEM	I/O

Bit 0 I/O - Enable Response to I/O Accesses
0 = Response to I/O space accesses is disabled
1 = Response to I/O space accesses enabled

Bit 1 MEM - Enable Response to Memory Accesses
0 = Response to memory space accesses is disabled
1 = Response to memory space accesses enabled

Bits 4–2 Reserved

Bit 5 DAC SNP - RAMDAC Register Access Snooping
0 = Trio64V+ claims and responds to all RAMDAC register access cycles
1 = Trio64V+ performs RAMDAC register writes but does not claim the PCI cycle. RAMDAC register read accesses are performed by the Trio64V+.

Bits 15–6 Reserved

Status

Read/Write Address: 06H
Power-On Default: 0200H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	DEVSEL		Reserved								

Bits 8–0 Reserved

Bits 10–9 DEVSEL - Device Select Timing

value = 01 (medium $\overline{\text{DEVSEL}}$ timing) (hardwired)

Bits 15–11 Reserved

Class Code

Read Only Address: 08H
Power-On Default: 30000xxH

This register is hardwired to 30000xxH. The 3 specifies that the Trio64V+ is a VGA-compatible display controller. The "x" in the revision ID will change with each revision.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROGRAMMING INTERFACE								REVISION ID							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASE CLASS CODE								SUB-CLASS							

Base Address 0

Read/Write Address: 12H (high) 10H (low)
Power-On Default: 0000 0000H

This is a 32-bit register in PCI configuration space that provides for address relocation. The Trio64V+ maps the upper 16 bits of the register to the Linear Address Window Position registers CR59-5A. Consequently, these bits map to system address bits 31-16. All 16 bits are writeable in either this register or CR59-5A. However, when this register is read, only bits 31-16 return valid data. Bits 25-16 return 0's. This specifies that the Trio64V+ requires a 64 MByte address space.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	PREF = 0	TYPE =00		MSI = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS 0						R	R	R	R	R	R	R	R	R	R

Bit 0 MSI - Memory Space Indicator

value = 0 (base registers map into memory space) (hardwired)

Bits 2–1 TYPE - Type of Address Relocation

value = 00 (locate anywhere in 32-bit address space) (hardwired)

Bit 3 PREF - Prefetchable

value = 0 (does not meet the prefetchable requirements) (hardwired)

Bits 22–4 Reserved

Bits 31–23 BASE ADDRESS 0

This field is normally programmed by the system BIOS at reset and should not be changed by graphics software. Note that writes to CR59_7-2 will also update this field, so is the linear addressing base address is being changed, the programmer must do a read-modify-write to ensure that this field is not changed.

BIOS ROM Base Address

Read/Write Address: 32H (high) 30H (low)
Power-On Default: 000C 0000H

This is a 32-bit register in PCI configuration space that provides for video BIOS ROM address relocation.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	ADE

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIOS ROM BASE ADDRESS															

Bit 0 ADE - Address Decode Enable
0 = Accesses to the BIOS ROM address space defined in this register are disabled
1 = Accesses to the BIOS ROM address space defined in this register are enabled

Bits 15–1 Reserved

Bits 31–16 BIOS ROM BASE ADDRESS

These are the upper 16 bits of the BIOS ROM address.

Interrupt Line

Read/Write Address: 3CH
Power-On Default: 00H

This register contains interrupt line routing information written by the POST program during power-on initialization.

7	6	5	4	3	2	1	0
INTERRUPT LINE							

Bits 7–0 INTERRUPT LINE

Interrupt Pin

Read Only Address: 3DH
Power-On Default: 01H

This register specifies that $\overline{\text{INTA}}$ is the interrupt pin used.

7	6	5	4	3	2	1	0
INTERRUPT PIN							

Bits 7–0 INTERRUPT PIN

value = 01H (hardwired)

Appendix A: Register Reference

This Appendix contains tables listing all the registers in each of categories corresponding to Sections 16-23 of this data book.

- VGA
- S3 VGA
- System Control
- System Extension
- Enhanced Commands
- Streams Processor
- LPB
- PCI Configuration Space

Within each table, registers are listed in order of increasing addresses/indices. Name, address, register bit descriptions with read/write status and the page number of the detailed register description are provided for each register. All addresses and indices are hexadecimal values.

A.1 VGA REGISTERS

? = B for monochrome, D for color.

Table A-1. VGA Registers

Address	Index Bit(s)		Register Name Bit Description	Description Page
General or External Registers				
3C2			**Miscellaneous Output**	**16-1**
	0	W	Color emulation. Address based at 3Dx	
	1	W	Enable CPU access of video memory	
	3-2	W	Video DCLK select. Enable DCLK PLL loading	
	4	W	Reserved	
	5	W	Select the high 64K page of memory	
	6	W	Make HSYNC an active low signal	
	7	W	Make VSYNC an active low signal	
3CC			**Miscellaneous Output**	**16-1**
	0	R	Color emulation. Address based at 3Dx	
	1	R	Enable CPU access of video memory	
	3-2	R	Video DCLK select. Enable DCLK PLL loading	
	4	R	Reserved	
	5	R	Select the high 64K page of memory	
	6	R	Make HSYNC an active low signal	
	7	R	Make VSYNC an active low signal	
3?A			**Feature Control**	**16-2**
	2-0	W	Reserved	
	3	W	VSYNC is ORed with the internal display enable signal	
	7-4	W	Reserved	
3CA			**Feature Control**	**16-2**
	2-0	R	Reserved	
	3	R	VSYNC is ORed with the internal display enable signal	
	7-4	R	Reserved	
3C2			**Input Status 0**	**16-3**
	3-0	R	Reserved	
	4	R	The internal SENSE signal is a logical 1	
	6-5	R	Reserved	
	7	R	Vertical retrace interrupt to the CPU is pending	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?A			**Input Status 1**	**16-3**
	0	R	The display in not in active display mode	
	1	R	Reserved	
	2	R	Reserved =1	
	3	R	Vertical retrace period is active	
	5-4	R	Feedback of two color outputs for test purposes	
	7-6	R	Reserved	
3C3			**Video Subsystem Enable**	**16-4**
	0	W	Enable VGA display	
	7-1	R/W	Reserved	
Sequencer Registers				
3C4			**Sequencer Index**	**16-5**
	4-0	R/W	Index to the sequencer register to be accessed	
	7-5	R/W	Reserved	
3C5			**Sequencer Data**	**16-5**
	7-0	R/W	Data to or from the sequencer register accessed	
3C5	**00**		**Reset (SR0)**	**16-6**
	0	R/W	Asynchronous reset (not functional for the Trio64V+)	
	1	R/W	Synchronous reset (not functional for the Trio64V+)	
	7-2	R/W	Reserved	
3C5	**01**		**Clocking Mode (SR1)**	**16-6**
	0	R/W	Character clocks are 8 dots wide	
	1	R/W	Reserved	
	2	R/W	Load the video serializers every second character clock	
	3	R/W	The internal character clock is 1/2 the DCLK frequency	
	4	R/W	Load the video serializers every fourth character clock	
	5	R/W	Screen is turned off	
3C5	**02**		**Enable Write Plane (SR2)**	**16-7**
	3-0	R/W	Enables a CPU write to the corresponding color plane	
	7-4	R/W	Reserved	
3C5	**03**		**Character Font Select (SR3)**	**16-8**
	4, 1-0	R/W	Select Font B	
	5,3-2	R/W	Select Font A	
	7-6	R/W	Reserved	
3C5	**04**		**Memory Mode Control (SR4)**	**16-9**
	0	R/W	Reserved	
	1	R/W	Memory access to 256K allowed (required for VGA)	
	2	R/W	Sequential addressing for CPU video memory accesses	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
	3	R/W	Modulo 4 addressing for CPU video memory accesses	
	7-4	R/W	Reserved	
3C5	**08**		**Unlock Extended Sequencer (SR8)**	**16-10**
	7-0	R/W	Load xxxx0110b to unlock SR9-SR1C	
3C5	**09**	**R/W**	**Extended Sequencer 9**	**16-10**
	6-0	R/W	Reserved	
	7	R/W	Memory-mapped I/O only (no PIO)	
3C5	**0A**		**Extended Sequencer A (SRA)**	**16-10**
	4-0	R/W	Reserved	
	5	R/W	PD[63:0] not tri-stated	
	6	R/W	Pin 50 is $\overline{\text{RAS1}}$	
	7	R/W	2 MCLK memory writes	
3C5	**0B**		**Extended Sequencer B (SRB)**	**16-11**
	0	R/W	Use VCLKI for internal dot clock functions (test only)	
	1	R/W	Pixel data from VAFC latched by VCLKI	
	2	R/W	Reserved	
	3	R/W	Enable 24 bits/pixel	
	7-4	R/W	Specify color mode for feature connector input	
3C5	**0D**		**Extended Sequencer D (SRD)**	**16-12**
	0	R/W	Enable feature connector operation	
	1	R/W	Select LPB feature connector	
	3-2	R/W	Reserved	
	5-4	R/W	HSYNC control for Green PC requirements	
	7-6	R/W	VSYNC control for Green PC requirements	
3C5	**10**		**MCLK Value Low (SR10)**	**16-13**
	4-0	R/W	MCLK N-divider value	
	6-5	R/W	MCLK R value	
	7	R/W	Reserved	
3C5	**11**		**MCLK Value High (SR11)**	**16-14**
	6-0	R/W	MCLK M-divider value	
	7	R/W	Reserved	
3C5	**12**		**DCLK Value Low (SR12)**	**16-14**
	4-0	R/W	DCLK N-divider value	
	6-5	R/W	DCLK R value	
	7	R/W	Reserved	
3C5	**13**		**DCLK Value High (SR13)**	**16-15**
	6-0	R/W	DCLK M-divider value	
	7	R/W	Reserved	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**14**		**CLKSYN Control 1 (SR14)**	**16-15**
	0	R/W	DCLK PLL powered down (test only)	
	1	R/W	MCLK PLL powered down (test only)	
	3	R/W	Test MCLK (test only)	
	4	R/W	Clear clock synthesizer counters (test only)	
	5	R/W	Pin 146 tri-stated	
	6	R/W	MCLK is input on pin 146 (test only)	
	7	R/W	DCLK is input on pin 156 (test only)	
3C5	**15**		**CLKSYN Control 2 (SR15)**	**16-17**
	0	R/W	Load new MCLK frequency	
	1	R/W	Load new DCLK frequency	
	2	R/W	MCLK output on pin 147 (test only)	
	3	R/W	VCLK direction determined by EVCLK	
	4	R/W	Divide DCLK by 2	
	5	R/W	Load MCLK and DCLK PLL values immediately	
	6	R/W	Invert DCLK	
	7	R/W	Enable 2 MCLK memory writes	
3C5	**16**		**CLKSYN Test High (SR16)**	**16-18**
	7-0	R/W	Reserved	
3C5	**17**		**CLKSYN Test High (SR17)**	**16-18**
	7-0	R/W	Reserved	
3C5	**18**		**RAMDAC/CLKSYN Control (SR18)**	**16-19**
	0	R/W	RAMDAC test counter enabled (test only)	
	1	R/W	Reset RAMDAC test counter	
	2	R/W	Place red data on internal data bus (test only)	
	3	R/W	Place green data on internal data bus (test only)	
	4	R/W	Place blue data on internal data bus (test only)	
	5	R/W	Power-down RAMDAC	
	6	R/W	Select 1 cycle LUT write	
	7	R/W	RAMDAC clock doubled mode enabled	
3C5	**1C**		**Extended Sequencer 1C (SR1C)**	**16-20**
	1-0	R/W	Select functions for pins 151 and 190	
	1	R/W	Reserved	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
CRT Controller Registers				
3?4			**CRT Controller Index**	**16-21**
	7-0	R/W	Index to the CRTC register to be accessed	
3?5			**CRT Controller Data**	**16-21**
	7-0	R/W	Data to or from the CRTC register accessed	
3?5	**00**		**Horizontal Total (CR0)**	**16-22**
	7-0	R/W	Number of characters in a line -5	
3?5	**01**		**Horizontal Display End (CR1)**	**16-22**
	7-0	R/W	One less than the total number of displayed characters	
3?5	**02**		**Start Horizontal Blank (CR2)**	**16-23**
	7-0	R/W	Character count where horizontal blanking starts	
3?5	**03**		**End Horizontal Blank (CR3)**	**16-23**
	4-0	R/W	End position of horizontal blanking	
	6-5	R/W	Display enable skew in character clocks	
	7	R/W	Reserved	
3?5	**04**		**Start Horizontal Sync Position (CR4)**	**16-24**
	7-0	R/W	Character count where HSYNC goes active	
3?5	**05**		**End Horizontal Sync Position (CR5)**	**16-24**
	4-0	R/W	Position where HSYNC goes inactive	
	6-5	R/W	Horizontal retrace end delay in character clocks	
	7	R/W	End horizontal blanking bit 5	
3?5	**06**		**Vertical Total (CR6)**	**16-25**
	7-0	R/W	Number of lines - 2	
3?5	**07**		**CRTC Overflow (CR7)**	**16-25**
	0	R/W	Vertical total bit 8	
	1	R/W	Vertical display end bit 8	
	2	R/W	Vertical retrace start bit 8	
	3	R/W	Start vertical blank bit 8	
	4	R/W	Line compare bit 8	
	5	R/W	Vertical total bit 9	
	6	R/W	Vertical display end bit 9	
	7	R/W	Vertical retrace start bit 9	
3?5	**08**		**Preset Row Scan (CR8)**	**16-26**
	4-0	R/W	Line where first character row begins	
	6-5	R/W	Number of bytes to pan horizontally	
	7	R/W	Reserved	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**09**		**Maximum Scan Line (CR9)**	**16-26**
	4-0	R/W	Character height in scan lines -1	
	5	R/W	Start vertical blank bit 9	
	6	R/W	Line compare bit 9	
	7	R/W	Double scanning (repeat each line) enabled	
3?5	**0A**		**Cursor Start Scan Line (CRA)**	**16-27**
	4-0	R/W	Cursor starting line within the character cell	
	5	R/W	Turns off the cursor	
	7-6	R/W	Reserved	
3?5	**0B**		**Cursor End Scan Line (CRB)**	**16-27**
	4-0	R/W	Cursor ending line within the character cell	
	6-5	R/W	Cursor skew to right in characters	
	7	R/W	Reserved	
3?5	**OC**		**Start Address High (CRC)**	**16-28**
	7-0	R/W	Bits 15-8 of the display start address	
3?5	**OD**		**Start Address Low (CRD)**	**16-28**
	7-0	R/W	Bits 7-0 of the display start address	
3?5	**OE**		**Cursor Location Address High (& Hardware Cursor Foreground Color in Enhanced Mode) (CRE)**	**16-28**
	7-0	R/W	Bits 15-8 of the cursor location start address	
3?5	**OF**		**Cursor Location Address Low (& Hardware Cursor Background Color in Enhanced Mode) (CRF)**	**16-28**
	7-0	R/W	Bits 7-0 of the cursor location start address	
3?5	**10**		**Vertical Retrace Start (CR10**	**16-29**
	7-0	R/W	Vertical retrace start in scan lines	
3?5	**11**		**Vertical Retrace End (CR11)**	**16-29**
	3-0	R/W	Vertical retrace end in scan lines	
	4	R/W	Clear the vertical retrace interrupt flip-flop	
	5	R/W	Disable vertical interrupts	
	6	R/W	Five RAM refresh cycles per horizontal line	
	7	R/W	Lock writes to CR0-CR7	
3?5	**12**		**Vertical Display End (CR12)**	**16-30**
	7-0	R/W	Number of scan lines of active video	
3?5	**13**		**Offset (CR13)**	**16-30**
	7-0	R/W	Memory start address jump from one scan line to the next	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**14**		**Underline Location (CR14)**	**16-31**
	4-0	R/W	Horizontal scan line where underline occurs	
	5	R/W	Memory address counter increment is 4 character clocks	
	6	R/W	Memory accessed as doublewords	
	7	R/W	Reserved	
3?5	**15**		**Start Vertical Blank (CR15)**	**16-31**
	7-0	R/W	Horizontal scan line where vertical blanking starts	
3?5	**16**		**End Vertical Blank (CR16)**	**16-32**
	7-0	R/W	Horizontal scan line where vertical blanking ends	
3?5	**17**		**CRTC Mode Control (CR17)**	**16-32**
	0	R/W	Enable bank 2 mode for CGA emulation	
	1	R/W	Enable bank 4 mode for CGA emulation	
	2	R/W	Use horizontal retrace clock divided by 2	
	3	R/W	Enable count by 2 mode	
	4	R/W	Reserved	
	5	R/W	Enable CGA mode address wrap	
	6	R/W	Use byte address mode	
	7	R/W	Horizontal and vertical retrace signals enabled	
3?5	**18**		**Line Compare (CR18)**	**16-34**
	7-0	R/W	Line at which memory address counter cleared to 0	
3?5	**22**		**CPU Latch Data (CR22)**	**16-34**
	7-0	R	Value in the CPU latch in the graphics controller	
3?5	**24,26**		**Attribute Controller Flag/Index**	**16-35**
	5-0	R	Value of the attribute controller index data at 3C0H	
	6	R	Reserved	
	7	R	State of inverted internal address flip-flop	
Graphics Controller Registers				
3CE			**Graphics Controller Index**	**16-36**
	3-0	R/W	Index to the graphics controller register to be accessed	
	7-4	R/W	Reserved	
3CF			**Graphics Controller Data**	**16-36**
	7-0	R/W	Data to or from the graphics controller register accessed	
3CF	**00**		**Set/Reset (GR0)**	**16-37**
	3-0	R/W	Color value for CPU memory writes	
	7-4	R/W	Reserved	
3CF	**01**		**Enable Set/Reset (GR1)**	**16-37**
	3-0	R/W	Enable planes for writing GR0 data	
	7-4	R/W	Reserved	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3CF	**02**		**Color Compare (GR2)**	**16-38**
	3-0	R/W	Reference color for color compare operations	
	7-4	R/W	Reserved	
3CF	**03**		**Raster Operation/Rotate Counter (GR3)**	**16-38**
	2-0	R/W	Number of right rotate positions for a CPU memory write	
	4-3	R/W	Select raster operation (logical function)	
	7-5	R/W	Reserved	
3CF	**04**		**Read Plane Select (GR4)**	**16-39**
	1-0	R/W	Select planes for reading	
	7-2	R/W	Reserved	
3CF	**05**		**Graphics Controller Mode (GR5)**	**16-40**
	1-0	R/W	Select write mode	
	2	R/W	Reserved	
	3	R/W	Enable read compare operation	
	4	R/W	Select odd/even addressing	
	5	R/W	Select odd/even shift mode	
	6	R/W	Select 256 color shift mode	
	7	R/W	Reserved	
3CF	**06**		**Memory Map Mode Control (GR6)**	**16-41**
	0	R/W	Select graphics mode memory addressing	
	1	R/W	Chain odd/even planes	
	3-2	R/W	Select memory mapping	
	7-4	R/W	Reserved	
3CF	**07**		**Color Don't Care (GR7)**	**16-42**
	3-0	R/W	Select color plane used for color comparison	
	7-4	R/W	Reserved	
3CF	**08**		**Bit Mask (GR8)**	**16-42**
	7-0	R/W	Each bit is a mask for the corresponding memory plane bit	
Attribute Registers				
3C0			**Attribute Controller Index**	**16-43**
	4-0	R/W	Index to the attribute controller register to be accessed	
	5	R/W	Enable video display	
	7-6	R/W	Reserved	
3C1/0			**Attribute Controller Data**	**16-44**
	7-0	R/W	Data to or from the attribute controller register accessed	
3C1/0	**00–0F**		**Palette Register (AR0–ARF)**	**16-44**
	5-0	R/W	Color value	
	7-6	R/W	Reserved	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C1/0	**10**		**Attribute Mode Control (AR10**	**16-45**
	0	R/W	Select graphics mode	
	1	R/W	Select monochrome display	
	2	R/W	Enable line graphics characters	
	3	R/W	Enable blinking	
	4	R/W	Reserved	
	5	R/W	Enable top panning	
	6	R/W	Select 256 color mode	
	7	R/W	Bits 5-4 of video output come from AR14_1-0	
3C1/0	**11**		**Border Color (AR11)**	**16-46**
	7-0	R/W	Border color value	
3C1/0	**12**		**Color Plane Enable (AR12)**	**16-46**
	3-0	R/W	Display plane enable	
	5-4	R/W	Select inputs to bits 5-4 of 3?AH	
	7-6	R/W	Reserved	
3C1/0	**13**		**Horizontal Pixel Panning (AR13)**	**16-47**
	3-0	R/W	Number of pixels to shift the display to the left	
	7-4	R/W	Reserved	
3C1/0	**14**		**Pixel Padding (AR14)**	**16-48**
	1-0	R/W	Bits 5-4 of the video output if AR10_7 = 1	
	3-2	R/W	Bits 7-6 of the video output	
	7-4	R/W	Reserved	
RAMDAC Registers				
3C6			**DAC Mask**	**16-49**
	7-0	R/W	Pixel read mask	
3C7			**DAC Read Index**	**16-49**
	7-0	W	Index to palette register to be read	
3C7			**DAC Status**	**16-50**
	1-0	R	Shows whether previous DAC cycle was a read or write	
	7-2	R	Reserved	
3C8	–		**DAC Write Index**	**16-50**
	7-0	R/W	Index to palette register to be written or General Input Port read data	
3C9			**DAC Data**	**16-51**
	7-0	R/W	Data from register pointed to by DAC Read or Write Index	

A.2 S3 VGA REGISTERS

The Trio64V+ has additional registers described in Table A-2 that are located in CRT Controller address space at locations not used by IBM. All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, the Register Lock 1 register (CR38) must be loaded with a binary unlock key pattern (see the register description). The registers will remain unlocked until the key pattern is reset. ? = B for monochrome, D for color.

Table A-2. S3 VGA Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**2D**		**Device ID High (CR2D)**	**17-1**
	7-0	R	High byte of device ID (88H)	
3?5	**2E**		**Device ID Low (CR2E)**	**17-2**
	7-0	R	Low byte of device ID (11H)	
3?5	**2F**		**Revision (CR2F)**	**17-2**
	7-0	R	4x	
3?5	**30**		**Chip ID/Rev (CR30)**	**17-2**
	3-0	R	Chip Identification - EH	
	7-4	R	Chip revision status (stepping) - See CR2F	
3?5	**31**		**Memory Configuration (CR31)**	**17-3**
	0	R/W	Enable base address offset (CR6A_6-0)	
	1	R/W	Enable two-page screen image	
	2	R/W	Enable VGA 16-Bit Memory Bus Width	
	3	R/W	Use Enhanced mode memory mapping	
	5-4	R/W	Old display start address bits 17-16 (see CR69_3-0)	
	6	R/W	Enable high speed text display font fetch mode	
	7	R/W	Reserved	
3?5	**32**		**Backward Compatibility 1 (CR32)**	**17-4**
	3-0	R/W	Reserved	
	4	R/W	Enable interrupt generation	
	5	R/W	Reserved	
	6	R/W	Use standard VGA memory wrapping at 256K boundary	
	7	R/W	Reserved	
3?5	**33**		**Backward Compatibility 2 (CR33)**	**17-5**
	0	R/W	Reserved	
	1	R/W	Disable write protection provided by CR11_7 on CR7_1,6	
	2	R/W	Reserved	
	3	R/W	VCLK is inverted DCLK	
	4	R/W	Disable writes to RAMDAC registers (3C6H-3C9H)	
	5	R/W	$\overline{\text{BLANK}}$ signal active during entire non-active video period	
	6	R/W	Disable writes to Palette/Overscan registers (AR0-ARF)	
	7	R/W	Reserved	

Table A-2. S3 VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**34**		**Backward Compatibility 3 (CR34)**	**17-6**
	0	R/W	PCI DAC snoop method select	
	1	R/W	Disable PCI master abort handling during DAC snoop	
	2	R/W	Disable PCI retry handling during DAC snoop	
	3	R/W	Reserved	
	4	R/W	Enable Display Start FIFO Fetch register (CR3B)	
	7-5	R/W	Reserved	
3?5	**35**		**CRT Register Lock (CR35)**	**17-7**
	3-0	R/W	Old CPU base address (see CR6A_6-0)	
	4	R/W	Lock Vertical Timing registers	
	5	R/W	Lock Horizontal Timing registers	
	7-6	R/W	Reserved	
3?5	**36**		**Configuration 1 (CR36)**	**17-8**
	1-0	R	Select System bus (PCI or VL-Bus)	
	3-2	R/W	Select Memory page mode (fast page, EDO or 1-cycle EDO)	
	4	R/W	Enable BIOS ROM accesses (VL-Bus)	
	7-5	R/W	Define display memory size	
3?5	**37**		**Configuration 2 (CR37)**	**17-8**
	0	R/W	Enable Trio32/64 operation (VL-Bus)	
	1	R/W	Reserved	
	2	R/W	Select 32K or 64K BIOS ROM size (VL-Bus)	
	3	R/W	Use internal MCLK, DCLK	
	4	R/W	Define RAMDAC write snooping (VL-Bus)	
	7-5	R/W	Reserved	
3?5	**38**		**Register Lock 1 (CR38)**	**17-10**
	7-0	R/W	Unlock S3 VGA registers (CR30-CR3C)	
3?5	**39**		**Register Lock 2 (CR39)**	**17-10**
	7-0	R/W	Unlock System Control, System Extension and Strapping registers (CR40-CR4F, CR50-CR6D)	
3?5	**3A**		**Miscellaneous 1 (CR3A)**	**17-10**
	1-0	R/W	Select alternate refresh count per horizontal line	
	2	R/W	Enable alternate refresh count (CR3A_1-0)	
	3	R/W	Enable simultaneous VGA text and Enhanced modes	
	4	R/W	Enable 8-, 16- or 24/32-bit color Enhanced modes	
	5	R/W	Enable high speed text font writing	
	6	R/W	Reserved	
	7	R/W	Disable PCI bus read burst cycles	

Table A-2. S3 VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**3B**		**Start Display FIFO Fetch (CR3B)**	**17-11**
	7-0	R/W	Specify start of display FIFO fetches for screen refreshing	
3?5	**3C**		**Interlace Retrace Start (CR3C)**	**17-12**
	7-0	R/W	Specify interlaced mode retrace start position	

A.3 SYSTEM CONTROL REGISTERS

System Control registers are configuration registers, mode control registers, and hardware graphics cursor control registers. They are positioned in the same indexed register space as VGA S3 registers. All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, the Register Lock 2 register (CR39) must be loaded with a binary unlock key pattern (see the register description). The registers will remain unlocked until the key pattern is reset. ? = B for monochrome, D for color.

The following table summarizes the System Control registers.

Table A-3. System Control Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**40**		**System Configuration (CR40)**	**18-1**
	0	R/W	Enable Enhanced mode register access	
	3-1	R/W	Reserved	
	4	R/W	Ready (Wait State) Control (VL-Bus)	
	5	R/W	Reserved = 1	
	7-6	R/W	Reserved	
3?5	**41**		**BIOS Flag (CR41)**	**18-2**
	7-0	R/W	Used by the video BIOS	
3?5	**42**		**Mode Control (CR42)**	**18-2**
	4-0	R/W	Reserved	
	5	R/W	Select Interlaced mode	
	6	R/W	Reserved	

Table A-3. System Control Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**43**		**Extended Mode (CR43)**	**18-2**
	1-0	R/W	Reserved	
	2	R/W	Old logical screen width bit 8	
	6-3	R/W	Reserved	
	7	R/W	Enable horizontal counter double mode	
3?5	**45**		**Hardware Graphics Cursor Mode (CR45)**	**18-3**
	0	R/W	Enable hardware graphics cursor	
	3-1	R/W	Reserved	
	4	R/W	Set up space at right of bit map for hardware cursor	
	7-5	R/W	Reserved	
3?5	**46–47**		**Hardware Graphics Cursor Origin-X (CR46-CR47)**	**18-3**
	10-0	R/W	X-coordinate of the hardware cursor left side	
	15-11	R/W	Reserved	
3?5	**48–49**		**Hardware Graphics Cursor Origin-Y (CR48-CR49)**	**18-4**
	10-0	R/W	Y-coordinate of the hardware cursor upper line	
	15-11	R/W	Reserved	
3?5	**4A**		**Hardware Graphics Cursor Foreground Stack (CR4A)**	**18-4**
	7-0	R/W	Hardware cursor foreground color (3 registers)	
3?5	**4B**		**Hardware Graphics Cursor Background Stack (CR4B)**	**18-4**
	7-0	R/W	Hardware cursor background color (3 registers)	
3?5	**4C–4D**		**Hardware Graphics Cursor Start Address (CR4C-CR4D)**	**18-5**
	12-0	R/W	Hardware cursor start address	
	15-13	R/W	Reserved	
3?5	**4E**		**Hardware Graphics Cursor Pattern Display Start X-Pixel Position (CR4E)**	**18-5**
	5-0	R/W	Hardware cursor display start x-coordinate	
	7-6	R/W	Reserved	
3?5	**4F**		**Hardware Graphics Cursor Pattern Display Start Y-Pixel Position (CR4F)**	**18-5**
	5-0	R/W	Hardware cursor display start y-coordinate	
	7-6	R/W	Reserved	

A.4 SYSTEM EXTENSION REGISTERS

These registers provide extended system and memory control, external sync control and addressing window control. They are enabled in the same way as the System Control registers via the Register Lock 2 register (CR39). ? = B for monochrome, D for color.

Table A-4. System Extension Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**50**		**Extended System Cont 1 (CR50)**	**19-1**
	0	R/W	Most significant bit of screen width definition (see bits 7-6)	
	3-1	R/W	Reserved	
	5-4	R/W	Pixel length select	
	7-6	R/W	With bit 0, screen width definition	
3?5	**51**		**Extended System Cont 2 (CR51)**	**19-2**
	1-0	R/W	Old display start address bits 19-18	
	3-2	R/W	Old CPU base address bits 19-18	
	5-4	R/W	Logical screen width bits 9-8	
	7-6	R/W	Reserved	
3?5	**52**		**Extended BIOS Flag 1 (CR52)**	**19-3**
	7-0	R/W	Used by the video BIOS	
3?5	**53**		**Extended Memory Cont 1 (CR53)**	**19-3**
	0	R/W	Reserved	
	2-1	R/W	Big endian byte swap select for linear addressing	
	4-3	R/W	Memory-mapped I/O type select	
	5	R/W	MMIO window select (A8000H or B8000H)	
	6	R/W	Enable nibble swap	
	7	R/W	Reserved	
3?5	**54**		**Extended Memory Cont 2 (CR54)**	**19-4**
	1-0	R/W	Big endian byte swap select (not linear addressing or image transfers)	
	2, 7-3	R/W	Specify M parameter for display FIFO control	
3?5	**55**		**Extended DAC Control (CR55)**	**19-4**
	1-0	R/W	Reserved	
	2	R/W	Enable General Input Port read	
	3	R/W	Reserved	
	4	R/W	Enable X-11 windows hardware cursor mode	
	6-5	R/W	Reserved	
	7	R/W	VCLK output pin is tri-stated	
3?5	**56**		**External Sync Cont 1 (CR56)**	**19-5**
	0	R/W	Reserved	
	1	R/W	HSYNC output buffer tri-stated	

Table A-4. System Extension Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**56**		**External Sync Cont 1 (CR56)**	**19-5**
	2	R/W	VSYNC output buffer tri-stated	
	7-3	R/W	Reserved	
3?5	**58**		**Linear Address Window Control (CR58)**	**19-6**
	1-0	R/W	Linear addressing window size	
	2	R/W	Reserved	
	3	R/W	Address latch timing control (VL-Bus)	
	4	R/W	Enable linear addressing	
	6-5	R/W	Reserved	
	7	R/W	$\overline{\text{RAS}}$ timing adjustment	
3?5	**59-5A**		**Linear Address Window Position (CR59-5A)**	**19-7**
	15-0	R/W	Linear addressing window position bits 31-16	
3?5	**5C**		**General Out Port (CR5C)**	**19-8**
	7-0	R/W	General Output Port	
3?5	**5D**		**Extended Horizontal Overflow (CR5D)**	**19-8**
	0	R/W	Horizontal total bit 8 (CR0)	
	1	R/W	Horizontal display end bit 8 (CR1)	
	2	R/W	Start horizontal blank bit 8 (CR2)	
	3	R/W	End horizontal blank bit 7 (CR3, CR5)	
	4	R/W	Start horizontal sync position bit 8 (CR4)	
	5	R/W	End horizontal sync position bit 6 (CR5)	
	6	R/W	Start FIFO Fetch bit 8 (CR3B)	
	7	R/W	Reserved	
3?5	**5E**		**Extended Vertical Overflow (CR5E)**	**19-9**
	0	R/W	Vertical total bit 10 (CR6)	
	1	R/W	Vertical display end bit 10 (CR12)	
	2	R/W	Start vertical blank bit 10 (CR15)	
	3	R/W	Reserved	
	4	R/W	Vertical retrace start bit 10 (CR10)	
	5	R/W	Reserved	
	6	R/W	Line compare position bit 10 (CR18)	
	7	R/W	Reserved	

Table A-4. System Extension Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**60**		**Extended Memory Control 3 (CR60)**	**19-9**
	7-0	R/W	Specify N parameter for display FIFO control	
3?5	**61**		**Extended Memory Control 4 (CR61)**	**19-10**
	4-0	R/W	Reserved	
	6-5	R/W	Big endian byte swap select for image writes	
	7	R/W	Reserved	
3?5	**65**		**Extended Miscellaneous Control (CR65)**	**19-10**
	2-0	R/W	Reserved	
	4-3	R/W	Delay $\overline{\text{BLANK}}$ by DCLK	
	7-5	R/W	Reserved	
3?5	**66**		**Extended Miscellaneous Control 1 (CR66)**	**19-11**
	0	R/W	Enable enhanced functions	
	1	R/W	Software reset of the Graphics Engine	
	2	R/W	Reserved	
	3	R/W	PCI disconnect on write with FIFO full or read with FIFO empty	
	5-4	R/W	Reserved	
	6	R/W	PA[15:0] are tri-stated off	
	7	R/W	Enable PCI bus disconnect	
3?5	**67**		**Extended Miscellaneous Control 2 (CR67)**	**19-12**
	0	R/W	VCLK is in phase with DCLK	
	1	R/W	Reserved	
	3-2	R/W	Streams Processor mode select	
	7-4	R/W	Select RAMDAC color mode	
3?5	**68**		**Configuration 3 (CR68)**	**19-13**
	0	R/W	$\overline{\text{CAS}}$, $\overline{\text{OE}}$ stretch time selection	
	1	R/W	Reserved	
	2	R/W	$\overline{\text{RAS}}$ low timing select	
	3	R/W	$\overline{\text{RAS}}$ precharge timing select	
	6-4	R/W	Video BIOS area	
	7	R/W	Memory data bus size select	
3?5	**69**		**Extended System Control 3 (CR69)**	**19-14**
	4-0	R/W	Display start address bits 19-16	
	7-5	R/W	Reserved	
3?5	**6A**		**Extended System Control 4 (CR6A)**	**19-14**
	5-0	R/W	CPU base address bits 19-14	
	7-6	R/W	Reserved	

Table A-4. System Extension Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**6B**		**Extended BIOS Flag 3 (CR6B)**	**19-15**
	7-0	R/W	Used by the video BIOS	
3?5	**6C**		**Extended BIOS Flag 4 (CR6C)**	**19-15**
	7-0	R/W	Used by the video BIOS	
3?5	**6D**		**Extended BIOS Flag 5 (CR6D)**	**19-15**
	7-0	R/W	Used by the video BIOS	
3?5	**6E**		**Extended BIOS Flag 6 (CR6E)**	**19-16**
	7-0	R/W	Used by the video BIOS	
3?5	**6F**		**Configuration 4 (CRF)**	**19-16**
	0	R/W	Select LPB vs Trio64-compatible mode	
	1	R/W	Select I/O address for MMFF20	
	2	R/W	Disable effect of bit 1 of this register	
	4-3	R/W	$\overline{WE}$ delay	
	7-5	R/W	Reserved	

A.5 ENHANCED COMMANDS REGISTERS

This section lists the registers which support the Trio64V+ enhanced drawing functions. All of these registers are enabled only if bit 0 of the System Configuration register (CR40) is set to 1.

Table A-5. Enhanced Commands Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
42E8			**Subsystem Status**	**20-1**
	0	R	Vertical sync interrupt status	
	1	R	Graphics Engine busy interrupt status	
	2	R	Command FIFO overflow interrupt status	
	3	R	Command FIFO empty interrupt status	
	6-4	R	Reserved	
	7	R	4 or 8 bit planes	
	15-8	R	Reserved	
42E8			**Subsystem Control**	**20-2**
	0	W	Clear vertical sync interrupt status	
	1	W	Clear Graphics Engine busy interrupt status	
	2	W	Clear Command FIFO overflow interrupt status	
	3	W	Clear Command FIFO empty interrupt status	
	7-4	W	Reserved	
	8	W	Vertical sync interrupt enabled	
	9	W	Graphics Engine busy interrupt enabled	
	10	W	Command FIFO overflow interrupt enabled	
	11	W	Command FIFO empty interrupt enabled	
	13-12	W	Reserved	
	15-14	W	Graphics Engine software reset selection	
4AE8			**Advanced Function Control**	**20-3**
	0	R/W	Enable Enhanced mode functions	
	1	R/W	Reserved	
	2	R/W	Specify 4 bits/pixel Enhanced mode	
	3	R/W	Reserved	
	4	R/W	Enable linear addressing	
	15-5	R/W	Reserved	
82E8			**Current Y-Position**	**20-4**
	11-0	R/W	Pixel vertical screen coordinate	
	15-12	R/W	Reserved	
86E8			**Current X-Position**	**20-4**
	11-0	R/W	Pixel horizontal screen coordinate	
	15-12	R/W	Reserved	

Table A-5. Enhanced Commands Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
8AE8			**Destination Y Position/Axial Step Constant**	**20-5**
	11-0/ 13-0	R/W	Specifies ending vertical coordinate or axial step constant for a number of drawing commands	
	15-12	R/W	Reserved (Bits 15-14 for step constant)	
8EE8			**Destination X Position/Diagonal Step Constant**	**20-5**
	11-0/ 13-0	R/W	Specifies ending horizontal coordinate or diagonal step constant for a number of drawing commands	
	15-12	R/W	Reserved (Bits 15-14 for step constant)	
92E8			**Line Error Term**	**20-6**
	13-0	R/W	Error term for line draws	
	15-14	R/W	Reserved	
96E8			**Major Axis Pixel Count**	**20-6**
	11-0	R/W	Length of the longest axis (pixels - 1)	
	15-12	R/W	Reserved	
9AE8			**Graphics Processor Status**	**20-7**
	7-0	R	Low 8 bits of field showing FIFO slots available (see bits 15-11)	
	8	R	Reserved	
	9	R	Graphics Engine busy	
	10	R	All FIFO slots empty	
	15-11	R	High 5 bits of FIFO status (see bits 7-0)	
9AE8			**Drawing Command**	**20-8**
	0	W	Must be programmed to 1	
	1	W	Select across the plane pixel mode	
	2	W	Last pixel will not be drawn	
	3	W	Select radial drawing direction	
	4	W	Draw pixels	
	7-5	W	Select drawing direction	
	8	W	Wait for CPU data	
	10-9	W	Select system bus size	
	11	W	Reserved	
	12	W	Enable byte swap	
	15-13	W	Select command type	

Table A-5. Enhanced Commands Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
9EE8			**Short Stroke Vector Transfer**	**20-10**
	3-0	W	Length of vector 1 (pixels - 1)	
	4	W	Draw pixels	
	7-5	W	Select drawing direction	
	15-8	W	Duplicate of bits 7-0 to define second short stroke vector	
A2E8			**Background Color**	**20-11**
	31-0	R/W	Background color value	
A6E8			**Foreground Color**	**20-11**
	31-0	R/W	Foreground Color value	
AAE8			**Bitplane Write Mask**	**20-12**
	31-0	R/W	Each bit enables updating of corresponding bit plane	
AEE8			**Bitplane Read Mask**	**20-12**
	31-0	R/W	Each bit enables reading of corresponding bit plane	
B2E8			**Color Compare**	**20-13**
	31-0	R/W	Color value to be compared with current bitmap color	
B6E8			**Background Mix**	**20-13**
	3-0	W	Select mix type	
	4	W	Reserved	
	6-5	W	Select color source	
	15-7	W	Reserved	
BAE8			**Foreground Mix**	**20-13**
	3-0	W	Select mix type	
	4	W	Reserved	
	6-5	W	Select color source	
	15-7	W	Reserved	
BEE8			**Read Register Data**	**20-14**
	15-0	R	Data from register selected by bits 2-0 of BEE8H_E	
BEE8	**0**		**Minor Axis Pixel Count**	**20-15**
	11-0	W	Rectangle height (pixels - 1)	
	15-12	W	Reserved	
BEE8	**1**		**Top Scissors**	**20-15**
	11-0	W	Top side of the clipping rectangle	
	15-12	W	Reserved	
BEE8	**2**		**Left Scissors**	**20-15**
	11-0	W	Left side of the clipping rectangle	
	15-12	W	Reserved	

Table A-5. Enhanced Commands Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
BEE8	**3**		**Bottom Scissors**	**20-16**
	11-0	W	Bottom side of the clipping rectangle	
	15-12	W	Reserved	
BEE8	**4**		**Right Scissors**	**20-16**
	11-0	W	Right side of the clipping rectangle	
	15-12	W	Reserved	
BEE8	**A**		**Pixel Control**	**20-16**
	5-0	W	Reserved	
	7-6	W	Select mix register	
	11-8	W	Reserved	
	15-12	W	0AH (index)	
BEE8	**D**		**Multifunction Control Miscellaneous 2**	**20-17**
	2-0	W	Destination base address location in memory	
	3	W	Reserved	
	6-4	W	Source base address location in memory	
	11-7	W	Reserved	
	15-12	W	0DH (index)	
BEE8	**E**		**Multifunction Control Miscellaneous**	**20-18**
	1-0	W	Destination base address bits 21-20	
	3-2	W	Source base address bits 21-20	
	4	W	Select upper word for 32-bit register accesses	
	5	W	Only pixels outside the clipping rectangle are drawn	
	6	W	Reserved	
	7	W	Don't update bitmap if source is not equal to color compare color	
	8	W	Enable color comparison	
	9	W	Select 32-bit command registers	
	11-10	W	Reserved	
	15-12	W	0EH (index)	
BEE8	**F**		**Read Register Select**	**20-19**
	2-0	W	Select register to be read	
	11-4	W	Reserved	
	15-12	W	0FH (index)	
E2E8			**Pixel Data Transfer**	**20-20**
	15-0	W	Data transfer register (CPU to Graphics Engine) - low word	
E2EA			**Pixel Data Transfer-Extension**	**20-20**
	15-0	W	Data transfer register (CPU to Graphics Engine) - high word	

A.6 STREAMS PROCESSOR REGISTERS

Table A-6. Streams Processor Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
8180			**Primary Stream Control**	**21-1**
	23-0	R/W	Reserved	
	26-24	R/W	Primary stream input data format	
	27	R/W	Reserved	
	30-28	R/W	Primary stream filter characteristics	
	31	R/W	Reserved	
8184			**Color/Chroma Key Control**	**21-2**
	7-0	R/W	B/V/Cr key value (lower bound for chroma)	
	15-8	R/W	G/U/Cb key value (lower bound for chroma)	
	23-16	R/W	R/Y key value (lower bound for chroma)	
	26-24	R/W	RGB color comparison precision	
	27	R/W	Reserved	
	28	R/W	Color key control (full compare or bit 16 of 1.5.5.5)	
	31-29	R/W	Reserved	
8190			**Secondary Stream Control**	**21-3**
	11-0	R/W	DDA horizontal accumulator initial value	
	23-12	R/W	Reserved	
	26-24	R/W	Secondary stream input data format	
	27	R/W	Reserved	
	30-28	R/W	Secondary stream filter characteristics	
	31	R/W	Reserved	
8194			**Chroma Key Upper Bound**	**21-4**
	7-0	R/W	V/Cr key value (upper bound)	
	15-8	R/W	U/Cb key value (upper bound)	
	23-16	R/W	Y key value (upper bound)	
	31-24	R/W	Reserved	
8198			**Secondary Stream Stretch/Filter Constants**	**21-4**
	10-0	R/W	K1 horizontal scale factor	
	15-11	R/W	Reserved	
	26-16	R/W	K2 horizontal scale factor	
	31-27	R/W	Reserved	

Table A-6. Streams Processor Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
81A0			**Blend Control**	**21-5**
	1-0	R/W	Reserved	
	4-2	R/W	Secondary stream blend coefficient	
	9-5	R/W	Reserved	
	12-10	R/W	Primary stream blend coefficient	
	23-13	R/W	Reserved	
	26-24	R/W	Compose mode	
	31-27	R/W	Reserved	
81C0			**Primary Stream Frame Buffer Address 0**	**21-6**
	21-0	R/W	Primary stream frame buffer starting address 0	
	31-22	R/W	Reserved	
81C4			**Primary Stream Frame Buffer Address 1**	**21-6**
	21-0	R/W	Primary stream frame buffer starting address 1	
	31-22	R/W	Reserved	
81C8			**Primary Stream Stride**	**21-7**
	11-0	R/W	Primary stream stride	
	31-12	R/W	Reserved	
81CC			**Double Buffer/LPB Support**	**21-7**
	0	R/W	Select primary frame buffer address 1	
	2-1	R/W	Select secondary frame buffer address	
	3	R/W	Reserved	
	4	R/W	Select LPB frame buffer start address 1	
	5	R/W	LPB input buffer select loading at end of frame	
	6	R//w	Selected LPB input buffer toggles at end of frame	
	31-7	R/W	Reserved	
81D0			**Secondary Stream Frame Buffer Address 0**	**21-9**
	21-0	R/W	Secondary stream frame buffer starting address 0	
	31-22	R/W	Reserved	
81D4			**Secondary Stream Frame Buffer Address 1**	**21-9**
	21-0	R/W	Secondary stream frame buffer starting address 1	
	31-22	R/W	Reserved	
81D8			**Secondary Stream Stride**	**21-10**
	11-0	R/W	Secondary stream stride	
	31-12	R/W	Reserved	

Table A-6. Streams Processor Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
81DC			**Blend Control**	**21-10**
	2-0	R/W	Reserved	
	12-3	R/W	Pixel stop fetch position	
	18-13	R/W	Reserved	
	28-19	R/W	Pixel start fetch position	
	29	R/W	Reserved	
	30	R/W	Primary stream on top	
	31	R/W	Enable opaque overlay control	
81E0			**K1 Vertical Scale Factor**	**21-12**
	10-0	R/W	K1 vertical scale factor	
	31-11	R/W	Reserved	
81E4			**K2 Vertical Scale Factor**	**21-12**
	10-0	R/W	K2 vertical scale factor	
	31-11	R/W	Reserved	
81E8			**DDA Vertical Accumulator Initial Value**	**21-13**
	11-0	R/W	DDA vertical accumulator initial value	
	31-12	R/W	Reserved	
81EC			**Streams FIFO and RAS Controls**	**21-13**
	4-0	R/W	Streams FIFO allocation	
	9-5	R/W	Secondary FIFO threshold	
	14-10	R/W	Primary FIFO threshold	
	15	R/W	$\overline{\text{RAS}}$ low time control	
	16	R/W	$\overline{\text{RAS}}$ precharge control	
	17	R/W	Reserved	
	18	R/W	Specify memory size for LPB memory cycles	
	19	R/W	Do not tri-state PD[63:16] during ROM cycles	
	20	R/W	Disable memory arbitration for ROM cycles	
	21	R/W	Do not delay PD output	
	31-22	R/W	Reserved	
81F0			**Primary Stream Window Start Coordinates**	**21-15**
	10-0	R/W	Primary stream Y start	
	15-11	R/W	Reserved	
	26-16	R/W	Primary stream X start	
	31-27	R/W	Reserved	
81F4			**Primary Stream Window Size**	**21-15**
	10-0	R/W	Primary stream height	
	15-11	R/W	Reserved	
	26-16	R/W	Primary stream width	
	31-27	R/W	Reserved	

Table A-6. Streams Processor Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
81F8			**Secondary Stream Window Start Coordinates**	**21-16**
	10-0	R/W	Secondary stream Y start	
	15-11	R/W	Reserved	
	26-16	R/W	Secondary stream X start	
	31-27	R/W	Reserved	
81FC			**Secondary Stream Window Size**	**21-16**
	10-0	R/W	Secondary stream height	
	15-11	R/W	Reserved	
	26-16	R/W	Secondary stream width	
	31-27	R/W	Reserved	

A.7 LPB REGISTERS

Table A-7. LPB Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
FF00			**LPB Mode**	**22-1**
	0	R/W	Enable LPB	
	3-1	R/W	LPB mode	
	4	R/W	Reset LPB	
	5	R/W	Write every other received frame to memory	
	6	R/W	No byte swap for incoming video	
	8-7	R/W	Reserved	
	9	R/W	LPB vertical sync is active high	
	10	R/W	LPB horizontal sync is active high	
	11	W	CPU VSYNC	
	12	W	CPU HSYNC	
	13	W	Load base address currently pointed to	
	15-14	R/W	Reserved	
	17-16	R/W	Maximum compressed data bust size	
	20-18	R/W	Reserved	
	22-21	R/W	Video FIFO threshold	
	23	R/W	Reserved	
	24	R/W	LPB clock driven by LCLK	
	25	R/W	Don't add stride after first HSYNC	
	26	R/W	Invert the LCLK input	
	30-27	R/W	Reserved	
	31	R	CFLEVEL status	
FF04			**LPB FIFO Status**	**22-4**
	3-0	R	LPB output FIFO status	
	10-4	R	Reserved	
	11	R	LPB output FIFO full	
	12	R	LPB output FIFO empty	
	13	R	LPB output FIFO almost empty	
	19-14	R	Reserved	
	20	R	LPB video FIFO 0 full	
	21	R	LPB video FIFO 0 empty	
	22	R	LPB video FIFO 0 almost empty	
	28-23	R	Reserved	
	29	R	LPB video FIFO 1 full	
	30	R	LPB video FIFO 1 empty	
	31	R	LPB video FIFO 1 almost empty	

Table A-7. LPB Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
FF08			**LPB Interrupt Flags**	**22-5**
	0	R/W	LPB Output FIFO empty	
	1	R/W	HSYNC (end of line) input on pin 202	
	2	R/W	VSYNC (end of frame) input on pin 203	
	3	R/W	Serial port start condition detected	
	15-4	R/W	Reserved	
	16	R/W	Enable LPB output FIFO empty interrupt	
	17	R/W	Enable HSYNC (end of line) input interrupt	
	18	R/W	Enable VSYNC (end of frame) input interrupt	
	19	R/W	Enable serial port start condition detect interrupt	
	23-20	R/W	Reserved	
	24	R/W	Drive SPCLK low on receipt of a serial port start condition	
	31-25	R/W	Reserved	
FF0C			**LPB Frame Buffer Address 0**	**22-7**
	21-0	R/W	LPB frame buffer address 0	
	31-22	R/W	Reserved	
FF10			**LPB Frame Buffer Address 1**	**22-7**
	21-0	R/W	LPB frame buffer address 1	
	31-22	R/W	Reserved	
FF14			**LPB Direct Read/Write Address**	**22-8**
	20-0	R/W	Address of MPEG decoder address to read/write	
	23-21	R/W	MPEG decoder transaction type	
	31-24	R/W	Reserved	
FF18			**LPB Direct Read/Write Data**	**22-8**
	31-0	R/W	LPB direct read/write data	
FF1C			**LPB General Purpose Input/Output Port**	**22-9**
	3-0	R/W	General purpose output data port	
	7-4	R	General purpose input data port	
	31-8	R/W	Reserved	

Table A-7. LPB Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
FF20			**Serial Port**	**22-9**
	0	R/W	0 = Serial clock write on pin 205, 1 = pin 205 tri-state	
	1	R/W	0 = Serial data write on pin 206, 1 = pin 206 tri-state	
	2	R	0 = Serial clock low on pin 205, 1 = pin 205 tri-state	
	3	R	0 = Serial data low on pin 206, 1 = pin 206 tri-state	
	4	R/W	Enable serial port function	
	5-7	R/W	Reserved	
	8	R	Bit 0 mirror (data on byte lane 2 at E2H)	
	9	R	Bit 1 mirror (data on byte lane 2 at E2H)	
	10	R	Bit 2 mirror (data on byte lane 2 at E2H)	
	11	R	Bit 3 mirror (data on byte lane 2 at E2H)	
	12	R	Bit 4 mirror (data on byte lane 2 at E2H)	
	31-13	R/W	Reserved	
FF24			**LPB Video Input Window Size**	**22-11**
	11-0	R/W	Video input line width	
	15-12	R/W	Reserved	
	24-16	R/W	Video input window height	
	31-25	R/W	Reserved	
FF28			**LPB Video Data Offsets**	**22-12**
	11-0	R/W	Horizontal video data offset	
	15-12	R/W	Reserved	
	24-16	R/W	Vertical video data offset	
	31-25	R/W	Reserved	
FF2C			**LPB Horizontal Decimation Control**	**22-12**
	31-0	R/W	Video data byte mask	
FF30			**LPB Vertical Decimation Control**	**22-13**
	7-0	R	Video data line mask	
FF34			**LPB Line Stride**	**22-13**
	11-0	R/W	Line stride	
	31-12	R/W	Reserved	
FF40			**LPB Output FIFO**	**22-14**
	31-0	R/W	Output FIFO data	

A.8 PCI CONFIGURATION SPACE REGISTERS

When a PCI configuration read or write command is issued, AD[7:0] contain the address of the register in the configuration space to be accessed.

Table A-8. PCI Configuration Space Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
00			**Vendor ID**	**23-1**
	15-0	R	Hardwired to 5333H	
02			**Device ID**	**23-2**
	15-0	R	Hardwired to 8811H	
04			**Command**	**23-2**
	0	R/W	Response to I/O space accesses enabled	
	1	R/W	Response to memory space accesses enabled	
	4-2	R/W	Reserved	
	5	R/W	Enable DAC snooping	
	15-6	R/W	Reserved	
06			**Status**	**23-3**
	8-0	R/W	Reserved	
	10-9	R/W	Hardwired to select medium device select timing	
	15-11	R/W	Reserved	
08			**Class Code**	**23-3**
	31-0	R	Hardwired to indicate VGA-compatible display controller and revision level	
10			**Base Address 0**	**23-4**
	0	R/W	Hardwired to indicate base registers map into memory space	
	2-1	R/W	Hardwired to allow mapping anywhere in 32-bit address space	
	3	R/W	Hardwired to indicate does not meet prefetchable requirements	
	22-4	R/W	Reserved	
	31-23	R/W	Base address 0	
30			**BIOS Base Address**	**23-5**
	0	R/W	Enable access to BIOS ROM address space	
	15-1	R/W	Reserved	
	31-16	R/W	Upper 16 bits of BIOS ROM address	
3C			**Interrupt LIne**	**23-3**
	7-0	R/W	Interrupt line routing information	
3D			**Interrupt Pin**	**23-6**
	7-0	R	Hardwired to specify use of INTA	

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