Trim-Slice

Reference Guide

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Table 1 Document Revision Notes

Date	Description
May 2011	• First release
July 2011	• Added power modes description in 4.1.2 • Added power button operation description in 5.14

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab Trim-Slice.

1.2 Related Documents

For additional information not covered in this manual, please refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
Trim-Slice Resources	http://www.trimslice.com

2 OVERVIEW

2.1 Highlights

The Trim-Slice is a fully functional miniature computer based on the NVIDIA Tegra2 SoC – a dual core ARM Cortex-A9 CPU with an integrated GeForce GPU and multimedia acceleration engines.

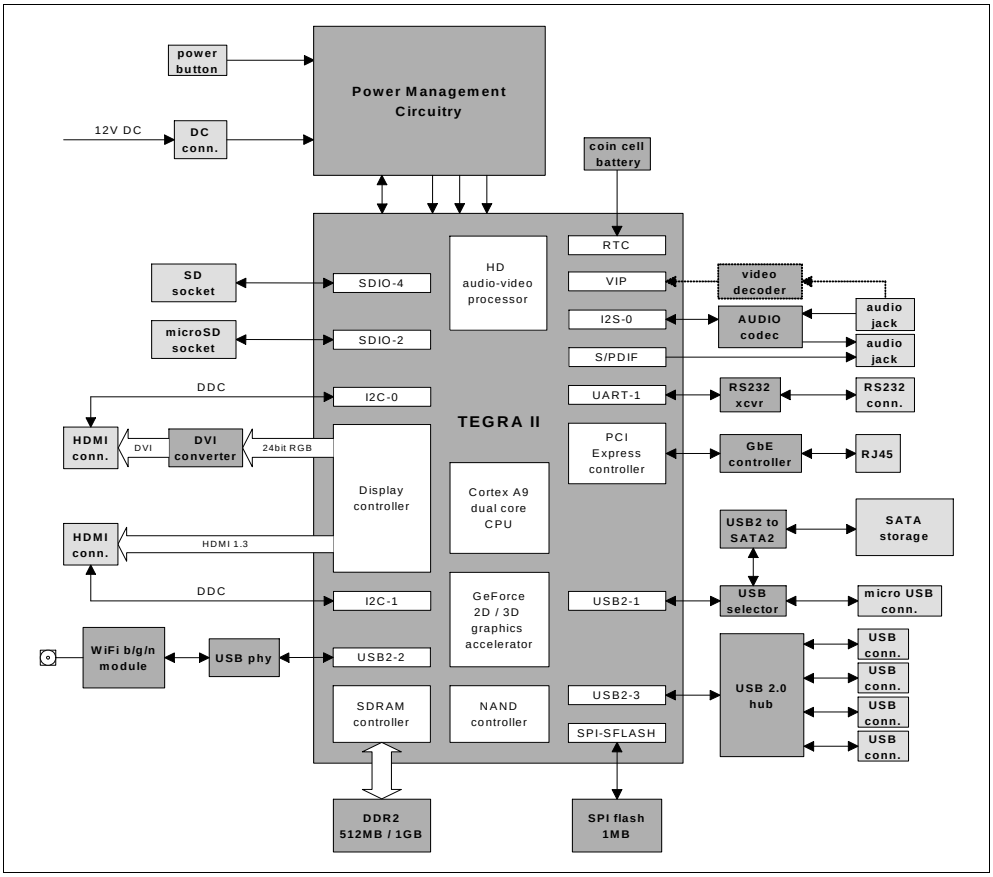
The device enables versatile connectivity through a variety of peripheral interfaces – Gigabit Ethernet, 802.11n WiFi, Bluetooth and high-speed USB.

The Trim-Slice is designed into a miniature form-factor with unprecedentedly low-power envelope, while providing rich multimedia capabilities and PC-like user experience.

High performance, low-power, rich I/O and miniature rugged design, position Trim-Slice as an attractive solution for a wide range of applications – media player, IPTV, infotainment system, signage, gaming or even desktop replacement.

2.2 Block Diagram

Figure 1 Trim-Slice Block Diagram



2.3 Features

Table 3 CPU, Graphics and Memory

Feature	Specifications	Notes
CPU	NVIDIA Tegra2 dual-core ARM Cortex-A9 1GHz	
GPU	Ultra low-power GeForce	
RAM	1 GB, DDR2, 333 MHz, 32-bit	
Boot Flash	1 MB SPI NOR flash, bootable	

Table 4 Peripheral Interfaces

Feature	Specifications	Notes
HDMI	HDMI 1.3a, up to 1920 x 1080, DDC support, HDMI connector	
DVI	DVI, up to 1680 x 1050, DDC support, HDMI connector	Optional
Analog Audio	Stereo line-out and stereo line-in, 3.5mm audio jacks	
Digital Audio	5.1 channel S/PDIF, data rates up to 24 bit, 96kHz, 3.5mm audio jack	
Video input	Composite analog NTCS / PAL / SECAM input, 3.5mm audio jack	Optional
Gigabit Ethernet	1000 BaseT Ethernet port, activity LEDs, RJ-45 connectors	
WiFi	802.11n WiFi, modular	Optional
Bluetooth	Bluetooth V2.1+EDR, modular	Optional
USB2.0	Four USB 2.0 host ports, 480 Mbps, type-A connectors	
	USB device port, micro USB connector	
Full-size SD	MMC / SD / SDIO, SDHC support, full-size SD socket	
Micro-SD	MMC / SD / SDIO, SDHC support, micro-SD socket	
RS232	Partial modem controls, RS232, ultra mini serial connector	
Extension	JTAG, UART x2, SPI, 24-pin FPC connector	

Table 5 Electrical and Mechanical

Supply Voltage	Unregulated 8 to 16 volt input
Power consumption	2W to 6W in full activity, depending on devices in use, operating system and CPU/graphics load
Dimensions	130 mm x 95 mm x 15 mm

3 CORE SYSTEM COMPONENTS

3.1 Tegra 250 SoC

3.1.1 Dual-Core ARM Cortex-A9 CPU

The Tegra2 CPU core incorporates a dual Cortex-A9 symmetric multi-processing ARM core supporting dual instruction issue and out-of-order and speculative execution. The CPU supports full cache coherency for the dual symmetric processors. The processors feature dedicated 32 KB instruction and 32 KB data L1 caches and a shared 1 MB L2 cache.

3.1.2 Ultra-Low-Power GeForce GPU

The ultra-low-power NVIDIA GeForce Graphics Processing Unit (GPU) handles 2D graphics rendering and 3D pixel and vertex shading. The 2D engine provides all relevant low-level 2D composition functionality including alpha blending, stretch-bit function, video scaling, anti-aliasing and image rotation. The 3D engine is a fully programmable 3D graphics core supporting the OpenGL ES 2.0 rendering model. The geometry and pixel processing performance make it highly suitable for rendering advanced user interfaces and complex gaming applications.

The GPU supports the following main features:

- OpenGL ES 2.0
- Peak triangle rate of 71 million triangles per second
- Peak fill rate (with Z-reject) of 1200 million pixels per second
- Programmable pixel shader
- Programmable vertex and lighting
- Advanced 2D and vector engine

3.1.3 Audio-Video Processor Subsystem

The Audio-Video processor (AVP) subsystem includes dedicated audio and video decode hardware acceleration, an ARM7 processor and embedded RAM. This subsystem provides full motion playback up to 1080p high-definition video and supports H.264, VC-1 and MPEG-4 video standards and multiple audio standards with dedicated hardware.

3.2 System Memory

3.2.1 DRAM

The Trim-Slice features 1 GB of DDR2. The DRAM interface is 32-bits wide and runs with a 333 MHz clock.

3.2.2 SPI Flash

The Trim-Slice features 1 MB of SPI NOR flash.

The SPI NOR flash functions as the primary bootable memory device, used for the boot-loader and configuration blocks storage.

The NOR flash is interfaced with the Tegra2 SoC SPI-SFLASH port.

3.3 Display Subsystem

3.3.1 HDMI

The Trim-Slice HDMI output is implemented with the Tegra2 HDMI interface. HDMI DDC is implemented with the Tegra2 I2C-1 interface. HDMI_DETECT signal is connected to the Tegra2 HDMI_INT input. HDMI signals are routed to the primary display output connector J1. The HDMI output supports resolutions of up to 1920 x 1080.

3.3.2 DVI

The Trim-Slice features a DVI transmitter that is based on the TFP410/SIL164 IC. DVI output signals are routed to the secondary display output connector J2. The DVI transmitter is connected to the Tegra2 24-bit parallel RGB interface. The DVI output supports resolutions of up to 1680 x 1050.

The DVI DDC is implemented with the Tegra2 I2C-0 interface.

In order to use the DVI interface, the Tegra2 display system has to be configured properly for RGB888 operation mode.

NOTE: DVI functionality is optional. Availability depends on Trim-Slice model configuration.

3.4 Audio Subsystem

3.4.1 Analog Audio

The Trim-Slice analog audio subsystem is implemented with Texas Instruments TLV320AIC23b audio codec. The analog audio subsystem supports the following features:

- Single ended stereo-line output
- Single ended stereo-line input
- Integrated electret-microphone biasing and buffering solution
- 8-kHz – 96-kHz Sampling-Frequency Support
- 100-dB SNR multi-bit Sigma-Delta DAC (A-weighted at 48 kHz)
- 90-dB SNR multi-bit Sigma-Delta ADC (A-weighted at 48 kHz)

The audio codec is connected to the Tegra2 I2S-0 port.

Analog line output is routed to the audio jack P4. Analog line input is routed to the audio jack P5.

Table 6 Audio Characteristics

Parameter	Test conditions		Min	Typ	Max	Unit
Headphone Output						
0-dB full-scale output voltage				1.0		Vrms
Maximum output power, PO	Rload = 32Ω			30		
	Rload = 16Ω			40		
Signal-to-noise ratio, A-weighted (see Note 2)			90	97		dB
Total harmonic distortion	1kHz output	Pout = 10mW			0.1	%
		Pout = 20mW			1.0	%
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
Programmable gain	1 kHz output		-73		6	
Programmable-gain step size				1		
Mute attenuation	1 kHz output			80		
Line Input to ADC						
Input signal level (0 dB)				1.0		Vrms
Signal-to-noise ratio, A-weighted, 0-dB gain (see Notes 1 and 2)	Fsample = 48 kHz.		85	90		dB
Dynamic range, A-weighted, −60-dB full-scale input (see Note 2)			85	90		dB
Total harmonic distortion, −1-dB input, 0-dB gain				-80		dB
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
ADC Channel Separation	1 kHz input tone			90		dB
Programmable-gain step size	Monotonic			1.5		dB
Mute attenuation	0dB, 1 kHz input tone			80		dB
Input resistance	12 dB input gain		10		20	kΩ
	0 dB input gain		30	35		
Input capacitance				10		pF

For additional details, please refer to the TLV320AIC23B datasheet, available from http://focus.ti.com/.

3.4.2 S/PDIF

The S/PDIF output is implemented with the Tegra2 S/PDIF interface. The S/PDIF output signal is routed to audio jack P5.

3.5 USB Subsystem

3.5.1 USB Hub

The Trim-Slice features four external USB ports that are implemented with the SMSC USB2514 hub.

The USB hub is interfaced with the Tegra2 USB-3 port. USB hub down-stream ports are routed to the USB connectors P6, P8, P9 and P11.

For additional details, please refer to the USB2514 datasheet, available from http://www.smsc.com/.

3.5.2 USB-1

The Tegra2 USB-1 port is routed to a USB selector that allows utilizing the port for two separate, mutually exclusive functions:

- On-board USB2-to-SATA controller that implements the Trim-Slice SATA storage interface. For additional details, please refer to section 3.7 of this document.
- USB device port. For additional details, please refer to section 5.10 of this document.

The USB selector path is controlled with the Tegra2 GPIO_PV2 signal.

3.5.3 USB-2

The Tegra2 USB-2 port is utilized for internal Trim-Slice mother-board functionality and is not available for external use. The port is implemented with an on-board SMSC USB3320 phy. The USB signals are routed to connector P38.

3.6 Gigabit Ethernet

The Trim-Slice Gigabit Ethernet interface is implemented with the RTL8111D Realtek Gigabit Ethernet controller. The controller is connected to the PCIe-0 interface of the Tegra2 SoC. The interface supports the following main features:

- Full compliance with IEEE 802.3 standard
- Crossover Detection and Auto-Correction
- Auto-negotiation
- Activity and speed indicator LED controls

Gigabit Ethernet signals are routed to the RJ-45 connector P7.

3.7 SATA Controller

The Trim-Slice SATA functionality is implemented with the Genesys Logic GL830 USB-to-SATA controller. The controller supports the following main features:

- Compliance with Universal Serial Bus specification rev. 2.0
- Compliance with USB Storage Class specification ver.1.0
- Compliance with Serial ATA specification rev. 2.6
- Compliance with Serial ATA II Electrical Specification 1.0

The SATA controller is interfaced with the Tegra2 USB-1 port through the USB selector. The SATA output signals are routed to connector P18.

NOTE: SATA functionality is optional. Availability depends on Trim-Slice model configuration.

3.8 Video Decoder

The Trim-Slice video input port is implemented with the on-board Texas Instruments TVP5151 video decoder that converts NTCS / PAL / SECAM composite analog video into digital 8-bit ITU-R BT.656 format. The analog video input is routed to audio jack P4. The digital BT.656 data is transmitted into the Tegra2 digital video input port.

For additional details, please refer to the TVP5151 datasheet, available from http://focus.ti.com/.

NOTE: Video decoder functionality is optional. Availability depends on Trim-Slice model configuration.

3.9 RS232 Transceiver

The Trim-Slice RS232 port is implemented with the MAX3243 transceiver.

The RS232 port supports the following features:

- 16550 compatibility
- 16-byte FIFO for receiver and 16-byte FIFO for transmitter
- Programmable baud rate of up to 250 Kbps
- Configurable data format
- RS-232 bus-pin ESD protection exceeds ±15 kV using the Human-Body Model

The RS232 port is derived from the UART-1 port of the Tegra2 SoC.

4 SYSTEM LOGIC

4.1 Power Subsystem

4.1.1 Power Rails

The Trim-Slice is powered with a single 12V power supply.

Table 7 Power signals

Signal Name	Type	Description
VIN_12V	P	Main power supply. Typical voltage – 12V.
GND	P	Common ground.

4.1.2 Power Modes

The Trim-Slice supports two hardware power modes.

Table 8 Power modes

Power Mode	Description
ON	All internal power rails are enabled. Mode entered automatically when main power supply is connected.
OFF	All internal power rails except those required for the power management logic are switched off.

4.1.3 RTC Back-Up Battery

The Trim-Slice features an on-board 18mAh rechargeable coin cell lithium battery, which maintains the Trim-Slice RTC whenever the main power supply is not present.

4.2 Firmware Boot Options

The Trim-Slice supports the following firmware boot options:

- Boot from on-board SPI NOR flash
- Boot from external SD card inserted into the P2 SD socket

The boot option is selected with the recovery-boot button SW2. The default boot option is designed for normal system operation with the on-board SPI NOR flash acting as the boot media. The alternate boot option is intended mainly for system recovery.

NOTE: The recovery-boot button only affects the firmware (Tegra2 BCT and boot-loader) boot process. O/S and file-system boot configuration is determined by the boot-loader settings.

Table 9 Boot options

Boot option	Recovery-boot button (SW2) state	Boot device
Default	Not pressed.	On-board flash
Alternate	Pressed during system reset / power cycle.	SD card

4.3 Real Time Clock

The Trim-Slice RTC is implemented with the EM Microelectronic EM3027 IC that provides clock and calendar information in BCD format. The EM3027 is connected to the I2C-2 port of the Tegra2 SoC. The on-board backup battery keeps the RTC running to maintain clock and time information whenever the main Trim-Slice power supply is not present.

For additional details, please refer to the EM3027 datasheet, available from http://www.emmicroelectronic.com/.

5 INTERFACES AND CONNECTORS

5.1 HDMI Connector (J1)

The primary HDMI display output is provided through the standard HDMI socket (J1).

For additional details, please refer to section 3.3.1 of this document.

Table 10 J1 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	HDMI_TXD2+	11	GND
2	GND	12	HDMI_TXC-
3	HDMI_TXD2-	13	NC
4	HDMI_TXD1+	14	NC
5	GND	15	HDMI_DDC_SCL
6	HDMI_TXD1-	16	HDMI_DDC_SDA
7	HDMI_TXD0+	17	GND
8	GND	18	HDMI_5V
9	HDMI_TXD0-	19	HDMI_DETECT
10	HDMI_TXC+		

5.2 DVI Connector (J2)

The secondary DVI display output is provided through the standard HDMI socket (J2).

For additional details, please refer to section 3.3.2 of this document.

Table 11 J2 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	DVI_TXD2+	11	GND
2	GND	12	DVI_TXC-
3	DVI_TXD2-	13	NC
4	DVI_TXD1+	14	NC
5	GND	15	DVI_DDC_SCL
6	DVI_TXD1-	16	DVI_DDC_SDA
7	DVI_TXD0+	17	GND
8	GND	18	DVI_5V
9	DVI_TXD0-	19	NC
10	DVI_TXC+		

5.3 DC Power Jack (J3)

DC power input connector.

Table 12 J3 connector pin-out

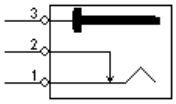
Pin	Signal Name	
1	GND	
2	GND	
3	VIN_12V	

Table 13 J3 connector data

Manufacturer	Mfg. P/N
Contact Technology	DC-022

The connector is compatible with the Trim-Slice power supply unit supplied by CompuLab.

5.4 Micro-SD Socket (P1)

The micro-SD socket (P1) is connected directly to the Tegra2 SDIO-2 port.

Table 14 P1 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	SDIO2_DAT2	5	SDIO2_CLK
2	SDIO2_DAT3	6	GND
3	SDIO2_CMD	7	SDIO2_DAT0
4	VDD_3V3	8	SDIO2_DAT1

5.5 SD Socket (P2)

The SD socket (P2) is connected directly to the Tegra2 SDIO-4 port.

P5 power is supplied by the VDD_SDIO voltage rail. VDD_SDIO can be controlled with the Tegra2 SoC GPIO_PP0 signal.

The SD write protect signal, “SDIO4_WP”, is routed to the Tegra2 SoC GPIO_PP2 signal. The SD card-detect signal, “SDIO4_CD”, is routed to the GPIO_PP1 signal.

Table 15 P2 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	SDIO4_DAT3	7	SDIO4_DAT0
2	SDIO4_CMD	8	SDIO4_DAT1
3	GND	9	SDIO4_DAT2
4	VDD_SDIO	10	GND
5	SDIO4_CLK	11	SDIO4_CD
6	GND	12	SDIO4_WP

5.6 RS232 connector (P3)

The Trim-Slice RS232 port is routed to the on-board RS232 ultra-mini connector (P3). All signals are at RS232 levels.

Table 16 P3 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	RS232_TXD	5	RS232_DTR
2	RS232_RTS	6	RS232_DSR
3	RS232_RXD	7	NC
4	RS232_CTS	8	GND

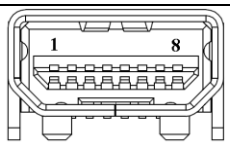


Table 17 P3 connector data

Manufacturer	Mfg. P/N	Mating connector
Wieson	G3169-500001	Wieson, P/N: 4306-5000

The connector is compatible with the serial cable adapter (CompuLab P/N 199D10230) supplied by CompuLab.

5.7 Audio Jacks (P4, P5)

The Trim-Slice features two 3.5mm jacks. The analog audio signal pin-outs are compatible with standard 3-pole audio cables. The additional pins (video input on P4 and S/PDIF output on P5) are accessible with the 3.5mm-to-RCA adapter cable (CompuLab P/N 199D10300) available from CompuLab.

Table 18 P4 connector pin-out

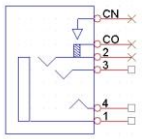
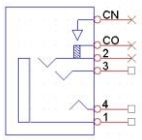
Pin	Signal Name	Jack pin-out	Mating plug
1	AUDIO_GND		
2	VIDEO_IN		
3	AUDIO_OUT_R		
4	AUDIO_OUT_L		

Table 19 P5 connector pin-out

Pin	Signal Name	Jack pin-out	Mating plug
1	AUDIO_GND		
2	SPDIF_OUT		
3	AUDIO_IN_R		
4	AUDIO_IN_L		

5.8 USB Host Connectors (P6, P8, P9, P11)

The Trim-Slice external USB2.0 host ports are available through four standard type-A USB connectors (P6, P8, P9 and P11).

Table 20 P6 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	USBHUB_VBUS1	3	USBHUB_P1_DP
2	USBHUB_P1_DM	4	GND

Table 21 P8 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	USBHUB_VBUS2	3	USBHUB_P2_DP
2	USBHUB_P2_DM	4	GND

Table 22 P9 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	USBHUB_VBUS3	3	USBHUB_P3_DP
2	USBHUB_P3_DM	4	GND

Table 23 P11 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	USBHUB_VBUS4	3	USBHUB_P4_DP
2	USBHUB_P4_DM	4	GND

5.9 Gigabit Ethernet Connector (P7)

The Trim-Slice Gigabit Ethernet port is routed to the standard RJ-45 connector (P7).

Table 24 P7 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	LAN_CT1	7	LAN_MDIP2
2	LAN_MDIP0	8	LAN_MDIN2
3	LAN_MDIN0	9	LAN_MDIP3
4	LAN_MDIP1	10	LAN_MDIN3
5	LAN_MDIN1	11	LAN_CT2
6	LAN_CT3		

5.10 USB Device Connector (P10)

The Tegra2 USB-1 port is routed through the USB selector to the micro-USB connector P10.

For additional details, please refer to section 3.5.2 of this document.

Table 25 P10 connector pin-out

Pin	Signal Name
1	NC
2	USB_DEV_DM
3	USB_DEV_DP
4	NC
5	GND

5.11 SATA Connector (P18)

The SATA output signals are routed to connector P18. The SATA connector is utilized for the Trim-Slice internal SATA storage. The connector is not intended for external usage.

Table 26 P18 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	GND	7	GND
2	SATA_TXP	8	NC
3	SATA_TXN	9	VDD_5V
4	GND	10	VDD_5V
5	SATA_RXN	11	NC
6	SATA_RXP	12	NC

5.12 Extension Connector (P19)

NOTE: JTAG signals operate at 1.8V voltage levels.

Table 27 P19 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	UART2_TXD	13	GND
2	UART2_RXD	14	UART3_RXD
3	UART2_nRTS	15	UART3_nRTS
4	UART2_nCTS	16	UART3_nCTS
5	SPDIF_IN	17	JTAG_nTRST
6	SPI2_SCK	18	JTAG_TDI
7	SPI2_nCS0	19	JTAG_TMS
8	SPI2_nCS1	20	JTAG_TCK
9	RESERVED	21	JTAG_RTCK
10	SPI2_MOSI	22	JTAG_TDO
11	SPI2_MISO	23	SYS_nRST
12	UART3_TXD	24	VDD_1V8

Table 28 P19 connector data

Manufacturer	Mfg. P/N	Mating connector
CVILux	CF20-241D0R0	FFC, 24 contacts, 0.5mm pitch

The connector is compatible with the FFC cable (CompuLab P/N 410X60240) available from CompuLab.

5.13 WLAN USB Connector (P38)

The WLAN USB connector is utilized for the Trim-Slice WLAN module. The connector is not intended for external usage.

Table 29 P38 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	VDD_3V3	4	GND
2	USB2_DM	5	NC
3	USB2_DP	6	WLAN_EN

Table 30 P38 connector data

Manufacturer	Mfg. P/N
Aces	87213-0600G

5.14 Power Button (SW1)

The Trim-Slice power button SW1 controls the system power state. The table below describes the button functions.

Table 31 Power button functions

User action	System state	System behavior
Short press	OFF	Power on.
Short press	ON	Notify the O/S of a shut-down request.
Long press (> 5sec)	ON	Shut down unconditionally.

For additional details, please refer to section 4.1.2 of this document.

5.15 Recovery-Boot Button (SW2)

The Trim-Slice recovery-boot button SW2 controls the system firmware boot options.

For additional details, please refer to section 4.2 of this document.

5.16 Indicator LEDs

The table below describes the Trim-Slice indicator LEDs.

Table 32 LED description

LED	Color	System	LED activity
DS1	Green	Power	System power state indicator.
DS2	Green	TBD	TBD
DS3	Green	TBD	TBD

6 MECHANICAL DRAWINGS

The mechanical drawings below are provided for connector location information.

Full mechanical drawings are available at the Trim-Slice website.

Figure 2 Trim-Slice mother-board top

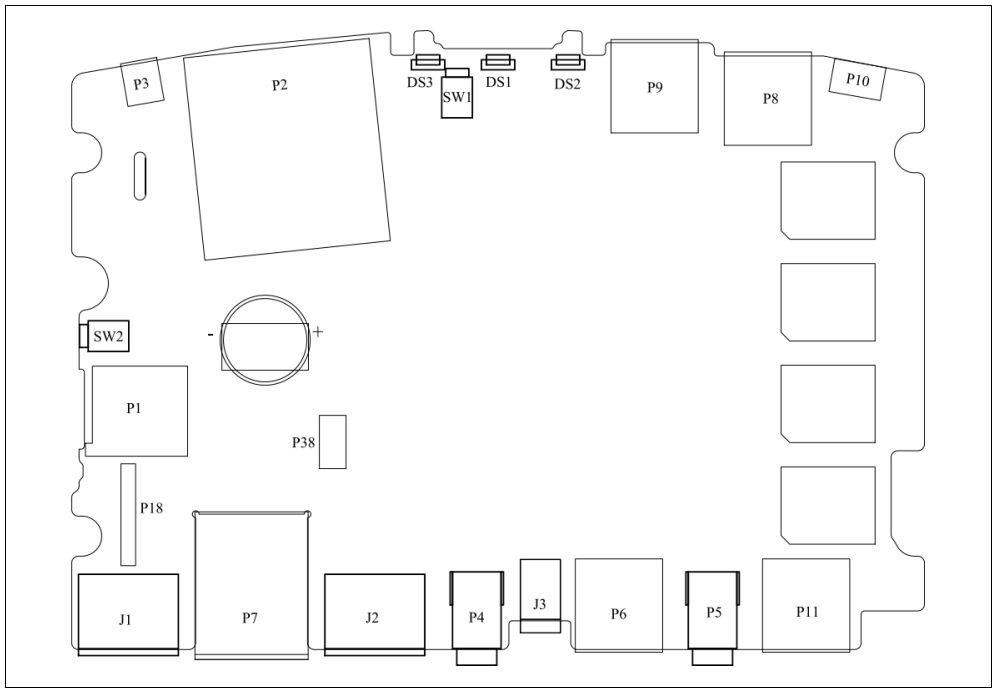
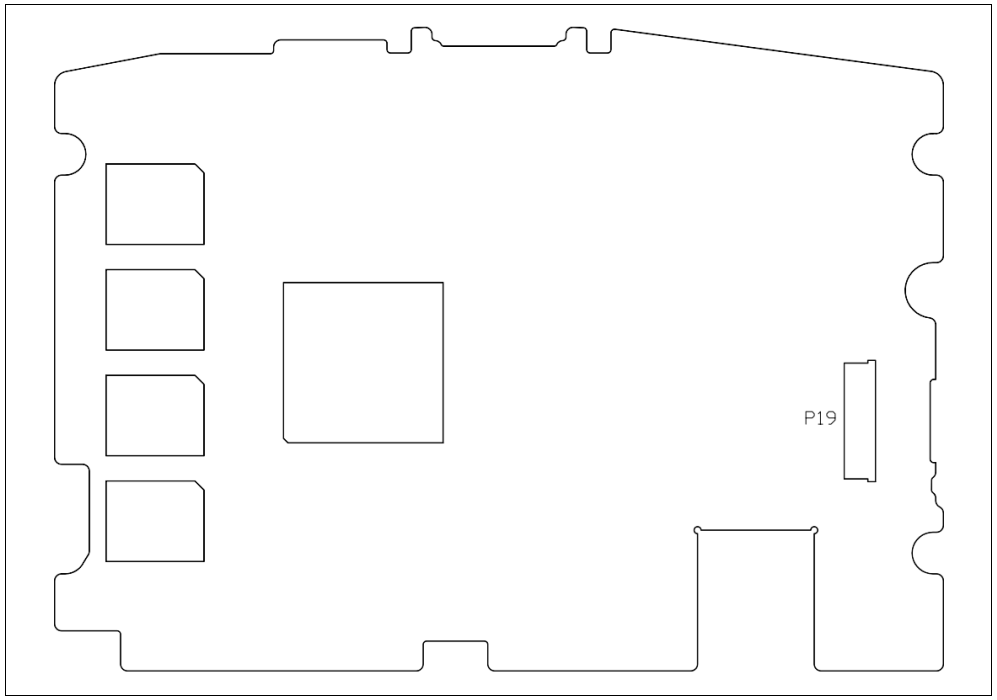


Figure 3 Trim-Slice mother-board bottom (x-ray view - as seen from top side)



7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 33 Absolute Maximum Ratings

Parameter	Min	Typ.	Max	Unit
Main power supply voltage	-0.3	12	18	V

NOTE: Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device.

7.2 Recommended Operating Conditions

Table 34 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage	8	12	16	V

7.3 DC Electrical Characteristics

Table 35 DC Electrical Characteristics

Parameter	Operating Conditions	Min	Typ	Max	Unit
3.3V Digital I/O					
V_{IH}		2.475		3.6	V
V_{IL}		-0.5		0.8	V
V_{OH}		2.8			V
V_{OL}				0.5	V
Open drain with internal pull up to 3.3V					
V_{IH}		2.3		3.8	V
V_{IL}		-0.5		1.0	V
V_{OL}	IOL = 3 mA	-		0.4	V
RS232					
TX Voltage Swing		±5	±5.4		V
RX Voltage Swing			±25		V