VESA®

Extended Display Identification Data (EDID™) Standard

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EXTENDED DISPLAY IDENTIFICATION DATA STANDARD

Version 3
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Purpose

This standard defines data formats to carry configuration information to allow optimum use of displays.

Summary

Today's computing environment demands that systems offer user friendly set-up. With the growing popularity of intuitive and simpler software user interfaces, hardware manufacturers are responding with plug-and-play systems and peripherals. However, for the user to receive full benefit from these advances, standardization is necessary. VESA, as the prominent standards organization for graphic sub-systems, has developed the EDID data format as a compact method to specify the capabilities of various types of monitors as well as integrated displays. It is anticipated that EDID format data will be transported by a variety of communication protocols.

Note

This version of the EDID standard contains documentation for several variations of the EDID data structure. The definition of each of these is determined by version and revision codes contained in the data structure itself. These codes in no way correspond to the version number of the EDID document which is shown on this page. A reference chart of the EDID data structures contained in this document as well as their version and revision codes is shown below.

Version	Revision	Structure Size	Created by Standard	Chapter reference
1	0	128 bytes	VESA DDC v1 r0	Chapter 3
1	1	128 bytes	VESA EDID v2 r0	Chapter 3
1	2	128 bytes	VESA EDID v3 r0	Chapter 3
2	0	256 bytes	VESA EDID v3 r0	Chapter 4

Preface

Scope

This revision of the EDID Standard is intended to clarify unclear areas of previous revisions of the standard and define additional data formats to support displays as defined in the VESA Plug & Display and FPDI standards.

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Support for this Standard

Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product which incorporates EDID, you should ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarification you may require. All comments or reported errors should be submitted in writing to VESA using one of the following methods.

- Fax 408-435-8225, *direct this note to Technical Support at VESA*
- e-mail support@vesa.org
- mail to Technical Support
  VESA - Video Electronics Standards Association
  2150 North First Street, Suite 440
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Revision History

Version 3 November 13, 1997

Addition of EDID data structure version 2.
Addition of Appendix A: Digital Data Formats
Addition of sample EDID data for version 2 data structure.

Version 2 Revision 1 July 24th 1996

Addition of Appendix B : Answers to commonly asked questions
Change of source of EISA ID codes
Correction of known typographic errors
Applied a consistent approach to byte numbering in the definitions of Descriptor Descriptions (Section 3.9)
Correction to reference to EDID and DDC standards version and revision numbers.

Version 2 Revision 0 April 9th 1996

Separation of EDID Standard (this document) from the DDC Standard
Clarification of Version 1.0
Allow alternate uses of 'detailed timing description' area(s)
Incorporation of corrections and comments from VESA membership review
Note : The information in this document is identical with the VESA EDID Proposal Version 2p, Revision 0p, dated January 11th 1996.

Version 1.0 Revision 0 August 12, 1994

Original EDID specification incorporated in the VESA Display Data Channel (DDC) Standard
Note : The information in this document is identical with the VESA DDC Proposal Version 1.0p, Revision 0.64p, dated June 10, 1994

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1. OVERVIEW

1.1 Summary

The Extended Display Identification Data, EDID, described in this document, is a format, with optional variants, to allow the display to inform the host about its identity and capabilities. The EDID format is independent of the communication protocol used between the monitor and host.

> Note : It is important that the software used to decode the EDID data recognizes that the interpretation is dependent on the EDID version and revision levels.

1.2 Background

Earlier monitor identification schemes are only capable of handling a limited number of display types and parameters. Since these schemes carry no information about the capabilities of the display, they are of limited value.

1.3 Standard Objectives

The EDID was developed by VESA to meet, exceed and / or complement certain criteria. These criteria are set forth as Standard Objectives as follows :

- Support Microsoft® Plug and Play definition
- Provide information in a compact format to allow the graphic sub-system to be configured based on the capabilities of the attached display

1.4 Reference Documents

Note : Versions identified here are current but user's of this standard are advised to ensure they have the latest versions of referenced standards and documents.

- VESA, Display Data Channel Standard, Version 1.0, Revision 0, August 12th 1994
- VESA, Display Data Channel Standard, Version 2, Revision 0, April 9th 1996
- VESA, Display Data Channel Standard, Version 3 (currently in proposal stage)
- VESA Plug & Display Standard, Version 1, June 11, 1997
- VESA, Video BIOS Extensions For Display Data Channel - VBE/DDC - Standard.
- VESA, Video Image Area Definition Standard, Revision 1.0, August 12th 1993
- VESA, Generalized Timing Formula Standard - GTF, Version 1.0, December 18, 1996
- Microsoft / Intel Plug and Play ISA Specification, Version 1.0, May 28th 1993.
- Microsoft / Intel Plug and Play Errata and Clarification Document, 12/10/93.
- IBM Personal System/2 Hardware Interface Technical Reference- Common Interfaces Video Subsystem

2. DATA FORMATS

2.1 EDID Introduction

The DDC standard Version 1.0, Revision 0 issued in August 1994 specified the EDID Version 1, Revision 0 data strucutre. The EDID Standard Version 2 Revision 0 issued in April 1996 added definitions for the EDID Version 1 Revision 1 data structure which offered additional features and flexibility. Both of these data structures are based on 128-byte records.

This version of the standard preserves these data structures and adds definitions for two additional EDID data structures.

- Version 1 Revision 2 structure is based on the existing 128-byte Version 1 structures with some additional field definitions.
- Version 2 Revision 0 data structure, defined in Section 4, is a completely new EDID data structure based on 256-byte records. This new structure is designed to provide additional information that is required for displays that follow the VESA Plug & Display (P&D) and Flat Panel Display Interface-2 (FPDI-2) Standards.

2.2 EDID Structure Version 1

All revisions of the EDID structure Version 1 share the same basic layout and data structure size with a large portion allocated for display timings. Unused Standard Timing Identification fields shall be set = 0101h and unused Detailed Timing Descriptions shall contain data for a supported timing standard (generally this will be a standard already identified in the Established Timing of Standard Timing Identification fields).

Note: Monitors designed to the VESA DDC Standard Version 1 Revision 0 dated August 12, 1994 may not be in compliance with this requirement.

Details of EDID structure Version 1 are described in Section 3 of this document.

2.2.1 Version 1 Revision 0

This is the original EDID structure definition from the DDC standard Version 1.0, Revision 0.
The EDID structure is outlined in following table.

No.		Description
8	Bytes	Header
10	Bytes	Vendor / Product Identification
2	Bytes	EDID Structure Version / Revision Level *: Store as 01h / 00h*
15	Bytes	Basic Display Parameters / Features
19	Bytes	Established / Standard Timings
72	Bytes	Detailed Timing Descriptions (18 bytes each)
1	Byte	Extension Flag
1	Byte	Checksum

Table 2.1 - EDID Structure Version 1 Revision 0

2.2.2 Version 1 Revisions 1 & 2

These variations of the EDID Version 1 Revision 0 structure allows for alternate definition(s) of one or more of the Detailed Timing Description(s). Revision 2 adds further information to specific areas like the features byte. It shares the same basic structure as Revision 1 which is outlined in Table 2.2.

EDID structure Version 1 Revision 2 defines uses for two previously reserved bits in the features support byte and allows for additional manufacturer specific alternate definitions of the detailed timing descriptions.

No.		Description
8	Bytes	Header
10	Bytes	Vendor / Product Identification
2	Bytes	EDID Structure Version / Revision Level : *Store as 01h / 0xh*
15	Bytes	Basic Display Parameters / Features
19	Bytes	Established / Standard Timings
72	Bytes	Detailed Timing Descriptions (18 bytes each) and / or Monitor Descriptors (18 bytes each).
1	Byte	Extension Flag
1	Byte	Checksum

Table 2.2 - EDID Structure Version 1 Revisions 1&2

Note **:** If a mixture of Detailed Timing and Monitor Descriptors are used then Detailed Timings shall precede the Monitor Descriptor blocks.

2.2.3 EDID Version 1 Extensions

EDID Version 1 information may be extended in increments of 128 bytes. These extensions may contain any number of different formats, including an Extended EDID information format, sets of additional detailed timings, manufacturer's proprietary formats etc. Each 128-byte data block shall have its own checksum.
There may be as many detailed timing extensions as desired but there may only be one Basic EDID section and one Extended EDID section.
If an Extended EDID is used then it shall immediately follow the Basic EDID section.

Extended EDID functions will be defined outside of this standard.

2.3 EDID Structure Version 2 Revision 0

This is the EDID structure definition for use with the VESA Plug & Display and FPDI-2 standards. The EDID structure is outlined in following table and defined in detail in Section 4 of this document.

No.		Description
64	Bytes	Manufacture and Product Identifiers
64	Bytes	Basic Display Parameters / Features
127	Bytes	Standard & Detailed Timing Descriptions
1	Byte	Checksum

Table 2.3 - EDID Structure Version 2

2.3.1 EDID Version 2 Extensions

EDID Version 2 information may be extended with a single 256-byte block. The format for this extension is currently not defined by VESA except for the requirement that it must have its own checksum located at the 256th byte of the block.

2.4 Data Format Conventions

The EDID data structures are designed to be compact in their representation of data in order to fit the most information into a limit space. To accommodate this, many data lengths have been used according to the needs of the particular data. These include fields from single bit up to two bytes in length. In all cases except where explicitly stated the following conventions are used:

Data length	Convention used	Example
1 to 7 bits	stored in order stated	
8 bits (1 byte)	stored at location stated	
9 to 15 bits	location of bits stated in field definition	
16 bits (2 bytes)	bytes are a binary format (not BCD) stored in locations specified with least significant byte (LSB) stored in first location.	1280 decimal = 0500h Stored 00 at first location 50 next location
Character string (More than 2 bytes)	bytes are ASCII stored in order they are appear in the string.	"ACED" Stored 41h at first location, 43h at the next location, 45h at the next location, and 44h at the next location.

Table 2.4 - Data Format Conventions

3. Extended Display Identification Data (EDID) Structure Version 1

3.1 EDID Format Overview

Address	No. bytes		Description	Format
00h	**8**	**Bytes**	**Header**	**See Section 3.2**
00h		1	00h	
01h		1	FFh	
02h		1	FFh	
03h		1	FFh	
04h		1	FFh	
05h		1	FFh	
06h		1	FFh	
07h		1	00h	
08h	**10**	**Bytes**	**Vendor / Product Identification**	**See Section 3.3**
08h		2	ID Manufacturer Name	EISA 3-character ID
0Ah		2	ID Product Code	Vendor assigned code
0Ch		4	ID Serial Number	32-bit serial number
10h		1	Week of Manufacture	Week number
11h		1	Year of Manufacture	Year
12h	**2**	**Bytes**	**EDID Structure Version / Revision**	**See Sections 2.2, 2.3 & 3.4**
12h		1	Version #	Binary
13h		1	Revision #	Binary
14h	**5**	**Bytes**	**Basic Display Parameters / Features**	**See Section 3.5**
14h		1	Video Input Definition	
15h		1	Max. Horizontal Image Size	cm.
16h		1	Max. Vertical Image Size	cm.
17h		1	Display Transfer Characteristic (Gamma)	Binary
18h		1	Feature Support	See Table 3.10
19h	**10**	**Bytes**	**Color Characteristics**	**See Section 3.6**
19h		1	Red / Green Low Bits	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1Gy0
1Ah		1	Blue / White Low Bits	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0
1Bh		1	Red-x	Red-x Bits 9 - 2
1Ch		1	Red-y	Red-y Bits 9 - 2
1Dh		1	Green-x	Green-x Bits 9 - 2
1Eh		1	Green-y	Green-y Bits 9 - 2
1Fh		1	Blue-x	Blue-x Bits 9 - 2
20h		1	Blue-y	Blue-y Bits 9 - 2
21h		1	White-x	White-x Bits 9 - 2
22h		1	White-y	White-y Bits 9 - 2
23h	**3**	**Bytes**	**Established Timings**	**See Section 3.7**
23h		1	Established Timings 1	
24h		1	Established Timings 2	
25h		1	Manufacturers Reserved Timings	
26h	**16**	**Bytes**	**Standard Timing Identification**	**See Section 3.8**
26h		2	Standard Timing Identification # 1	
28h		2	Standard Timing Identification # 2	
2Ah		2	Standard Timing Identification # 3	
2Ch		2	Standard Timing Identification # 4	
2Eh		2	Standard Timing Identification # 5	

Address	No. bytes		Description	Format
30h		2	Standard Timing Identification # 6	
32h		2	Standard Timing Identification # 7	
34h		2	Standard Timing Identification # 8	
36h	**72**	**Bytes**	**Detailed Timing Descriptions**	**See Section 3.9**
36h		18	Detailed Timing Description # 1 or Monitor Descriptor.	Use is dependent on EDID structure version and revision numbers
48h		18	Detailed Timing Description # 2 or Monitor Descriptor	Use is dependent on EDID structure version and revision numbers
5Ah		18	Detailed Timing Description # 3 or Monitor Descriptor	Use is dependent on EDID structure version and revision numbers
6Ch		18	Detailed Timing Description # 4 or Monitor Descriptor	Use is dependent on EDID structure version and revision numbers
7Eh	**1**	**Byte**	**Extension Flag**	**Number of (optional) 128-byte EDID extension blocks to follow.**
7Fh	**1**	**Byte**	**Checksum**	**The 1-byte sum of all 128 bytes in this EDID block shall equal zero**

Table 3.1 - EDID Structure Version 1

The sections following this provide details on each byte of the EDID Version 1 data structure. Format is 'least significant byte, most significant byte'.

3.2 Header : 8 bytes

The header is an 8-byte pattern designed to be easily recognizable from other bytes in the data structure. Its format is shown in Table 3.2

8	Bytes	Header
	1	00h
	1	FFh
	1	FFh
	1	FFh
	1	FFh
	1	FFh
	1	FFh
	1	00h

Table 3.2 - EDID Header

3.3 Vendor / Product ID : 10 bytes

The Vendor/Product ID block is made up of several fields used to uniquely identify the monitor. The size and order of the fields is shown in the table below.

10	Bytes	Vendor / Product Identification
	2	ID Manufacturer Name
	2	ID Product Code
	4	ID Serial Number
	1	Week of Manufacture
	1	Year of Manufacture

Table 3.3 - Vendor/Product ID

The ID Manufacturer Name field, shown in Table 3.4, contains a 2-byte representation of the monitors manufacturer. This is the same as the EISA ID. Based on compressed ASCII, “0001=A” ... “11010=Z”.

EISA manufacturer ID’s are issued by Microsoft, contact by:

e-mail : pnpid@microsoft.com
fax : +1 - 206 - 936 - 7329 marked for the attention of PNPID in Building 27.

Description	Byte	Bit							
		7	6	5	4	3	2	1	0
ID Manufacturer Name	1	0) *	(4	3	2	1	0)	(4	3
		Character 1						Char 2	
	2	2	1	0)	(4	3	2	1	0)
		Character 2			Character 3				

Table 3.4 - ID Manufacturer Name

The ID Product code field contains a 2-byte vendor assigned product code. This is used to differentiate between different model from the same manufacturer. If this field is used to represent a model number then the number is stored in hex with the least significant byte first.

The ID serial number is a 32-bit Serial number used to differentiate between individual instances of the same model of monitor. Its use is optional. When used the bit order for this field follows that shown in Table 3.5. The EDID structure Version 1 Revision 1 offers a way to represent the serial number of the monitor as an ASCII string in a separate descriptor block. When the serial number is represented in as a string then the bytes of this field shall not be 00h. Field may either contain a partial serial number or, if unused, shall be set with each byte = 01h

Description	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID Serial Number.	1	(7	6	5	4	3	2	1	0)
	2	(15	14	13	12	11	10	9	8)
	3	(23	22	21	20	19	18	17	16)
	4	(31	30	29	28	27	26	25	24)

Table 3.5 - ID Serial Number

The Week of Manufacture field, if used, is set to a value in the range of 1-53. If this field is not used the value should be set to 0.

The Year of Manufacture field is used to represent the year of the monitor’s manufacture. The value that is stored is an offset from the year 1990 as derived from the following equation:

Value stored = (Year of manufacture - 1990)

For example for a monitor manufactured in 1997 the value stored in this field would be 7.

3.4 EDID Structure Version / Revision : 2 bytes

2	Bytes	EDID Structure Version, Revision	
	1	Version no.	Binary
	1	Revision no.	Binary

Table 3.6 - EDID Structure Version & Revision

The appropriate version and revision numbers shall be stored here. These values define on the EDID structure being used.

3.5 Basic Display Parameters and Features : 5 bytes

5	Bytes	Basic Display Parameters / Features	
	1	Video Input definition	See Table 3.8
	1	Max. Horizontal Image Size	cm.
	1	Max. Vertical Image Size	cm.
	1	Display Transfer characteristic (Gamma)	(gamma x 100)-100, [range 1.00 → 3.55]
	1	Feature Support (DPMS)	See Table 3.10

Table 3.7 - Basic Display Parameters & Features

The Video Input Definition field provides information describing how the host's video outputs should be configured to drive the attached display. This definition applies to displays which use analog signal levels for the video inputs. Displays which use digital signals for these inputs should use the EDID structure Version 2 definition described in chapter 4 of this document. The format of this one-byte field is described below in Table 3.8

Bit	Description	Detailed Description
7	Analog / Digital Signal Level	Defines usage of the rest of byte as "analog" or "digital" input. Analog = 0, Digital = 1. If input is defined as analog then following definitions apply to bits 6 - 0. Digital input requires use of the EDID structure Version 2.
6	Signal Level Standard [6:5]	Refer to following definitions. Format is 'reference white above blank', 'level of sync. tip below blank". (volts) Bit 6 Bit 5 Operation 0 0 0.700 , 0.300 (1.000 V p-p) 0 1 0.714 , 0.286 (1.000 V p-p) 1 0 1.000 , 0.400 (1.400 V p-p) 1 1 0.700 , 0.000 (0.700 V p-p) : See EVC std.
5	Signal Level Standard [6:5]	See above entry for definition
4	Setup	If set = 1, the display expects a blank-to-black setup or pedestal per appropriate Signal Level Standard
3	Sync. Inputs Supported [3]	If set = 1, separate syncs. supported
2	Sync. Inputs Supported [2]	If set = 1, composite sync. (on Hsync line) supported
1	Sync. Inputs Supported [1]	If set = 1, sync. on green video supported
0	Sync. Inputs Supported [0]	If set = 1, serration of the Vsync. Pulse is required when composite sync. or sync-on-green video is used.

Table 3.8 - Video Input Definition

The Maximum Image Size parameters provide information on the maximum image dimensions that can be correctly displayed, as defined by VESA Video Image Area Definition (VIAD) standard, rounded to the nearest centimeter (cm). These values are intended to be the maximum image size that can be properly displayed over the entire set of supported timing / format combinations. The host system is expected to use this data to get a rough idea of the image size and aspect ratio to allow properly scaled text to be selected.

If either or both bytes are set to zero then the system shall make no assumptions regarding the display size.
e.g. A projection display may be of indeterminate size.

2	Bytes	Description	Format
	1	Max. Horizontal Image Size	From 1 → 255 cm See above for special case = 0
	1	Max. Vertical Image size	From 1 → 255 cm See above for special case = 0

Table 3.9 - Maximum Image Size

The display transfer characteristic, referred to as gamma, is stored in a 1-byte field capable of representing gamma values in the range of 1.00 to 3.55. The integer value stored is determined by the formula:

Value stored = (gamma x 100)-100

For example, a gamma value of 2.2 would be represented as 120.

The feature support field is used to indicate support for the VESA Display Power Management Signaling (DPMS) Standard. It is also used to indicate the basic display type. The format of this one-byte field is shown in Table 3.10. Bit 2 and Bit 0 of this field were reserved and set to zero under EDID structure Version 1 Revisions 0 and 1.

1	Byte	Bits	Feature Support	Description
	1	7	Stand-by	Refer to VESA DPMS Specification
		6	Suspend	Refer to VESA DPMS Specification
		5	Active Off	Refer to VESA DPMS Specification
		4-3	Display Type [4:3]	Bit 4 Bit 3 Interpretation 0 0 Monochrome / grayscale display 0 1 R/G/B color display 1 0 Non R/G/B multicolor display e.g. R/G/Y 1 1 Undefined
		2	Standard Default Color Space	If this bit is set to 1, the displays uses a standard default color space as its primary color space.
		1	Preferred Timing Mode	If this bit is set to 1, the display's preferred timing mode is indicated in the first detailed timing block.
		0	GTF supported	If this bit is set to 1, the display supports timings based on the GTF standard

Table 3.10 - Feature Support

3.6 Phosphor or Filter Chromaticity : 10 bytes

These bytes provide colorimetry and white point information. The data is stored in the order shown in Table 3.11.

The white point value shall be the default white point (the white point set at power on or on a reset of the display to its default setting). Provision for multiple white points is made in one of the alternate definitions of the detailed Timing Descriptions permitted in EDID structure Version 1, Revisions 1 & 2 - see Section 3.9.2.

10	Bytes	Color Characteristic	Based on CIE publication 15.2 on colorimetry space
	1	Red / Green Low Bits	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0
	1	Blue / White Low Bits	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0
	1	Red_x	Red_x bits 9 → 2
	1	Red_y	Red_y bits 9 → 2
	1	Green_x	Green_x bits 9 → 2
	1	Green_y	Green_y bits 9 → 2
	1	Blue_x	Blue_x bits 9 → 2
	1	Blue_y	Blue_y bits 9 → 2
	1	White_x	White_x bits 9 → 2
	1	White_y	White_y bits 9 → 2

Table 3.11 - Chromaticity and Default White Point

The chromaticity and white point values are expressed as fractional numbers accurate to the thousandth place. Each number is represented by a binary fraction which is 10 bits in length. In this fraction a value of one for the bit immediately right of the decimal point (bit 9) represents 2 raised to the -1 power. A value to 1 in the right most bit (bit 0) represents a value of 2 raised to the -10 power.

The high order bits (9 → 2) are stored as a single byte. The low order bits (1 → 0) are paired with other low order bits to form a byte. With this representation, all values should be accurate to +/- 0.0005 of the actual value. Examples are shown in Table 3.12.

Actual Value	Binary value	Converted Back to Decimal
0.610	1001110001	0.6103516
0.307	0100111010	0.3066406
0.150	0010011010	0.1503906

Table 3.12 - Ten bit Binary Fraction Representation

3.7 Established Timings : 3 bytes

The established timing block is a field of one-bit flags which are used to indicate support for established VESA and other common timings in a very compact form. Other standardized timings can be described in the Standard Timings block defined in Section 3.8. Non-standard timings are described using the Detailed Timings block, defined in Section 3.9.

Bits 6 → 0 (inclusive) of byte 3 are used to define manufacturer's proprietary timings, and may be used if a manufacturer wants to identify such timings through the use of one-bit flags. VESA takes no responsibility for coordinating or documenting the use of these bits by any manufacturer(s).

A bit set to "1" indicates support for that timing.

3	Bytes	Bit	Description	Source
	1		**Established Timing I**	
		7	720 x 400 @ 70Hz	IBM, VGA
		6	720 x 400 @ 88Hz	IBM, XGA2
		5	640 x 480 @ 60Hz	IBM, VGA
		4	640 x 480 @ 67Hz	Apple, Mac II
		3	640 x 480 @ 72Hz	VESA
		2	640 x 480 @ 75Hz	VESA
		1	800 x 600 @ 56Hz	VESA
		0	800 x 600 @ 60Hz	VESA
	1		**Established Timing II**	
		7	800 x 600 @ 72Hz	VESA
		6	800 x 600 @ 75Hz	VESA
		5	832 x 624 @ 75Hz	Apple, Mac II
		4	1024 x 768 @ 87Hz(I)	IBM
		3	1024 x 768 @ 60Hz	VESA
		2	1024 x 768 @ 70Hz	VESA
		1	1024 x 768 @ 75Hz	VESA
		0	1280 x 1024 @ 75Hz	VESA
	1		**Manufacturer's Timings**	
		7	1152 x 870 @ 75Hz	Apple, Mac II
		6-0	Reserved	

Table 3.13 - Established Timings

3.8 Standard Timing Identification

The next 16 bytes provide identification for up to 8 additional timings, each identified by a unique 2-byte code derived from the mode format and refresh rate as described below. It is expected that this scheme will be used to identify future standard timings not included in the Established Timings section (see Section 3.7), and that it may also be used in monitors intended to be used exclusively with proprietary systems where the host already has the complete timing information. Additional standard timings may be listed by using one of the alternate definitions of the detailed Timing Descriptions permitted in EDID Structure Version 1, Revision 1&2 - see Section 3.9.2.

Note : The 2-bytes identifier codes for VESA standard timing modes are defined as part of each VESA Timing Standard.

Unused fields in this section shall be set to 01h.

16	Byte	Bit	Description	Source
2			**Standard Timing Identification 1**	**Comment**
	1		**(Horizontal active pixels / 8) - 31**	The range of Horizontal active pixels that can be described in each byte is 256 → 2288 pixels, in increments of 8 pixels.
	1	**7,6**	**Image Aspect ratio** Bit 7 Bit 6 Operation 0 0 1:1 Aspect ratio 0 1 4:3 Aspect ratio 1 0 5:4 Aspect ratio 1 1 16:9 Aspect ratio	The vertical active line count may be calculated from the aspect ratio and the Horizontal active pixel count given in the first byte. "Square" pixels (1:1 pixel aspect ratio) shall be assumed.
		5→0	Refresh Rate (Hz) - 60	Range 60 → 123 Hz
2			**Standard Timing Identification 2**	See above definition for Standard Timing 1
2			**Standard Timing Identification 3**	See above definition for Standard Timing 1
2			**Standard Timing Identification 4**	See above definition for Standard Timing 1
2			**Standard Timing Identification 5**	See above definition for Standard Timing 1
2			**Standard Timing Identification 6**	See above definition for Standard Timing 1
2			**Standard Timing Identification 7**	See above definition for Standard Timing 1
2			**Standard Timing Identification 8**	See above definition for Standard Timing 1

Table 3.14 - Standard Timings

3.9 Detailed Timing Block - 72 bytes

The detailed timing block is divided into four descriptors which are 18 bytes each. In all revisions of the EDID structure Version 1, these blocks can be used to describe detailed timings that the monitor supports. EDID structure Version 1 Revisions 1 & 2 also allows use of these blocks to describe other types of data as specified in Section 3.9.2.

Note: Unused Detailed Timing and Descriptor Descriptions shall contain the data for a supported timing standard (generally this will be a standard already identified in the Established Timing or Standard Timing identification fields).

3.9.1 Detailed Timing Descriptor - 18 bytes - EDID Structure Version 1 All Revsions

18	Bytes	Detailed Timing Descriptions	Format
	2	Pixel clock / 10,000	Stored LSB first Example : 135 MHz would be 13500 decimal, stored as BCh,34h
	1	Horizontal Active	Pixels, lower 8 bits
	1	Horizontal Blanking	Pixels, lower 8 bits
	1	Horizontal Active : Horizontal Blanking	Upper nibble : upper 4 bits of Horizontal Active Lower nibble : upper 4 bits of Horizontal Blanking
	1	Vertical Active	Lines, lower 8 bits
	1	Vertical Blanking	Lines, lower 8 bits
	1	Vertical Active : Vertical Blanking	Upper nibble : upper 4 bits of Vertical Active Lower nibble : upper 4 bits of Vertical Blanking
	1	Horizontal Sync. Offset	Pixels , from blanking starts, lower 8 bits
	1	Horizontal Sync Pulse Width	Pixels, lower 8 bits
	1	Vertical Sync Offset : Vertical Sync Pulse Width	Upper nibble : lines, lower 4 bits of Vertical Sync Offset Lower nibble : lines, lower 4 bits of Vertical Sync Pulse Width
	1	Horizontal Sync Offset Horizontal Sync Pulse Width Vertical Sync Offset Vertical Sync Pulse Width	bits 7,6 : upper 2 bits of Horizontal Sync Offset bits 5,4 : upper 2 bits of Horizontal Sync Pulse Width bits 2,3 : upper 2 bits of Vertical Sync Offset bits 0,1 : upper 2 bits of Vertical Sync Pulse Width
	1	Horizontal Image Size	mm, lower 8 bits
	1	Vertical Image Size	mm, lower 8 bits
	1	Horizontal & Vertical Image Size	Upper nibble : upper 4 bits of Horizontal Image Size Lower nibble : upper 4 bits of Vertical Image Size
	1	Horizontal Border	Pixels, see Section 3.11
	1	Vertical Border	Lines, see Section 3.11
	1	Flags	Interlace, Stereo, Horizontal polarity, Vertical polarity, Sync Configuration, etc. Bit 7 Function 0 Non-interlaced 1 Interlaced Bit 6 Bit 5 Function 0 0 Normal display, no stereo x x See Table 3.16 for definition Bit 4 Bit 3 Function 0 0 Analog composite 0 1 Bipolar analog composite 1 0 Digital composite 1 1 Digital separate Bit 2 Bit 1 Function The interpretation of bits 2 and 1 is dependent on the decode of bit 4 and 3 - see Table 3.17. Bit 0 See Table 3.16 for definition

Table 3.15 - Detailed Timing Description

Note : Unused Detailed Timing Descriptors shall contain the data for a supported timing standard (generally this will be a standard already identified in the Established Timing or Standard Timing Identification fields).

Bit 6	Bit 5	Bit 0	Definition
0	1	0	Field sequential stereo, right image when stereo sync. = 1
1	0	0	Field sequential stereo, left image when stereo sync. = 1
0	1	1	2-way interleaved stereo, right image on even lines
1	0	1	2-way interleaved stereo, left image on even lines
1	1	0	4-way interleaved stereo
1	1	1	Side-by-Side interleaved stereo

Table 3.16 - Decode of Stereo Mode Bits

The sync scheme for a detailed timing is described in bits 4-1 of the Flag byte. Bits 4 and 3 describe one of four schemes. Bits 2 and 1 give further details dependent on the values in bits 4 & 3. This is shown in Table 3.17.

Bits 4 and 3	Bit 2	Bit 2 Defn.	Bit 1	Bit 1 Defn.
0,0 Analog Composite	Serrate	If set, controller shall supply serration (Hsync during Vsync).	On RGB	If set, sync pulses should appear on all 3 video signal lines. If not set, sync on green video line only.
0,1 Bipolar Analog Composite	Serrate	If set, controller shall supply serration (Hsync during Vsync).	On RGB	If set, sync pulses should appear on all 3 video signal lines. If not set, sync on green video line only.
1,0 Digital Composite	Serrate	If set, controller shall supply serration (Hsync during Vsync).	Composite Polarity	This is the polarity of the Hsync pulses outside of Vsync. Polarity is positive if bit is set to 1
1,1 Digital Separate	Vertical Polarity	Vsync signal Polarity is Positive if bit is set to 1.	Horizontal Polarity	Hsync signal polarity is Positive if bit is set to 1.

Table 3.17 - Sync Signal Description

3.9.2 Descriptor Description - 18 bytes each - EDID Structure Version 1 Revision 1

In EDID structure Version 1, Revisions 1 and 2, any or all of the 18-byte Detailed Timing Description blocks may be redefined as a Monitor Descriptor block using the general format shown in Table 3.18. Detailed description of the data types are shown in Table 3.19. Those not redefined shall use the EDID structure Version 1, Revision 0 format defined in Table 3.15. In this case all detailed timings shall appear before any alternate descriptor blocks.

18	Bytes	Monitor Descriptor	Values
	2	Flag	Flag = 0000h when block used as descriptor
	1	Flag	Reserved = 00h when block used as descriptor
	1	Data Type Tag (Binary coded)	FFh : Monitor Serial Number - Stored as ASCII, code page # 437, ≤ 13 bytes. FEh : ASCII String - Stored as ASCII, code page # 437, ≤ 13 bytes. FDh : Monitor range limits, binary coded FCh : Monitor name, stored as ASCII, code page # 437 FBh : Descriptor contains additional color point data FAh : Descriptor contains additional Standard Timing Identifications F9h - 10h : Currently undefined 0Fh - 00h : Descriptor defined by manufacturer.
	1	Flag	00h when block used as descriptor
	13	Descriptor Data	definition dependent on data type tag chosen. Tag definitions in Table 3.19

Table 3.18 - Monitor Descriptor Block Summary

Data Tag	Monitor Descriptor Data	Format
FFh	Monitor S/N (ASCII)	If < 13 bytes then terminate with ASCII code 0Ah and pad field with ASCII code 20h. Data shall be sequence such that 1st byte = 1st character etc.
FEh	ASCII Data String	If < 13 bytes then terminate with ASCII code 0Ah and pad field with ASCII code 20h. Data shall be sequence such that 1st byte = 1st character etc.
FDh	Monitor Range Limits	Byte 5 : Min. Vertical rate (for interlace this refers to field rate) Binary coded rate in Hz., integer only Byte 6 : Max. Vertical rate (for interlace this refers to field rate) Binary coded rate in Hz., integer only Byte 7 : Min. Horizontal in KHz, integer only, binary coded Byte 8 : Max. Horizontal in KHz, integer only, binary coded Byte 9 : Max. Supported Pixel Clock (manufacturer's defn.- see note) Binary coded clock rate in MHz / 10 e.g. 130 MHz is 0Dh Set to FFh if not specified Byte 10 - 17 are reserved for VESA GTF Standard If not used for GTF Standard then following applies. Byte 10 : Set = 00h if unused for GTF. Byte 11 : Set to 0Ah if unused for GTF. Byte 12-17 : Set = 20h if unused for GTF. Note : Check with monitor manufacturer for definition.
FCh	Monitor Name (ASCII)	If < 13 bytes then terminate with ASCII code 0Ah and pad field with ASCII code 20h. Note : Intent of this field is to provide a meaningful name to the user

Data Tag	Monitor Descriptor Data	Format
FBh	Color Point	Note : Chromaticity data to be coded as Section 3.6 Note : Gamma data to be coded as Section 3.5 Byte 5 : White point index number (binary) Byte 6 : White low bits Byte 7 : White_x Byte 8 : White_y Byte 9 : White Gamma Byte 10 : White point index number (binary) Byte 11 : White low bits Byte 12 : White_x Byte 13 : White_y Byte 14 : White Gamma Byte 15 : Set = 0Ah Byte 16 - 17 : Set = 20h Note : An index number of 00h indicates that no color point data follows
FAh	Standard Timing Identifiers	Note : Data format as Section 3.8 Bytes 5 & 6 : Standard Timing Identification 9 Bytes 7 & 8 : Standard Timing Identification 10 Bytes 9 & 10 : Standard Timing Identification 11 Bytes 11 & 12 : Standard Timing Identification 12 Bytes 13 & 14 : Standard Timing Identification 13 Bytes 15 & 16 : Standard Timing Identification 14 Byte 17 : Set = 0Ah Note : It is permissible to redefine more than one detailed timing block as Standard Timing Identifiers.
00-0Fh	Manufacturer Specified	Note : Descriptors with data type tags in this range are defined by the monitor manufacturers and are not specified by VESA. Questions regarding interpretation should be directed to the monitor manufacturer. Note: EDID structure version 1 revision 1 reserved only tags 00h & 01h for manufacturer specific use.

Table 3.19 - Monitor Descriptor Details

Note :Unused Detailed Timing and Descriptor Descriptions shall contain the data for a supported timing standard (generally this will be a standard already identified in the Established Timing or Standard Timing identification fields).

3.10 Extension Flag and Checksum

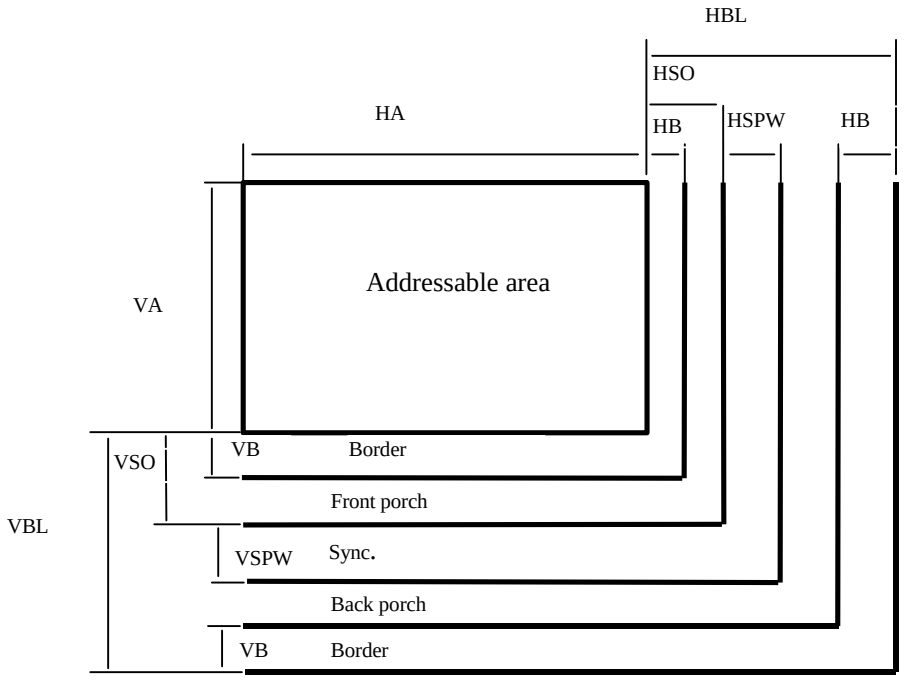
2	Bytes	Description	Function
	1	Extension Flag	Indicates the number of (optional) Extension EDID blocks to follow.
	1	Checksum	This byte should be programmed such that a one-byte checksum of the entire 128 byte EDID equals 00h.

Table 3.20 - Extension Flag and Checksum

3.11 Note Regarding Borders

This section is included to provide a frame of reference for the use of borders in detailed timings.

- Both the horizontal and vertical border sizes are for one side only. i.e. the actual number of pixels or lines taken up by both borders is twice the listed value.
- Borders are assumed to be symmetric.
- Borders are not considered part of the active image time and do not affect the total line time which should always be found by adding the active and blanking times for each axis.
- Borders may be part of the blanking time, but that portion that may be safely used to provide an illuminated solid-color border around the active image area.



VA	Vertical Active	HA	Horizontal Active
VBL	Vertical Blanking	HBL	Horizontal Blanking
VB	Vertical Border	HB	Horizontal Border
VSO	Vertical Sync. Offset	HSO	Horizontal Sync. Offset
VSPW	Vertical Sync. Pulse Width	HSPW	Horizontal Sync. Pulse Width

4. Extended Display Identification Data (EDID) Structure Version 2

4.1 EDID Format Overview

Address	No. bytes		Description	Format
00h	**1**	**Bytes**	**EDID Structure Version / Revision**	Binary
01h	**7**	**Bytes**	**Vendor / Product Identification**	
01h		2	ID Manufacturer Name	EISA 3-character ID
03h		2	ID Product Code	Vendor assigned code
05h		1	Week of Manufacture	Week number
06h		2	Year of Manufacture	Binary
08h	**32**	**Bytes**	**Manufacturer/product ID string**	ASCII
28h	**16**	**Bytes**	**Serial number string**	ASCII
38h	**8**	**Bytes**	**Unused (Reserved)**	Set each byte to 20h
40h	**15**	**Bytes**	**Display Interface Parameters**	
40h		1	Physical Interface Type (connector)	
41h		1	Video Interface Type	
42h		8	Interface Data Format	
4Ah		5	Interface Color/Luminance Encoding	
4Fh	**5**	**Bytes**	**Display Device Description**	
4Fh		1	Display Technology Type/Subtype	
50h		1	Major Display Characteristics	
51h		3	Features Support	
54h	**2**	**Bytes**	**Display Response Time**	
56h	**28**	**Bytes**	**Color/Luminance Description**	
56h		4	Display Transfer Characteristic (Gamma)	Binary
5Ah		4	Max Luminance & Offset	
5Eh		20	Colorimetry / White Point(s)	See Tables 4.21 & 4.22
72h	**10**	**Bytes**	**Display Spatial Description**	
72h		4	Max. Image Size	mm.
76h		4	Max. Addressibility	pixels
7Ah		2	Dot/Pixel Pitch	mm*100
7Ch	**1**	**Byte**	**Unused (Reserved)**	Set to 0
7Dh	**1**	**Bytes**	**GTF Support Information**	
7Eh	**2**	**Bytes**	**Map Of Timing Information**	
80h	**127**	**Bytes**	**Luminance Table & Timing Descriptions**	
*		*x**A	Luminance Table	Size *x* specified in Section 4.4
*		8*B	Range Limits	
*		27*C	27-Byte - Detailed Range Limits	
*		4*D	4-Byte Timing Codes	
*		18*E	18-byte Detailed Timing Descriptions	
*		X	X=127 - (*x**A+8*B+27*C+4*D+18*D)	Set to 00h
FFh	**1**	**Byte**	**Checksum**	The 1-byte sum of all 256 bytes = 0

Table 4.1 - EDID Structure Version 2 Revision 0

4.2 Manufacturer and Product Identifiers - 64 Bytes

4.2.1 EDID Structure Version / Revision

The appropriate Version and Revision numbers of the data structure are stored here.

Bit	Description	Detailed Description
7-4	Version Number	Binary encoding of EDID Structure Version
3-0	Revision Number	Binary encoding of EDID Structure Revision

Table 4.2 - EDID Structure Version and Revision

Note that the version number cannot be set to a value of 1 since EDID data structure Version 1 does not use this layout.

4.2.2 Vendor / Product IDs

The Vendor/Product ID block is made up of several fields used to uniquely identify the monitor. The size and order of the fields is shown in the table below. These fields share the same format as their corresponding fields in the Version 1 data structure.

7	Bytes	Vendor / Product Identification
	2	ID Manufacturer Name
	2	ID Product Code
	1	Week of Manufacture
	2	Year of Manufacture

Table 4.3 - Vendor/Product ID

The ID Manufacturer Name field, shown in Table 4.4, contains a 2-byte representation of the monitors manufacturer. This is the same as the EISA ID. Based on compressed ASCII, “0001=A” ... “11010=Z”.

EISA manufacturer ID’s are issued by Microsoft, contact by:

e-mail : pnpid@microsoft.com
fax : +1 - 206 - 936 - 7329 marked for the attention of PNPID in Building 27.

Description	Byte	Bit							
		7	6	5	4	3	2	1	0
ID Manufacturer Name	1	0) *	(4	3	2	1	0)	(4	3
		Character 1						Char 2	
	2	2	1	0)	(4	3	2	1	0)
		Character 2			Character 3				

Table 4.4 - ID Manufacturer Name

The ID Product code field contains a 2-byte vendor assigned product code. This is used to differentiate between different model from the same manufacturer. If this is used to represent a model number then the number is stored in hex with least significant byte first.

The Week of manufacture field is set to a value in the range of 1-53 if used. If this field is not used the value should be set to 0.

The year of manufacture is stored in a 2-byte hex format with least significant byte first. Note, that this is the actual year value and not an offset as in EDID structure 1. For example the year 1997 (07CDh) would be stored CDh at location 06 and 07 at location 07

4.2.3 Manufacturer/Product Name and Serial Number Strings

These fields provide ASCII strings with the manufacture name product name and serial number of the display. The strings allow a user readable representation of this information. The manufacturer and product name are combined in a single field described in Table 4.5. The serial number string is described in Table 4.6.

Bytes	Description	Detailed Description
32	ASCII string	This string is comprised of both manufacture name and model name. The two names are separated using ASCII code 09h so that the two sub-fields can be parsed separately. If the entire string is < 32 bytes then it is terminated with ASCII code 0Ah and the field is padded with ASCII code 20h. Note : This field is intended to provide a meaningful name to the user.

Table 4.5 - Manufacturer/Product Name String

Bytes	Description	Detailed Description
16	ASCII string	If < 16 bytes then the string is terminated with ASCII code 0Ah and the field padded with ASCII code 20h.

Table 4.6 - Serial Number String

4.3 Basic Display Parameters/Features - 64 Bytes

4.3.1 Display Interface Parameters

This section defines parameters for the interface between the display and the host system. It allows for a default and secondary display interface to be defined. In this case both interfaces are addressing the same display. The order and size of the parameter blocks is shown below in Table 4.7. If the display does not have a secondary interface, corresponding fields are set to 0.

15	Bytes	Display Interface Parameters	
	1	Physical Connector Type(s)	see Table 4.8
	1	Video Interface Type(s)	see Table 4.9
	8	Interface Data Format	see Table 4.10 or Table 4.11
	5	Interface Color/Luminance Encoding(s)	see Table 4.12

Table 4.7 - Display Interface Parameters

The physical connector type parameter indicates the connector that is used on the back of the display. If the display uses a captive cabling system, it indicates the connector at the end of the cable. Available selections are listed below in Table 4.8. The upper nibble indicates the connector for the default interface. If a secondary interface is available, its connector is indicated using the lower nibble.

Bit	Description	Detailed Description
7-4	Default physical interface	0 = None (Not valid for default connector) 1 = BNC 2 = 15 pin VGA 3 = 13w3 4 = VESA EVC 5 = VESA P&D-D 6 = Micro-ribbon Connector (per the VESA P&D standard) 7 = IEEE-1394 connector 8 = VESA FPDI-2 9-E = Reserved F = Non-standard connector
3-0	Secondary physical interface	Same as above

Table 4.8 - Physical Connector Type

The video interface type parameter indicates the interface that is used to transmit the video data to the display. Available selections are listed below in Table 4.9. The default interface is indicated in the upper nibble. If a secondary interface is available, its video interface is indicated in the lower nibble.

Bit	Description	Detailed Description
7-4	Default interface	0 = None (Not valid for default interface) 1 = Analog 2 = Analog w/ sampled pixel clock 3 = TMDS (Transition Minimized Differential Signaling) 4 = IEEE-1394-1995 5 = LVDS 6 = Parallel 7 - F = Reserved
3-0	Secondary interface	Same as above

Table 4.9 - Video Interface Type

The interface data format parameters describe details of the video interface(s) selected above. The first 4 bytes of the field describe the parameters for the default interface. The fifth through eighth bytes describe parameters for the secondary interface if supported. If a secondary interface is not supported, bytes 5-8 should each be set to 00h. Analog interfaces are described using the 4-byte definition shown in Table 4.10. Digital interfaces are described using the 4-byte definition shown in Table 4.11.

4	Byte	Bit	Description	Detailed Description
	1	7	Reserved	Set to 0.
		6	Signal Level Standard [6:5]	Refer to following definitions. Format is 'reference white above blank', 'level of sync. tip below blank". (volts) Bit 6 Bit 5 Operation 0 0 0.700 , 0.300 (1.000 V p-p) 0 1 0.714 , 0.286 (1.000 V p-p) 1 0 1.000 , 0.400 (1.400 V p-p) 1 1 0.700 , 0.000 (0.700 V p-p) (See EVC std.)
		5	Signal Level Standard [6:5]	See above entry for definition
		4	Setup	If set = 1, the display expects a blank-to-black setup or pedestal per appropriate Signal Level Standard
		3	Sync. Inputs Supported [3]	If set = 1, separate syncs. supported
		2	Sync. Inputs Supported [2]	If set = 1, composite sync. (on Hsync line) supported
		1	Sync. Inputs Supported [1]	If set = 1, sync. on green video supported
		0	Sync. Inputs Supported [0]	If set = 1, serration of the Vsync. Pulse is required when composite sync. or sync-on-green video is used.
	1	7	Pixel Clock Supported	If set = 1, display directly supports use of pixel clock
		6-0	Reserved	set to 0
	1	-	Reserved	set to 0
	1	-	Reserved	set to 0.

Table 4.10 - Analog Interface Data Format Description

4	Byte	Bit	Description	Detailed Description
	1	7	Display Enable Polarity	0 = Display enabled when DE is low 1 = Display enabled when DE is high
		6	Edge of Shift clock used	0 = Display uses falling edge of shift clock 1= Display uses rising edge of shift clock Note: If the display receives data on both edges of the shift clock, this field is ignored. See tables 4.32 & 4.35
		5-4	Number of receiver units	Indicates number of data receiver units (Range 1-3) Note: Multiple receivers may be required to support "dual pixel per clock" interfaces
		3-0	Channel Speed Exponent	0 = expressible range is 0 - 255 MHz in 1 MHz increments 1 = expressible range is 0 - 510 MHz in 2 MHz increments 2 = expressible range is 0 - 1.02 GHz in 4 MHz increments 3 = expressible range is 0 - 2.04 GHz in 8 MHz increments 4 = expressible range is 0 - 4.08 GHz in 16 MHz increments 5 = expressible range is 0 - 8.16 GHz in 32 MHz increment . . . F = expressible range is 0 - 8.36 THz in 32.8 GHz increments
	1	-	Minimum channel speed	Range 0-255 * 2^n MHz n = channel speed exponent
	1	-	Maximum channel speed	Range 0-255 * 2^n MHz n = channel speed exponent
	1	-	digital interface data format Note: Format details shown in Appendix A. P&D supports displays using 15h, 19h or 24h FPDI-2 supports displays using 15h, 19h, or 24h	00h = 8-Bit Mono STN-SS 01h = 8-Bit RGB STN-SS 04h = 16-Bit RGB STN-SS 10h = 4-Bit Over 4-Bit Mono STN-DD 11h = 4-Bit Over 4-Bit RGB STN-DD 14h = 8-Bit Over 8-Bit Mono STN-DD 15h = 8-Bit Over 8-Bit RGB STN-DD 19h = 12-Bit Over 12-Bit RGB STN-DD 20h = Pseudo 18-Bit RGB TFT 24h = 24-Bit MSB-Aligned RGB TFT 25h = 24-Bit LSB-Aligned RGB TFT 30h = Double 12-Bit RGB TFT 34h = Double 18-Bit RGB TFT 38h = Double 24-Bit RGB TFT 40h = 8-Bit or 10-Bit Parallel YCrCb 41h = 8-Bit Serial YCrCb 42h = 10-Bit Serial YCrCb

Table 4.11 - Digital Interface Data Format Description

Color/luminance encoding for both the default interface and the optional secondary interface are described in the 5 byte field shown in Table 4.12. The parameters indicate the color encoding method used. They also indicate bit depth that is supported for each of the subchannels used by the encoding methods.

5	Byte	Bit	Description	Detailed Description
	1	7-4	Color encoding default interface Note: In all cases the signals specified for each of these color encoding systems map to the physical sub-channels in the order given above (i.e. in an RGB system, the Red information is carried on sub-channel 0, the Green is on 1 and the Blue is on 2. In a YIQ system, the Y information is on sub-channel 0, the I on 1 and the Q on 2)	0 = Monochrome 1 = RGB (additive color) 2 = CMY (subtractive color) 3 = CMYK (4 color subtractive) 4 = Y/C color (luminance/chrominance on separate channels per the S-video standard, NTSC encoding) 5 = Y/C color (luminance/chrominance on separate channels per the S-video standard, PAL encoding 6 = Y/C color (luminance/chrominance on separate channels per the S-video standard, SECAM encoding 7 = YIQ (Luminance plus two separate chroma channels, using NTSC encoding) 8 = YIQ (Luminance plus two separate chroma channels, using PAL encoding) 9 = YIQ (Luminance plus two separate chroma channels, using SECAM encoding) A = YCrCb (per SMPTE 293M) B = YPrPb (per SMPTE 240M-1995) C = XYZ (CIE color coordinates) D = CIE Luv E = CIE Lab F = Digital color per the ATSC standard
		3-0	Color encoding secondary interface	same as above.
	1	7-4	supported bit-depth of sub-channel 0 (“Red”)	bits per color (1-15) Primary interface 0 indicates no information for this channel
		3-0	supported bit-depth of sub-channel 1 (“Green”)	bits per color (1-15) Primary interface 0 indicates no information for this channel
	1	7-4	supported bit-depth of sub-channel 2 (“Blue”)	bits per color (1-15) Primary interface 0 indicates no information for this channel
		3-0	supported bit-depth of sub-channel 3	bits per color (1-15) Primary interface Most devices will supply only 3 channels of color data and set this to zero. CMYK is the exception. In this case no colorimetry information is available for this channel
	1	7-4	supported bit-depth of sub-channel 0 (“Red”)	bits per color (1-15) Secondary interface 0 indicates no information for this channel
		3-0	supported bit-depth of sub-channel 1 (“Green”)	bits per color (1-15) Secondary interface 0 indicates no information for this channel
	1	7-4	supported bit-depth of sub-channel 2 (“Blue”)	bits per color (1-15) Secondary interface 0 indicates no information for this channel
		3-0	supported bit-depth of sub-channel 3	bits per color (1-15) Secondary interface Most devices will supply only 3 channels of color data and set this to zero. CMYK is the exception. In this case no colorimetry information is available for this channel

Table 4.12 - Color/Luminance Encoding Description

4.3.2 Display Device Description

This group of parameters describe characteristics of the physical display device as well as indicating additional features that the display supports or that are located within the display device. The ordering and size of the parameters are shown in Table 4.13.

5	Bytes	Display Device Description	
	1	Display technology type/subtype	see Table 4.14
	1	Major display characteristics	see Table 4.15
	3	Feature Support	see Table 4.16

Table 4.13 - Display Device Description

The display technology field is used to indicate the physical device used to implement the display. The field is organized to allow indication of a major type of display technology as well as indication of various subtype of that technology. Table 4.14 shows defined types and subtypes along with their assigned values.

Bits 7-4 Type	Bits 3-0 Subtype	Description
0	--	**Cathode Ray Tube (CRT)**
	0	Monochrome
	1	Shadowmask Color (e.g. dot trio mask, slot mask and appeture grill)
	2	Beam Index Color
	3	Beam Penetration Color
	4-F	Reserved
1	--	**Liquid Crystal Display (LCD)**
	0	Super Twisted Nematic (STN)
	1	Dual Scan Twisted Nematic (DSTN)
	2	Ferroelectric (FLCD)
	3	Conventional Thin Film Transistor (TFT)
	4	In Plane Switching Thin Film Transistor (TFT)
	5	Polymer Dispersed (PDLCD)
	6	Polymer-Stabilized Cholesteric Liquid Crystal Dispersion (PSCLCD)
	7	Plasma Addressed Liquid Crystal Display (PALCD)
	8-F	Reserved
2	--	**Electroluminescent Display (EL)**
	0	AC Thin film
	1	AC Thick film
	2	DC Thin film
	3	DC Thick film
	4-F	Reserved
3	--	**Plasma Display Panels (PDP)**
	0	AC
	1	DC
	2-F	Reserved
4	--	**Field Emission Displays (FED)**
	0	TBD
	1-F	Reserved
5	--	**Light Emitting Diode (LED)**
	0	TBD
	1-F	Reserved
6	--	**Integrated Reflective Display (e.g. TI Digital Micro-mirror Device)**
	0	1 Chip
	1	2 Chip
	2	3 Chip
	3-F	Reserved
7-F	--	**Reserved**

Table.4.14 - Display Technology Types & Subtypes

The major characteristics of the display are described in a 1-byte field as defined in Table 4.15.

Bit	Description	Detailed Description
7	Color	0 = Mono 1 = Color
6	Selectable Display chromaticity	If set to 1 the display supports at least one alternate set of primary chromaticity in addition to the set which is described in Section 4.3.4. These alternate values and the mechanism to switch to them are not described in this document.
5	Conditional update	If set = 1 the display has an image store and need only be updated if the image changes
4-3	Scan Orientation	00 = not scanned - update via random access 01 = Fast axis Left to Right slow axis Top to Bottom (normal landscape) 10 = Fast axis Top to Bottom slow axis Left to Right (normal portrait) 11 = Fast Axis Top to Bottom slow axis Right to Left (reverse portrait)
2	Display Background	0 = Display uses non-transparent background 1 = Display uses transparent background. Note: When this bit is set to 1, areas of the display that are not active allow the user to see through the display (e.g. heads-up display)
1-0	Physical Implementation	00 = Large Image device for group viewing 01 = Desktop or personal display 10 = Eyepiece type personal display 11 = Reserved

Table 4.15 - Major Characteristics

Three bytes are used to described the features of the display. The definition of these bytes are shown below in Table 4.16. Some of these features directly relate to the display of video. Others features may not be related to the display of video but instead are additional devices connected to or located in the same housing as the display device.

3	Byte	Bit	Feature Support	Description
	1	7	Stand-by	Refer to VESA DPMS Specification
		6	Suspend	Refer to VESA DPMS Specification
		5	Active Off	Refer to VESA DPMS Specification
		4	Off (with no DPMS recovery)	Refer to VESA DPMS Specification
		3-1	Stereo Support	000 = no direct stereo 001 = Field seq stereo via stereo sync signal 010 = directview autostereo, column interleave 011 = directview autostereo, line interleave 100-111 = reserved
		0	Reserved	Set = 0
	1	7	Audio Input	0 = Mono 1 = Stereo
		6-5	Audio Input Interface	00 = None 01 = Analog 10 = USB 11 = IEEE-1394
		4	Audio Output	0 = Mono 1 = Stereo
		3-2	Audio Output Interface	00 = None 01 = Analog 10 = USB 11 = IEEE-1394
		1-0	Video input	00 = None 01 = Analog -Y/C connection on EVC 10 = USB Camera 11 = IEEE-1394 Camera
	1		Additional features	
		7	Touch screen	1=Display contains touch screen
		6	Light Pen	1=Display supports light pen
		5	Luminance probe	1=Display supports luminance probe
		4	Colorimeter	1=Display supports colorimeter
		3	Adjustable Orientation	1= Display can be switched between landscape and portrait modes
		2-0	Reserved	Set = 0

Table 4.16 - Feature Support

4.3.3 Display Response Time

This parameter is used to characterize the visual response time of the display defined as the time required for the display to transition from 10% luminance to 90% luminance (rise time), or 90% luminance to 10% luminance (fall time), assuming no limitation imposed by the transition time of the input signal, i.e., an instantaneous change on all inputs.

2	Byte	Bit	Description	Format
	1	7-4	Rise time exponent	n
		3-0	Rise time response in seconds	Range 0-15 * 10^{-n} n = rise time exponent
	1	7-4	Fall time exponent	n
		5-0	Fall time response in seconds	Range 0-15 * 10^{-n} n = fall time exponent

Table 4.17 - Display Response Time Parameters.

4.3.4 Color/Luminance Description

This group of parameters describe the chromaticity, white point(s), gamma(s), offset and maximum luminance for the display. Provisions for alternate white points and gammas are provided for cases where the display offers a mechanism to select between several.

The gamma, luminance, and offset values provided by this section of EDID are intended to be used to describe the display's output luminance vs. Input signal level characteristic, per the CIE gamma model, defined in CIE technical report number 122 as:

$$Y = (Ax + B)^g$$

where Y is the output luminance, x is the input signal level, the exponent g is the "gamma", and A and B are parameters typically referred to as "gain" and "offset", and defined such that A + B = 1 for normalized luminance and input signal levels. The offset ("B") value stored in EDID is given assuming such normalized conditions, i.e., the output luminance is exactly 1 when the input signal level is exactly 1. The gain parameter "A" is not explicitly given in EDID, as it may be calculated by the application based on the relationship between "A" and "B" mentioned above.

The display transfer characteristic, or gamma, is described using the definition shown in Table 4.18. This allows the description of the white gamma as well as gamma values for red green and blue in a range 1.00 to 3.55. The value stored here is the display's default gamma. Alternate selectable white gamma values can also be given as shown in Table 4.22. If the display has an adjustable gamma, this can be indicated as shown in Table 4.19.

4	Bytes	Gamma	
	1	White Gamma	(gamma x 100)-100, [range 1.00 → 3.55]
	1	Color 0 ("red") Gamma (optional)	same as above. If unused set to FFh
	1	Color 1 ("green") Gamma (optional)	same as above. If unused set to FFh
	1	Color 2 ("blue") Gamma (optional)	same as above. If unused set to FFh

Table 4.18 - Display Transfer Characteristic (Gamma)

The maximum luminance value refers to the luminance as measured under conditions defined in ISO 9241/3 and DIS ISO 13406-2

The offset value shown in Table 4.19 is the parameter defined as "B" in the CIE gamma model described previously in this section.

4	Byte	Bit	Description	Format
	2	-	Maximum Luminance (white)	in units of cd/m^2*10
	1	7	Standard RGB model	If set the display conforms to the "standard RGB" model, or at least conforms to this model under at least one user-selectable setting of color temperature, etc.
		6	Adjustable Gamma	If set, signifies a display with adjustable gamma. If this bit is set, the information provided in Table 4.18 should be interpreted as the factory default setting; current setting must be obtained through use of a command over a control channel (e.g. DDC2B+ or USB). Note: this bit is NOT set solely due to the presence of a "brightness" control or similar adjustment which admittedly can affect the parameters of the gamma model; in displays with these adjustments, such as typical CRT monitors, the information in Table 4.18 is still assumed to be the factory defaults settings even though this bit is not set.
		5-1	Reserved	set to 0
		0	Offset sign bit	0 = Offset value is Positive 1 = Offset value is Negative
	1	-	Offset Value	Offset*100 (Range 0.000 to 0.255)

Table 4.19 - Luminance & Offset Value

The phosphor or filter chromaticity and default white point data are stored in the order shown in Table 4.21 below. Additional white points and gamma values that the display supports can be described using the definitions in Table 4.22.

The chromaticity and white point values are expressed as fractional numbers accurate to the thousandth place. Each number is represented by a binary fraction which is 10 bits in length. In this fraction a value of one for the bit immediately right of the decimal point (bit 9) represents 2 raised to the -1 power. A value to 1 in the right most bit (bit 0) represents a value of 2 raised to the -10 power. With this representation, all values should be accurate to +/- 0.0005 of the actual value.

Actual Value	Binary value	Converted Back to Decimal
0.610	1001110001	0.6103516
0.307	0100111010	0.3066406
0.150	0010011010	0.1503906

Table 4.20 - Binary Fraction Encoding Examples

In Tables 4.21 and 4.22 the high order bits (9 → 2) are stored as a single byte. The low order bits (1 → 0) are paired with other low order bits to form a byte.

10	Bytes	Color Characteristic	Based on CIE publication 15.2 on colorimetry space
	1	Red / Green Low Bits	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0
	1	Blue / White Low Bits	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0
	1	Red_x	Red_x bits 9 → 2
	1	Red_y	Red_y bits 9 → 2
	1	Green_x	Green_x bits 9 → 2
	1	Green_y	Green_y bits 9 → 2
	1	Blue_x	Blue_x bits 9 → 2
	1	Blue_y	Blue_y bits 9 → 2
	1	White_x	White_x bits 9 → 2
	1	White_y	White_y bits 9 → 2

Table 4.21 - Chromaticity & Default White Point Coordinates

10	Bytes	Description	Format
	10	Color Point	Note : Chromaticity data to be coded as in Table 4.19 Note : Gamma data to be coded as in Table 4.17 Byte 1 : White point index number (binary) Byte 2 : White low bits Byte 3 : White_x Byte 4 : White_y Byte 5 : White Gamma Byte 6 : White point index number (binary) Byte 7 : White low bits Byte 8 : White_x Byte 9 : White_y Byte 10 : White Gamma

Table 4.22 - Additional White Points And Gamma

4.3.5 Display Spatial Description

Three sets of parameters are used to describe the spatial characteristics of the display. These are maximum image size, maximum addressibility and dot/pixel pitch. The size and order of the fields is shown in Table 4.23

10	Bytes	Display Spatial Description
	4	Max. Image Size
	4	Max. addressibility
	2	Dot/pixel pitch

Table 4.23 - Display Spatial Description

The maximum image size parameters, shown in Table 4.24, provide information on the maximum image dimensions that can be correctly displayed, as defined by VESA Video Image Area Definition (VIAD) standard, rounded to the nearest millimeter (mm). These values are intended to be the maximum image size that can be properly displayed over the entire set of supported timing / format combinations. The host system is expected to use this data to get a rough idea of the image size and aspect ratio to allow properly scaled text to be selected.

If either or both bytes are set to zero then the system shall make no assumptions regarding the display size.

e.g. A projection display may be of indeterminate size.

4	Bytes	Description	Format
	2	Maximum Horizontal Image Size	From 1 → 65535 mm See above for special case = 0
	2	Maximum Vertical Image size	From 1 → 65535 mm See above for special case = 0

Table 4.24 - Maximum Image Size

Maximum addressibilty, shown in Table 4.25, is expressed in units of pixels for both the horizontal and vertical directions.

4	Bytes	Description	Format
	2	Max. Horizontal Addressibility	From 1 → 65535 pixels
	2	Max. Vertical Addressibilty	From 1 → 65535 pixels

Table 4.25 - Maximum Addressibility

The dot/pixel pitch, shown in Table 4.26, is given in horizontal and vertical components. The value stored in EDID is equal to the actual pitch value multiplied by one hundred. For example, A dot pitch of .31mm would be represented in EDID by the value 31

2	Bytes	Description	Format
	1	Horiz pixel pitch	in mm * 100
	1	Vert. pixel pitch	in mm * 100

Table 4.26 - Dot/Pixel Pitch

The pitch specified in these bytes is that of the visible screen structure, i.e. the phosphor or filter dot pitch, as opposed to the shadow mask pitch or other such measurement. Display devices which use continuous 'stripes' or similar phosphor or filter patterns should indicate this by setting the appropriate byte to zero; for example, the typical aperture-grille tube would specify a vertical pitch of zero in this section. Displays which do not use a discrete dot structure in their screens, such as a monochrome CRT, should set both bytes to zero.

4.3.6 GTF support

This field indicates support of up to 2 sets of GTF parameters by the monitor. The default GTF mode is indicated in the upper nibble. The lower nibble indicates support for additional GTF parameters sets.

Note: GTF support also requires inclusion of range limit parameters (see Sections 4.4.1 & 4.4.2)

Bit	Description	Detailed Description
7-4	GTF parameter set supported	0 = no GTF support 1 = Standard CRT parameters 2 = Default “reduced blanking” parameters (TBD) 3-E = Reserved F = Custom parameters (requires monitor command set)
3-0	2nd GTF parameter set support	Same as above

Table 4.27 - GTF Support

4.3.7 Number of timing codes/detailed timings

This section describes the usage of the 127 bytes of the EDID data beginning at offset 80h to offset FEh (Offset FFH is reserved for the checksum). This area can be used for any combination of the 5 data types listed below. The ordering of the data will be gamma table followed by frequency ranges followed by detailed range limits followed by timing codes followed by detailed timings. Any remaining bytes should be set to 00h.

Total space used for timing parameters cannot exceed 127 bytes. The number of bytes used can be calculated using the following formula:

*x**A + 8*B + 27*C + 4*D + 18*E
where: A = number of luminance tables listed (0 or 1)
x = size of luminance table (see section 4.4)
B = number of frequency ranges listed (0-7)
C = number of detailed range limits (0-3)
D = number of timing codes (0-31)
E = number of detailed timings (0-7)

2	Byte	Bit	Description	
	1	7	Extension Flag	If set to 1 a 2nd EDID structure follows this one.
		6	Preferred Timing Mode	If set to 1 the display's preferred timing mode is indicated in the first detailed timing listed
		5	Luminance Table provided	If set to 1 the display provides a luminance table which is x bytes in length.. This table if provided immediately follows this descriptor. (offset 80h). The size of the table, x, is the first entry in this table.
		4-2	Number of frequency ranges listed	up to 7 Range limits can be listed for the monitor. If GTF is supported at least one range limit must be listed. These range limit descriptors immediately follow the gamma table.
		1-0	Number of Detailed Range Limits Listed	up to 3 Detailed Range limits can be listed. It is intended that these will be used by displays that restrict the range of timing parameters which cannot be described. This data immediately follows any frequency range data.
	1	7-3	Number of 4-byte timing codes listed	up to 31 timing codes can be listed. These immediately follow any detailed range limit data
		2-0	Number of detailed timing descriptions	up to 7 detailed timing descriptions can be listed. These immediately follow any timing code data Unused bytes between the last detailed timing and the checksum byte are set to 00h.

Table 4.28 - Number and Type of Timing Codings

4.4 Luminance Table

A luminance table must be used to provide information for the display output characteristic in the case where the display does not follow the CIE gamma model shown in Section 4.3.4. The table contains values based on luminance measured at equally spaced points from minimum to maximum luminance of the display. This may be a single set of values based on the combined color sub-channels (white) or it may be three sets of values (one for each color sub-channel). Accurate representation of the output characteristic requires at least sixteen measured values for each set. Thirty-two values are recommended. The measurements are normalized to one-byte values such that the value at maximum luminance is always FFh. Since this maximum value is constant, it is not recorded in the table.

The size of the table, *x*, is either *n*+1 if white values are specified or 3*n*+1 if separate sub-channels are specified.
where: *n* = number of values recorded per set.

x	Bytes	Bit	Description	Format
	1	7	Combined or separate sub-channels	0= table contains *n* luminance values for white 1 = table contains 3**n* total luminance values: n with for sub channel 0, followed by *n* luminance values for sub channel 1 followed by *n* luminance values for sub-channel 2.
		6-5	Reserved	Set to 0
		4-0	Number of luminance entries	*n* = the number of luminance values recorded in the table. This value is one less than the number of measurement actually taken since the maximum value is always normalized to FFh and is not recorded in the table. If the table has entries for each of the color sub-channels, *n* represents the number of entries for each sub channel.
	1	7-0	1st luminance value	normalized such that the $(n + 1)^{th}$ value is always FFh.
	1	7-0	2nd luminance value	
	1		.	
	1		.	
	1		.	
	1	7-0	nth luminance value	normalized such that the $(n + 1)^{th}$ value is always FFh.
	1	7-0	1st luminance value sub-channel 1 (if used)	normalized such that the $(n + 1)^{th}$ value is always FFh.
	1		.	
	1		.	
	1		.	
	1	7-0	nth luminance value sub-channel 1 (if used)	normalized such that the $(n + 1)^{th}$ value is always FFh.
	1	7-0	1st luminance value sub-channel 2 (if used)	normalized such that the $(n + 1)^{th}$ value is always FFh.
	1		.	
	1		.	
	1		.	
	1	7-0	nth luminance value sub-channel 2 (if used)	normalized such that the $(n + 1)^{th}$ value is always FFh.

Table 4.29 - Luminance Table

4.5 Timing Descriptions

This timing description block is designed to allow a flexible mix of standard (timing codes) and non-standard (detailed timings) timing descriptions. Near the front of the block is an indicator of how many timings of each type will follow.

4.5.1 Display timing range limits

The display timing range descriptor provides minimum and maximum values frame/field rate, line rate and pixel rates. The frame and field rates range from 0 to 1024 and are stored as 10-bit values which are organized across bytes as indicated in Table 4.30. Pixel rates range from 0 to 255. For fixed frequency displays these fields are set to 0.

8	Bytes	Bit	Description	Format
	1	7-0	Min. Frame/field rate in Hz	bits 9-2
	1	7-0	Max. frame/field rate in Hz	bits 9-2
	1	7-0	Min. line rate in kHz	bits 9-2
	1	7-0	Max. line rate in kHz	bits 9-2
	1	7-0	Lower bits frame/field & line rates	Min_field 1-0, Max_field 1-0, Min_line 1-0, Max_line 1-0
	1	7-0	Min. pixel rate in MHz	bits 7-0
	1	7-0	Max. pixel rate in MHz	bits 7-0
	1	7-4	Upper bits min pixel rate	Min_pixel 11-8
		3-0	Upper bits max pixel rate	Max_pixel 11-8

Table 4.30 - Range Limits Descriptor

Note: The pixel rate parameters represent true pixel rates and are not necessarily equivalent to the shift clock. In cases where two pixels are transmitted during a single shift clock cycle, the pixel rate is twice the shift clock rate. The number of pixels per shift clock is determined by the data format as shown in tables 6.1 and 6.2.

4.5.2 27-byte detailed timing range format

For displays based on CRT technology, the minimum and maximum dot clock, line rate, and refresh rate parameters provided for in the previous 64-byte section are likely to be sufficient. This timing parameter range block is provided for displays based on other technologies in which greater variations in design exist, or a more complete specification is required.

Parameters for which there isn't a range, but a single fixed value, should simply provide the same value for both the minimum and maximum.

Horizontal timing parameters shown are in units of pixels. Tables 6.1 and 6.2 show the relationship between shift clock and pixels for digital data formats.

27	Bytes	Detailed Timing Descriptions	Format
	2	Min Pixel clock / 10,000	Stored LSB first Example : 135 MHz would be 13500 decimal, stored as BCh,34h
	1	Min Horizontal Blanking	Pixels, lower 8 bits
	1	Min Vertical Blanking	Lines, lower 8 bits
	1	Min Horizontal Blanking : Min Vertical Blanking	Upper nibble : upper 4 bits of Horizontal Blanking Lower nibble : upper 4 bits of Vertical Blanking
	1	Min Horizontal Sync. Offset	Pixels , from blanking starts, lower 8 bits
	1	Min Horizontal Sync Pulse Width	Pixels, lower 8 bits
	1	Min Vertical Sync Offset : Min V Sync Pulse Width	Upper nibble : lines, lower 4 bits of Vertical Sync Offset Lower nibble : lines, lower 4 bits of Vertical Sync Pulse Width
	1	Min Horizontal Sync Offset Min Horizontal Sync Pulse Width Min Vertical Sync Offset Min Vertical Sync Pulse Width	bits 7,6 : upper 2 bits of Horizontal Sync Offset bits 5,4 : upper 2 bits of Horizontal Sync Pulse Width bits 2,3 : upper 2 bits of Vertical Sync Offset bits 0,1 : upper 2 bits of Vertical Sync Pulse Width
	2	Max Pixel clock / 10,000	Stored LSB first Example : 135 MHz would be 13500 decimal, stored as BCh,34h
	1	Max Horizontal Blanking	Pixels, lower 8 bits
	1	Max Vertical Blanking	Lines, lower 8 bits
	1	Max Horizontal Blanking : Max Vertical Blanking	Upper nibble : upper 4 bits of Vertical Active Lower nibble : upper 4 bits of Vertical Blanking
	1	Max Horizontal Sync. Offset	Pixels , from blanking starts, lower 8 bits
	1	Max Horizontal Sync Pulse Width	Pixels, lower 8 bits
	1	Max Vertical Sync Offset : Max Vertical Sync Pulse Width	Upper nibble : lines, lower 4 bits of Vertical Sync Offset Lower nibble : lines, lower 4 bits of Vertical Sync Pulse Width
	1	Max Horizontal Sync Offset Max Horizontal Sync Pulse Width Max Vertical Sync Offset Max Vertical Sync Pulse Width	bits 7,6 : upper 2 bits of Horizontal Sync Offset bits 5,4 : upper 2 bits of Horizontal Sync Pulse Width bits 2,3 : upper 2 bits of Vertical Sync Offset bits 0,1 : upper 2 bits of Vertical Sync Pulse Width
	1	Horizontal Image Size	mm, lower 8 bits
	1	Vertical Image Size	mm, lower 8 bits
	1	Horizontal & Vertical Image Size	Upper nibble : upper 4 bits of Horizontal Image Size Lower nibble : upper 4 bits of Vertical Image Size
	1	Horizontal Active	Pixels, lower 8 bits
	1	Vertical Active	Lines, lower 8 bits
	1	Horizontal Active : Vertical Active	Upper nibble : upper 4 bits of Horizontal Active Lower nibble : upper 4 bits of Vertical Active

27	Bytes	Detailed Timing Descriptions	Format
	1	Horizontal Border	Pixels, see Section 3.11
	1	Vertical Border	Lines, see Section 3.11
	1	Flags: Interlace, Horizontal & Vertical polarities, Sync Configuration, etc.	Bit 7 Function 0 Non-interlaced 1 Interlaced Bits 6 - 5 Set = 0 (See Note-1) Bits 4 - 1 Defined in Tables 4.33 & 4.34 Bit 0 Set = 0 (See Note-1) Note-1: Stereo display support listed in feature support (Table 4.16)

Table 4.31 - Detailed Range Limits Descriptor

4.5.3 4-byte timing code format

These codes describe timings that have been documented by VESA and therefore do not require full details. Their uniqueness from other standard timings can be determined by the parameters provided.

4	Byte	Bit	Description	
	1	-	Active pixels per line	(# of pixels - 256)/16 [range 256-4336]
	1	7	reduced blanking	set = 1 if reduced blanking timing
		6	Interlaced timing	set = 1 if interlaced timing (byte 4 is field rate)
		5	Stereo	set = 1 if field sequential stereo timing
		4	Portrait	set = 1 if timing is portrait mode
		3	LP Polarity	LP -equivalent of HS for flat panels 0 = LP is active low 1 = LP is active high
		2	FLM Polarity	FLM -equivalent of VS for flat panels 0 = FLM is active low 1 = FLM is active high
		1	SHFTCLK edges used	0 = data transferred on a single edge of the SHFTCLK indicated in interface data format (see Table 4.11) 1= data is transferred on both edges of the SHFTCLK
		0	Reserved	set to 0
	1	-	Format aspect ratio (H:V)	given as N:100 example: 4:3 is indicated as 133:100 16:9 is indicated as 178:100
	1	-	Refresh rate	in Hz Note 59 is reserved for 59.94 Hz (NTSC)

Table 4.32 - Timing Code Format

4.5.4 18-byte detailed timing format

Note: EDID data structure Version 2 does not support alternate uses of detailed timing blocks.

Horizontal timing parameters shown are in units of pixels. Tables 6.1 and 6.2 show the relationship between shift clock and pixels for digital data formats.

18	Bytes	Detailed Timing Descriptions	Format
	2	Pixel clock / 10,000	Stored LSB first Example : 135 MHz would be 13500 decimal, stored as BCh,34h
	1	Horizontal Active	Pixels, lower 8 bits
	1	Horizontal Blanking	Pixels, lower 8 bits
	1	Horizontal Active : Horizontal Blanking	Upper nibble : upper 4 bits of Horizontal Active Lower nibble : upper 4 bits of Horizontal Blanking
	1	Vertical Active	Lines, lower 8 bits
	1	Vertical Blanking	Lines, lower 8 bits
	1	Vertical Active : Vertical Blanking	Upper nibble : upper 4 bits of Vertical Active Lower nibble : upper 4 bits of Vertical Blanking
	1	Horizontal Sync. Offset	Pixels , from blanking starts, lower 8 bits
	1	Horizontal Sync Pulse Width	Pixels, lower 8 bits
	1	Vertical Sync Offset : Vertical Sync Pulse Width	Upper nibble : lines, lower 4 bits of Vertical Sync Offset Lower nibble : lines, lower 4 bits of Vertical Sync Pulse Width
	1	Horizontal Sync Offset Horizontal Sync Pulse Width Vertical Sync Offset Vertical Sync Pulse Width	bits 7,6 : upper 2 bits of Horizontal Sync Offset bits 5,4 : upper 2 bits of Horizontal Sync Pulse Width bits 2,3 : upper 2 bits of Vertical Sync Offset bits 0,1 : upper 2 bits of Vertical Sync Pulse Width
	1	Horizontal Image Size	mm, lower 8 bits
	1	Vertical Image Size	mm, lower 8 bits
	1	Horizontal & Vertical Image Size	Upper nibble : upper 4 bits of Horizontal Image Size Lower nibble : upper 4 bits of Vertical Image Size
	1	Horizontal Border	Pixels, see Section 3.11
	1	Vertical Border	Lines, see Section 3.11
	1	Flags	Interlace, Horizontal polarity, Vertical polarity, Sync Configuration, etc. Bit 7 Function 0 Non-interlaced 1 Interlaced Bits 6 - 5 Set = 0 Note: Stereo display support listed in feature support (Table 4.16) Bits 4 - 1 Defined in Tables 4.33 & 4.34 Bit 0 Set = 0 Note: Stereo display support listed in feature support (Table 4.16)

Table 4.33 - Detailed Timing Description

4.5.4.1 Expansion of Detailed Timing Descriptor Flag Byte bits 4-1

Analog Interface

Bits 4 and 3	Bit 2	Bit 2 Defn.	Bit 1	Bit 1 Defn.
0,0 Analog Composite	Serrate	If set, controller shall supply serration (Hsync during Vsync).	On RGB	If set, sync pulses should appear on all 3 video signal lines. If not set, sync on green video line only.
0,1 Bipolar Analog Composite	Serrate	If set, controller shall supply serration (Hsync during Vsync).	On RGB	If set, sync pulses should appear on all 3 video signal lines. If not set, sync on green video line only.
1,0 Digital Composite	Serrate	If set, controller shall supply serration (Hsync during Vsync).	Composite Polarity	Composite sync polarity is the polarity of the Hsync pulses outside of Vsync.
1,1 Digital Separate	Vertical Polarity	Vsync signal Polarity is Positive if bit is set to 1.	Horizontal Polarity	Hsync signal polarity is Positive if bit is set to 1.

Table 4.34 - Detailed Timing Flag 'sync' Bits for Analog Interfaces

For Digital Interface

Bit	Description	Detailed description
4	Shift clock use	If set, data is transferred on both edges of shift clock.. Otherwise data is shift on edge specified in Digital interface byte.
3	Reserved	If set, controller shall supply serration (Hsync during Vsync).
2	FLM Polarity	If set, FLM is active when high
1	LP Polarity	If set, LP is active when high

Table 4.35 - Detailed Timing Flag 'sync' Bits for Digital Interfaces

4.6 Checksum

Bytes	Description	Function
1	Checksum	This byte should be programmed such that a one-byte checksum of the entire 256-byte EDID equals 00h.

Table 4.36 - Checksum

5. Compliance with this Standard

Compliance with the VESA EDID Standard requires that all the requirements of Sections 1 to 2 inclusive and either Section 3 or Section 4 are met.

5.1 Existing Monitor Designs

Existing Monitor designs capable of supplying EDID data will generally comply with the EDID Structure Version 1 data formats defined by the EDID Standard Version 2.0, Revisions 0 only and not support the new features added in later versions of the EDID Standard.

5.2 New Monitor Designs

New monitor designs capable of supplying EDID data may contain EDID data in a format valid for the particular display.

Monitors designed to conform to the VESA Plug and Display Standard Version 1.0 require EDID structure version 2 as defined in Section 4. These monitors may also contain a second EDID structure if the monitor is also compatible with non-P&D systems.

Displays designed to conform with the VESA FPDI-2 standard (currently in proposal state) are recommended to use EDID data structure version 2 as defined in Section 4 of this document.

The software used to decode the EDID data shall use the EDID Structure Version and Revision levels to determine the appropriate decode.

5.3 Existing Host Systems

Existing host system designs claiming compliance with DDC Standard Version 1 Revision 0 will only be able to decode the features of EDID Structure Version 1 Revision 0 but should be able to tolerate the, potentially, different structure of EDID Structure Version 1 Revisions 1 and 2.

Existing host systems claiming compliance with VESA DDC Standard Version 2 Revision 0 shall be able to decode features of EDID Structure Version 1 Revisions 0 and 1. They should also be able to tolerate the potentially different structure of EDID Structure Version 1 Revision 2.

5.4 New host Systems

New host system designs claiming compliance with VESA DDC Version 3 Revision 0 (or later) shall be able to decode the features of EDID Structure Version 1 Revisions 0 - 2 and EDID Structure Version 2 Revision 0 as determined by examination of the EDID Structure version and revision number fields.

6. APPENDIX A - Digital Data Formats

This appendix document the details of the digital data formats referenced in Table 4.11.

6.1 Pixel Data Mapping Codes

Single scan STN data formats are assigned codes 00h-04h. Dual scan STN use codes 10h-19h. TFT modes have codes in the range 20h-38h. Codes 40h-42h are assigned to formats using YCrCb data encodings.

6.2 Summary Tables

Tables 6.1 and 6.2 summarize the pixel mappings for codes digital interface codes 00h-38h

Digital Interface Code #	00h	01h	04h	10h	11h	14h	15h	19h
Bit Number	8-Bit Mono STN-SS	8-Bit RGB STN-SS	16-Bit RGB STN-SS	4-Bit Over 4-Bit Mono STN-DD	4-Bit Over 4-Bit RGB STN-DD	8-Bit Over 8-Bit Mono STN-DD	8-Bit Over 8-Bit RGB STN-DD	12-Bit Over 12-Bit RGB STN-DD
0	P0	R0	R0	UD3	UR0	UD7	UR0	UR0
1	P1	G0	G0	UD2	UG0	UD6	UG0	UG0
2	P2	G1	B0	UD1	UB0	UD5	UB0	UB0
3	P3	R2	R1	UD0	UR1	UD4	UR1	LR0
4	P4	B2	G1	LD3	LR0	UD3	LR0	LG0
5	P5	G3	B1	LD2	LG0	UD2	LG0	LB0
6	P6	R4	R2	LD1	LB0	UD1	LB0	UR1
7	P7	B4	G2	LD0	LR1	UD0	LR1	UG1
8	–	–	B2	–	–	LD7	UG1	UB1
9	–	–	R3	–	–	LD6	UB1	LR1
10	–	–	G3	–	–	LD5	UR2	LG1
11	–	–	B3	–	–	LD4	UG2	LB1
12	–	–	R4	–	–	LD3	LG1	UR2
13	–	–	G4	–	–	LD2	LB1	UG2
14	–	–	B4	–	–	LD1	LR2	UB2
15	–	–	R5	–	–	LD0	LG2	LR2
16	–	SHFCLK*	SHFCLK*	–	SHFCLK*	–	SHFCLK*	LG2
17	–	–	–	–	–	–	–	LB2
18	–	–	–	–	–	–	–	UR3
19	–	–	–	–	–	–	–	UG3
20	–	–	–	–	–	–	–	UB3
21	–	–	–	–	–	–	–	LR3
22	–	–	–	–	–	–	–	LG3
23	–	–	–	–	–	–	–	LB3
Pixels per SHFCLK	8	8/3	16/3	8	8/3	16	16/3	8
Min Req'd for P&D & FPDI-2							Yes	Yes

Table 6.1 - Summary of STN Data Formats

*Needed only if TMDS interface is being used.

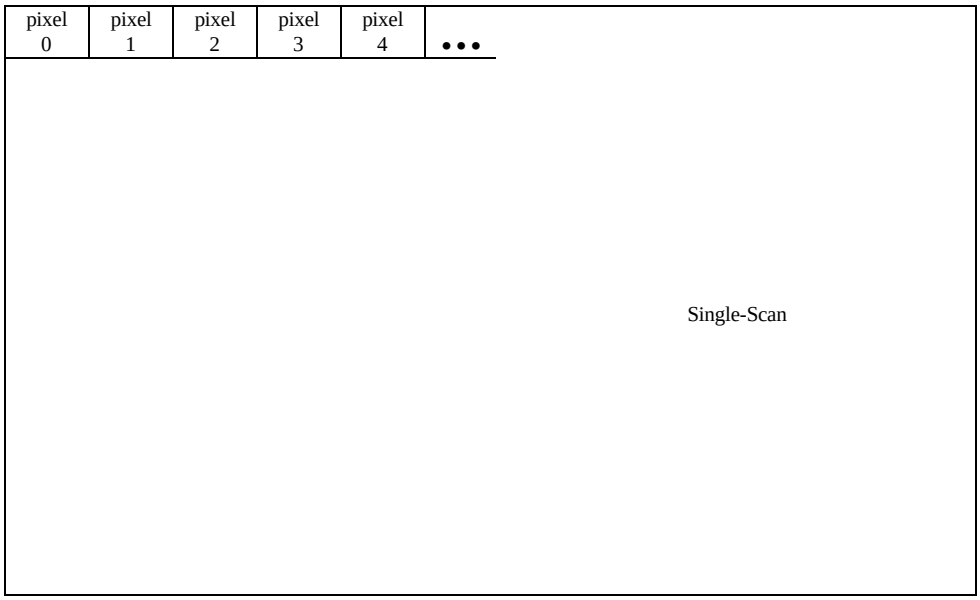
Note: EDID specifies horizontal timing parameters in units of pixels. The relationship between pixels and SHFCLK is determined by the data format as shown here.

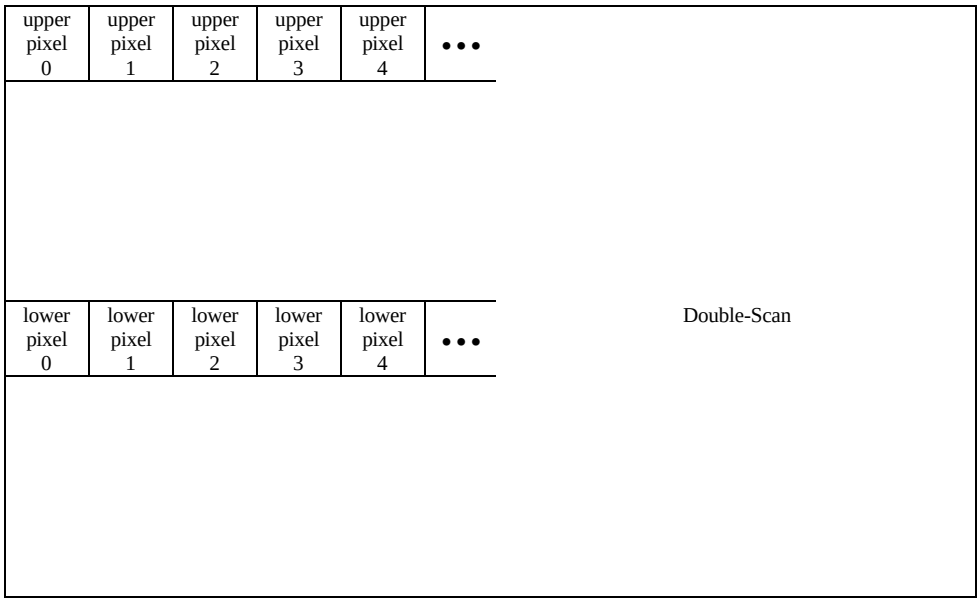
Digital Interface Code #	20h			24h			25h			30h		34h		38h		
Bit Number	Pseudo 18-Bit RGB TFT			24-Bit MSB-Aligned RGB TFT			24-Bit LSB-Aligned RGB TFT			Double 12-Bit RGB TFT		Double 18-Bit RGB TFT		Double 24-Bit RGB TFT		
0	B1	–	–	B0	–	–	B0	B0	B0	FB0	–	FB0	–	FB0	–	–
1	B2	B0	–	B1	–	–	B1	B1	B1	FB1	FB0	FB1	–	FB1	–	–
2	B3	B1	B0	B2	B0	–	B2	B2	B2	FB2	FB1	FB2	FB0	FB2	FB0	–
3	B4	B2	B1	B3	B1	–	B3	B3	B3	FB3	FB2	FB3	FB1	FB3	FB1	–
4	B5	B3	B2	B4	B2	B0	B4	B4	–	SB0	–	FB4	FB2	FB4	FB2	FB0
5	G0	–	–	B5	B3	B1	B5	B5	–	SB1	SB0	FB5	FB3	FB5	FB3	FB1
6	G1	–	–	B6	B4	B2	B6	–	–	SB2	SB1	SB0	–	FB6	FB4	FB2
7	G2	G0	–	B7	B5	B3	B7	–	–	SB3	SB2	SB1	–	FB7	FB5	FB3
8	G3	G1	G0	G0	–	–	G0	G0	G0	FG0	–	SB2	SB0	SB0	–	–
9	G4	G2	G1	G1	–	–	G1	G1	G1	FG1	FG0	SB3	SB1	SB1	–	–
10	G5	G3	G2	G2	G0	–	G2	G2	G2	FG2	FG1	SB4	SB2	SB2	SB0	–
11	R1	–	–	G3	G1	–	G3	G3	G3	FG3	FG2	SB5	SB3	SB3	SB1	–
12	R2	R0	–	G4	G2	G0	G4	G4	–	SG0	–	FG0	–	SB4	SB2	SB0
13	R3	R1	R0	G5	G3	G1	G5	G5	–	SG1	SG0	FG1	–	SB5	SB3	SB1
14	R4	R2	R1	G6	G4	G2	G6	–	–	SG2	SG1	FG2	FG0	SB6	SB4	SB2
15	R5	R3	R2	G7	G5	G3	G7	–	–	SG3	SG2	FG3	FG1	SB7	SB5	SB3
16	–	–	–	R0	–	–	R0	R0	R0	FR0	–	FG4	FG2	FG0	–	–
17	–	–	–	R1	–	–	R1	R1	R1	FR1	FR0	FG5	FG3	FG1	–	–
18	–	–	–	R2	R0	–	R2	R2	R2	FR2	FR1	SG0	–	FG2	FG0	–
19	–	–	–	R3	R1	–	R3	R3	R3	FR3	FR2	SG1	–	FG3	FG1	–
20	–	–	–	R4	R2	R0	R4	R4	–	SR0	–	SG2	SG0	FG4	FG2	FG0
21	–	–	–	R5	R3	R1	R5	R5	–	SR1	SR0	SG3	SG1	FG5	FG3	FG1
22	–	–	–	R6	R4	R2	R6	–	–	SR2	SR1	SG4	SG2	FG6	FG4	FG2
23	–	–	–	R7	R5	R3	R7	–	–	SR3	SR2	SG5	SG3	FG7	FG5	FG3
24	–	–	–	–	–	–	–	–	–	–	–	FR0	–	SG0	–	–
25	–	–	–	–	–	–	–	–	–	–	–	FR1	–	SG1	–	–
26	–	–	–	–	–	–	–	–	–	–	–	FR2	FR0	SG2	SG0	–
27	–	–	–	–	–	–	–	–	–	–	–	FR3	FR1	SG3	SG1	–
28	–	–	–	–	–	–	–	–	–	–	–	FR4	FR2	SG4	SG2	SG0
29	–	–	–	–	–	–	–	–	–	–	–	FR5	FR3	SG5	SG3	SG1
30	–	–	–	–	–	–	–	–	–	–	–	SR0	–	SG6	SG4	SG2
31	–	–	–	–	–	–	–	–	–	–	–	SR1	–	SG7	SG5	SG3
32	–	–	–	–	–	–	–	–	–	–	–	SR2	SR0	FR0	–	–
33	–	–	–	–	–	–	–	–	–	–	–	SR3	SR1	FR1	–	–
34	–	–	–	–	–	–	–	–	–	–	–	SR4	SR2	FR2	FR0	–
35	–	–	–	–	–	–	–	–	–	–	–	SR5	SR3	FR3	FR1	–
36	–	–	–	–	–	–	–	–	–	–	–	–	–	FR4	FR2	FR0
37	–	–	–	–	–	–	–	–	–	–	–	–	–	FR5	FR3	FR1
38	–	–	–	–	–	–	–	–	–	–	–	–	–	FR6	FR4	FR2
39	–	–	–	–	–	–	–	–	–	–	–	–	–	FR7	FR5	FR3
40	–	–	–	–	–	–	–	–	–	–	–	–	–	SR0	–	–
41	–	–	–	–	–	–	–	–	–	–	–	–	–	SR1	–	–
42	–	–	–	–	–	–	–	–	–	–	–	–	–	SR2	SR0	–
43	–	–	–	–	–	–	–	–	–	–	–	–	–	SR3	SR1	–
44	–	–	–	–	–	–	–	–	–	–	–	–	–	SR4	SR2	SR0
45	–	–	–	–	–	–	–	–	–	–	–	–	–	SR5	SR3	SR1
46	–	–	–	–	–	–	–	–	–	–	–	–	–	SR6	SR4	SR2
47	–	–	–	–	–	–	–	–	–	–	–	–	–	SR7	SR5	SR3
Pixels per SHFCLK	1			1			1			2		2		2		
Min Req'd for P&D & FPDI-2				Yes												

Table 6.2 - Summary of TFT Data Formats

6.3 Single-Scan Versus Double-Scan

LCD single-scan (SS) displays are operated very much like CRT displays in that the image is drawn one pixel at a time, starting with the first pixel on one end of the first scan line, and then proceeding through adjacent scan lines from one edge of the display to the other. By contrast, double-scan (DS) displays are operated very much like a pair of single-scan displays that are glued, one above the other, and are written to simultaneously. The differences between the two are illustrated below:





6.4 Data format details

Digital data formats allow a group of a pixel or group of pixels to be addressed at each transfer. Due to differing color depths and other factors, bit assignments may differ from transfer to transfer in a periodic fashion. The tables in this section show several transfers for each encoding to show the pattern of bit assignments.

6.4.1 8-Bit Monochrome STN-SS - Code 00h

Bus Signal	1st Transfer	2nd Transfer	

Bit 0	pixel 0	pixel 8	...
Bit 1	pixel 1	pixel 9	...
Bit 2	pixel 2	pixel 10	...
Bit 3	pixel 3	pixel 11	...
Bit 4	pixel 4	pixel 12	...
Bit 5	pixel 5	pixel 13	...
Bit 6	pixel 6	pixel 14	...
Bit 7	pixel 7	pixel 15	...
Bit 8			
Bit 9			
Bit 10			
Bit 11			
Bit 12			
Bit 13			
Bit 14			
Bit 15			
Bit 16			
Bit 17			
Bit 18			
Bit 19			
Bit 20			
Bit 21			
Bit 22			
Bit 23			

Table 6.3 - Digital Format 00h

6.4.2 8-Bit Color STN-SS - Code 01h

Bus Signal	1st Transfer	2nd Transfer	3rd Transfer	4th Transfer	5th Transfer	6th Transfer	
Bit 0	pixel 0 red	pixel 0 green	pixel 5 green	pixel 5 blue	pixel 10 blue	pixel 11 red	...
Bit 1	pixel 0 blue	pixel 1 red	pixel 6 red	pixel 6 green	pixel 11 green	pixel 11 blue	...
Bit 2	pixel 1 green	pixel 1 blue	pixel 6 blue	pixel 7 red	pixel 12 red	pixel 12 green	...
Bit 3	pixel 2 red	pixel 2 green	pixel 7 green	pixel 7 blue	pixel 12 blue	pixel 13 red	...
Bit 4	pixel 2 blue	pixel 3 red	pixel 8 red	pixel 8 green	pixel 13 green	pixel 13 blue	...
Bit 5	pixel 3 green	pixel 3 blue	pixel 8 blue	pixel 9 red	pixel 14 red	pixel 14 green	...
Bit 6	pixel 4 red	pixel 4 green	pixel 9 green	pixel 9 blue	pixel 14 blue	pixel 15 red	...
Bit 7	pixel 4 blue	pixel 5 red	pixel 10 red	pixel 10 green	pixel 15 green	pixel 15 blue	...
Bit 8							
Bit 9							
Bit 10							
Bit 11							
Bit 12							
Bit 13							
Bit 14							
Bit 15							
Bit 16	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	...
Bit 17							
Bit 18							
Bit 19							
Bit 20							
Bit 21							
Bit 22							
Bit 23							

Table 6.4 - Digital Format 01h

6.4.3 16-Bit Color STN-SS - Code 04h

Bus Signal	1st Transfer	2nd Transfer	3rd Transfer	
Bit 0	pixel 0 red	pixel 5 green	pixel 10 blue	...
Bit 1	pixel 0 green	pixel 5 blue	pixel 11 red	...
Bit 2	pixel 0 blue	pixel 6 red	pixel 11 green	...
Bit 3	pixel 1 red	pixel 6 green	pixel 11 blue	...
Bit 4	pixel 1 green	pixel 6 blue	pixel 12 red	...
Bit 5	pixel 1 blue	pixel 7 red	pixel 12 green	...
Bit 6	pixel 2 red	pixel 7 green	pixel 12 blue	...
Bit 7	pixel 2 green	pixel 7 blue	pixel 13 red	...
Bit 8	pixel 2 blue	pixel 8 red	pixel 13 green	...
Bit 9	pixel 3 red	pixel 8 green	pixel 13 blue	...
Bit 10	pixel 3 green	pixel 8 blue	pixel 14 red	...
Bit 11	pixel 3 blue	pixel 9 red	pixel 14 green	...
Bit 12	pixel 4 red	pixel 9 green	pixel 14 blue	...
Bit 13	pixel 4 green	pixel 9 blue	pixel 15 red	...
Bit 14	pixel 4 blue	pixel 10 red	pixel 15 green	...
Bit 15	pixel 5 red	pixel 10 green	pixel 15 blue	...
Bit 16	SHFCLK	SHFCLK	SHFCLK	...
Bit 17				
Bit 18				
Bit 19				
Bit 20				
Bit 21				
Bit 22				
Bit 23				

Table 6.5 - Digital Format 04h

6.4.4 4-Bit Over 4-Bit Monochrome STN-DD - Code 10h

Bus Signal	1st Transfer	2nd Transfer	
Bit 0	upper pixel 3	upper pixel 7	...
Bit 1	upper pixel 2	upper pixel 6	...
Bit 2	upper pixel 1	upper pixel 5	...
Bit 3	upper pixel 0	upper pixel 4	...
Bit 4	lower pixel 3	lower pixel 7	...
Bit 5	lower pixel 2	lower pixel 6	...
Bit 6	lower pixel 1	lower pixel 5	...
Bit 7	lower pixel 0	lower pixel 4	...
Bit 8			
Bit 9			
Bit 10			
Bit 11			
Bit 12			
Bit 13			
Bit 14			
Bit 15			
Bit 16			
Bit 17			
Bit 18			
Bit 19			
Bit 20			
Bit 21			
Bit 22			
Bit 23			

Table 6.6 - Digital Format 10h

6.4.5 4-Bit Over 4-Bit RGB STN-DD - Code 11h

Bus Signal	1st Transfer	2nd Transfer	3rd Transfer	
Bit 0	upper pixel 0 red	upper pixel 1 green	upper pixel 2 blue	...
Bit 1	upper pixel 0 green	upper pixel 1 blue	upper pixel 3 red	...
Bit 2	upper pixel 0 blue	upper pixel 2 red	upper pixel 3 green	...
Bit 3	upper pixel 1 red	upper pixel 2 green	upper pixel 3 blue	...
Bit 4	lower pixel 0 red	lower pixel 1 green	lower pixel 2 blue	...
Bit 5	lower pixel 0 green	lower pixel 1 blue	lower pixel 3 red	...
Bit 6	lower pixel 0 blue	lower pixel 2 red	lower pixel 3 green	...
Bit 7	lower pixel 1 red	lower pixel 2 green	lower pixel 3 blue	...
Bit 8				
Bit 9				
Bit 10				
Bit 11				
Bit 12				
Bit 13				
Bit 14				
Bit 15				
Bit 16	SHFCLK	SHFCLK	SHFCLK	...
Bit 17				
Bit 18				
Bit 19				
Bit 20				
Bit 21				
Bit 22				
Bit 23				

Table 6.7 - Digital Format 11h

6.4.6 8-Bit Over 8-Bit Monochrome STN-DD - Code 14h

Bus Signal	1st Transfer	2nd Transfer	
Bit 0	upper pixel 7	upper pixel 15	...
Bit 1	upper pixel 6	upper pixel 14	...
Bit 2	upper pixel 5	upper pixel 13	...
Bit 3	upper pixel 4	upper pixel 12	...
Bit 4	upper pixel 3	upper pixel 11	...
Bit 5	upper pixel 2	upper pixel 10	...
Bit 6	upper pixel 1	upper pixel 9	...
Bit 7	upper pixel 0	upper pixel 8	...
Bit 8	lower pixel 7	lower pixel 15	...
Bit 9	lower pixel 6	lower pixel 14	...
Bit 10	lower pixel 5	lower pixel 13	...
Bit 11	lower pixel 4	lower pixel 12	...
Bit 12	lower pixel 3	lower pixel 11	...
Bit 13	lower pixel 2	lower pixel 10	...
Bit 14	lower pixel 1	lower pixel 9	...
Bit 15	lower pixel 0	lower pixel 8	...
Bit 16			
Bit 17			
Bit 18			
Bit 19			
Bit 20			
Bit 21			
Bit 22			
Bit 23			

Table 6.8 - Digital Format 14h

6.4.7 8-Bit Over 8-Bit RGB STN-DD - Code 15h

Bus Signal	1st Transfer	2nd Transfer	3rd Transfer	
Bit 0	upper pixel 0 red	upper pixel 2 blue	upper pixel 5 green	...
Bit 1	upper pixel 0 green	upper pixel 3 red	upper pixel 5 blue	...
Bit 2	upper pixel 0 blue	upper pixel 3 green	upper pixel 6 red	...
Bit 3	upper pixel 1 red	upper pixel 3 blue	upper pixel 6 green	...
Bit 4	lower pixel 0 red	lower pixel 2 blue	lower pixel 5 green	...
Bit 5	lower pixel 0 green	lower pixel 3 red	lower pixel 5 blue	...
Bit 6	lower pixel 0 blue	lower pixel 3 green	lower pixel 6 red	...
Bit 7	lower pixel 1 red	lower pixel 3 blue	lower pixel 6 green	...
Bit 8	upper pixel 1 green	upper pixel 4 red	upper pixel 6 blue	...
Bit 9	upper pixel 1 blue	upper pixel 4 green	upper pixel 7 red	...
Bit 10	upper pixel 2 red	upper pixel 4 blue	upper pixel 7 green	...
Bit 11	upper pixel 2 green	upper pixel 5 red	upper pixel 7 blue	...
Bit 12	lower pixel 1 green	lower pixel 4 red	lower pixel 6 blue	...
Bit 13	lower pixel 1 blue	lower pixel 4 green	lower pixel 7 red	...
Bit 14	lower pixel 2 red	lower pixel 4 blue	lower pixel 7 green	...
Bit 15	lower pixel 2 green	lower pixel 5 red	lower pixel 7 blue	...
Bit 16	SHFCLK	SHFCLK	SHFCLK	...
Bit 17				
Bit 18				
Bit 19				
Bit 20				
Bit 21				
Bit 22				
Bit 23				

Table 6.9 - Digital Format 15h

6.4.8 12-Bit Over 12-Bit RGB STN-DD - Code 19h

Bus Signal	1st Transfer	2nd Transfer	
Bit 0	upper pixel 0 red	upper pixel 4 red	...
Bit 1	upper pixel 0 green	upper pixel 4 green	...
Bit 2	upper pixel 0 blue	upper pixel 4 blue	...
Bit 3	lower pixel 0 red	lower pixel 4 red	...
Bit 4	lower pixel 0 green	lower pixel 4 green	...
Bit 5	lower pixel 0 blue	lower pixel 4 blue	...
Bit 6	upper pixel 1 red	upper pixel 5 red	...
Bit 7	upper pixel 1 green	upper pixel 5 green	...
Bit 8	upper pixel 1 blue	upper pixel 5 blue	...
Bit 9	lower pixel 1 red	lower pixel 5 red	...
Bit 10	lower pixel 1 green	lower pixel 5 green	...
Bit 11	lower pixel 1 blue	lower pixel 5 blue	...
Bit 12	upper pixel 2 red	upper pixel 6 red	...
Bit 13	upper pixel 2 green	upper pixel 6 green	...
Bit 14	upper pixel 2 blue	upper pixel 6 blue	...
Bit 15	lower pixel 2 red	lower pixel 6 red	...
Bit 16	lower pixel 2 green	lower pixel 6 green	...
Bit 17	lower pixel 2 blue	lower pixel 6 blue	...
Bit 18	upper pixel 3 red	upper pixel 7 red	...
Bit 19	upper pixel 3 green	upper pixel 7 green	...
Bit 20	upper pixel 3 blue	upper pixel 7 blue	...
Bit 21	lower pixel 3 red	lower pixel 7 red	...
Bit 22	lower pixel 3 green	lower pixel 7 green	...
Bit 23	lower pixel 3 blue	lower pixel 7 blue	...

Table 6.10 - Digital Format 19h

6.4.9 Pseudo 18-Bit RGB TFT - Code 20h

Bus Signal	1st Transfer	6 to 1 bpp	2nd Transfer	6 to 1 bpp	
Bit 0		bit 1 / 0		bit 1 / 0	...
Bit 1		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 2	pixel 0 blue	bit 3 / 2 / 1 / 0	pixel 1 blue	bit 3 / 2 / 1 / 0	...
Bit 3		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 4		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 5		bit 0		bit 0	...
Bit 6		bit 1 / 0		bit 1 / 0	...
Bit 7	pixel 0 green	bit 2 / 1 / 0	pixel 1 green	bit 2 / 1 / 0	...
Bit 8	or mono	bit 3 / 2 / 1 / 0	or mono	bit 3 / 2 / 1 / 0	...
Bit 9		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 10		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 11		bit 1 / 0		bit 1 / 0	...
Bit 12		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 13	pixel 0 red	bit 3 / 2 / 1 / 0	pixel 1 red	bit 3 / 2 / 1 / 0	...
Bit 14		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 15		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 16					
Bit 17					
Bit 18					
Bit 19					
Bit 20					
Bit 21					
Bit 22					
Bit 23					

Table 6.11 - Digital Format 20h

6.4.10 24-Bit MSB-Aligned RGB TFT - Code 24h

Bus Signal	1st Transfer	8 to 1 bpp	2nd Transfer	8 to 1 bpp	
Bit 0		bit 0		bit 0	...
Bit 1		bit 1 / 0		bit 1 / 0	...
Bit 2		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 3	pixel 0 blue	bit 3 / 2 / 1 / 0	pixel 1 blue	bit 3 / 2 / 1 / 0	...
Bit 4		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 5		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 6		bit 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 7		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 8		bit 0		bit 0	...
Bit 9		bit 1 / 0		bit 1 / 0	...
Bit 10		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 11	pixel 0 green	bit 3 / 2 / 1 / 0	pixel 1 green	bit 3 / 2 / 1 / 0	...
Bit 12	or mono	bit 4 / 3 / 2 / 1 / 0	or mono	bit 4 / 3 / 2 / 1 / 0	...
Bit 13		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 14		bit 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 15		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 16		bit 0		bit 0	...
Bit 17		bit 1 / 0		bit 1 / 0	...
Bit 18		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 19	pixel 0 red	bit 3 / 2 / 1 / 0	pixel 1 red	bit 3 / 2 / 1 / 0	...
Bit 20		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 21		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 22		bit 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 23		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0	...

Table 6.12 - Digital Format 24h

6.4.11 24-Bit LSB-Aligned RGB TFT - Code 25h

Bus Signal	1st Transfer	8 to 1 bpp	2nd Transfer	8 to 1 bpp	
Bit 0	pixel 0 blue	bit 0 / 0 / 0 / 0 / 0 / 0 / 0 / 0	pixel 1 blue	bit 0 / 0 / 0 / 0 / 0 / 0 / 0 / 0	...
Bit 1		bit 1 / 1 / 1 / 1 / 1 / 1 / 1		bit 1 / 1 / 1 / 1 / 1 / 1 / 1	...
Bit 2		bit 2 / 2 / 2 / 2 / 2 / 2		bit 2 / 2 / 2 / 2 / 2 / 2	...
Bit 3		bit 3 / 3 / 3 / 3 / 3		bit 3 / 3 / 3 / 3 / 3	...
Bit 4		bit 4 / 4 / 4 / 4		bit 4 / 4 / 4 / 4	...
Bit 5		bit 5 / 5 / 5		bit 5 / 5 / 5	...
Bit 6		bit 6 / 6		bit 6 / 6	...
Bit 7		bit 7		bit 7	...
Bit 8	pixel 0 green or mono	bit 0 / 0 / 0 / 0 / 0 / 0 / 0 / 0	pixel 1 green or mono	bit 0 / 0 / 0 / 0 / 0 / 0 / 0 / 0	...
Bit 9		bit 1 / 1 / 1 / 1 / 1 / 1 / 1		bit 1 / 1 / 1 / 1 / 1 / 1 / 1	...
Bit 10		bit 2 / 2 / 2 / 2 / 2 / 2		bit 2 / 2 / 2 / 2 / 2 / 2	...
Bit 11		bit 3 / 3 / 3 / 3 / 3		bit 3 / 3 / 3 / 3 / 3	...
Bit 12		bit 4 / 4 / 4 / 4		bit 4 / 4 / 4 / 4	...
Bit 13		bit 5 / 5 / 5		bit 5 / 5 / 5	...
Bit 14		bit 6 / 6		bit 6 / 6	...
Bit 15		bit 7		bit 7	...
Bit 16	pixel 0 red	bit 0 / 0 / 0 / 0 / 0 / 0 / 0 / 0	pixel 1 red	bit 0 / 0 / 0 / 0 / 0 / 0 / 0 / 0	...
Bit 17		bit 1 / 1 / 1 / 1 / 1 / 1 / 1		bit 1 / 1 / 1 / 1 / 1 / 1 / 1	...
Bit 18		bit 2 / 2 / 2 / 2 / 2 / 2		bit 2 / 2 / 2 / 2 / 2 / 2	...
Bit 19		bit 3 / 3 / 3 / 3 / 3		bit 3 / 3 / 3 / 3 / 3	...
Bit 20		bit 4 / 4 / 4 / 4		bit 4 / 4 / 4 / 4	...
Bit 21		bit 5 / 5 / 5		bit 5 / 5 / 5	...
Bit 22		bit 6 / 6		bit 6 / 6	...
Bit 23		bit 7		bit 7	...

Table 6.13 - Digital Format 25h

6.4.12 Double 12-Bit RGB TFT - Code 30h

Bus Signal	1st Transfer	4 to 1 bpp	2nd Transfer	4 to 1 bpp	
Bit 0	pixel 0 blue	bit 0	pixel 2 blue	bit 0	...
Bit 1		bit 1 / 0		bit 1 / 0	...
Bit 2		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 3		bit 3 / 2 / 1 / 0		bit 3 / 2 / 1 / 0	...
Bit 4	pixel 0 green or mono	bit 0	pixel 2 green or mono	bit 0	...
Bit 5		bit 1 / 0		bit 1 / 0	...
Bit 6		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 7		bit 3 / 2 / 1 / 0		bit 3 / 2 / 1 / 0	...
Bit 8	pixel 0 red	bit 0	pixel 2 red	bit 0	...
Bit 9		bit 1 / 0		bit 1 / 0	...
Bit 10		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 11		bit 3 / 2 / 1 / 0		bit 3 / 2 / 1 / 0	...
Bit 12	pixel 1 blue	bit 0	pixel 3 blue	bit 0	...
Bit 13		bit 1 / 0		bit 1 / 0	...
Bit 14		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 15		bit 3 / 2 / 1 / 0		bit 3 / 2 / 1 / 0	...
Bit 16	pixel 1 green or mono	bit 0	pixel 3 green or mono	bit 0	...
Bit 17		bit 1 / 0		bit 1 / 0	...
Bit 18		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 19		bit 3 / 2 / 1 / 0		bit 3 / 2 / 1 / 0	...
Bit 20	pixel 1 red	bit 0	pixel 3 red	bit 0	...
Bit 21		bit 1 / 0		bit 1 / 0	...
Bit 22		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 23		bit 3 / 2 / 1 / 0		bit 3 / 2 / 1 / 0	...

Table 6.14 - Digital Format 30h

6.4.13 Double 18-Bit RGB TFT - Code 34h

Bus Signal	1st Transfer	6 to 1 bpp	2nd Transfer	6 to 1 bpp	
Bit 0	pixel 0 blue	bit 0	pixel 2 blue	bit 0	...
Bit 1		bit 1 / 0		bit 1 / 0	...
Bit 2		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 3		bit 3 / 2 / 1 / 0		bit 3 / 2 / 1 / 0	...
Bit 4		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 5		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 6	pixel 0 green or mono	bit 0	pixel 2 green or mono	bit 0	...
Bit 7		bit 1 / 0		bit 1 / 0	...
Bit 8		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 9		bit 3 / 2 / 1 / 0		bit 3 / 2 / 1 / 0	...
Bit 10		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 11		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 12	pixel 0 red	bit 0	pixel 2 red	bit 0	...
Bit 13		bit 1 / 0		bit 1 / 0	...
Bit 14		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 15		bit 3 / 2 / 1 / 0		bit 3 / 2 / 1 / 0	...
Bit 16		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 17		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 18	pixel 1 blue	bit 0	pixel 3 blue	bit 0	...
Bit 19		bit 1 / 0		bit 1 / 0	...
Bit 20		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 21		bit 3 / 2 / 1 / 0		bit 3 / 2 / 1 / 0	...
Bit 22		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 23		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 24	pixel 1 green or mono	bit 0	pixel 3 green or mono	bit 0	...
Bit 25		bit 1 / 0		bit 1 / 0	...
Bit 26		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 27		bit 3 / 2 / 1 / 0		bit 3 / 2 / 1 / 0	...
Bit 28		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 29		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 30	pixel 1 red	bit 0	pixel 3 red	bit 0	...
Bit 31		bit 1 / 0		bit 1 / 0	...
Bit 32		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 33		bit 3 / 2 / 1 / 0		bit 3 / 2 / 1 / 0	...
Bit 34		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 35		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...

Table 6.15 - Digital Format 34h

6.4.14 Double 24-Bit RGB TFT - Code 38h

Bus Signal	1st Transfer	8 to 1 bpp	2nd Transfer	8 to 1 bpp	
Bit 0		bit 0		bit 0	...
Bit 1		bit 1 / 0		bit 1 / 0	...
Bit 2		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 3	pixel 0 blue	bit 3 / 2 / 1 / 0	pixel 2 blue	bit 3 / 2 / 1 / 0	...
Bit 4		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 5		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 6		bit 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 7		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 8		bit 0		bit 0	...
Bit 9		bit 1 / 0		bit 1 / 0	...
Bit 10		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 11	pixel 0 green	bit 3 / 2 / 1 / 0	pixel 2 green	bit 3 / 2 / 1 / 0	...
Bit 12	or mono	bit 4 / 3 / 2 / 1 / 0	or mono	bit 4 / 3 / 2 / 1 / 0	...
Bit 13		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 14		bit 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 15		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 16		bit 0		bit 0	...
Bit 17		bit 1 / 0		bit 1 / 0	...
Bit 18		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 19	pixel 0 red	bit 3 / 2 / 1 / 0	pixel 2 red	bit 3 / 2 / 1 / 0	...
Bit 20		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 21		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 22		bit 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 23		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 24		bit 0		bit 0	...
Bit 25		bit 1 / 0		bit 1 / 0	...
Bit 26		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 27	pixel 1 blue	bit 3 / 2 / 1 / 0	pixel 3 blue	bit 3 / 2 / 1 / 0	...
Bit 28		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 29		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 30		bit 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 31		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 32		bit 0		bit 0	...
Bit 33		bit 1 / 0		bit 1 / 0	...
Bit 34		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 35	pixel 1 green	bit 3 / 2 / 1 / 0	pixel 3 green	bit 3 / 2 / 1 / 0	...
Bit 36	or mono	bit 4 / 3 / 2 / 1 / 0	or mono	bit 4 / 3 / 2 / 1 / 0	...
Bit 37		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 38		bit 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 39		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 40		bit 0		bit 0	...
Bit 41		bit 1 / 0		bit 1 / 0	...
Bit 42		bit 2 / 1 / 0		bit 2 / 1 / 0	...
Bit 43	pixel 1 red	bit 3 / 2 / 1 / 0	pixel 3 red	bit 3 / 2 / 1 / 0	...
Bit 44		bit 4 / 3 / 2 / 1 / 0		bit 4 / 3 / 2 / 1 / 0	...
Bit 45		bit 5 / 4 / 3 / 2 / 1 / 0		bit 5 / 4 / 3 / 2 / 1 / 0	...
Bit 46		bit 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 6 / 5 / 4 / 3 / 2 / 1 / 0	...
Bit 47		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0		bit 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0	...

Table 6.16 - Digital Format 38h

6.5 Digital Component Video Data Formats

Codes 40h-42h in Table 4.11 are used to indicate data formats for Digital Component Video (4:2:2). In this mode, the data format follows that of ANSI/SMPTE 125M-1992.

The 24 bits input into the transmitter are Y, Cr, and Cb rather than R, G, and B. Cr and Cb are subsampled by 2 in the horizontal direction. Formulas for conversion from RGB to Y,Cr,Cb are repeated here for reference:

Y = 0.299R + 0.587G + 0.114B
Cr = 0.713(R-Y) = 0.500R - 0.419G - 0.081B
Cb = 0.564(B-Y) = 0.500B - 0.169R - 0.331G

The modes described in this proposal may be distinguished through the use of the "bit-depth per sub-channel" fields in Table 4.12, as follows:

YCrCb mode	sub channel bit depth specified			
	0	1	2	3
Parallel 10-bit mode	10	10	0	0
Parallel 8-bit mode	8	8	0	0
Serial 10-bit mode	10	0	X	0
Serial 8-bit mode	8	0	X	X

Table 6.17 - Sub Channel Bit Depth for YCrCb Formats

In the serial component modes, the "X" locations are set to either "10" (in the 10-bit case) or "8" (in the 8-bit case) to indicate support for the optional second and third optional video streams.

6.5.1 Parallel 8-Bit or 10-Bit Component Mode - Code 40h

In parallel component mode, the luminance and color difference signals for each pixel are sent in parallel. The data for each pixel (one Y component sample and one C component sample) is sent in parallel on 20 of the 24 lines. Chrominance samples alternate between Cr and Cb on each pixel with Cb coming first. The remaining 4 lines are user-defined and may be used, for example, as pixel specific z-buffer applications such as OSD overlay or closed caption.

Bus Signal	1st Transfer	10 or 8 bpp	2nd Transfer	10 or 8 bpp	
Bit 0	pixel 0 Y	bit 0	pixel 1 Y	bit 0	...
Bit 1		bit 1		bit 1	...
Bit 2		bit 2 / 0		bit 2 / 0	...
Bit 3		bit 3 / 1		bit 3 / 1	...
Bit 4		bit 4 / 3		bit 4 / 3	...
Bit 5		bit 5 / 4		bit 5 / 4	...
Bit 6		bit 6 / 5		bit 6 / 5	...
Bit 7		bit 7 / 6		bit 7 / 6	...
Bit 8		bit 8 / 7		bit 8 / 7	...
Bit 9		bit 9 / 8		bit 9 / 8	...
Bit 10	pixel 0 Cb	bit 0	pixel 1 Cr	bit 0	...
Bit 11		bit 1		bit 1	...
Bit 12		bit 2 / 0		bit 2 / 0	...
Bit 13		bit 3 / 1		bit 3 / 1	...
Bit 14		bit 4 / 3		bit 4 / 3	...
Bit 15		bit 5 / 4		bit 5 / 4	...
Bit 16		bit 6 / 5		bit 6 / 5	...
Bit 17		bit 7 / 6		bit 7 / 6	...
Bit 18		bit 8 / 7		bit 8 / 7	...
Bit 19		bit 9 / 8		bit 9 / 8	...
Bit 20	user defined		user defined		...
Bit 21					...
Bit 22					...
Bit 23					...

Table 6.18 - Digital Format 40h

6.5.2 Serial 8-bit Mode - Code 41h

In 8-bit serial mode, up to three video streams may be sent using a 24 bit interface. The pixel components are sent serially with the 8 bits of each component sent in parallel.

Bus Signal	1st Transfer	8-bpp	2nd Transfer	8-bpp	3rd Transfer	8-bpp	4th Transfer	8-bpp	
Bit 0		bit 0		bit 0		bit 0		bit 0	...
Bit 1		bit 1		bit 1		bit 1		bit 1	...
Bit 2		bit 2		bit 2		bit 2		bit 2	...
Bit 3	pixel 0 Cb	bit 3	pixel 0 Y	bit 3	pixel 1 Cr	bit 3	pixel 1 Y	bit 3	...
Bit 4	(primary	bit 4	(primary	bit 4	(primary	bit 4	(primary	bit 4	...
Bit 5	stream)	bit 5	stream)	bit 5	stream)	bit 5	stream)	bit 5	...
Bit 6		bit 6		bit 6		bit 6		bit 6	...
Bit 7		bit 7		bit 7		bit 7		bit 7	...
Bit 8		bit 0		bit 0		bit 0		bit 0	...
Bit 9		bit 1		bit 1		bit 1		bit 1	...
Bit 10		bit 2		bit 2		bit 2		bit 2	...
Bit 11	pixel 0 Cb	bit 3	pixel 0 Y	bit 3	pixel 1 Cr	bit 3	pixel 1 Y	bit 3	...
Bit 12	(optional	bit 4	(optional	bit 4	(optional	bit 4	(optional	bit 4	...
Bit 13	stream 2)	bit 5	stream 2)	bit 5	stream 2)	bit 5	stream 2)	bit 5	...
Bit 14		bit 6		bit 6		bit 6		bit 6	...
Bit 15		bit 7		bit 7		bit 7		bit 7	...
Bit 16		bit 0		bit 0		bit 0		bit 0	...
Bit 17		bit 1		bit 1		bit 1		bit 1	...
Bit 18		bit 2		bit 2		bit 2		bit 2	...
Bit 19	pixel 0 Cb	bit 3	pixel 0 Y	bit 3	pixel 1 Cr	bit 3	pixel 1 Y	bit 3	...
Bit 20	(optional	bit 4	(optional	bit 4	(optional	bit 4	(optional	bit 4	...
Bit 21	stream 3)	bit 5	stream 3)	bit 5	stream 3)	bit 5	stream 3)	bit 5	...
Bit 22		bit 6		bit 6		bit 6		bit 6	...
Bit 23		bit 7		bit 7		bit 7		bit 7	...

Table 6.19 - Digital Format 41h

6.5.3 Serial 10-bit Mode - Code 42h

In 10-bit serial mode, up to two video streams may be sent using a 24 bit interface. The pixel components are sent serially with the 10 bits of each component sent in parallel.

Bus Signal	1st Transfer	10-bpp	2nd Transfer	10-bpp	3rd Transfer	10-bpp	4th Transfer	10-bpp	
Bit 0		bit 0		bit 0		bit 0		bit 0	...
Bit 1		bit 1		bit 1		bit 1		bit 1	...
Bit 2		bit 2		bit 2		bit 2		bit 2	...
Bit 3	pixel 0 Cb	bit 3	pixel 0 Y	bit 3	pixel 1 Cr	bit 3	pixel 1 Y	bit 3	...
Bit 4	(primary	bit 4	(primary	bit 4	(primary	bit 4	(primary	bit 4	...
Bit 5	stream)	bit 5	stream)	bit 5	stream)	bit 5	stream)	bit 5	...
Bit 6		bit 6		bit 6		bit 6		bit 6	...
Bit 7		bit 7		bit 7		bit 7		bit 7	...
Bit 8		bit 0		bit 0		bit 0		bit 0	...
Bit 9		bit 1		bit 1		bit 1		bit 1	...
Bit 10		bit 2		bit 2		bit 2		bit 2	...
Bit 11	pixel 0 Cb	bit 3	pixel 0 Y	bit 3	pixel 1 Cr	bit 3	pixel 1 Y	bit 3	...
Bit 12	(optional	bit 4	(optional	bit 4	(optional	bit 4	(optional	bit 4	...
Bit 13	stream 2)	bit 5	stream 2)	bit 5	stream 2)	bit 5	stream 2)	bit 5	...
Bit 14		bit 6		bit 6		bit 6		bit 6	...
Bit 15		bit 7		bit 7		bit 7		bit 7	...
Bit 16	LSB pel 0 Cb	bit 8	LSB pel 0 Y	bit 0	LSB pel 1 Cr	bit 8	LSB pel 1 Y	bit 0	...
Bit 17	stream 1	bit 9	stream 1	bit 1	stream 1	bit 9	stream 1	bit 1	...
Bit 18	LSB pel 0 Cb	bit 8	LSB pel 0 Y	bit 2	LSB pel 1 Cr	bit 8	LSB pel 1 Y	bit 2	...
Bit 19	stream 2	bit 9	stream 2	bit 3	stream 2	bit 9	stream 2	bit 3	...
Bit 20		bit 4		bit 4		bit 4		bit 4	...
Bit 21	user defined	bit 5	user defined	bit 5	user defined	bit 5	user defined	bit 5	...
Bit 22		bit 6		bit 6		bit 6		bit 6	...
Bit 23		bit 7		bit 7		bit 7		bit 7	...

Table 6.20 - Digital Format 42h

7. APPENDIX B - Sample EDID

7.1 Version 1 Revision 1 data structure format

This sample EDID is included for illustration only, it should not be considered as representative of any particular monitor.

Byte # (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01		FF	11111111
2	02		FF	11111111
3	03		FF	11111111
4	04		FF	11111111
5	05		FF	11111111
6	06		FF	11111111
7	07		00	00000000
8	08	EISA manufacturer code = *IBM*	24	00100100
9	09	*(Compressed ASCII)*	4D	01001101
10	0A	Product code = *6542*	8E	10001110
11	0B	*(Hex, LSB first)*	19	00011001
12	0C	32-bit serial number = *00000000*	00	00000000
13	0D		00	00000000
14	0E		00	00000000
15	0F		00	00000000
16	10	Week of manufacture = *10*	0A	00001010
17	11	Year of manufacture = *1995*	05	00000101
18	12	EDID Structure version # = *1*	01	00000001
19	13	EDID revision # = *1*	01	00000001
20	14	Video i/p definition = *Analog i/p, 1.0 Vp-p, separate syncs*	08	00001000
21	15	Max H image size (cm) = *40 cm*	28	00101000
22	16	Max V image size (cm) = *30 cm*	1E	00011110
23	17	Display gamma = *2.8*	B4	10110100
24	18	Feature support (DPMS) = *Standby, Suspend, RGB Color*	C8	11001000
25	19	Red / Green low bits	00	00000000
26	1A	Blue / White low bits	B2	10110010
27	1B	Red x *Rx = 0.625*	A0	10100000
28	1C	Red y *Ry = 0.340*	57	01010111
29	1D	Green x *Gx = 0.285*	49	01001001
30	1E	Green y *Gy = 0.605*	9B	10011011
31	1F	Blue x *Bx = 0.150*	26	00100110
32	20	Blue y *By = 0.065*	10	00010000
33	21	White x *Wx = 0.281*	48	01001000
34	22	White y *Wy = 0.311*	4F	01001111
35	23	Established timings I = *720 x 400 @ 70Hz* *640 x 480 @ 60Hz, 75Hz*	A4	10100100
36	24	Established timings *II* = *800 x 600 @ 72Hz, 75Hz* *1024 x 768 @ 60Hz, 70Hz, 75Hz* *1280 x 1024 @ 75Hz*	CF	11001111
37	25	Established timings III / Manufacturer's reserved timings *640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 @ 85Hz* *1600 x 1200 @ 75Hz*	7C	01111100
38	26	Standard timing identification # 1	31	00110001
39	27	*640 x 480 @ 70 Hz*	4A	01001010

Byte # (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
40	28	Standard timing identification # 2	A9	10101001
41	29	*1600 x 1200 @ 60 Hz*	40	01000000
42	2A	Standard timing identification # 3	A9	10101001
43	2B	*1600 x 1200 @ 70 Hz*	4A	01001010
44	2C	Standard timing identification # 4	A9	10101001
45	2D	*1600 x 1200 @ 75 Hz*	4F	01001111
46	2E	Standard timing identification # 5	81	10000001
47	2F	*1280 x 1024 @ 60 Hz*	80	10000000
48	30	Standard timing identification # 6	01	00000001
49	31	*Unused*	01	00000001
50	32	Standard timing identification # 7	01	00000001
51	33	*Unused*	01	00000001
52	34	Standard timing identification # 8	01	00000001
53	35	*Unused*	01	00000001
54	36	Detailed timing descriptor # 1 / Monitor Descriptor # 1	10	00010000
55	37	*720 x 350 @ 70 Hz mode : pixel clock = 28.32 MHz*	0B	00001011
56	38	*Horizontal active = 720 pixels*	D0	11010000
57	39	*Horizontal blanking = 180 pixels*	B4	10110100
58	3A		20	00100000
59	3B	*Vertical active = 350 lines*	5E	01011110
60	3C	*Vertical blanking = 99 lines*	63	01100011
61	3D		10	00010000
62	3E	*Horizontal sync. offset = 18 pixels*	12	00010010
63	3F	*Horizontal sync. width = 108 pixels*	6C	01101100
64	40	*Vertical sync. offset = 38 lines*	62	01100010
65	41	*Vertical sync. width = 2 lines*	08	00001000
66	42	*Horizontal image size = 250 mm*	FA	11111010
67	43	*Vertical image size = 184 mm*	B8	10111000
68	44		00	00000000
69	45	*No Horizontal border*	00	00000000
70	46	*No Vertical Border*	00	00000000
71	47	*Separate digital syncs., Horizontal +ve, Vertical -ve polarity*	1A	00011010
72	48	Detailed timing descriptor # 2 / Monitor Descriptor # 2	00	00000000
73	49	*Flag (byte 2)*	00	00000000
74	4A	*Reserved*	00	00000000
75	4B	*FF(hex) defines Serial Number (ASCII)*	FF	11111111
76	4C	*Flag*	00	00000000
77	4D	*1st character of serial number = 3*	33	00110011
78	4E	*2nd character of serial number = 0*	30	00110000
79	4F	*3rd character of serial number = 9*	39	00111001
80	50	*4th character of serial number = A*	41	01000001
81	51	*5th character of serial number = B*	42	01000010
82	52	*6th character of serial number = C*	43	01000011
83	53	*7th character of serial number = 0*	30	00110000
84	54	*8th character of serial number = 0*	30	00110000
85	55	*9th character of serial number = 0*	30	00110000
86	56	*10th character of serial number = 2*	32	00110010
87	57	*11th character of serial number = 5*	35	00110101
88	58	*New line character : indicates end of s/n*	0A	00001010
89	59	*Padding with "blank" character*	20	00100000
90	5A	Detailed timing descriptor # 3 / Monitor Descriptor # 3	00	00000000

Byte # (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
91	5B	*Flag (byte 2)*	00	00000000
92	5C	*Reserved*	00	00000000
93	5D	*FE(hex) defines ASCII String*	FE	11111110
94	5E	*Flag*	00	00000000
95	5F	*1st character of string = T*	54	01010100
96	60	*2nd character of string = H*	48	01001000
97	61	*3rd character of string = I*	49	01001001
98	62	*4th character of string = S*	53	01010011
99	63	*5th character of string = <space>*	20	00100000
100	64	*6th character of string = I*	49	01001001
101	65	*7th character of string = S*	53	01010011
102	66	*8th character of string = <space>*	20	00100000
103	67	*9th character of string = A*	41	01000001
104	68	*New line character : indicates end of ASCII String*	0A	00001010
105	69	*Padding with "blank" character*	20	00100000
106	6A	*Padding with "blank" character*	20	00100000
107	6B	*Padding with "blank" character*	20	00100000
108	6C	Detailed timing descriptor # 4 / Monitor Descriptor # 4	00	00000000
109	6D	*Flag (byte 2)*	00	00000000
110	6E	*Reserved*	00	00000000
111	6F	*FE(hex) defines ASCII String*	FE	11111110
112	70	*Flag*	00	00000000
113	71	*1st character of string = T*	54	01010100
114	72	*2nd character of string = E*	45	01000101
115	73	*3rd character of string = S*	53	01010011
116	74	*4th character of string = T*	54	01010100
117	75	*5th character of string = ,*	2C	00101100
118	76	*6th character of string =* <space>	20	00100000
119	77	*7th character of string = T*	54	01010400
120	78	*8th character of string = H*	48	01001000
121	79	*9th character of string = E*	45	01000101
122	7A	*10th character of string =* <space>	20	00100000
123	7B	*11th character of string = E*	45	01000101
124	7C	*12th character of string = N*	4E	01001110
125	7D	*13th character of string = D*	44	01000100
126	7E	Extension flag = *0 EDID extension blocks*	00	00000000
127	7F	Checksum	8F	10001111

7.2 Version 2 Revision 0 data structure format for TFT monitor using TMDS interface

This sample EDID is included for illustration only, it should not be considered as representative of any particular monitor.

Byte# (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
0	00	EDID Structure version 2 revision 0	20	00100000
1	01	EISA manufacture code =IBM	24	00100100
2	02	(Compressed ASCII)	4D	01001101
3	03	Product code = 9704h	04	00000100
4	04	(Hex, LSB First)	97	10010111
5	05	Week of manufacture =15	0F	00001111
6	06	Year of manufacture =2001 = 07D1h	D1	11010001
7	07		07	00000111
8	08	Manufacturer's ID string - 32 bytes: "IBM TFT-LCD MONITOR" 1st character of string = I	49	01001001
9	09	2nd character of string = B	42	01000010
10	0A	3rd character of string = M	4D	01001101
11	0B	4th character of string = <tab>	09	00001001
12	0C	5th character of string = T	54	01010100
13	0D	6th character of string = F	46	01000110
14	0E	7th character of string = T	54	01010100
15	0F	8th character of string = <space>	2D	00101101
16	10	9th character of string = L	4C	01001100
17	11	10th character of string = C	43	01000011
18	12	11th character of string = D	44	01000100
19	13	12th character of string = <space>	20	00100000
20	14	13th character of string = M	4D	01001101
21	15	14thcharacter of string = O	4F	01001111
22	16	15th character of string = N	4E	01001110
23	17	16thcharacter of string = I	49	01001001
24	18	17th character of string = T	54	01010100
25	19	18thcharacter of string = O	4F	01001111
26	1A	19th character of string = R	52	01010010
27	1B	20th character of string = <new line>	0A	00001010
28	1C	21st character of string = <space>	20	00100000
29	1D	22nd character of string = <space>	20	00100000
30	1E	23rd character of string = <space>	20	00100000
31	1F	24th character of string = <space>	20	00100000
32	20	25th character of string = <space>	20	00100000
33	21	26th character of string = <space>	20	00100000
34	22	27th character of string = <space>	20	00100000
35	23	28th character of string = <space>	20	00100000
36	24	29th character of string = <space>	20	00100000
37	25	30th character of string = <space>	20	00100000
38	26	31st character of string = <space>	20	00100000
39	27	32nd character of string = <space>	20	00100000
40	28	Serial number string - 16 bytes: "52000001" 1st character of string = 5	35	00110101

Byte# (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
41	29	2nd character of string = 2	32	00110010
42	2A	3rd character of string = 0	30	00110000
43	2B	4th character of string = 0	30	00110000
44	2C	5th character of string = 0	30	00110000
45	2D	6th character of string = 0	30	00110000
46	2E	7th character of string = 0	30	00110000
47	2F	8th character of string = 1	31	00110001
48	30	9th character of string = <new line>	0A	00001010
49	31	10tht character of string = <space>	20	00100000
50	32	11th character of string = <space>	20	00100000
51	33	12th character of string = <space>	20	00100000
52	34	13tht character of string = <space>	20	00100000
53	35	14th character of string = <space>	20	00100000
54	36	15th character of string = <space>	20	00100000
55	37	16th character of string = <space>	20	00100000
56	38	Unused - 8 bytes: set to 20h	20	00100000
57	39		20	00100000
58	3A		20	00100000
59	3B		20	00100000
60	3C		20	00100000
61	3D		20	00100000
62	3E		20	00100000
63	3F		20	00100000
64	40	Default physical interface = P&D (no secondary interface)	50	01010000
65	41	Default video interface = TMDS (no secondary interface)	30	00110000
66	42	Default interface data format = Digital type (Table 4.11) display enable DE high / shift clock rising edge / 1 channel / exponent = 0	D0	11010000
67	43	Default interface minimum channel speed = 65 MHz	41	01000001
68	44	Default interface maximum channel speed = 112 MHz	70	01110000
69	45	TFT 24 bpp (P&D supported)	24	00100100
70	46	Secondary Interface = none	00	00000000
71	47		00	00000000
72	48		00	00000000
73	49		00	00000000
74	4A	Default color/luminance encoding = RGB (no secondary interface)	10	00010000
75	4B	R = 6 bits / G = 6 bits	66	01100110
76	4C	B = 6 bits / no subchannel 3	60	01100000
77	4D	No secondary interface	00	00000000
78	4E		00	00000000
79	4F	Display Technology type/subtype LCD/TFT	13	00010011
80	50	Major characteristics: color / not selectable chromaticity / not conditional update / normal landscape / not transparent background / desktop display	89	10001001
81	51	DPMS / stereo / standard color space	E0	11100000
82	52	Audio input mono USB/audio output stereo USB	58	01011000
83	53	No additional features	00	00000000
84	54	Display response rise time 10ms	3A	00111010
85	55	Display response fall time 40 ms	24	00100100

Byte# (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
86	56	White gamma =2.4 *(2.4*100-100=140)*	8C	10001100
87	57	No additional gamma	FF	11111111
88	58		FF	11111111
89	59		FF	11111111
90	5A	Max luminance 150 cd/m^2	DC	11011100
91	5B	*1500 = 5DCh*	05	00000101
92	5C	Standard RGB / adjustable gamma / offset positive	C0	11000000
93	5D	Offset value=0	00	00000000
94	5E	Red/Green low bits	32	00110010
95	5F	Blue/White low bits	EC	11101100
96	60	Red x= 0.621	9F	10011111
97	61	Red y= 0.347	58	01011000
98	62	Green x = 0.281	48	01001000
99	63	Green y= 0.615	9D	10011101
100	64	Blue x= 0.140	23	00100011
101	65	Blue y= 0.092	17	00010111
102	66	White x = 0.292	4A	01001010
103	67	White y = 0.320	52	01010010
104	68	No additional gammas or color points *set values = 0*	00	00000000
105	69		00	00000000
106	6A		00	00000000
107	6B		00	00000000
108	6C		00	00000000
109	6D		00	00000000
110	6E		00	00000000
111	6F		00	00000000
112	70		00	00000000
113	71		00	00000000
114	72	Max horizontal image size 318.7 mm=319	3F	00111111
115	73		01	00000001
116	74	Max vertical image size 255.0 mm	FF	11111111
117	75		00	00000000
118	76	Max horizontal addressibility =1280	00	00000000
119	77		05	00000101
120	78	Max vertical addressibility =1024	00	00000000
121	79		04	00000100
122	7A	Horizontal pixel pitch = 0.247 mm	19	00011001
123	7B	Vertical pixel pitch = 0.247 mm	19	00011001
124	7C	Unused	00	00000000
125	7D	GTF not supported	00	00000000
126	7E	No extension, 1 Gamma Table, 1 Range limits, 1 detailed range	25	00100101
127	7F	One 4-byte code, no detailed timing	08	00001000
128	80	Luminance Table with 15 entries (white only)	0F	00001111
129	81	1^{st} table entry	03	00000011
130	82	2^{nd} table entry	03	00000011
131	83	3^{rd} table entry	06	00000110
132	84	4^{th} table entry	0A	00001010
133	85	5^{th} table entry	10	00010000
134	86	6^{th} table entry	19	00011001
135	87	7^{th} table entry	24	00100100

Byte# (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
136	88	8th table entry	32	00110010
137	89	9th table entry	42	01000010
138	8A	10th table entry	55	01010101
139	8B	11th table entry	6A	01101010
140	8C	12th table entry	82	10000010
141	8D	13th table entry	9D	10011101
142	8E	14th table entry	BB	10111011
143	8F	15th table entry	DC	11011100
144	90	Range Limits: Min frame rate = 60 HZ = *00001111 00b*	0F	00001111
145	91	Max frame rate = 60 HZ = *00001111 00b*	0F	00001111
146	92	Min line rate = 63.36 KHz = *63 = 00001111 11b*	0F	00001111
147	93	Max line rate = 63.36 KHz = *64 = 00010000 00b*	10	00010000
148	94	Low bits *00 00 11 00*	0C	00001100
149	95	Min pixel rate 108 MHz = 0000 01101100b	6C	01101100
150	96	Max pixel rate 114 MHz = 0000 01110010b	72	01110010
151	97	Upper bits Min/Max Pixel rate 0000 0000b	00	00000000
152	98	Detailed timings minimum pixel clock 108 MHz	30	00110000
153	99	10800 = 2A30h	2A	00101010
154	9A	Min horizontal blanking = 478 pixels	DE	11011110
155	9B	Min vertical blanking = 32 lines	20	00100000
156	9C	Min horizontal blanking & vertical blanking upper bits	10	00010000
157	9D	Min horizontal sync offset = 26	1A	00011010
158	9E	Min horizontal pulse width = 200	C8	11001000
159	9F	Min vertical sync offset=3min vertical sync pulse width=3	33	00110011
160	A0		00	00000000
161	A1	Max pixel clock=114.00	88	10001000
162	A2	11400 = 2c88h	2C	00101100
163	A3	Max horizontal blanking = 478	DE	11011110
164	A4	Max vertical blanking =32	20	00100000
165	A5	Max horizontal blanking and max vertical blanking	10	00010000
166	A6	Max horizontal sync offset = 3max vertical sync pulse width = 3	33	00110011
167	A7	Horizontal image size =318.7mm	3F	00111111
168	A8	Vertical image size = 255.0 mm	FF	11111111
169	A9		10	00010000
170	AA	Horizontal active = 1280	00	00000000
171	AB	Vertical active = 1024	00	00000000
172	AC		54	01010100
173	AD	Horizontal border = 0	00	00000000
174	AE	Vertical border = 0	00	00000000
175	AF	Flags ni,flm=1, lp=1	06	00000110
176	B0	4-byte timing -active pixels 1280 *(1280-256)/16 = 64*	40	01000000
177	B1	Portait / no stereo / no reduced blanking / not interlaced / LP=1, FLM=1 / SHF=1	1E	00011110
178	B2	H:V 4:3 133:100	85	10000101
179	B3	Refresh rate 60Hz	3C	00111100
180	B4	Unused - fill with 00h	00	00000000
181	B5		00	00000000
182	B6		00	00000000
183	B7		00	00000000
184	B8		00	00000000

Byte# (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
185	B9		00	00000000
186	BA		00	00000000
187	BB		00	00000000
188	BC		00	00000000
189	BD		00	00000000
190	BE		00	00000000
191	BF		00	00000000
192	C0		00	00000000
193	C1		00	00000000
194	C2		00	00000000
195	C3		00	00000000
196	C4		00	00000000
197	C5		00	00000000
198	C6		00	00000000
199	C7		00	00000000
200	C8		00	00000000
201	C9		00	00000000
202	CA		00	00000000
203	CB		00	00000000
204	CC		00	00000000
205	CD		00	00000000
206	CE		00	00000000
207	CF		00	00000000
208	D0		00	00000000
209	D1		00	00000000
210	D2		00	00000000
211	D3		00	00000000
212	D4		00	00000000
213	D5		00	00000000
214	D6		00	00000000
215	D7		00	00000000
216	D8		00	00000000
217	D9		00	00000000
218	DA		00	00000000
219	DB		00	00000000
220	DC		00	00000000
221	DD		00	00000000
222	DE		00	00000000
223	DF		00	00000000
224	E0		00	00000000
225	E1		00	00000000
226	E2		00	00000000
227	E3		00	00000000
228	E4		00	00000000
229	E5		00	00000000
230	E6		00	00000000
231	E7		00	00000000
232	E8		00	00000000
233	E9		00	00000000
234	EA		00	00000000

Byte# (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
235	EB		00	00000000
236	EC		00	00000000
237	ED		00	00000000
238	EE		00	00000000
239	EF		00	00000000
240	F0		00	00000000
241	F1		00	00000000
242	F2		00	00000000
243	F3		00	00000000
244	F4		00	00000000
245	F5		00	00000000
246	F6		00	00000000
247	F7		00	00000000
248	F8		00	00000000
259	F9		00	00000000
250	FA		00	00000000
251	FB		00	00000000
252	FC		00	00000000
253	FD		00	00000000
254	FE		00	00000000
255	FF	Checksum	51	01010001

7.3 Version 2 Revision 0 data structure format for CRT monitor using Analog interface

This sample EDID is included for illustration only, it should not be considered as representative of any particular monitor.

Byte# (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
0	00	EDID Structure version 2 revision 0	20	00100000
1	01	EISA manufacture code =NEC	38	00111000
2	02	(Compressed ASCII)	A3	10100011
3	03	Product code =1750	D6	11010110
4	04	(Hex, LSB First)	06	00000110
5	05	Week of manufacture =21	15	00010101
6	06	Year of manufacture =1997 = 07CDh	CD	11001101
7	07		07	00000111
8	08	Manufacturer's ID string - 32 bytes: "NEC Generic 17" monitor name" 1st character of string = N	4E	01001110
9	09	2nd character of string = E	45	01000101
10	0A	3rd character of string = C	43	01000011
11	0B	4th character of string = <tab>	09	00001001
12	0C	5th character of string = G	47	01000111
13	0D	6th character of string = e	65	01100101
14	0E	7th character of string = n	6E	01101110
15	0F	8th character of string = e	65	01100101
16	10	9th character of string = r	72	01110010
17	11	10th character of string = i	69	01101001

Byte# (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
18	12	11th character of string = c	63	01100011
19	13	12th character of string = <space>	20	00100000
20	14	13th character of string = 1	31	00110001
21	15	14th character of string = 7	37	00110111
22	16	15th character of string = "	22	00100010
23	17	16th character of string = <space>	20	00100000
24	18	17th character of string = m	6D	01101101
25	19	18th character of string = o	6F	01101111
26	1A	19th character of string = n	6E	01101110
27	1B	20th character of string = i	69	01101001
28	1C	21st character of string = t	74	01110100
29	1D	22nd character of string = o	6F	01101111
30	1E	23rd character of string = r	72	01110010
31	1F	24th character of string = <space>	20	00100000
32	20	25th character of string = n	6E	01101110
33	21	26th character of string = a	61	01100001
34	22	27th character of string = m	6D	01101101
35	23	28th character of string = e	65	01100101
36	24	29th character of string = <new line>	0A	00001010
37	25	30th character of string = <space>	20	00100000
38	26	31st character of string = <space>	20	00100000
39	27	32nd character of string = <space>	20	00100000
40	28	Serial number string - 16 bytes: “XY1234500” 1st character of string = X	58	01011000
41	29	2nd character of string = Y	59	01011001
42	2A	3rd character of string = 1	31	00110001
43	2B	4th character of string = 2	32	00110010
44	2C	5th character of string = 3	33	00110011
45	2D	6th character of string = 4	34	00110100
46	2E	7th character of string = 5	35	00110101
47	2F	8th character of string = 0	30	00110000
48	30	9th character of string = 0	30	00110000
49	31	10th character of string = <new line>	0A	00001010
50	32	11th character of string = <space>	20	00100000
51	33	12th character of string = <space>	20	00100000
52	34	13th character of string = <space>	20	00100000
53	35	14th character of string = <space>	20	00100000
54	36	15th character of string = <space>	20	00100000
55	37	16th character of string = <space>	20	00100000
56	38	Unused - 8 bytes: *set to 20h*	20	00100000
57	39		20	00100000
58	3A		20	00100000
59	3B		20	00100000
60	3C		20	00100000
61	3D		20	00100000
62	3E		20	00100000
63	3F		20	00100000
64	40	Default physical interface = EVC (no secondary interface)	40	01000000
65	41	Default video interface = Analog (no secondary interface)	10	00010000

Byte# (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
66	42	Default interface data format = Analog type (Table 4.10) Signal level .700V&.300V / Separate & Composite Syncs Supported	0C	00001100
67	43	Default interface - no direct pixel clock support	00	00000000
68	44	Default interface reserved - set to 0	00	00000000
69	45	Default interface reserved - set to 0	00	00000000
70	46	Secondary Interface = none	00	00000000
71	47		00	00000000
72	48		00	00000000
73	49		00	00000000
74	4A	Default color/luminance encoding = RGB (no secondary interface)	10	00010000
75	4B	R / G = 0 (unlimited bit depth)	00	00000000
76	4C	B / no subchannel 3 = 0	00	00000000
77	4D	No secondary interface	00	00000000
78	4E		00	00000000
79	4F	Display Technology type/subtype LCD/TFT	01	00000001
80	50	Major characteristics: color / not selectable chromaticity / not conditional update / normal landscape / not transparent background / desktop display	89	10001001
81	51	DPMS / stereo / standard color space	E0	11100000
82	52	No audio input / no Audio output / no video input	00	00000000
83	53	No additional features	00	00000000
84	54	Display response rise time 7 ns = $7*10^{-9}$ seconds	97	10010111
85	55	Display response fall time 1 ms = $1*10^{-3}$ seconds	31	00110001
86	56	White gamma =2.2 (2.2*100-100=120)	78	01111000
87	57	No additional gamma	FF	11111111
88	58		FF	11111111
89	59		FF	11111111
90	5A	Max luminance 150 cd/m^2 *1500 = 5DCh*	DC	11011100
91	5B		05	00000101
92	5C	Standard RGB / adjustable gamma / offset positive	80	10000000
93	5D	Offset value=0	00	00000000
94	5E	Red/Green low bits	F4	11110100
95	5F	Blue/White low bits	B2	10110010
96	60	Red x= 0.628	A0	10100000
97	61	Red y= 0.335	55	01010101
98	62	Green x = 0.290	4A	01001010
99	63	Green y= 0.605	9B	10011011
100	64	Blue x= 0.150	26	00100110
101	65	Blue y= 0.065	10	00010000
102	66	White x = 0.281	48	01001000
103	67	White y = 0.311	4F	01001111
104	68	No additional gammas or color points set values = 0	00	00000000
105	69		00	00000000
106	6A		00	00000000
107	6B		00	00000000
108	6C		00	00000000
109	6D		00	00000000
110	6E		00	00000000

Byte# (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
111	6F		00	00000000
112	70		00	00000000
113	71		00	00000000
114	72	Max horizontal image size 316mm	3C	00111100
115	73		01	00000001
116	74	Max vertical image size 237 mm	ED	11101101
117	75		00	00000000
118	76	Max horizontal addressibility =1280	00	00000000
119	77		05	00000101
120	78	Max vertical addressibility =1024	00	00000000
121	79		04	00000100
122	7A	Horizontal pixel pitch = 0.242 mm	18	00011000
123	7B	Vertical pixel pitch = 0.14 mm	0E	00001110
124	7C	Unused	00	00000000
125	7D	GTF not supported	00	00000000
126	7E	No extension, no gamma table, 1 range limits	04	00000100
127	7F	22 4-byte codes, no detailed timing	B0	10110000
128	80	Range Limits: Min frame rate = 55 HZ = 00001101 11b	0D	00001101
129	81	Max frame rate = 100 HZ = 00011001 00b	19	00011001
130	82	Min line rate = 31 KHZ = 00000111 11b	07	00000111
131	83	Max line rate = 82 KHZ = 00010100 10b	14	00010100
132	84	low bits 11 00 11 10	CE	11001110
133	85	Min Pixel Rate = 25MHz = 0000 00011001b	19	00011001
134	86	Max Pixel Rate = 150MHz = 0000 10010110b	96	10010110
135	87	Upper bits Min/Max Pixel rate = 0000 0000b	00	00000000
136	88	4-byte timing -active pixels 1280 (1280-256)/16 = 64	40	01000000
137	89	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
138	8A	H:V 5:4 125:100	7D	01111101
139	8B	Refresh rate 75Hz	4B	01001011
140	8C	4-byte timing -active pixels 1280 (1280-256)/16 = 64	40	01000000
141	8D	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
142	8E	H:V 5:4 125:100	7D	01111101
143	8F	Refresh rate 60Hz	3C	00111100
144	90	4-byte timing -active pixels 1280 (1280-256)/16 = 64	40	01000000
145	91	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
146	92	H:V 4:3 133:100	85	10000101
147	93	Refresh rate 60Hz	3C	00111100
148	94	4-byte timing -active pixels 1152 (1152-256)/16 = 56	38	00111000
149	95	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
150	96	H:V 1152:870 132:100	84	10000100
151	97	Refresh rate 75Hz	4B	01001011
152	98	4-byte timing -active pixels 1152 (1152-256)/16 = 56	38	00111000
153	99	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
154	9A	H:V 4:3 133:100	85	10000101
155	9B	Refresh rate 85Hz	55	01010101

Byte# (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
156	9C	4-byte timing -active pixels 1024 (1024-256)/16 = 48	30	00110000
157	9D	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
158	9E	H:V 4:3 133:100	85	10000101
159	9F	Refresh rate 85Hz	55	01010101
160	A0	4-byte timing -active pixels 1024 (1024-256)/16 = 48	30	00110000
161	A1	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
162	A2	H:V 4:3 133:100	85	10000101
163	A3	Refresh rate 75Hz	4B	01001011
164	A4	4-byte timing -active pixels 1024 (1024-256)/16 = 48	30	00110000
165	A5	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
166	A6	H:V 4:3 133:100	85	10000101
167	A7	Refresh rate 70Hz	46	01000110
168	A8	4-byte timing -active pixels 1024 (1024-256)/16 = 48	30	00110000
169	A9	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
170	AA	H:V 4:3 133:100	85	10000101
171	AB	Refresh rate 60Hz	3C	00111100
172	AC	4-byte timing -active pixels 1024 (1024-256)/16 = 48	30	00110000
173	AD	Landscape / no stereo / no reduced blanking / interlaced / LP=0, FLM=0 / SHF=0	40	01000000
174	AE	H:V 4:3 133:100	85	10000101
175	AF	Refresh rate 87Hz	57	01010111
176	B0	4-byte timing -active pixels 832 (832-256)/16 = 36	24	00100100
177	B1	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
178	B2	H:V 4:3 133:100	85	10000101
179	B3	Refresh rate 75Hz	4B	01001011
180	B4	4-byte timing -active pixels 800 (800-256)/16 = 34	22	00100010
181	B5	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
182	B6	H:V 4:3 133:100	85	10000101
183	B7	Refresh rate 85Hz	55	01010101
184	B8	4-byte timing -active pixels 800 (800-256)/16 = 34	22	00100010
185	B9	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
186	BA	H:V 4:3 133:100	85	10000101
187	BB	Refresh rate 75Hz	4B	01001011
188	BC	4-byte timing -active pixels 800 (800-256)/16 = 34	22	00100010
189	BD	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
190	BE	H:V 4:3 133:100	85	10000101
191	BF	Refresh rate 72Hz	48	01001000
192	C0	4-byte timing -active pixels 800 (800-256)/16 = 34	22	00100010
193	C1	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
194	C2	H:V 4:3 133:100	85	10000101
195	C3	Refresh rate 60Hz	3C	00111100

Byte# (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
196	C4	4-byte timing -active pixels 800 (800-256)/16 = 34	22	00100010
197	C5	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
198	C6	H:V 4:3 133:100	85	10000101
199	C7	Refresh rate 56Hz	38	00111000
200	C8	4-byte timing -active pixels 640 ((640-256)/16 = 24	18	00011000
201	C9	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
202	CA	H:V 4:3 133:100	85	10000101
203	CB	Refresh rate 85Hz	55	01010101
204	CC	4-byte timing -active pixels 640 ((640-256)/16 = 24	18	00011000
205	CD	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
206	CE	H:V 4:3 133:100	85	10000101
207	CF	Refresh rate 75Hz	4B	01001011
208	D0	4-byte timing -active pixels 640 ((640-256)/16 = 24	18	00011000
209	D1	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
210	D2	H:V 4:3 133:100	85	10000101
211	D3	Refresh rate 72Hz	48	01001000
212	D4	4-byte timing -active pixels 640 ((640-256)/16 = 24	18	00011000
213	D5	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
214	D6	H:V 4:3 133:100	85	10000101
215	D7	Refresh rate 67Hz	43	01000011
216	D8	4-byte timing -active pixels 640 ((640-256)/16 = 24	18	00011000
217	D9	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
218	DA	H:V 4:3 133:100	85	10000101
219	DB	Refresh rate 60Hz	3C	00111100
220	DC	4-byte timing -active pixels 720 (720-256)/16 = 29	1D	00011101
221	DD	Landscape / no stereo / no reduced blanking / not interlaced / LP=0, FLM=0 / SHF=0	00	00000000
222	DE	H:V 9:5 180:100	B4	10110100
223	DF	Refresh rate 70Hz	46	01000110
224	E0	Unused - fill with 00h	00	00000000
225	E1		00	00000000
226	E2		00	00000000
227	E3		00	00000000
228	E4		00	00000000
229	E5		00	00000000
230	E6		00	00000000
231	E7		00	00000000
232	E8		00	00000000
233	E9		00	00000000
234	EA		00	00000000
235	EB		00	00000000
236	EC		00	00000000
237	ED		00	00000000
238	EE		00	00000000

Byte# (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
239	EF		00	00000000
240	F0		00	00000000
241	F1		00	00000000
242	F2		00	00000000
243	F3		00	00000000
244	F4		00	00000000
245	F5		00	00000000
246	F6		00	00000000
247	F7		00	00000000
248	F8		00	00000000
259	F9		00	00000000
250	FA		00	00000000
251	FB		00	00000000
252	FC		00	00000000
253	FD		00	00000000
254	FE		00	00000000
255	FF	Checksum	C2	11000010

7.4 Version 2 Revision 0 data structure format for DSTN display using TMDS interface

This sample EDID is included for illustration only, it should not be considered as representative of any particular display.

Note: Many existing DSTN displays require special consideration for vertical blanking parameters. This sample EDID provides the following conventions. The number of lines required at the end of an image is specifed as the vertical front porch. At least one additional line is used for vertical sync. Vertical back porch and vertical borders are typically set to 0.

Byte # (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
0	00	EDID Structure version 2 revision 0	20	00100000
1	01	EISA manufacture code =HIT	21	00100001
2	02	(Compressed ASCII)	34	00110100
3	03	Product code =1750	D6	11010110
4	04	(Hex, LSB First)	06	00000110
5	05	Week of manufacture =22	16	00010110
6	06	Year of manufacture =1997 = 07CDh	CD	11001101
7	07		07	00000111
8	08	Manufacturer's ID string - 32 bytes: "Hitachi LCD DSTN Panel" 1st character of string = H	48	01001000
9	09	2nd character of string = i	69	01101001
10	0A	3rd character of string = t	74	01110100
11	0B	4th character of string = a	61	01100001
12	0C	5th character of string = c	63	01100011
13	0D	6th character of string = h	68	01101000
14	0E	7th character of string = i	69	01101001
15	0F	8th character of string = <tab>	09	00001001
16	10	9th character of string = L	4C	01001100
17	11	10th character of string = C	43	01000011

Byte # (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
18	12	11th character of string = D	44	01000100
19	13	12th character of string = <space>	20	00100000
20	14	13th character of string = D	44	01000100
21	15	14th character of string = S	53	01010011
22	16	15th character of string = T	54	01010100
23	17	16th character of string = N	4E	01001110
24	18	17th character of string = <space>	20	00100000
25	19	18th character of string = P	50	01010000
26	1A	19th character of string = a	61	01100001
27	1B	20th character of string = n	6E	01101110
28	1C	21st character of string = e	65	01100101
29	1D	22nd character of string = l	6C	01101100
30	1E	23rd character of string = <new line>	0A	00001010
31	1F	24th character of string = <space>	20	00100000
32	20	25th character of string = <space>	20	00100000
33	21	26th character of string = <space>	20	00100000
34	22	27th character of string = <space>	20	00100000
35	23	28th character of string = <space>	20	00100000
36	24	29th character of string = <space>	20	00100000
37	25	30th character of string = <space>	20	00100000
38	26	31st character of string = <space>	20	00100000
39	27	32nd character of string = <space>	20	00100000
40	28	Serial number string - 16 bytes: “SX31S003” 1st character of string = S	53	01010011
41	29	2nd character of string = X	58	01011000
42	2A	3rd character of string = 3	33	00110011
43	2B	4th character of string = 1	31	00110001
44	2C	5th character of string = S	53	01010011
45	2D	6th character of string = 0	30	00110000
46	2E	7th character of string = 0	30	00110000
47	2F	8th character of string = 3	33	00110011
48	30	9th character of string = <new line>	0A	00001010
49	31	10th character of string = <space>	20	00100000
50	32	11th character of string = <space>	20	00100000
51	33	12th character of string = <space>	20	00100000
52	34	13th character of string = <space>	20	00100000
53	35	14th character of string = <space>	20	00100000
54	36	15th character of string = <space>	20	00100000
55	37	16th character of string = <space>	20	00100000
56	38	Unused - 8 bytes: set to 20h	20	00100000
57	39	set to 20h	20	00100000
58	3A		20	00100000
59	3B		20	00100000
60	3C		20	00100000
61	3D		20	00100000
62	3E		20	00100000
63	3F		20	00100000
64	40	Default physical interface, P&D-D	50	01010000
65	41	Video interface:TMDS	30	00110000

Byte # (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
66	42	Digital data interface,	60	01100000
67	43	Default interface minimum channel speed = 25MHz	19	00011001
68	44	Default interface maximum speed = 47MHz	2F	00101111
69	45	Digital data format = 8/8 bit RGB DSTN	15	00010101
70	46	Secondary Interface = none	00	00000000
71	47		00	00000000
72	48		00	00000000
73	49		00	00000000
74	4A	Default color/luminance encoding = RGB (no secondary interface)	10	00010000
75	4B	R=1/G=1	11	00010001
76	4C	B=1 / no subchannel 3 = 0	10	00010000
77	4D	No secondary interface	00	00000000
78	4E		00	00000000
79	4F	Display Technology type/subtype LCD/DSTN	11	00010001
80	50	Major characteristics: color / not selectable chromaticity / not conditional update / normal landscape / not transparent background / desktop display	89	10001001
81	51	DPMS / stereo / standard color space	E0	11100000
82	52	No audio input / no Audio output / no video input	00	00000000
83	53	No additional features	00	00000000
84	54	Display response rise time 90ms	29	00101001
85	55	Display response fall time 60 ms	26	00100110
86	56	White gamma =2.2 (2.2*100-100=120)	78	01111000
87	57	No additional gamma	FF	11111111
88	58		FF	11111111
89	59		FF	11111111
90	5A	Max luminance 70 cd/m^2	BC	10111100
91	5B	700 = 02BCh	02	00000010
92	5C	Standard RGB / fixed gamma / offset positive	80	10000000
93	5D	Offset value=0	00	00000000
94	5E	Red/Green low bits	AF	10101111
95	5F	Blue/White low bits	A1	10100001
96	60	Red x= 0.51	82	10000010
97	61	Red y= 0.33	54	01010100
98	62	Green x = 0.30	4C	01001100
99	63	Green y= 0.53	87	10000111
100	64	Blue x= 0.17	2B	00101011
101	65	Blue y= 0.17	2B	00101011
102	66	White x = 0.27	45	01000101
103	67	White y = 0.31	4F	01001111
104	68	No additional gammas or color points, set values = 0	00	00000000
105	69		00	00000000
106	6A		00	00000000
107	6B		00	00000000
108	6C		00	00000000
109	6D		00	00000000
110	6E		00	00000000
111	6F		00	00000000

Byte # (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
112	70		00	00000000
113	71		00	00000000
114	72	Max horizontal image size 246mm	F6	11110110
115	73		00	00000000
116	74	Max vertical image size 184.5=184 mm	B8	10111000
117	75		00	00000000
118	76	Max horizontal addressibility =800	20	00100000
119	77		03	00000011
120	78	Max vertical addressibility =600	58	01011000
121	79		02	00000010
122	7A	Horizontal pixel pitch = 0.3075=0.31 mm	1F	00011111
123	7B	Vertical pixel pitch = 03075=0.31 mm	1F	00011111
124	7C	Unused	00	00000000
125	7D	GTF not supported	00	00000000
126	7E	No extensions, no gamma table, 1 range limit, 1detailed limit	05	00000101
127	7F	no 4-byte code, no detailed timing	00	00001000
128	80	Min frame rate = 120Hz	1E	00011110
129	81	Max frame rate = 180Hz	2D	00101101
130	82	Min line rate = 36.6kHz = 37	09	00001001
131	83	Max line rate = 54.9kHz = 55	0D	00001101
132	84	Low bits frame/line = 00 00 / 01 11	07	00000111
133	85	Min pixel rate = 31MHz	1F	00011111
134	86	Max pixel rate = 46.55MHz=47	2F	00101111
135	87	Upper bits min pixel rate / max pixel rate	00	00000000
136	88	Detailed timing range; min pixel clock = 38.79MHz = 3879 = 0F27h	27	00100111
137	89		0F	00001111
138	8A	Min horz blanking = 48 pixels	30	00110000
139	8B	Min vertical blanking = 5 lines	05	00000101
140	8C	Min horz / vert upper bits = 0/0	00	00000000
141	8D	Min horz sync offset = 40 pixels	28	00101000
142	8E	Min horz sync width = 8 pixels	08	00001000
143	8F	Min vert sync offset/pulse width = 4/1	41	01000001
144	90	Upper bits of min horz & vert offset/sync	00	00000000
145	91	Max pixel clock = 38.79MHz = 3879	27	00100111
146	92		0F	00001111
147	93	Max horz blanking = 48 pixels	30	00110000
148	94	Max vertical blanking = 5 lines	05	00000101
149	95	Max horz / vert uper bits = 0/0	00	00000000
150	96	Max horz sync offset = 40 pixels	28	00101000
151	97	Max horz sync width = 8 pixels	08	00001000
152	98	Max vert sync offset/pulse width = 4/1	41	01000001
153	99	Upper bits of min horz & vert offset/sync	00	00000000
154	9A	Horz image size = 246mm	F6	11110110
155	9B	Vert image size = 184.5 = 184mm	B8	10111000
156	9C	Horz & Vert upper bits = 0	00	00000000
157	9D	Horz active pixels = 800 = 320h	20	00100000
158	9E	Vert active lines = 600 = 258h	58	01011000
159	9F	Horz & Vert active upper bits = 32h	32	00110010

Byte # (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
160	A0	Horz border = 0	00	00000000
161	A1	Vert border = 0	00	00000000
162	A2	Flags = nint,flm=0,lp=0	00	00000000
163	A3	Unused - fill with 00h	00	00000000
164	A4		00	00000000
165	A5		00	00000000
166	A6		00	00000000
167	A7		00	00000000
168	A8		00	00000000
169	A9		00	00000000
170	AA		00	00000000
171	AB		00	00000000
172	AC		00	00000000
173	AD		00	00000000
174	AE		00	00000000
175	AF		00	00000000
176	B0		00	00000000
177	B1		00	00000000
178	B2		00	00000000
179	B3		00	00000000
180	B4		00	00000000
181	B5		00	00000000
182	B6		00	00000000
183	B7		00	00000000
184	B8		00	00000000
185	B9		00	00000000
186	BA		00	00000000
187	BB		00	00000000
188	BC		00	00000000
189	BD		00	00000000
190	BE		00	00000000
191	BF		00	00000000
192	C0		00	00000000
193	C1		00	00000000
194	C2		00	00000000
195	C3		00	00000000
196	C4		00	00000000
197	C5		00	00000000
198	C6		00	00000000
199	C7		00	00000000
200	C8		00	00000000
201	C9		00	00000000
202	CA		00	00000000
203	CB		00	00000000
204	CC		00	00000000
205	CD		00	00000000
206	CE		00	00000000
207	CF		00	00000000
208	D0		00	00000000

Byte # (decimal)	Byte # (hex)	Field Name and *Comments*	Value (hex)	Value (binary)
209	D1		00	00000000
210	D2		00	00000000
211	D3		00	00000000
212	D4		00	00000000
213	D5		00	00000000
214	D6		00	00000000
215	D7		00	00000000
216	D8		00	00000000
217	D9		00	00000000
218	DA		00	00000000
219	DB		00	00000000
220	DC		00	00000000
221	DD		00	00000000
222	DE		00	00000000
223	DF		00	00000000
224	E0		00	00000000
225	E1		00	00000000
226	E2		00	00000000
227	E3		00	00000000
228	E4		00	00000000
229	E5		00	00000000
230	E6		00	00000000
231	E7		00	00000000
232	E8		00	00000000
233	E9		00	00000000
234	EA		00	00000000
235	EB		00	00000000
236	EC		00	00000000
237	ED		00	00000000
238	EE		00	00000000
239	EF		00	00000000
240	F0		00	00000000
241	F1		00	00000000
242	F2		00	00000000
243	F3		00	00000000
244	F4		00	00000000
245	F5		00	00000000
246	F6		00	00000000
247	F7		00	00000000
248	F8		00	00000000
249	F9		00	00000000
250	FA		00	00000000
251	FB		00	00000000
252	FC		00	00000000
253	FD		00	00000000
254	FE		00	00000000
255	FF	Checksum	B4	10110100

8. APPENDIX C - Answers To Commonly Asked Questions

Ref. #	Question	Answer
E1	What is relationship between EDID Version 1 Revision 0, EDID Version 1 Revision 1 and EDID Standard Version 2 Revision 0 ?	EDID standard document Version 2 Revision 0 contains definitions for 2 alternate data structures: a) EDID structure Ver 1 Rev 0 : This is the original data structure defined in DDC standard Version 1 Revision 0. b) EDID structure Ver 1 Rev 1 : This is a new data structure introduced in the EDID standard document Ver 2 Rev 0.
E2	What should 'ID Manufacturer Name' field contain?	Ref.: Sections 3.3 & 4.2.2 The registered EISA code for the manufacturer. EISA codes are now issued by Microsoft as part of their plug and play activity. Contact via e-mail : pnpid@microsoft.com Contact via fax : +1 206 936 7329 marked for attention of PNPID in Bldg. 27 Note: Previous versions of this standard made reference to BCPR as provider of this information. This is no longer correct. However, existing EISA ID codes issued by BCPR remain valid.
E3	What should the 'product code' field contain ?	Ref.: Sections 3.3 & 4.2.2 An identifier for the product type, e.g. the model number. Note that some s/w expects the combination of the 'manufacturer code' + the 'product code' to give an unique identifier.
E4	Table 3.16 Decode for Stereo Modes If bits 5 & 6 = 0 what should bit 0 equal ?	Ref.: Table 3.16 Bits 5 & 6 = 0 when there is no stereo image present. In this condition bit 0 should be set to 0, bit 0 =1 is reserved.
E5	3.9.1 Detailed Timing Description Is following true ? Horizontal sync offset = Horizontal front porch, if Horizontal border = 0	Ref.: Section 3.9.1 Yes
E6	3.9.2 Descriptor Description What is meaning of 'code page # 437' ?	Ref.: Section 3.9.2 ASCII has multiple code pages to allow for national language variations, code page # 437 corresponds to American English.
E7	Does 'Horizontal active pixel' = the total number of pixels on a horizontal line ?	Ref.: Sections 3.9.1 & 3.11 The horizontal component of timing consists of the Horizontal active + the Horizontal blanking periods.
E8	Is 'Image aspect ratio' = (Horizontal active pixel) / (Vertical active pixel) ?	Ref.: Section 3.8 Yes.
E9	If calculated aspect ratio is not 1:1, 4:3, 5:4 or 16:9 what should be used ?	Ref.: Section 3.8 Only applies to standard timings defined by VESA, all match except for 720x400
E10	How should VESA standard timings not listed in the 'established timings' section be handled?	Ref.: Section 3.7 The 'standard timing identification' fields (2 bytes each) provide for a coded way to identify timings not included in the 'established timings' section. It is also possible to fully describe a required timing in a 'detailed timing descriptor'.

Ref. #	Question	Answer
E11	If I want to use the 'standard timing identification' fields, where do I get the 'Horizontal active pixel' and 'image aspect ratio' for a particular timing ?	Ref.: Section 3.8 VESA timing standards include these parameters.
E12	If I want to use a 'detailed timing descriptor' block, where do I get the detailed information?	Ref.: Section 3.9 If it is a standard VESA timing then all the details are part of the standard. If it is a proprietary timing then details need to be established by the developer.
E13	Section 3.7 Established Timing Section says "... one-bit flags and are used to indicate support for established VESA and other common timings ..." Does 'support' mean that the mode is pre-set in the monitor or that monitor is capable of handling the mode ?	Ref.: Section 3.7 Different manufacturers have applied different interpretations, it appears that most define "support" to mean that the monitor is capable of handling the mode but may require user adjustment of image size, centering, etc.
E14	3.9.2 Descriptor Description, Definition # 5 Color Point "An index number of 00h means that no color data follows" Does this mean that only white gamma follows or neither white chromaticity and gamma follow ?	Ref.: Section 3.9.2 An index value = 00h means that neither white chromaticity nor white gamma values follow.
E15	Ref. as E14 What binary index value should the white point index start from ? Arbitrary ?	Ref.: Section 3.9.2 It is arbitrary and left to individual manufacturers. However, there is white color and gamma data stored in bytes 24 - 27 (decimal) with no explicit index number. Implementers may wish to assume that this is an implicit index number of 1 and hence the explicit index numbers in a descriptor block should start at 2.
E16	Ref. as E14 How many color point monitor descriptors are allowed ? One or up to four ?	Ref.: Section 3.9.2 Up to four. There are no restrictions on the number of blocks that may be redefined to a particular type of descriptor.
E17	What is the most reliable way for a graphic sub-system to determine the operating range of the attached monitor ?	Ref.: Sections 3.9.2 & 4.4 For EDID structure Version 1 it is recommended that the Monitor Range Limit Descriptor (if provided) be used. For EDID structure Version 2 range limits can be expressed using the fields defined in Section 4.4.1 or 4.4.2 Monitor operating range limits cannot be reliably inferred from any other source within the EDID.