VESA®

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VESA Standard:
Enhanced Video Connector (P&D-A)
(formerly EVC)
Pinout and Signal Standards

Version 2, Revision 1
Date: July 13, 1998

Purpose:

To establish a standard video output connector for personal computers, workstations, and similar products, including the ability to support high-frequency video signals and including ”multimedia” and other signals expected to be required in future computer displays.

Background and Summary:

To date, the computer display industry has relied on several different video output connector schemes, none of which adequately address the need for a small, low-cost system providing support for a number of different signals relating to the human interface system. This document establishes standards for a connector pinout and the related signals in order to address these needs and provide superior performance over what was possible with earlier systems.

This revision of the Enhanced Video Connector standard incorporates the abbreviation change from EVC to P&D-A in accordance with the VESA Display Committee. This change is to assist in the understanding that the Enhanced Video Connector is part of the family of Plug & Display connectors. All changes have been enumerated on the last page of the document.

1. General Information and Intent of Standard

The VESA Enhanced Video Connector standard is intended to provide a new standard for the host/display interface for personal computers, workstations, and similar applications. This is achieved by providing a new standard video output connector and a set of supporting signal standards. The goal of these standards is a next-generation display interface providing improved video performance, support for a large range of additional features, and a reduction in the overall system cost and complexity.

1.1 Referenced Standards and Documents

Several standards are referenced by this document, and should be considered a part of its requirements. In the event of a conflict between this standard and any of the non-VESA standards listed below, the requirements of the other standard apply.

VESA Enhanced Video Connector (P&D-A) - Physical Connector Specifications, Version 2
VESA Display Data Channel (DDC) and Extended Display Identification Data (EDID) Standards, both Version 3
VESA Plug & Display Standard, Version 1
VESA Connector and Signal Standards for Stereoscopic Display Hardware, Ver. 1
ACCESS.bus Specifications (latest revision; Version 3.0 as of this writing)

ACCESS.bus Industry Group
370 Altair Way
Suite 215
Sunnyvale, CA 94086

Universal Serial Bus Specification (latest revision; Rev. 1.0 as of this writing).
Universal Serial Bus Specification , Copyright 1995, Compaq Computer Corporation, Digital Equipment Corporation, IBM PC Company, Intel Corporation, Microsoft Corporation, Northern Telecom.

IEEE-1394-1995 Standard

Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, NY 10017-2394, USA.

1.2 Intellectual Property

While every precaution has been taken in the preparation of this standard, the Video Electronics Standards Association and its contributors assume no responsibility for errors or omissions, and make no warranties, expressed or implied, of functionality or suitability for any purpose.

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1.4 Patents

VESA proposals and standards are adopted by the Video Electronics Standards Association without regard to whether their adoption may involve any patents or articles, materials, or processes. Such adoption does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the proposals or standards.

The connectors specified by this standard for the video output connector and the related cable connector are covered by one or more patents held by Molex, Incorporated. Molex has provided VESA with a statement regarding their licensing policies for these designs, in keeping with the established VESA policy regarding the use of patented technology in VESA standards. A copy of this statement is available from the VESA office.

1.5 Part Number References

Several connector part numbers are provided in this document, as a convenience to users of this standard. The listing of any such number or manufacturer's identification does not imply an endorsement or recommendation of that manufacturer or specific component type by the Video Electronics Standards Association or its member companies.

1.6 Support

Clarifications and application notes to support this standard may be available. To obtain the latest standard and any support documentation, contact the Video Electronics Standards Association.

If you have a product which incorporates the Enhanced Video Connector, you should ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarifications you may require regarding this standard. All questions, comments, or reported errors should be submitted in writing to VESA using one of the following methods:

- Fax to 1-408-435-8225 (San Jose, CA, USA); direct your fax to "Technical Support"
- E-mail to support@vesa.org
- Mail to:

  Technical Support
  Video Electronics Standards Association
  2150 North First Street, Suite 440
  San Jose, CA 95131-2029

1.7 Changes from Version 1 and Compatibility with Earlier P&D-A Implementations

This release of the VESA P&D-A standard represents a modification of this standard from the original Version 1 release of Nov. 1995. This new version has been made primarily for the purpose of making sure that the P&D-A standard is compatible with the newer VESA "Plug & Display" standard. Due to the requirements of the VP&D standard, some minor changes have had to be made in the P&D-A pinout and signal definitions to maintain this compatibility. This involves pins and features of the P&D-A which, as far as the VESA Monitor Committee has been able to determine at the time of this release, were not in use in any existing P&D-A implementation, specifically the charge power input and the return used for the USB interface. The changes from Version 1 to Version 2 may be summarized as follows:

1. The location of the "reserved" and "charge power" pins have been changed, in order to provide compatibility with the location of the charge power pins as defined under the P&D standard. In addition, the charge power feature has been redefined such that charge power is now provided as a single-ended supply, rather than the floating supply defined in P&D-A Version 1.
2. The return for the charge power supply is now on pin 18, where it is commoned with the optional IEEE-1394 shield connection. This was required to keep pin 7 (originally a reserved pin) defined as "unused", so that the use of this pin would not conflict with its usage under the VP&D standard.
3. The definition of the stereo sync signal (see Section 4.3) has been changed slightly to match that used in the VESA stereo connector standard ("Connector and Signal Standards for Stereoscopic Display Hardware").
4. The connector, PC layout, and panel cutout drawings shown in Section 2 have been updated per the current recommendations from the manufacturers of these connectors. Please note that these changes should not affect the interoperability between connectors used under this revision of the standard and earlier P&D-A implementations.
5. Several sections have been changed to permit support of the "hot plugging" functionality as originally defined by the VESA Plug & Display standard. These involve the use of the "charge power" pins by VP&D compatible display devices, and how the system responds to this. Please see Section 6 for further information.

1.8 Compatibility Between P&D-A Version 3 and the VESA Plug & Display Standard (VP&D)

As noted above, the primary reason for this change to the VESA P&D-A standard is to provide compatibility with the VESA Plug & Display standard. The VP&D standard provides definitions for signals and standard connectors to be used for the

support of both analog-interface and digital-interface displays in a single connection (the VESA P&D-A/D connector), or for a compatible connector intended for the support of digital-interface monitors only. Within this family of standards, the P&D-A now becomes the connector of choice for those systems intending to provide analog video support ONLY. As the connectors defined under P&D were intended to provide a high degree of compatibility with P&D-A, P&D-A-equipped analog-input monitors can be used on hosts providing *either* P&D-A or P&D-A/D receptacles. However, as the original P&D-A standard was developed prior to P&D, some features supported on P&D-A will be unavailable on systems equipped with the P&D-A/D receptacle. Compatibility between the P&D-A and P&D standards may be summarized as follows:

1. The analog video outputs, the pixel clock output associated with the analog interface, the separate sync signals associated with the analog outputs (including the stereo sync signal), and the USB and IEEE-1394 signals are located on the same pins on the P&D-A/D connector as on P&D-A, and so these features will be available to all monitors connecting to either host receptacle. For this reason, the preferred plug (the connector at the host end of the video cable) for all analog-input monitors remains P&D-A, for use with both P&D-A and P&D-A/D hosts.
2. The analog audio I/O channels and the analog video (Y/C) video input supported on P&D-A are not available on the P&D-A/D receptacle. These pins have been redefined under the P&D standard to support the digital monitor interface provided on the P&D connectors. Analog monitors using the P&D-A and which support these analog channels will not be damaged if connected to a P&D host, but the analog audio I/O and video inputs will not be usable. As a P&D-equipped host will be able to determine monitor support for these features via the EDID data available over the VESA Display Data Channel (DDC) interface, the user may be informed by the system that these features will not be supported.
3. The “hot plugging” feature first defined by the VP&D standard and now included here in the P&D-A standard will, of course, not be supported by monitors or systems implementing P&D-A under the earlier Version 1 P&D-A standard.
4. Digital-interface monitors using the P&D connectors cannot be connected to a P&D-A host; the physical design of the two connectors prevents this. Similarly, an analog-interface monitor using the P&D-A plug cannot be connected to a host using the P&D-D (digital only) connector. Note that EITHER type of monitor and plug may be connected to the P&D-A/D receptacle, which supports both analog and digital interfaces. In short, no monitor may be connected to a host which does not provide support for the type of interface required by that monitor. See Appendix B for further information.

1.9 Acknowledgements

This document is the result of the work of many people serving on the VESA Monitor Committee and that committee's Enhanced Video Connector Work Group. We would like to specifically thank the following individuals for their contributions of time and expertise toward the development of this standard, in both its original and latest release (in alphabetical order):

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Bob Myers
Hewlett-Packard Co.
EVC Workgroup Leader

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2. Pinout and General Physical Specifications

2.1 List of Signals

The basic P&D-A provides support for the following signals. Please note that throughout this standard, the terms ”input” and ”output” are intended to be taken with respect to the host system, e.g., audio INPUT refers to those signals being sent FROM the display connected to the P&D-A TO the host, while audio OUTPUT refers to audio signals provided FROM the host TO the display.

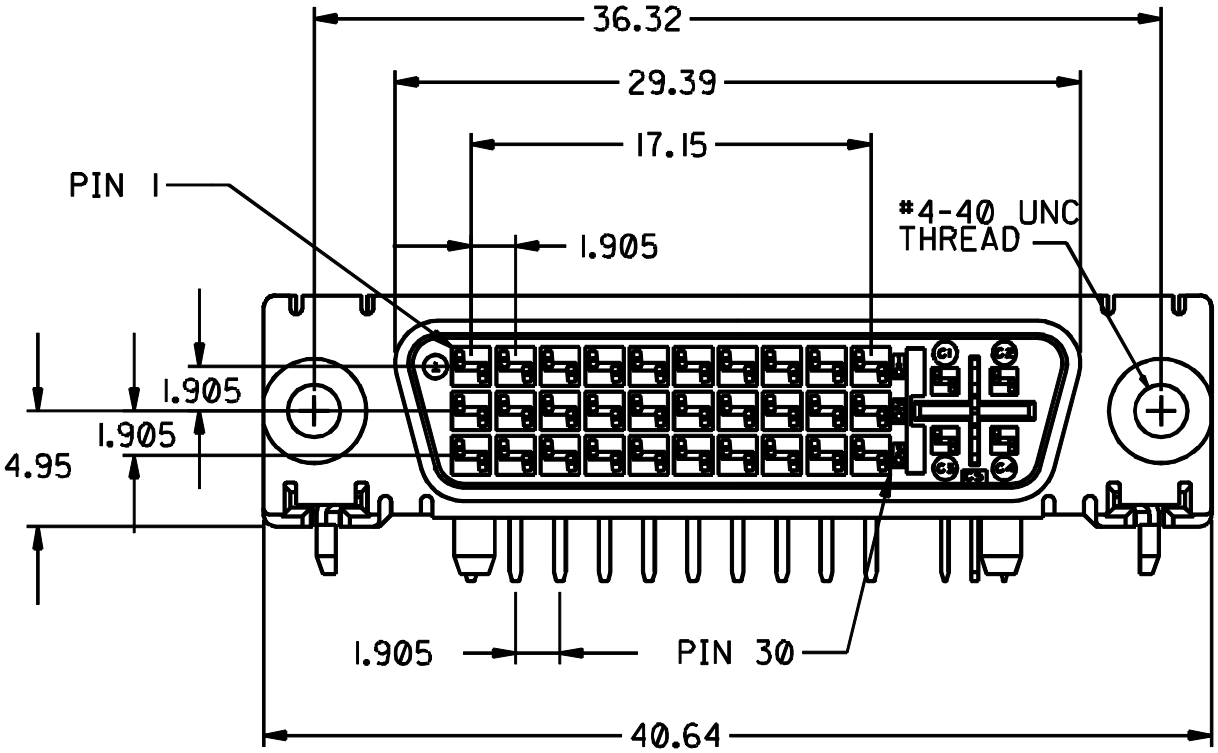
1. Analog video output - Red, Green, and Blue signals with a dedicated return.
2. TTL-level synchronization signals (horizontal and vertical sync) with a dedicated sync return.
3. Line-level audio output (from host to display); left and right channels with a dedicated audio output return.
4. Line-level audio input (from display to host); left and right channels with a dedicated audio input return.
5. The clock, data, and power connections required under the VESA Display Data Channel (DDC) Standard, plus a dedicated DDC return.
6. A pixel clock signal, with the pixel clock return shared with the video output signals’ return at the connector.
7. Analog video input signals, consisting of separate luminance (Y) and chrominance (C) signals.
8. A TTL-level signal for the synchronization of stereoscopic displays.
9. A pin for power to be supplied TO the host computer by the attached display or docking station. This power is intended for use by laptop and other portable computers so that they may obtain charging power via P&D-A.
10. A pair of connections to support the Universal Serial Bus (USB) data pair (power and ground for this interface are assumed to be shared as needed with the DDC connections above).
11. Those signals required for IEEE-1394-1995, a general-purpose, high-speed serial interface.

2.2 Connector Mechanical Specifications

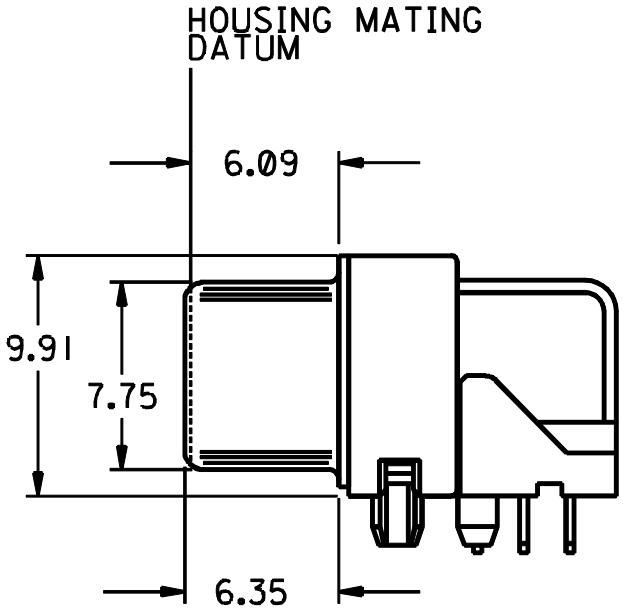
The connector (receptacle) used for the basic P&D-A as implemented on a host computer, graphics controller, monitor, or similar product shall be any of the following types or their equivalent. Note that the information given in this section is for reference only; the detailed mechanical specification of the connectors to be used under this standard may be found in a separate VESA standard, “Enhanced Video Connector - Physical Connector Specifications,” which in all cases takes precedence over the physical connector information given here.

1. Molex P/N SD-71182-**** or equivalent. (Note: the suffix for this part number depends on the specific version of the connector, e.g., through-hole vs. SMT, etc..)
2. JAE Electronics D30-R34W4 series or equivalent.

The physical dimensions (reference only) of the through-hole version of the connector, PC board (through-hole) layout, and recommended panel cutout are shown in the drawings on the following pages.



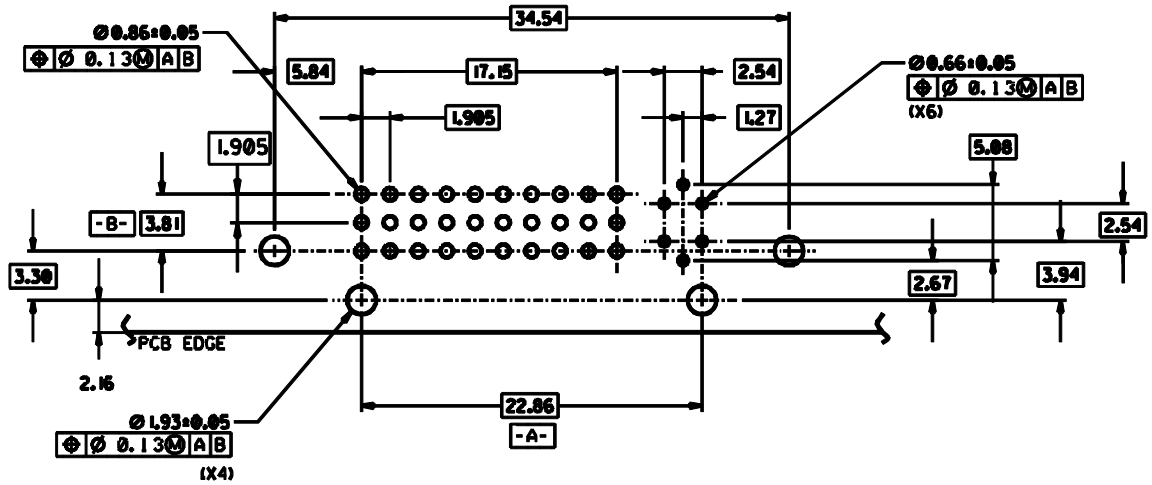
PC-mount receptacle, through-hole version, front view.



PC-mount receptacle, through-hole version, side view.

All dimensions given on this page are in
Do not scale any drawing on this page.

Note: All information given on this page is for reference only. For the detailed physical specifications of the connector, please refer to the VESA standard, ”Enhanced Video Connector - Physical Connector Specifications".

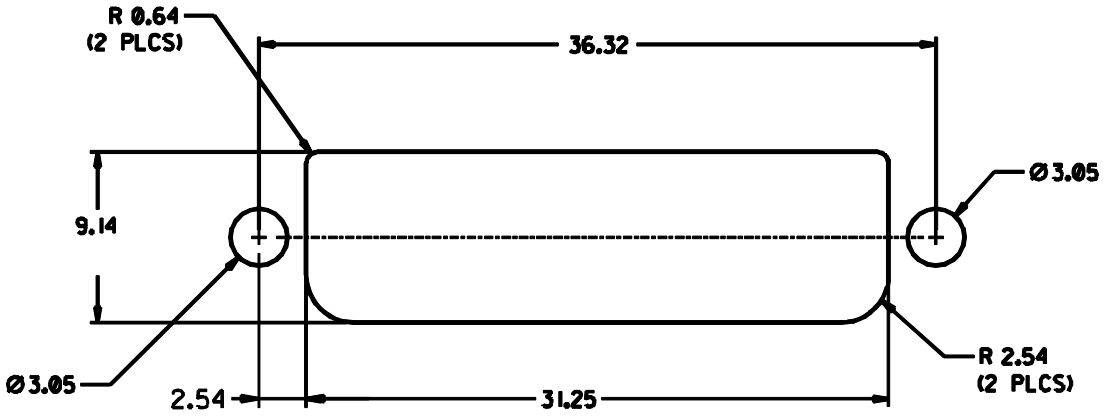


RECOMMENDED PCB LAYOUT

Recommended PC board layout (through-hole connector) component side.

All dimensions given on this page are in

Do not scale any drawing on this page.



PANEL CUT-OUT NOTES:

1. PANEL THICKNESS TO BE BETWEEN 0.76 AND 1.02.

Recommended panel cut-out.

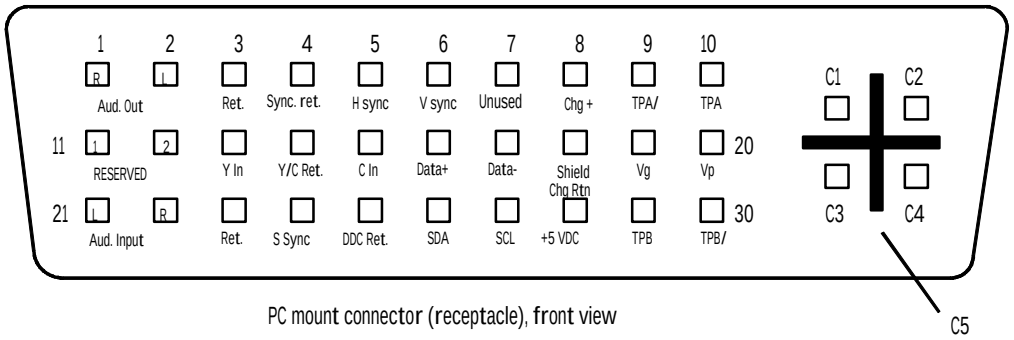
Note: All information given on this page is for reference only. For the detailed cal specifications of the connector, please refer to the VESA standard, “Enhanced Video Connector - Physical Connector Specifications".

2.3 Pinout

The signals supported by the P&D-A will be provided on the connector as shown below.

Note that the following signals are REQUIRED to be provided by the host in any implementation using the P&D-A: RGB analog video outputs and returns, horizontal and vertical sync. signals and return, DDC signals and return, +5 VDC.

NOTE: Throughout this list, ”in” and ”out” are defined with respect TO THE HOST COMPUTER. For example, the lines for ”audio input” are intended to carry audio signals TO the host from an external source. Similarly, ”audio output” carries audio signals FROM the host to an external device.



”MicroCross”/high-speed video pins:

C1	Red video out	C4	Blue video out
C2	Green video out	C5	Video/pixel clock return
C3	Pixel clock out		

Note: “C5” refers to either half of the crossed ground-plane structure, or the entire structure in the case of a mated connector pair. In this connector design, the vertical portion of this structure is provided by the receptacle (PCB-mount) connector, while the horizontal portion is provided by the plug (cable-end) connector. Note that this structure may connect to multiple physical pins in the PC board layout and/or the cable-side connection; please see the appropriate drawings in the connector physical specification standard for details.

Main pin field:

Pin	**Signal**	**Pin**	**Signal**
1	Audio output, Right	16	USB data+
2	Audio output, Left 17	USB data-	
3	Audio output return	18*	1394 shield (opt.l)**, & chg pwr rtrn
4	Sync return	19	1394 Vg
5	Horiz./Composite sync (TTL)	20	1394 Vp
6	Vertical sync (TTL)	21	Audio input, Left
7	Unused	22	Audio input, Right
8*	Charge power (Charge +)	23	Audio input return
9	1394 TPA*	24	Stereo sync (TTL)
10	1394 TPA	25	DDC return (opt. stereo rtn., see below)
11	RESERVED 1	26	DDC data (SDA)
12	RESERVED 2	27	DDC clock (SCL)
13	Video input, Y or composite in	28*	+5 VDC
14	Video input, return	29	1394 TPB
15	Video input, C in 30	1394 TPB*	

* - Pins 8 and 28 are recessed in the cable-end connector (plug), so as to provide for proper power/ground sequencing. The recessing of pin 18 is optional.

** - See note 5 in section 2.3.1, below.

2.3.1 Notes on the P&D-A Pinout

The pinout of the Enhanced Video Connector has been designed to maximize the performance of the signals provided and the ease of use of the connector. Specifically, please note the following:

1. The audio output signals (pins 1 and 2) are reversed (left vs. right) relative to the audio input signals on pins 21 and 22. This has been done to minimize the possibility of coupling or crosstalk between input and output pins of the same channel.
2. The video output (RGB) signals have been assigned to pins C1, C2, and C4 to provide for a simple PC layout with these signals all assigned to “outside” pins of the connector. This places the optional pixel clock signal on C3, and test data shows that this will not result in any significant noise problem for either the video signals or those in the main pin field.
3. Note that, in general, the slower, more noise-sensitive signals such as audio and analog video inputs have been assigned to pins located at the left end of the connector (in this view), with the expected frequency and noise-generation potential increasing in those signals assigned towards to right end of the connector. The “MicroCross” structure effectively isolates the video signals and the main pin field from each other, so this assignment strategy was felt to be the best for overall signal integrity on the P&D-A.
4. Control and identification of the display under this standard is supported through the VESA Display Data Channel (DDC) standard. There is no provision for the use of any of the other interfaces provided under P&D-A for the purposes of display identification and control.
5. Note that the IEEE-1394 internal cable bundle may need an outer shield to minimize internal crosstalk within the cable construction. The outer containment shield for the IEEE-1394 function will be provided by the overall cable shield. If the internal bundle shield for IEEE-1394 is required, this may be terminated to pin 18. It is recommended that this implementation be evaluated in the case where both the Charge Power return and the IEEE-1394 internal shield will be commoned to pin 18.
6. The VESA Plug and Display Standard has defined pin 25 as both the return for the DDC interface and for the stereo sync signal. This conflicts with the original version of the P&D-A standard, which assumed that the stereo sync line would use the same return as the separate horizontal and vertical TTL syncs (pin 4). As both pin 4 and pin 25 are expected to be connected to the common logic ground point in all implementations using either the P&D-A or P&D receptacles, use of either pin as the return for the stereo sync signal (at the manufacturer’s option) is permissible under this standard.
7. When a P&D-A monitor interface supporting analog audio and/or Y/C video is plugged into a P&D-A/D system interface it should be noted that there may be some low level feedback through the analog speakers or analog video device. The user should be made aware that the monitor features will not be supported in the case and advised to disable those functions. In any case if the Enhanced Video Connector Signal Standard and P&D standard are being followed, no damage to host or display will result.

2.4 Cable Requirements

The connector (plug) used to terminate cabling for connection to P&D-A-compliant products shall be any of the following: Molex SDA-71192-****, JAE D30-P34W4P-*** or equivalent. (Again, please note that the suffix for this part number depends on the specific type desired.)

Note: The physical specifications for this connector may be found in a separate VESA standard, ”Enhanced Video Connector - Physical Connector Specifications”.

2.5 Use of the P&D-A in Consumer/Video Applications

VESA recognizes that the P&D-A may be useful in applications which use display signals other than the RGB video typical of computer displays. For this reason, a ”video” configuration of the P&D-A has also been defined, as shown in the pinout definition. This replaces the RGB outputs with the following:

Red:	Baseband composite video (NTSC, PAL, or SECAM, for example)
Green:	Luminance (Y) output
Blue:	Chrominance (C) output.

2.5.1 **Displays and other devices using P&D-A-compatible connectors and intended for use with the ”video” configuration are to be identified by sensing the presence of a standard (75 ohms) load on the outputs listed above, per the following:**

Load on R,G, AND B:	**Normal RGB output desired**
Load on R ONLY:	**Provide composite video on R output.**
Load on G ONLY:	**Provide monochrome video on G output.**
Load on G AND B (no R):	**Provide Y/C video on G and B outputs**

2.5.2 **When either of the ”video” cases above is detected by the host, the host should provide the appropriate output signals and assume the standard timing (e.g., standard ”NTSC” video), until and unless a different format or timing is indicated by information provided in the display’s EDID information.**

3. Physical Compatibility and Labeling

3.1 Physical Compatibility

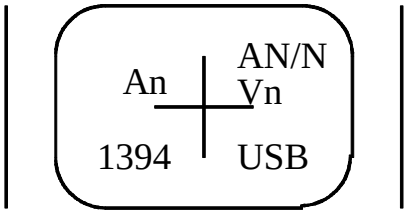
All implementations of P&D-A must be physically compatible with the standard connector as defined by this document. All implementations claiming P&D-A compatibility must be capable of physically mating to a standard P&D-A connector which supports the full P&D-A signal set, although it is permissible that contacts not be loaded for those signals not supported in a given implementation. Keying or otherwise restricting the connection ability or range of a connector claiming P&D-A compatibility is not permissible. Contact sequencing, achieved by staggering the contacts or any other means, is permissible as long as it does not impact the ability of the connector to mate with a standard P&D-A.

Note that the P&D-A connector as defined in this standard is also compatible with the VESA Plug and Display standard connector, in that P&D-A plugs will mate with any P&D receptacle which supports analog video outputs. For this reason, VESA expects all analog-input monitors to use the P&D-A plug, as this will be supported by either P&D-A or P&D receptacles on the host system. This compatibility is explained further in Appendix B of this document.

3.2 Labeling and Symbols for Indicating Signal Support

As of Version 2 of the P&D-A standard, the labeling to be used with this connector is intended to be compatible with that established as part of the VESA Plug & Display Standard. This labeling is intended to provide a clear indication of which interfaces are supported on a particular implementation using the P&D-A. The basic symbol is shown below:

This symbol is to be placed adjacent to an P&D-A receptacle, or molded into or otherwise provided on an P&D-A plug,



in order to provide the user with information regarding the interfaces support on this connector or cable.

Support for a given interface is indicated by the presence of the alphanumeric codes listed below, in the appropriate quadrant. If a given feature or interface is not supported, the corresponding quadrant shall be left blank.

3.2.1 **Upper Left Quadrant**

The information given here defines the type of analog video output provided in terms of the signal level standard(s) supported, as follows. Please see Section 4.1.1 for more information on these.

A1: RS-170 levels (1.0V blank-to-white, -0.4V sync pulses if provided)
A2: RS-343 levels (0.714V blank-to-white, -0.286V sync pulses if provided)
A3: “Euro” levels (0.700V blank-to-white, -0.300V sync pulses if provided)
A4: VESA signal standard (see Section 4.1 of this document)

NOTE: If multiple output level standards can be supported, this may be indicated by listing ALL of the corresponding number codes, e.g., “A23” would indicate support for both the “RS-343” output levels as well as the “Euro” levels.

3.2.2 **Upper Right Quadrant**

The information given here indicates the level of support provided for audio I/O and video input. The audio and video support indicators are given separately, with the audio information appearing above the video as shown in the examples. Note that this section is used to indicate digital video output support in the case of the P&D connector, where this information is preceded by a “D”.

Audio support (given in the form of N/N, where the first number indicates the level of INPUT support, while the second gives the level of output support):

A0: No support
A1: Mono
A2: Stereo

For example, “A0/2” would indicate a connector providing no audio input, but stereo audio output.

Video support:

Blank (no “Vn” label):
No support
V1: Video input, luminance (B/W) only
V2: Video input using NTSC color encoding
V3: Video input using PAL color encoding
V4: Video input using SECAM color encoding

NOTE: Any of V2 through V4 above should include a “C” suffix if this input is supported as a composite signal, rather than separate Y/C inputs. For example, “V2C” indicates support for NTSC composite-video input (using the “Y” input pin).

Again, support for multiple input standards may be indicated by using combinations of these numeric codes, for example “V23” to indicate support for both NTSC and PAL inputs.

3.2.3 Lower Left Quadrant

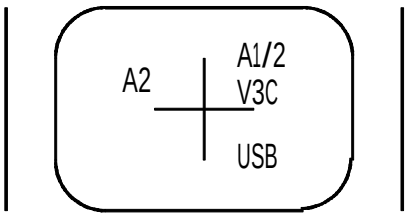
The presence of a “1394” label here indicates support for the IEEE-1394-1995 interface.

3.2.4 Lower Right Quadrant

The presence of a “USB” label here indicates support for the Universal Serial Bus.

3.2.5 Example

The following example shows the correct symbol/labeling to be used in the case of an P&D-A providing support for analog video outputs using the “RS-343” levels, monophonic audio input, stereo audio output, PAL composite video input support, no IEEE-1394 support, and with USB support:



4. Signal Specifications

4.1 Video Signals

The video signals provided by the P&D-A shall comply with the following requirements. Please note that this standard establishes a new VESA video signal standard which MAY be used if desired. Systems may continue to use the earlier signal standards while using the P&D-A, as long as support for the appropriate standard is identified by the display in the EDID information, and if the overall requirements for those signals under P&D-A are met.

4.1.1 Signal Amplitude and Polarity

All video signals provided by systems using the P&D-A shall be interpreted such that increasingly positive voltages in excess of the defined black level correspond to increasing luminance in the displayed image (i.e., the P&D-A shall always provide ”white-positive” video signals).

The signal amplitude standard expected by the display will be provided by that display via its EDID information, but must conform to one of the following standards:

	”RS-170”[1]	”RS-343”[1]	”Euro”	VESA
White (peak)[2]	+1.000 V	+0.714 V	+0.700 V	+0.700 VDC
Black[3]	+0.075 V	+0.054 V	+0.000 V**	+0.000 VDC
Blank	REFERENCE	REFERENCE	REFERENCE	+0.000 VDC
Sync tip[4]	-0.400 V	-0.286 V	-0.300 V	None

1 - - The terms ”RS-170” and ”RS-343” properly refer to two classes of former standards which were established by the Electronic Industries Association (EIA). As these terms have been commonly used within the computer display industry, they refer only to the signal level standards listed above. Refer to the standards themselves for the full definition of these signals.

2 - - White is defined as the peak signal level, excluding overshoot, ringing, noise, and similar transients, which is transmitted during the active video time, i.e., that period of the video signal exclusive of the blanking time.

3 - - Black is defined as the minimum signal level expected during the active video time. The RS-170 and RS-343 standards defined a difference between ”black” and ”blank”, known as ”setup”. Setup may be considered optional under these standards, but the display should communicate (via the EDID information) whether or not setup is expected.

4 - - The sync tip level refers to the signal amplitude defined for the case of sync-on-video. In systems providing sync on video, this information should appear only on the Green video signal except in the case where the Red, Green, and Blue signal outputs are being used to provide simultaneous monochrome outputs. Sync information shall not be provided on any video signal output when separate sync signals are in use. Sync-on-video may not be used when operating under the VESA video signal standard.

4.1.2 Reference Level

With the exception of the VESA video signal standard, the above-listed standards are intended for AC-coupled video inputs and use the blank level as the signal reference. The VESA video signal standard is intended for DC-coupled systems, and the reference point under this standard is the signal common as established by the return for the video signals (C5 on the P&D-A).

4.1.3 System Impedance

Any video output driver, display input, cabling, etc., used in an P&D-A-based system should be designed assuming a nominal impedance of 75 ohms for the video signal transmission system.

4.2 Synchronization Signals - VESA Video Signal Standard

Except as noted below, the following requirements shall apply to those systems employing the P&D-A AND using the VESA video signal standard.

4.2.1 Combining Synchronization and Video (Luminance) Signals

Video systems using the VESA video signal standard will not supply or use synchronization pulses combined with the luminance signals defined above (i.e., there shall be no ”sync-on-green” or equivalent systems). Synchronization signals must always be supplied to the display by means of separate, dedicated signal lines. NOTE: This should NOT be interpreted as meaning that composite sync or sync-on-green is not permissible on the P&D-A when other video standards are used.

4.2.2 Sync Signals Under the VESA Video Standard

Horizontal sync pulses must at all times continue to be supplied during the vertical sync pulse period. Under the VESA video signal standard, use of composite sync on either separate sync line is not permitted.

4.2.3 Synchronization Signal Levels and Tolerances

It is expected that the synchronization signals will be communicated using one or more standard logic family levels, and that strictly defining the expected signal levels for all cases is therefore beyond the scope of this standard. However, the following standard should be recognized for the specific cases of the TTL families.

Logic family:	TTL (all families)
Logic ”1” level:	min. 2.4V (driver); 2.0V (receiver)
Logic ”0” level:	max. 0.5V (driver); 0.8 V (receiver)

4.2.4 Termination of Synchronization Signal Lines; Loading

In the case of systems using the TTL logic levels as defined above, the standard termination presented on the synchronization lines by the display device shall be a nominal 2 kohms to +5 VDC.

4.2.5 Synchronization Signal Rise/Fall Time

The maximum rise/fall time of the synchronization signals, measured from the 20% to 80% levels, shall be 10 ns.

4.3 Stereo Synchronization

A signal for the synchronization of stereoscopic displays may optionally be provided on the P&D-A pin assigned in Section 2 of this standard. This signal shall meet the level, termination, and loading requirements as listed above, and shall be subject to the following additional requirements:

1. The stereo sync signal shall be a nominal 50% duty cycle square wave at one-half the vertical sync rate currently in use. The transitions of the stereo sync signal shall take place within three horizontal line times of the start of the vertical sync pulse, but in no case shall the stereo sync transition occur prior to the start of vertical blanking.
2. Unless otherwise specified by the EDID information, the sense of the stereo sync signal shall be that the signal is high (logical ”1” level) during that period corresponding to the left-eye field, and low during the right-eye field. An idle line in either state (where the line may be considered idle if more than three vertical sync pulses occur with no transition on the stereo sync line) shall be interpreted as meaning that stereoscopic display is no longer in use (the image being displayed is in the normal ”flat” mode).

4.4 Pixel Clock

The basic P&D-A connector provides support for a Pixel Clock output, intended for use by flat-panel based displays or similar systems which require such a clock to sample the video output signals. This pixel clock is not required to be present on the P&D-A unless some level of flat-panel support is intended, and may be enabled or disabled by the host depending on whether or not the display in question requests it via the display's EDID information. When provided, the clock output shall meet the following requirements, as measured at the P&D-A output pin and using a standard (75 ohm, +/- 1%) resistive termination connected as closely as possible to that point:

4.4.1 Signal Amplitude and Offset: The clock signal amplitude shall be 0.7 Vp-p, +/- 0.1 V. The signal shall have 0 VDC offset, meaning that the logical "0" portions of the signal shall be at 0.0 VDC (as defined by the signal ground, C5), with the logical "1" state at a nominal +0.7 V from this reference.

4.4.2 System impedance: 75 ohms nominal.

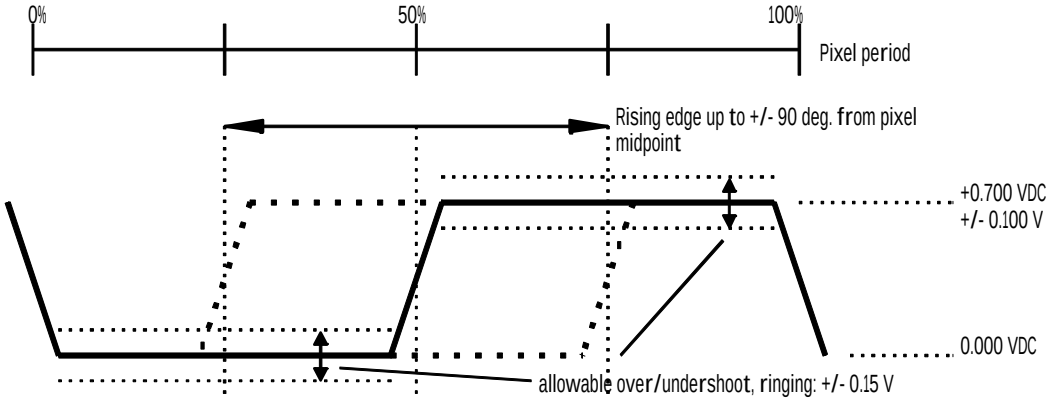
4.4.3 Active edge: It shall be standard that the active edge of the pixel clock (the edge on which the video signal is expected to be sampled) shall be the rising edge (i.e., the positive-going transition).

4.4.4 Skew: The skew of the pixel clock signal shall be controlled such that the 50% point of the rising edge of the clock occurs at the midpoint (50%) of the pixel period within the green video signal, plus or minus 90 degrees.

4.4.5 Rise/Fall Time: The rise time (positive-going transition) of the pixel clock signal, as measured between the 10% and 90% points, shall not be greater than 20% of the pixel period of the fastest pixel clock supported in this mode of operation. There is no specific requirement on the clock fall time, other than that it shall be sufficiently short so as to permit a low (logical "0") time (with the signal at or below 0.1V) of not less than 35% of the clock period.

4.4.6 Overshoot/Undershoot, Ringing: The overshoot, undershoot, and ringing of the pixel clock signal shall be controlled so that no portion of the clock signal falls outside of the range +/- 0.15V of the nominal amplitude for the high or low state following the rising or falling transition, respectively.

These requirements are summarized in the diagram below:



4.5 Audio Signals

All "Audio In" (from the display to the host) and "Audio Out" (from the host to the display) signals provided via the P&D-A are single-ended "line-level" signals which shall meet the following requirements:

4.5.1 Amplitude: Nominal 0.5V rms; maximum 2V rms.

4.5.2 Source impedance: Not more than 1 kohm.

4.5.3 Load impedance: Not less than 10 kohm.

4.5.4 Monophonic operation: If monophonic operation is desired, the channels should be used as follows:

1. External (outside the host) monophonic sources should be connected so as to feed only the LEFT input channel.
2. A monophonic source within the host should drive BOTH of the output channels.

4.6 Video Input

Video input (from the display to the host) may optionally be provided on the P&D-A using the pins assigned in section 2 of this standard. The format used shall be separate luminance (Y) and chrominance (C) signals which shall meet the following requirements, or composite video (e.g., per the NTSC, PAL, or SECAM encoding standards) on the Y input. It is the intention of VESA that this input be compatible with the signal definitions of consumer ”S-Video” when used with separate Y/C signals.

4.6.1 Signal amplitude, luminance (Y) signal: 1V p-p (from white level to tip of synchronizing pulses); white positive. If the Y input pin is used for composite video, the signal shall conform to the appropriate standard, but shall in no case exceed 2.0 Vp-p.

4.6.2 Signal amplitude, chrominance (C) signal: 286 mV p-p nominal if NTSC encoded; 300 mV p-p if PAL/SECAM encoded.

4.6.3 Impedance (source and load): 75 ohms nominal.

4.6.4 DC component: within 0 to +2.0 VDC for either Y or C signal.

4.6.5 Composite video: While the use of the Y input as a composite video input is permissible under this standard, host systems are not required to be capable of decoding composite color video on this line in order to be compliant with the standard. If the host system is not capable of decoding the video presented on this line, the video should be treated as a luminance signal.

4.7 Display Data Channel / ACCESS.bus

Support for the VESA Display Data Channel (DDC) standard, including support for the ACCESS.bus protocol, is provided on the P&D-A. The signal and power definitions of the DDC and ACCESS.bus standards shall apply in all cases.

NOTE: Identification of the display under this standard is supported only through the VESA Display Data Channel (DDC) standard. There is no provision for the use of any of the other interfaces provided under P&D-A for the purpose of display identification.

4.8 Charging Power Input

The charging power input is used by the host computer (typically a laptop or similar portable computer) as a source of charging power for its internal batteries, if any. Support for this input is optional and a host which has no need for charging power is not required to provide any connection or load on this line. Display devices and other products intended for connection TO a host-computer may provide charging power on this pin as desired. Note that, with the introduction of the VESA Plug & Display (VP&D) Standard, this pin is also used as part of the “hot plugging” support (permitting the host to detect disconnection of the display); the complete specifications regarding this feature are provided in section 6 of this standard, as well as in Section 3 of the VESA Plug & Display Standard. In terms of the use of this pin for charging power, the following restrictions apply:

4.8.1 Charging voltage: 18-20 VDC, referenced to charge power return pin (normally connected to the local ref. ground).

4.8.2 Current: Max. 1.5 A in the normal “full-on” state. The current available on this pin shall at all times be limited to not more than this value long-term, and not more than 5A for not more than 2 seconds. The device supplying power must be designed so that no damage or safety hazard occurs under any load condition, including a short to ground applied for an indefinite period of time.

4.8.3 Current control, default state, and loss of connection: The charging current shall at all times be under the control of the host device (the device being charged). The default (power-up) state for the charging supply shall be the trickle-charge state, as defined below. The charging supply is to be switched to the “full-on” state described above only upon detection of host connection via sensing the +5 VDC supply on pin 28 (any time the voltage present on this line exceeds + 2.0 VDC for a continuous period of not less than 10 us), or under the command of the host device via the DDC2 channel. The charging supply must also be designed so as to return to the trickle-charge state within 10 msec of disconnection, identified by loss of the +5V supply (pin 28) from the host (any time when the voltage on this line is less than +0.8 VDC for a continuous period of not less than 10 us).

4.8.4 Trickle charge current limit: In the ”trickle charge” state, which will be entered either under host control via a DDC2 command or upon disconnection from the host as described above, the charging current must not exceed 50 mA under any load condition.

4.8.5 Command set: The commands used to control the various states of the charging power connection shall be as defined in the VESA Monitor Command Set standard (under development as of this writing).

4.9 Universal Serial Bus (USB)

Support for the Universal Serial Bus (USB) is provided in the form of a pair of connections for the USB data pair. The USB interface will make use of the same power and ground connections as the DDC interface (+5 VDC on pin 28, ground on pin 25). All applicable requirements of the USB standard shall apply to this interface.

4.10 IEEE--1394--1995

Support for IEEE-1394-1995, a general-purpose, high-speed serial interface, is provided via pins 9, 10, 19, 20, 29, and 30. The IEEE-1394 internal cable bundle may need an outer shield to minimize internal crosstalk within the cable construction. The outer containment shield for the IEEE-1394 function will be provided by the overall cable shield. If the internal bundle shield for IEEE-1394 is required, this may be terminated to pin 18. It is recommended that this implementation be evaluated in the case where both the Charge Power return and the IEEE-1394 internal shield will be commoned to pin 18. Pin 18 is assigned as a common shield connection for both IEEE-1394 and USB. All applicable requirements of the IEEE-1394-1995 standard apply to this interface.

4.11 Power Output (+5 VDC)

All host devices (e.g., those supplying video output signals via the MicroCross section of P&D-A, and/or acting as the host under the DDC standard) using the P&D-A shall at all times provide a +5 VDC supply on pin 28, per the following specifications. This supply may be used by the USB or ACCESS.bus interfaces, and is also intended to provide power for minimal DDC support in the display device. In addition, displays or other peripheral devices connected to the P&D-A may use this line to indicate the connection of a powered-up host, as in section 4.8 above.

4.11.1 Voltage: +5.00 VDC, +/- 5%.

4.11.2 Current: This output must be capable of supplying not less than 300 mA for an indefinite period, but shall in all cases be limited to supplying not more than 1.5 A.

5. Intra-system Interconnect

As the P&D-A output connector provides support for a number of signals which may in some cases not be supplied or used by the board carrying the P&D-A itself, the following standard interconnect is required for use between that board and other boards within the host system, or between the board carrying the P&D-A and the system motherboard. It is required that any board intended for use in an expandable system and which carries an P&D-A provide this connector.

5.1 Connector Type

The connector used for this interconnect as provided by the graphics controller or other board carrying the P&D-A output connector shall be a 50 pin (2 rows of 25 pins each) 2mm x 2mm post type header, such as the following types or their equivalents:

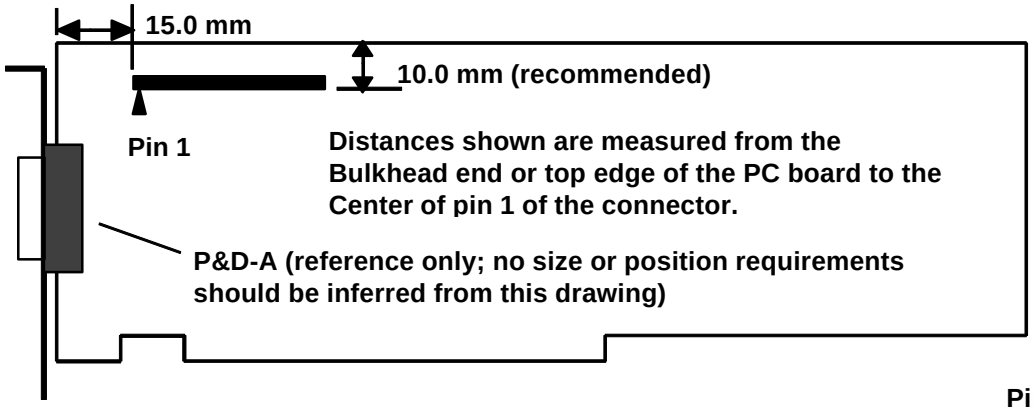
AMP AMPMODU 2mm family, 176264 Series (through-hole) or 84094 Series (SMT)
Molex “Milli-Grid” family, 87089 Series (through-hole) or 87267 Series (SMT)
Berg Electronics 88099-068 (through-hole) or 89100-029 (SMT).
Wearnes Hollingsworth 2690 series (straight through-hole) or 2691 series (rt. angle TH).

The use of multiple headers in place of the single 50 pin header is permissible, as long as pin position requirements are maintained (see Section 5.3).

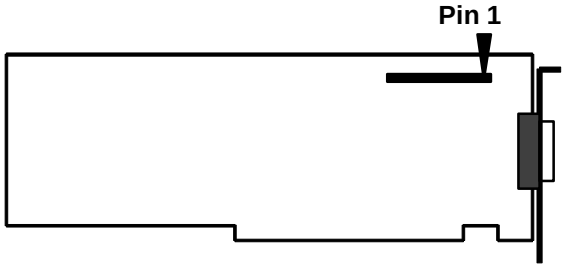
NOTE: This connector type permits the use of several smaller receptacles mating simultaneously with this single header. This is expected to be used by most manufacturers in providing, for example, a separate interconnect to the graphics controller from a sound card, carrying only the audio I/O signals. The recommended subdivision of the standard P&D-A interconnect is shown in the pinout diagram on the following page.

5.2 Connector Location

For PCI boards, the connector shall be located relative to the bulkhead end of the board as shown in the diagram below. Note that the location is fixed only along the long axis of the board; location of the connector vertically is left to the manufacturer’s discretion, although a recommended position is given.



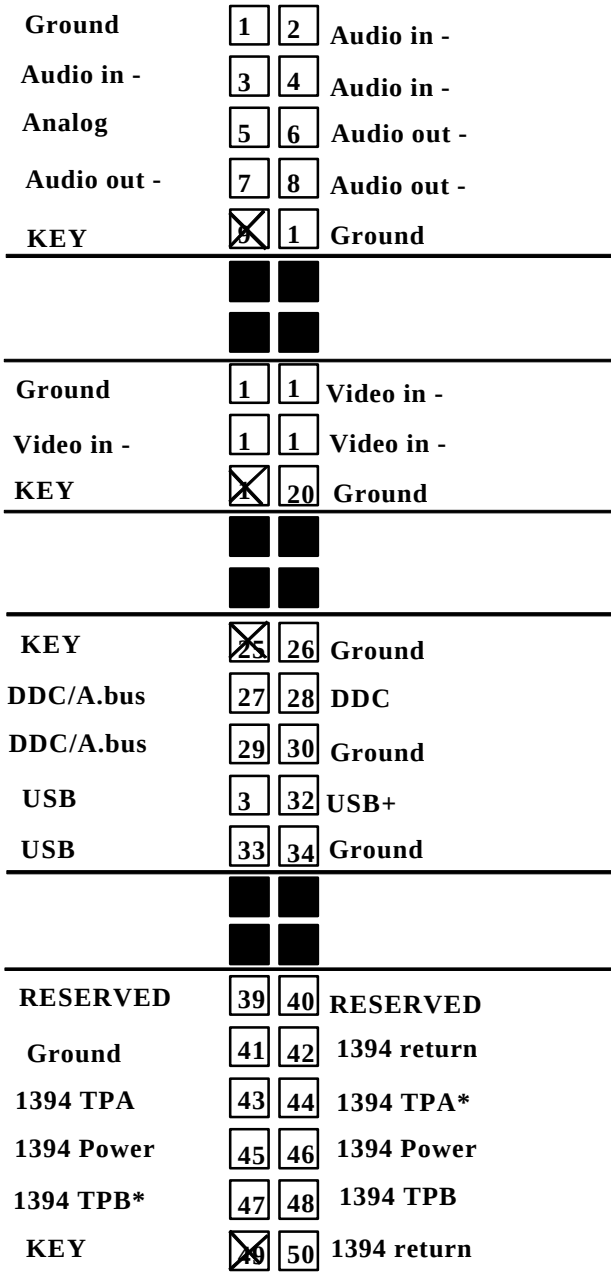
Note: The above drawing shows the location of the interconnect header on a PCI-type card. For VL-bus, ISA/EISA, etc. cards, it is recommended that the position guidelines shown be followed, but the header be rotated 180 degrees to place pin 1 on the top row, at the end nearest the bulkhead, as shown in the drawing to the right. Both drawings show component-side views.



5.3 Connector Signal Assignments/Pinout

The standard connector provided by the graphics controller (or other board carrying P&D-A) shall be a single 50-pin header, or multiple headers which are located so as to provide equivalent pin positions to a single 50-pin header. In the latter case, the header areas defined as “break areas” in the pin assignment list need not be physically present, although the spacing provided by these must be maintained.
Receptacle pin assignments:

1	Ground (cable shield)
2	Audio input, Left
3	Audio input, Return
4	Audio input, Right
5	Analog Ground (see note A)
6	Audio output, Left
7	Audio output, Return
8	Audio output, Right
9	KEY (N/C) (see note C)
10	Ground (cable shield)
11-14	Break area (see note B)
15	Ground
16	Video In - Chroma (C)
17	Video In - Return
18	Video In - Luminance (Y)
19	KEY (N/C) (see note C)
20	Ground
21-24	Break area (see note B)
25	KEY (N/C) (see note C)
26	Ground
27	DDC/ACCESS.bus clock (SCL)
28	DDC/ACCESS.bus return
29	DDC/ACCESS.bus data (SDA)
30	Ground
31	Universal Serial Bus return
32	USB data pair, +
33	USB data pair, -
34	Ground
35-38	Break area (see note B)
39	RESERVED 1
40	RESERVED 2
41	Ground
42	1394 return
43	1394 TPA
44	1394 TPA*
45	1394 power
46	1394 power
47	1394 TPB
48	1394 TPB*
49	KEY (N/C) (see note C)
50	1394 return



Connector

Notes
A - The ground assigned to position 5 is intended to be an analog ground, separate from the ground used for the other positions. This is intended to maintain an isolated audio signal section at positions 1-10, with guard grounds (cable shield grounds) appearing at positions 1 and 10.

B - It is expected that in most implementations, multiple separate cables and connectors will be used to connect to this single header. Breaks between sections of this header have been provided to give sufficient clearance to allow this.

These appear in the pinout diagram as solid black boxes in the affected pin positions. These have been assigned assuming the following:

1. The connectors used for the audio I/O section and the DDC/USB section (positions 1-10 and 25-34, respectively) may be of any type, including standard ribbon-cable receptacles.
2. The connectors used for the video input and IEEE-1394 sections (positions 15-20 and 39-50, respectively) will be discrete-wire types; ribbon cable connectors may not be used here, due to the requirements of these signals.

Since ribbon-cable receptacles (which may in some cases be IDT types) will not appear side by side at any point on the header, two rows' distance provides sufficient break between all sections. The positions assigned as inter-connector breaks on the header may be voided (no pin loaded) if desired by the manufacturer for clearer separation, but this is not required by this standard.

C - Positions identified as "KEY (N/C)" in the pinout list and diagram are required to be voided locations (no pin loaded) in the header, and molded-in voids in the mating receptacle(s). Keying is required in order to minimize the possibility of mismating of the connectors and the resulting potential for hardware damage.

D - Please note that the "video input" signals defined on this connector are identical to the video input provided by the P&D-A; in other words, these pins are intended to carry video signals being provided FROM an external device TO the host system. This connection is simply a pass-through of these signals from the P&D-A to a video input card or circuit elsewhere in the system, and is not to be confused with "video input" in terms of a signal or signals being provided TO the graphics controller from elsewhere in the system.

E - The pins marked "RESERVED" on this connector must be connected to the corresponding pins on the P&D-A.

F - The is a conflict between the specified location of this connector and the VESA Advanced Feature Connector (VAFC) location as specified in the VAFC standard. Due to the nature of the signals carried by P&D-A (particularly audio I/O and video input signals), it is recommended that location of the P&D-A interconnect be maintained as specified here, in order to minimize the length of the traces carrying these signals. If a manufacturer chooses to provide both VAFC and P&D-A on a given board, we recommend that the VAFC connector be moved slightly farther away from the bulkhead (a change of approximately 1 inch in required) in order to accommodate the P&D-A interconnect. Alternatively, either the VAFC or the P&D-A interconnect could be moved relative to the top edge of the board; we recommend that the VAFC be moved down, as the P&D-A interconnect is likely to be the one more often accessed by the user, due to the larger number of cables which may attach at this point.

6.0 Detection of Display Disconnect

The VESA Plug and Display Standard has established a protocol based on the +5VDC and charge power pins of the P&D video connector(s) such that a P&D-compliant host may detect the connection and disconnection of display devices, and respond accordingly (by re-reading the display's EDID data, etc.). This capability has been referred to as "hot-plugging". As of Version 2 of the P&D-A standard, this feature is also supported on P&D-A-equipped hosts, in order to keep the P&D-A standard compliant with the overall architecture used by the P&D and related standards. It is important to note, however, that this feature may not be supported on hosts and displays designed under the earlier Version 1 P&D-A standard. NOTE THAT SUPPORT OF THIS FEATURE REQUIRES SUPPORT OF THE DDC2 PROTOCOL, PER THE VESA DISPLAY DATA CHANNEL STANDARD. Support of the DDC1 protocol only is insufficient for compliance with this portion of the P&D-A standard.

This section is intended to provide the basic description and requirements for support of this feature under the VESA P&D-A and P&D standards. The reader is directed to the VESA Plug and Display Standard, Section 3, and also Appendices B and D of that same standard, for additional information. The information contained in this document is intended to duplicate those requirements established by the VESA Plug and Display Standard and is given here for convenience only; in the event of any conflict between these requirements and those of the relevant sections of the Plug and Display Standard, the requirements of the Plug and Display Standard should be used.

6.1 Detection Mechanism - Host

The following steps outline the requirements and detection process for the host system. Please reference the flowchart shown in Section 6.3 (intended for process illustration only).

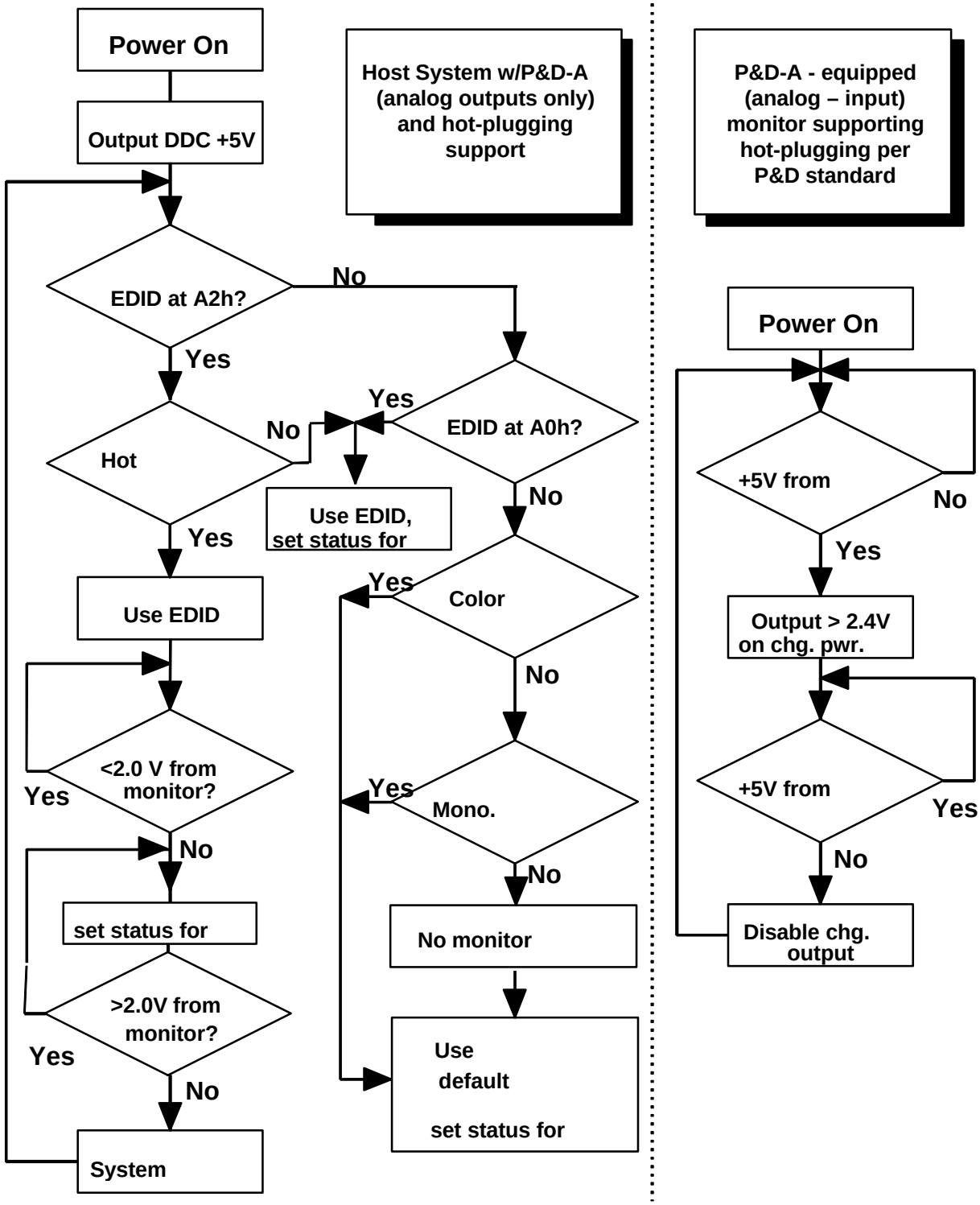
1. Initially, the host system should provide +5VDC on pin 28 of the P&D-A, per the requirements of this standard, and check to see if EDID information can be accessed at address A2h via the DDC2 protocol. The host should retry this operation for up to 30 seconds.
2. If no EDID information is detected at A2h, then the host shall check for EDID information readable at address A0h via the DDC2 protocol. If an EDID is present at this address, the EDID data should be decoded to provide information on the modes supported by the display.
3. If no EDID is found at either address, the host should check for the presence of a monitor and attempt to determine whether it is a color or monochrome unit by checking for loads on the RGB analog video lines. If a monitor is present, the host should assume that is has at least support for the minimum "VGA" modes (typically the "alphanumeric VGA mono" mode at 70 Hz refresh).
4. If an EDID is detected at A2h, the host must then check the EDID information to determine if the monitor is VP&D compliant (by checking the P&D flag as defined by the EDID standard). If this flag is set, it indicates (among other things) that the monitor supports the "hot plugging" feature described here. If this flag is set, the host should then check the "charge power" line to verify that there at least 2.0 VDC present on this line, indicating that the monitor is properly connected and ready. NOTE: The voltage present on the charge power line may be up to 20 VDC, per this standard; hosts must be designed to accept this voltage at any time without damage.
5. The host shall continue to monitor the charge power line; should the voltage on this line drop below 2.0V, the host may assume that the display has been unplugged and should restart the display detection process. The graphics subsystem should raise an interrupt to the operation system, causing the OS to restart this process, re-read the EDID information, and to reconfigure the graphics system as appropriate based on the new information at the time connection of a new display is detected.

6.2 Detection Mechanism - Display

The following items outline the requirements for "hot plugging" support for the display. Note that the following applies only to analog-interface displays providing the P&D-A plug; digital-interface displays, using the P&D-style plug should follow the requirements outlined in the VESA Plug and Display Standard. Please reference the flowchart shown in Section 6.3 (intended for process illustration only).

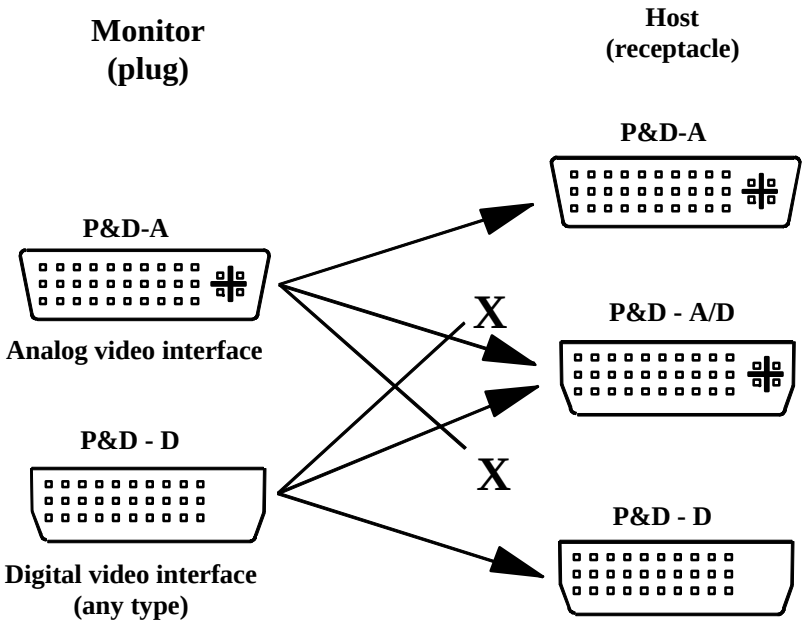
1. The display is required to monitor the +5VDC line from the host, and to provide at least +2.4 VDC on the charge power line whenever the +5VDC line is within the voltage range specified by this standard.
2. If at any time the +5 VDC line drops below 2.0 V for greater than one second, the display may assume that the host system has been disconnected or powered off, and take any appropriate action. Note that operation of the power management features under the VESA DPMS standard should remain independent of this “hot plugging” process.

6.3 Power-Up/Down and Hot-Plugging Flowchart for P&D-A Hosts & Monitors



Appendix A - Compatibility with VESA Plug & Display Standard

The VESA Plug & Display Standard builds on the Enhanced Video Connector physical standard, extending that concept into a family of related connectors which exist under a common logical interface architecture. The P&D-A definition, as documented here, fits into this family as the connector standard of choice for systems choosing to support only an analog video interface. The two new connector standards introduced under P&D make up the rest of this family, providing standards for supporting both analog and digital video interfaces on a single host connector, and for supporting a digital-only host. The relationship between the host connectors (receptacles) and the corresponding monitor video connectors (plugs) is shown in the diagram below.



This family of connectors uses a combination of shell shape and other physical features to ensure that displays using a given interface type (either analog or digital) will not be connected to hosts which do not provide support for that interface, but can always be connected to hosts on which that interface is supported. Analog-interface monitors should continue to use the P&D-A plug, and so will be supported on both analog-only hosts (using the P&D-A receptacle) and on those hosts which provide both analog and digital support (via the P&D-A/D receptacle). Digital-interface monitors, using a plug which has no provision for analog connections, are supported on any host which provides a digital output, but will not be capable of being connected to hosts supplying only analog video. Similarly, analog-input monitors cannot be connected to hosts providing support only for digital video.

Revision History

Original release (Version 1, Rev. 0) - 30 November 1995)

2nd release (Version 2 - 5 November 1997)

Version 2 includes a number of minor changes made to improve compatibility with the VESA Plug & Display (VP&D) standard and to correct minor errors in the initial release of the P&D-A standard. These include:

- Changing the locations of the “charge power” and “reserved” pins
- Redefinition of the “charge power” connection as a single-ended supply.
- Deletion of the “recommended implementations” of P&D-A, including the original Appendix A.
- Addition of a new Appendix A describing the compatibility between P&D-A Vers. 2 and other connectors in the P&D-A/P&D family.
- Addition of hot plugging support per the VP&D standard.
- Changes to the sync. signal rise/fall time requirements to match those of the VP&D standard.
- Overall typo correction and format clean-up, including minor corrections to the connector drawings and highlighting of the minimum signal set requirements.

3rd proposed release (Version 3.0 Draft 1, 29 April 1998)

- Changed abbreviation EVC to P&D-A, 102 places in standard

- Corrected 1394 signal name call-out on pages 11 and 22.

- Changed footer to incorporate new Copyright date and Version number and date.

4th proposed release (Version 2, Revision 1, 13 July 1998)

- Corrected Version number

- Added note 7 to subsection 2.3.1 in accordance with WG request.